NEWS

Tektronix Margin Tester Shrinks PCIe Test Time to Minutes

October 25, 2022 by Jeff Child

By creating a new class of test instrument, Tektronix touts its PCI Express (PCIe) margin tester as a tool that reduces PCIe link testing times from hours down to just minutes.

PCI Express (PCIe) ranks among the most consequential interconnect technologies in the history of computing. But doing testing and evaluation of PCIe subsystems can be a complex and lengthy process.

Offering a new approach to that process, today Tektronix announced its TMT4 Margin Tester. The company claims it as the industry's first dedicated Transmit/Receive (Tx/Rx) lane margining tool, enabling engineers to evaluate the link health of their PCIe Gen 3 and 4 systems in just minutes, rather than hours or days.

In this article, we examine the key details of the TMT4 Margin Tester, we review the problem that the new margin tester system is designed to solve, and we share insights from our interview with Michael Seaholm, Product Manager at Tektronix. Seaholm is the project lead on the TMT4 Margin Tester.

Margin Tester Acts as Active Link Partner

In contrast to traditional PCIe testing methods, the TMT4 functions as an "active link partner" with your device under test (DUT).

The TMT4 Margin Test acts as an active link tool, enabling engineers to quickly view the health of their PCIe links between devices. Image used courtesy of Tektronix

Engineers can use the instrument to control presets via protocol and quickly display eye diagrams with their associated link training parameters. In this way, they can view potential design flaws on a lane-by-lane or preset-by-preset basis.

As Seaholm explains, today's traditional approach for testing design margins on a technology like PCIe includes two methods. One is a combination of an oscilloscope and a Bit Error Tester (BERT). The other is using on-chip Lane Merging (LM) tools provided by chip manufacturers. Each has its trade offs.

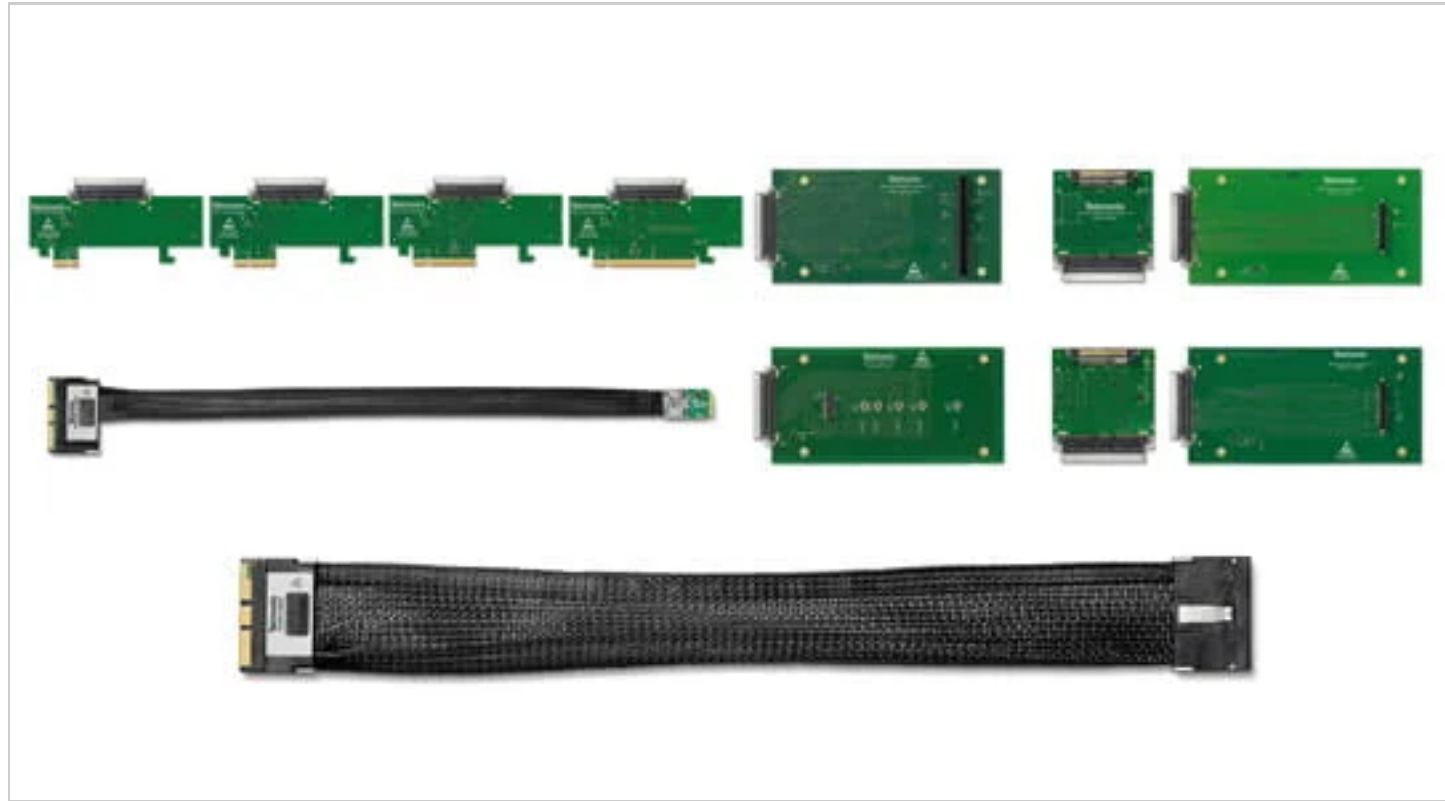
The scope/BERT approach is a comprehensive method, and it can achieve all the validation and compliance testing necessary for PCIe compliance. But it is an expensive method that not all system developers can afford. Then there is the time it takes. "Even very experienced engineers can need several days to do this kind of PCIe testing," says Seaholm. "And full testing of 16-lane PCIe links can even take weeks."

Meanwhile, LM tools are certainly less expensive than a scope/BERT setup, but they have limitations. For instance, LM tools can only do lane merging of their own receivers. That means that engineers can only use them to analyze the DUT receive paths, but not the transmitter path, says Seaholm.

A PCIe Solution for a Broad Set of EEs

In contrast to the traditional methods of PCIe testing as explained above, the TMT4 Margin Tester was created to be used by a broad set of users without requiring specialized expertise. According to Tektronix, TMT4 enables engineers at all levels of experience to evaluate the health of transmitter and receiver links faster, in minutes instead of hours or days.

Unlike the other PCIe testing alternatives, the TMT4 is fast and versatile enough that engineers can perform PCIe links at the board- or system-level more often. Likely any development process will still need to use a scope/BERT method to do the full validation and compliance testing. But the TMT4 makes it possible to tackle PCIe link issues earlier on in the design process.



The TMT4 Margin Tester supports most common PCIe form factors using 11 adapters available for CEM, M.2, U.2, and U.3. Image used courtesy of Tektronix

Using the TMT4, EEs can test PCIe devices across up to 160 combinations of lanes and presets in as little as 20 minutes at Gen 4 speeds. Multi-lane testing capabilities enable users to improve overall testing times by reducing the number of connection changes needed to perform testing.

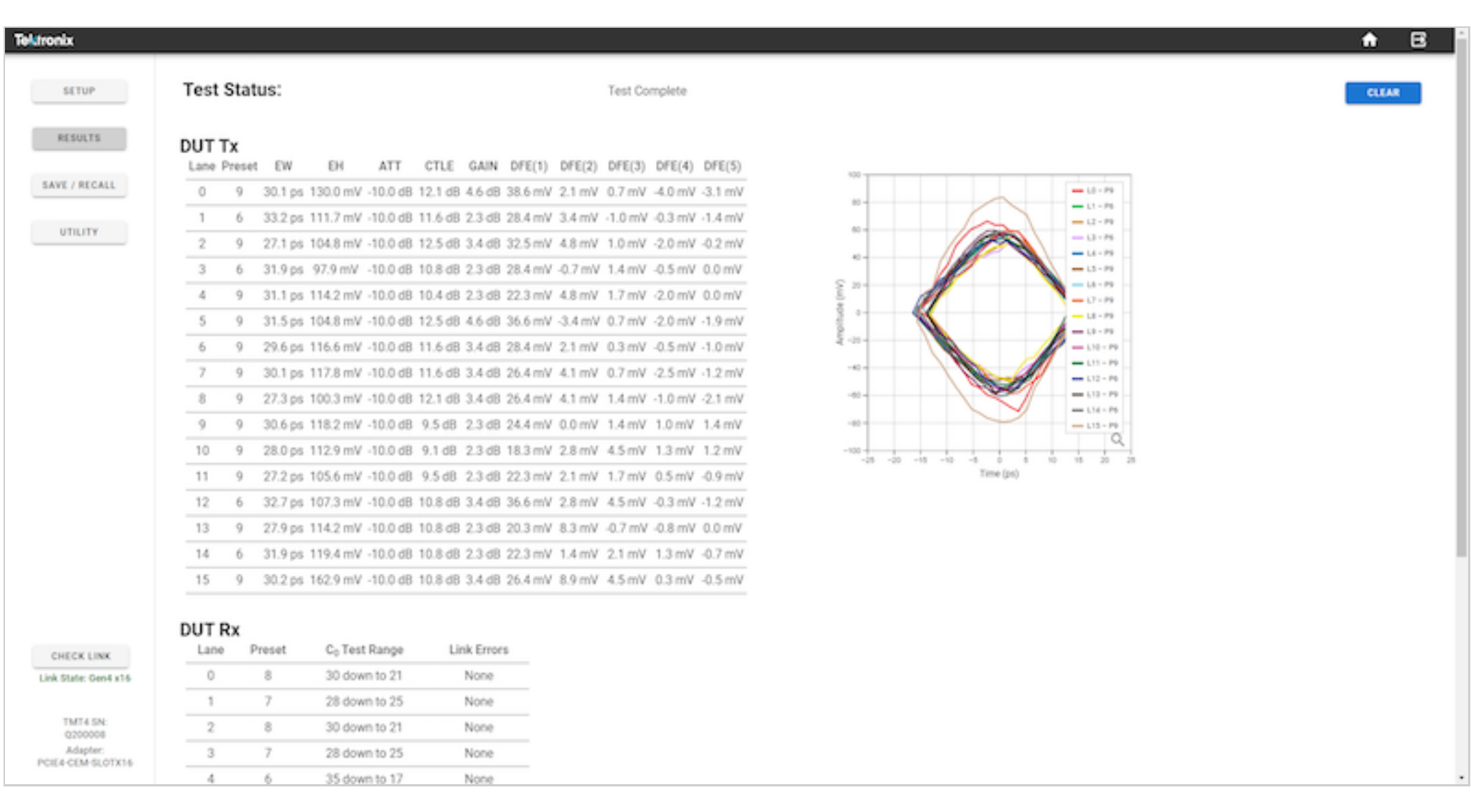
EEs can use the TMT4 as they design and validate PCIe Gen 3 and Gen 4 subsystems such as motherboards, add-in cards, and systems. The TMT4 Margin Tester supports most common PCIe form factors by means of 11 adapters available for CEM, M.2, U.2, and U.3.

Using a single 16-lane ribbon cable with high density PCIe connectors, the TMT4 connects to any of the adapters. The only exception is the M.2 edge adapter, which has its own integrated cable to accommodate different insertion loss specifications, says the company.

Quan Scan and Custom Scan

The user interface for TMT4 is intended to be simple and easy to use. Users can control the TMT4 Margin Tester using the front panel, a web browser, or the Rest API. The platform offers two options: Quick Scan and Custom Scan. In Quick Scan, the Margin Tester and the DUT engage in a natural link negotiation to determine the presets they will communicate over.

Meanwhile, Custom Scan provides engineers with more parameters to adjust for specific tests. It essentially forces the DUT into specific presets for tests. Tektronix offers a demo video that explains the scan options and other TMT4 features in more detail.



The TMT4 can perform PCIe link heath evaluation of both the Tx and Rx signals in as little as two minutes. Image used courtesy of Tektronix (Click image to enlarge)

As shown in the screenshot above, the DUT Tx test provides two key pieces of data:

- Eye diagrams for each lane-preset combination measured at the receiver of the TMT4
- The associated receiver training values the Margin Tester used to open the eye that is displayed

Also shown in the screenshot above, the DUT Rx test is a functional evaluation of the DUT's receiver path. The test determines how far the transmitted signal amplitude from the Margin Tester can be decreased, within an expected range of operation, before errors are returned.

PCIe Margin Testing: Huge Customer Implications

By creating essentially a new class of test instrument, Tektronix has opened up new options for engineering teams that want to analyze their PCIe links as they develop their designs. This fills an important need because the stakes of a PCIe device's reliability are higher than ever these days. When PCIe devices don't work well together, it becomes a real problem for customer support, explains Seaholm.

> *"When two products do not work together, who is to blame?" says Seaholm, "Is it the system board manufacturer? The add-in-card manufacturer? Both? Who does the consumer go to when there is a problem?"*

For those reasons, analyzing the design margins for PCIe boards and systems working together is critical. Tektronix's new TMT4 is perhaps the best approach to mitigating such issues before they become a problem.

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