DisplayPort Standard

06-12-2008

DisplayPort Standard
Tektronix MOI for Sink Tests
(AWG Jitter Generation using Direct Synthesis and calibration using Real Time DPO measurements for Sink Devices)

Table of Contents

Modification Records

October 22, 2007 (Tektronix Version .9) INITIAL RELEASE
Randy White, U N Vasudev, Chris Skach

December 04, 2007 (Tektronix Version .95)
Randy White,:
Updated jitter calibration connection

March 24, 2008 (Tektronix Version 1.1)
Randy White,:

May 21, 2008 (Tektronix version 1.11)
Muralidharan
Updated SerialXpress calibration procedure

Acknowledgements

Tektronix Inc.: -creation of the document
Randy White
John Calvin
UN Vasudev
Chris Skach
Sarah Boen
Muralidharan

INTRODUCTION

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. This document outlines precise and specific procedures required to conduct Display Port tests. This document covers a test which is Tektronix Real Time DSA or DPO and AWG7102 based.

Formally, each test description contains the following sections:

Test Objective

Interoperability statement

Test conditions

Measurement requirements and

Pass/fail criteria covering:

- ## RECIEVER COMPLIANCE TEST (Test 4.1)

Equipment Preparation

Prior to making any measurements, the following steps must be taken to assure accurate measurements:

1. Allow a minimum of 20 minutes warm-up time for oscilloscope and AWG.
2. Run scope SPC calibration routine and instrument calibration on AWG. It is necessary to remove all probes and cables from the scope and AWG before running calibration.
3. If using probes, perform the probe calibration defined for the specific probes being used.
4. Perform de-skew to compensate for skew between measurement channels. Note that it is critical to select “Off” for the “Display only” control on the De-skew setup window. This will assure that the de-skew data is stored with any waveforms that are stored.

RECIEVER COMPLIANCE TEST

4.1 Sink Jitter Tolerance Test (Normative)

4.1.1 Test Objective

The Display Port Standard outlines a minimum Receiver Eye diagram (Display Port Standard Figure 3-21) which is measured at the receiver silicon component junction. This test is designed to provide an impaired stimulus which has been calibrated to the minimum TP3 connector electrical properties. These properties are defined in Table 3.11 and Table 3.13 and differ for High Bit Rate (HBR, 2.7GB/s) and Reduced Bit Rate (RBR, 1.62GB/s) transmission speeds. This test outlines the pass fail criteria around these tests. (Reference Section 3.5.3 of Display Port Standard)

4.1.2 References

- **Display Port Specification version 1.1a dated January 11, 2008**
- **Display Port CTS version 1.1 draft 8 dated May 13 2008 Section 4.1.**

4.1.3 Test Conditions

The test shall be performed for all lanes of a receiver. Each lane is tested individually while adjacent lanes will be stimulated with a clock pattern to include cross-talk effects on the receiver's PCB.
Note: The Display Port Standard requires sink devices to support link training and PRBS7 test on individual lanes**.**

The amplitude of the applied signals shall be: (specified in section 3.5)

High Bit Rate: voltage = 150mVolts peak-peak (Table 3-16 of Display Port Standard ver1.1a)

Reduced Bit Rate: voltage = 46mVolts peak-peak. (Table 3-17 of DisplayPort Standard ver 1.1a)

The peak to peak voltage shall be measured by making an eye opening measurement using the 50% point (center of eye, horizontally) as the location to measure worst case peak and minimum for the peak to peak measurement.

No Pre-emphasis or spread spectrum clocking shall be present on the applied signal.

Note: Other standards are being followed with respect to Spread Spectrum Clocking. This requirement may change in the future.

The receiver tolerance test will be formed on a statistically relevant population of data. Two populations will be used. One is 100 times the 1/Bit Error Rate of 10-9 during which fewer than 100 receiver errors shall be observed. 10^{12} bits requires a direct test time of 370 seconds at HBR rates and 620 seconds at RBR rates.

Note: the crosstalk requirement does not apply to receivers that have only one lane. For sink devices with two lanes the lane that is not under test will receive the D24.3 pattern. Sink devices with four lanes will be tested four times using the following scheme:

- Lane 0 under stressed signal: D24.3 to lane 1 and 3, no signal to lane 2
- Lane 1 under stressed signal: D24.3 to lane 0 and 2, no signal to lane 3
- Lane 2 under stressed signal: D24.3 to lane 1 and 3, no signal to lane 0
- Lane 3 under stressed signal: D24.3 to lane 0 and 2, no signal to lane 1

4.1.4 Measurement Requirements

Receiver stress test is separated in multiple phases. First the signal generator initiates link training for the lane under test. Once link training is performed the pattern is changed to PRBS7 and it is verified that the sink device's PRBS7 counter actually works properly. Link training and counter operation are pass/fail criteria. After these verifications receiver stress tests with signals with specified level and jitter are performed. During these tests the number of bit errors is counted over a specified time interval. The total number of errors is compared against the specified value.

Note: It is a requirement for the SSG to change pattern without any interruption. This means that when transitioning between patterns that there be no disruption in clock frequency or symbol clocking integrity and when transitioning between jitter states that there be no disruption in data pattern or clock frequency.

Link training is done in two phases: The frequency lock phase and the symbol lock phase. Both phases require the SSG to send the necessary pattern as defined in the VESA Display Port Standard Ver. 1.1a specification**. Link training is performed with ISI, Rj and SJ injected**. This is required for the sink device to choose the appropriate equalization settings. It is anticipated for all tests to use the AUX channel to control the sink device and to read the PRBS7 counter. If no such tool is available, a vendor specific debug tool may be used.

Receiver stress test is separated in multiple phases.

1. First the signal generator initiates link training for the lane under test.
2. Once link training is performed the pattern is changed to PRBS7 and it is verified that the sink device's PRBS7 counter actually works properly. This is a pass/fail criteria.

3. After that the actual receiver stress tests are performed and the BER is recorded.

The following figure outlines the test setup in principle. It illustrates an example where the sink device has 4 lanes and lane 1 is under test.

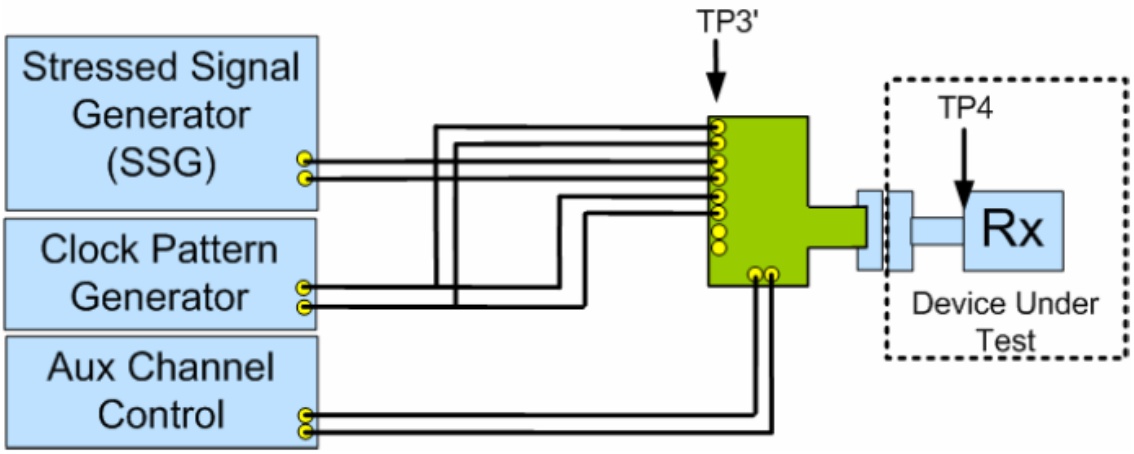


Figure 4-5: Jitter Test Setup

The following procedure applies for each lane:

1. Connect the SSG to the lane under test and clock pattern generator to the adjacent lanes. Adjust data rates for Reduced Bit Rate or High Bit Rate. All jitter sources and minimum eye for both cross talk and Data lanes were calibrated previously. ISI and Rj are turned on. **Sj is turned on at the highest frequency during the EYE height calibration and when generating all required patterns including the link training patterns.**

Frequency lock phase

2. SSG outputs a D10.2 Frequency Lock pattern (includes injected ISI, Rj and Sj jitter VESA Display Port Standard Ver. 1.1a specification)
3. AUX Control initiates the frequency lock phase
4. After >100us AUX Control verifies whether DUT achieved frequency lock. If not go to the previous step. If frequency lock cannot be achieved within 5 retries the test result shall be a failure.

Symbol lock phase

5. SSG outputs Symbol Lock pattern as defined in specification with ISI, Rj and SJ jitter injected
6. AUX Control initiates the symbol lock phase

7. After >100us AUX Control verifies whether DUT achieved symbol lock. If not go to the previous step. If symbol lock cannot be achieved within 5 retries the test result will be a failure.

PRBS7 counter test phase

8. SSG outputs a clean PRBS pattern and the AUX control verifies for zero bit error
9. SSG injects "n" single bit error while looping the PRBS7 pattern
10. AUX Control verifies that the PRBS7 counter shows "n" or "n+1" bit error. If not the test result will be a failure

BER test phase

11. Stressed Signal Generator outputs PRBS7 pattern as defined in specification with Rj, Sj, and ISI jitter injected. The SJ frequency has to be set to the current test case
12. AUX Control clears the PRBS7 error counter
13. Run test for specified time as indicted in Table 4.1 of the CTS document as shown below
14. The PRBS7 error counter is read through AUX Channel Control.
15. If no errors observed by the AUX channel control, then go to **Step 2** to repeat the test procedure for other Sj frequencies

Table 4-1: Test Parameters for BER Measurement

Data Rate	Jitter Frequency	Number of Bits	Max Num of Bit Errors Allowable	Observation Time[1] (seconds)	Data Rate Offset
HBR RBR	2 MHz	10^{12}	1000	HBR=370s RBR=620s	0
HBR RBR	10 MHz	10^{11}	100	HBR=37s RBR=62s	+350ppm +350ppm
HBR RBR	20 MHz	10^{11}	100	HBR=37s RBR=62s	0
HBR	100 MHz	10^{11}	100	HBR=37s	0

1. To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: 10^{11} bits at HBR = 370ps/UI * 10^{11} UI = 37 seconds

4.1.5 Test equipment required and calibration method

All the Training patterns (both Frequency Lock and Symbol Lock patterns), PRBS7 pattern and Cross talk are calibrated as per the Jitter specs.

Refer to **Appendix - A** for Test equipment list and calibration procedure

4.1.6 Connection Diagram

Refer to Appendix B of this MOI.

4.1.7 Detailed Procedure

1. The AWG analog interleave output with DC Block and attenuators are connected to a DP-P plug fixture. Markers output with attenuators and Rise Time Filters are connected to the adjacent lanes as appropriate for 2 and 4 lanes testing to inject cross talk in to the DUT.

2. DP-P fixture is connected to the DUT (Device Under Test)

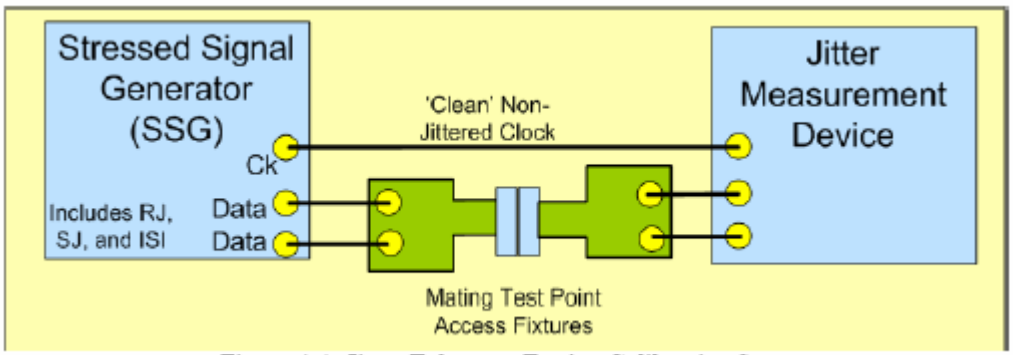
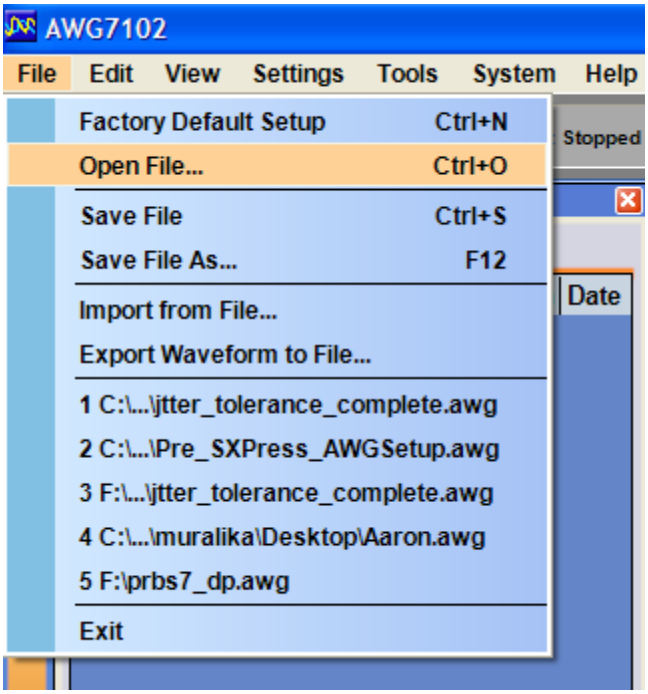


Figure 4-4: Jitter Tolerance Testing Calibration Setup

3. On the AWG Open **File -> Open File**

DP_HBRv1.awg for HBR compliance testing
DP_RBRv1.awg for RBR compliance testing



Now you have selected all the HBR or RBR patterns sequenced in a particular order as shown below

4. Turn all outputs **ON** and hit **Run** on the AWG Front Panel to run the first pattern in the sequence which is a **Frequency Lock Pattern (includes injected ISI, Rj and Sj jitter)**. Each index in the sequence listing corresponds to a required step in the Jitter tolerance test including link training and bit error rate test vectors.

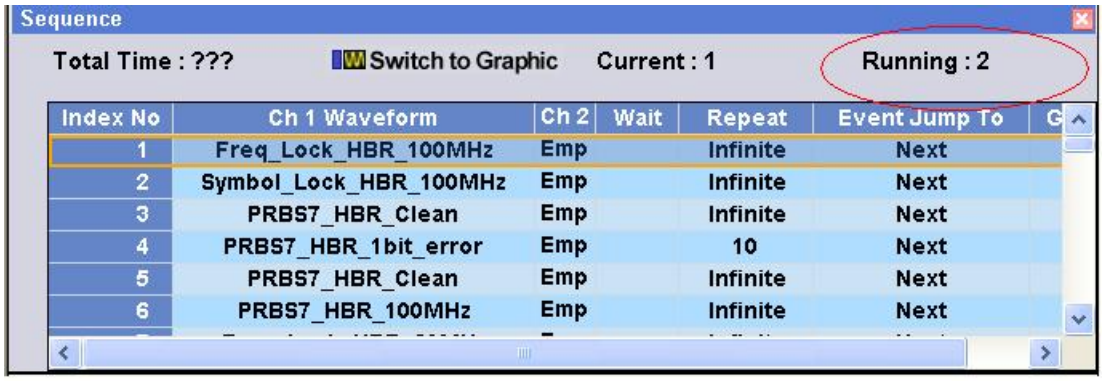
5. Initiate AUX Control frequency lock phase and disable scrambling by writing TRAINING_PATTERN_SET (address 0x102 bits 5, 1:0)

6. After >100µs AUX Control verifies whether DUT achieved frequency lock. If frequency lock cannot be achieved within 5 retries (with maximum consecutive AUX Defers allowable = 8) the test result shall be a failure. Lock is verified by polling CR_LOCK status for the data lane under test:

   If LANE0_CR_DONE (Address202h bit 0) = 1
   If LANE1_CR_DONE (Address202h bit 4) = 1
   If LANE2_CR_DONE (Address203h bit 0) = 1
   If LANE3_CR_DONE (Address203h bit 4) = 1

7. Press the **FORCE EVENT** button on the front panel of AWG to send the **Symbol Lock Pattern (includes injected ISI, Rj and Sj jitter)**

   Note that the AWG is now running the index no.2 which is a **Symbol Lock Pattern**



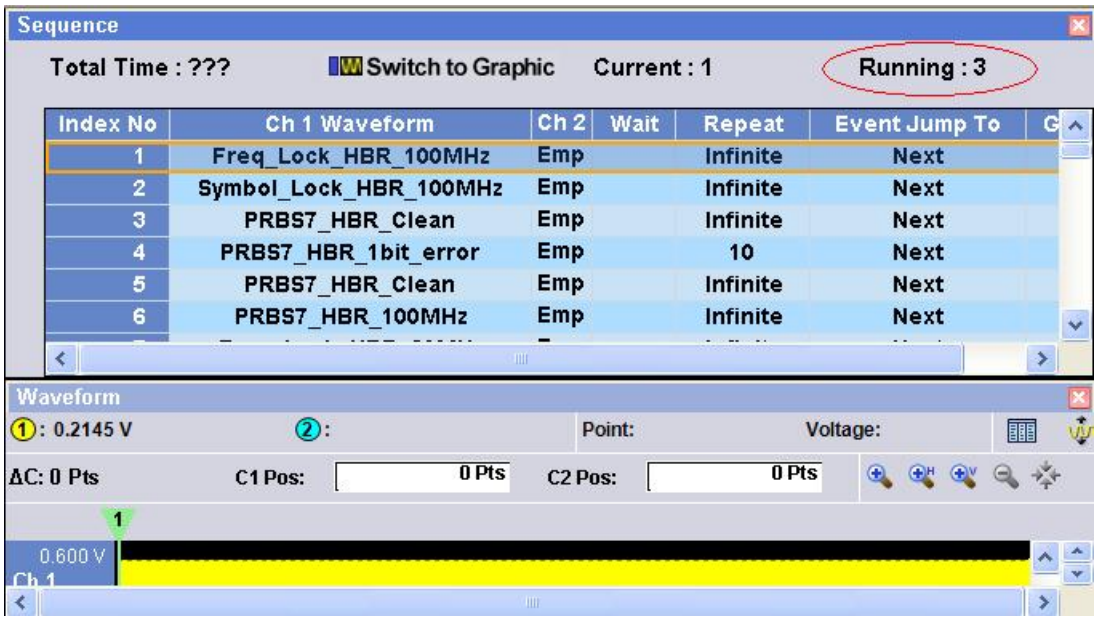
8. Initiate AUX Control the symbol lock phase and disables scrambling by writing TRAINING_PATTERN_SET (address 0x102 bits 5, 1:0)

9. After >100µs AUX Control verifies whether DUT achieved symbol lock. If not go to the previous step. If symbol lock cannot be achieved within 5 retries (with maximum consecutive AUX Defers allowable = 8) the test result will be a failure. Lock is verified by polling CR_LOCK status for the data lane under test:

   If LANE0_CHANNEL_EQ_DONE (Address202h bit 1)
   If LANE0_SYMBOL_LOCKED (Address202h bit 2)
   If LANE1_CHANNEL_EQ_DONE (Address202h bit 5)
   If LANE1_SYMBOL_LOCKED (Address202h bit 6)
   If LANE2_CHANNEL_EQ_DONE (Address203h bit 1)
   If LANE2_SYMBOL_LOCKED (Address203h bit 2)
   If LANE3_CHANNEL_EQ_DONE (Address203h bit 5)
   If LANE3_SYMBOL_LOCKED (Address203h bit 6

10. Press the **FORCE EVENT** button on the front panel of AWG

    Note that the AWG is now running the index no 3 and which is a **PRBS 7 pattern**



11. Initiate AUX Control to check whether the error counter is 0, to ensure the PRBS7 pattern is recognized.

12. Press the **FORCE EVENT** button on the front panel of AWG.

    Note that the AWG is now running the index no.5, after completing index no 4, which is a **PRBS7_HBR_1bit_error** pattern repeated 10 times

13. AUX Control verifies that the PRBS7 counter reads "10 or 10+1" errors. If not the test result will be a failure

14. Press the **FORCE EVENT** button on the front panel of AWG

    Note that the AWG is now running the index no.6, which is a P**RBS7_HBR_100MHz or a PRBS7_RBR_20MHz,** which is PRBS7 pattern with specified amount of Rj, Sj at specified frequency and ISI as specified in the CTS Jitter table

f(Sj)	Tj(JTRBRrx)	ISI	RJ(RMS)	SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1648	570	7.9	981
10	778	570	7.9	111
20	747	570	7.9	80

Table 4-2: Jitter Component Settings for Reduced Rate

Table 4-3: Jitter Component Settings for High Rate

f(Sj)	Tj(JTHBRrx)	ISI	RJ(RMS)	SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1079	161	13.2	756
10	509	161	13.2	186
20	489	161	13.2	166
100	484	161	13.2	161

15. AUX Control clears the PRBS7 error counter by reading SYMBOL_ERROR_COUNT_LANEx for lane x under test (address 0x210, 0x211 for lane 0, address 0x212, 0x213 for lane 1, address 0x214, 0x215 for lane 2, address 0x216, 0x217 for lane 3)

16. Run test for specified **"Observation Time"** as per below table

Table 4-1: Test Parameters for BER Measurement

Data Rate	Jitter Frequency	Number of Bits	Max Num of Bit Errors Allowable	Observation Time[1] (seconds)	Data Rate Offset
HBR RBR	2 MHz	10^{12}	1000	HBR=370s RBR=620s	0
HBR RBR	10 MHz	10^{11}	100	HBR=37s RBR=62s	+350ppm +350ppm
HBR RBR	20 MHz	10^{11}	100	HBR=37s RBR=62s	0
HBR	100 MHz	10^{11}	100	HBR=37s	0

1. To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: 10^{11} bits at HBR = 370ps/UI * 10^{11} UI = 37 seconds

17. The PRBS7 error counter is read through AUX Channel Control by reading SYMBOL_ERROR_COUNT_LANEx for lane x under test (address 0x210, 0x211 for lane 0, address 0x212, 0x213 for lane 1, address 0x214, 0x215 for lane 2, address 0x216, 0x217 for lane 3

18. Check for the **Pass / Fail** Criteria for the transmitted Jitter frequency

4.1.5 Pass/Fail Criteria

For each lane and all supported data rates:

- The receiver is required to achieve frequency lock and symbol lock within 5 retries.
- The PRBS7 counter has to be operational and must count no fewer than injected number of errors during the counter test, and no more than the injected number of errors + 1.
- Number of Errors doesn't exceed limit given in Table 4-1, for stressed signal testing.

19. **Repeat** the steps 5 to 18 for other frequencies in the Jitter table to complete the compliance test

4.2 APPENDIX A:

4.2.1 Test Equipment list:

High Speed Signal Source	AWG7102 with options 01, 06	1
Oscilloscope[2]	Tektronix Real Time DSA/DPO70000 or TDS6804B/TDS6124C/TDS6154C 8GHz or above (required bandwidth as per the Compliance Test Specification) captures the 5th harmonic of the 1.35GHz fundamental	1
Software	DPOJET[3] Jitter and Eye Diagram Analysis Tool or RT-Eye Serial Data Compliance and Analysis Software and TDSJIT3 Advanced Jitter Timing and Analysis software SerialXpress[1] – Advanced Jitter generation software for AWG	1
Test Fixtures	TPA-P and TPA-R fixtures from Efficere Technologies	1 set
Attenuators	Tek P/N: 015-1002-01 (14dB)	2 (for Analog output)
Attenuators	Tek P/N: 015-1001-01 (6dB)	4 (for Markers)
DC Block - Picosecond Pulse Lab	5501A	2 (for Analog output)
Rise Time Filter - Picosecond Pulse Lab	5915-110-100ps	4 (for Markers)

[1] SerialXpress – This optional Jitter generation software for AWG is required only if the jittered patterns are to being created by the user. See below for more details on Jitter creation using SerialXpress

[2]Oscilloscope required for jitter calibration process

[3] DSA70000 includes TDSRT-Eye and TDSJIT3 Advanced standard whereas both are optional on the DPO70000/TDS6000 series

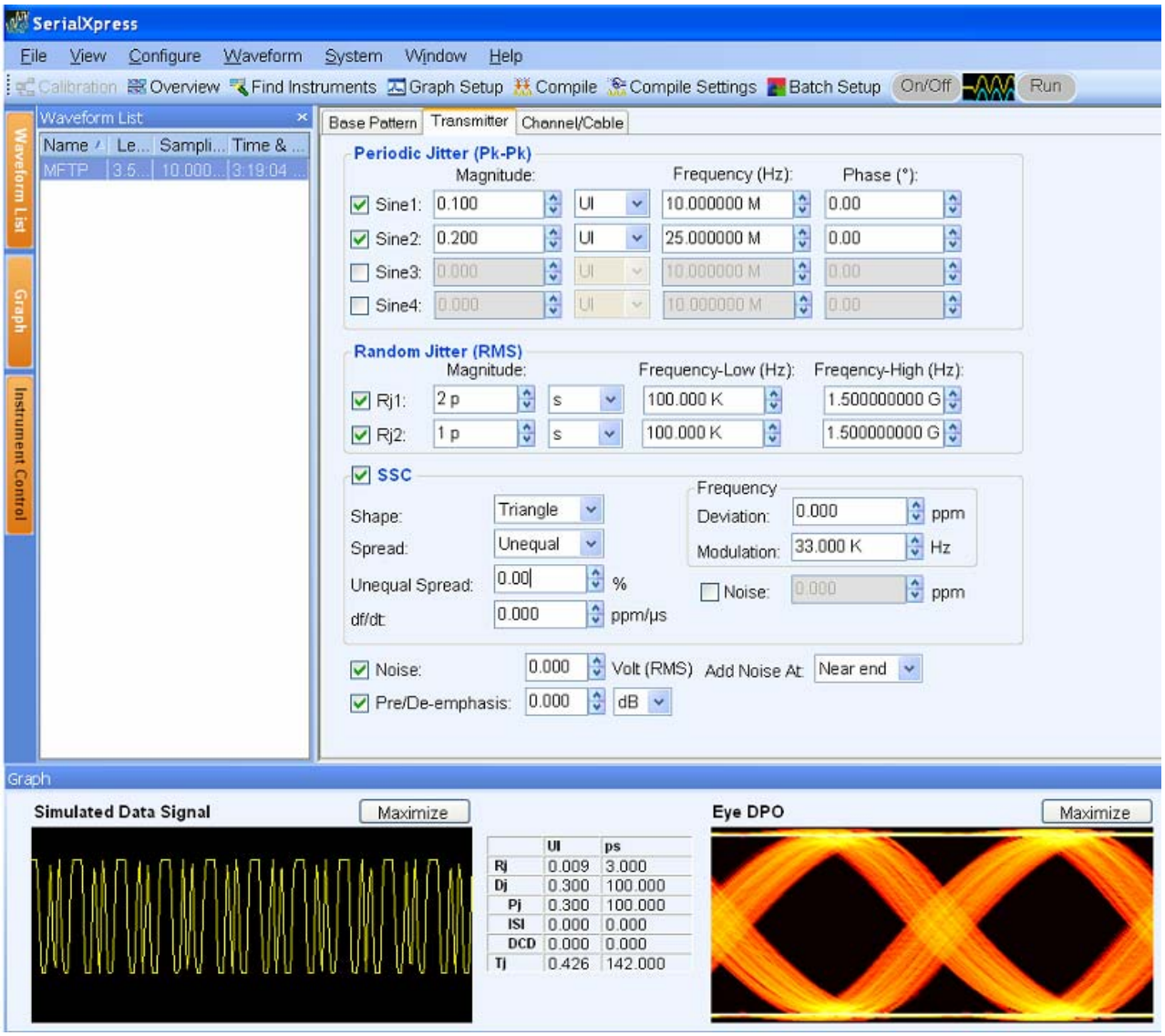
4.2.2 Detailed DP pattern creation and calibration procedure using SerialXpress.

Note - Tektronix will make every attempt to ensure that the patterns are updated and made available according to the latest Display Port CTS. The latest patterns and setup files are available on www.tek.com/displayport or from a local Tektronix representative. The below procedure can be used to create AWG patterns using SerialXpress just in case if the specs are revised and until those updated patterns are available.

1. The AWG analog output with DC Blocks and attenuators are connected to DP Receptacle fixture.
2. The markers with Rise Time filters and attenuators are configured to generate clock pattern injected to inject cross-talk.
3. The DP-P fixture is connected to another DP-R fixture using a DP cable.
4. The second DP-R fixture is then connected to the DSA70804 channel 1 and Channel 2.
5. On the AWG Open **File -> Open File**

   DP_HBRv1_calib.awg for HBR Calibration
   DP_RBRv1_calib.awg for RBR Calibration

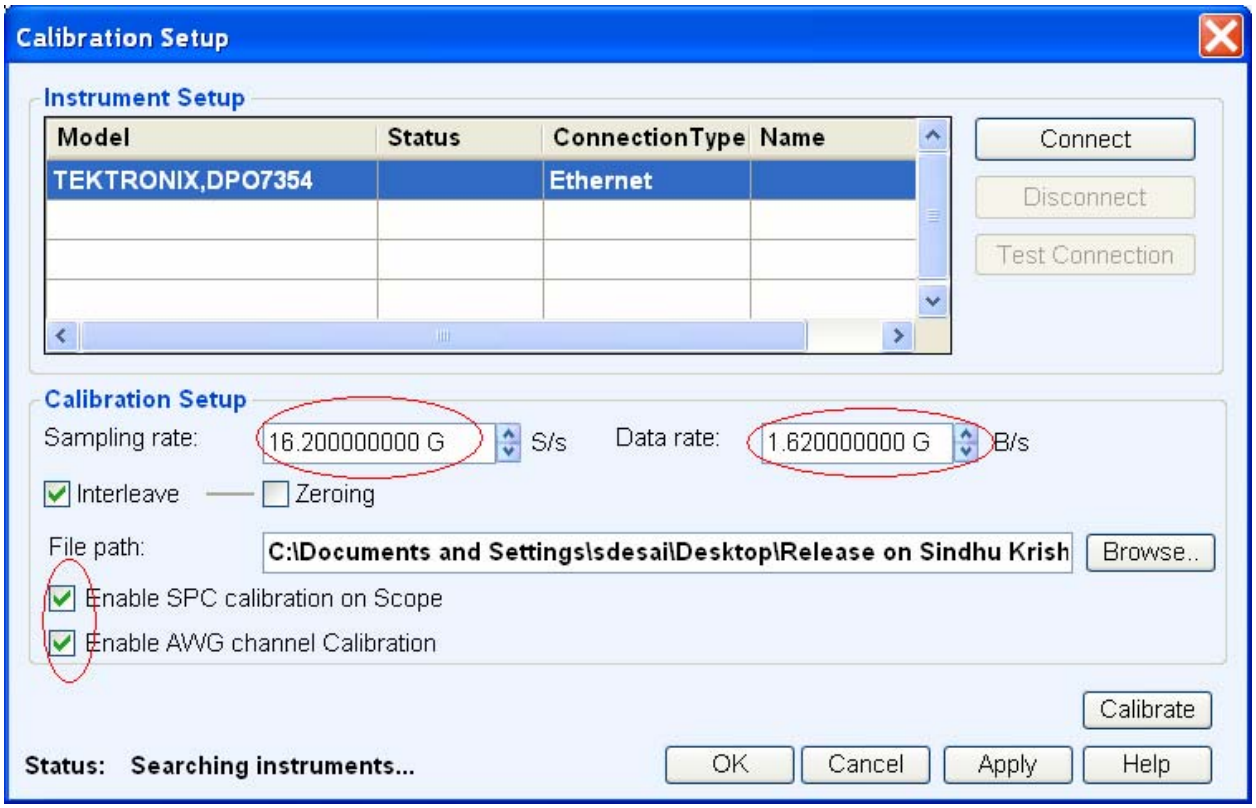
6. Run the SerialXpress application on the AWG as shown below



7. From the toolbar, click **Calibration**.
8. The Calibration window displays a table of instruments connected on the network. Select the oscilloscope and click Connect. Note that the status changes to Connected.
9. Ensure that AWG and scope are connected via LAN or GPIB cable

NOTE. *Update the TekVisa resource manager before performing calibration. Only TDS6000C, DPO70000, and DSO70000 series oscilloscopes are listed. . You can click Test Connection to test the status of the instrument.*

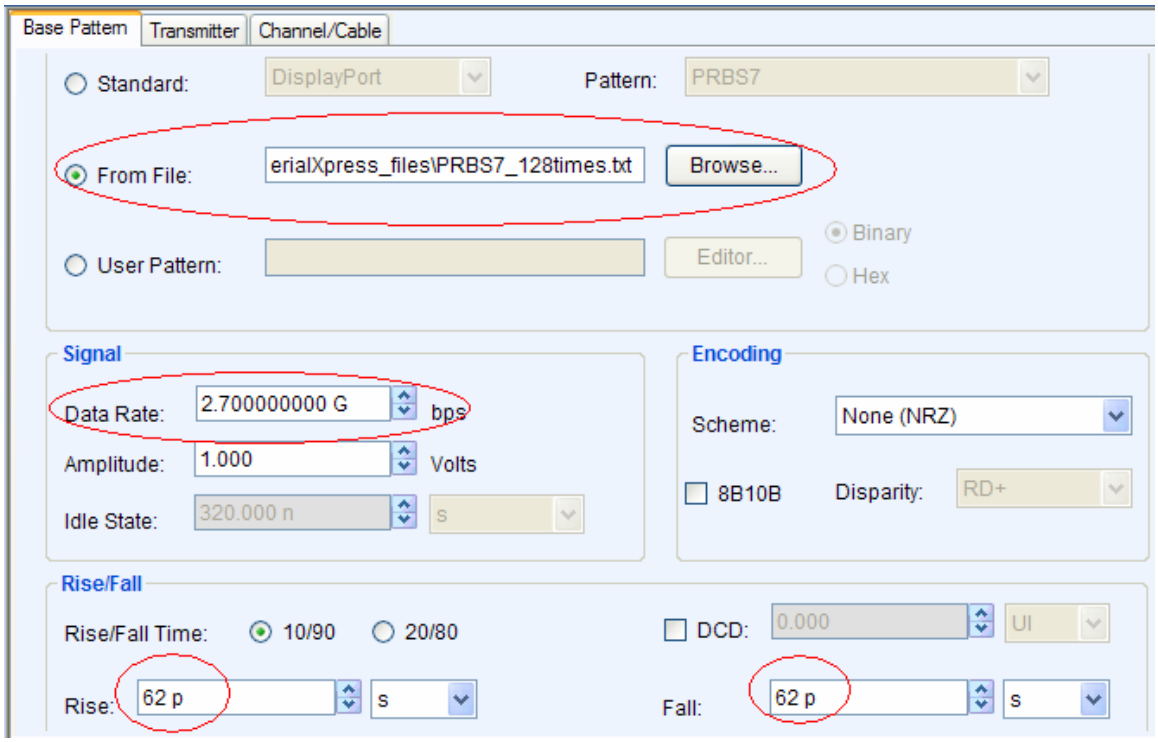
10. Sampling rate is set to 16.2 GS/s and the data rate should be entered as 1.62 Gb/s for RBR and 2.7 Gb/s HBR testing as shown below
11. Scope and AWG calibration is recommended when the system calibration is performed for first time



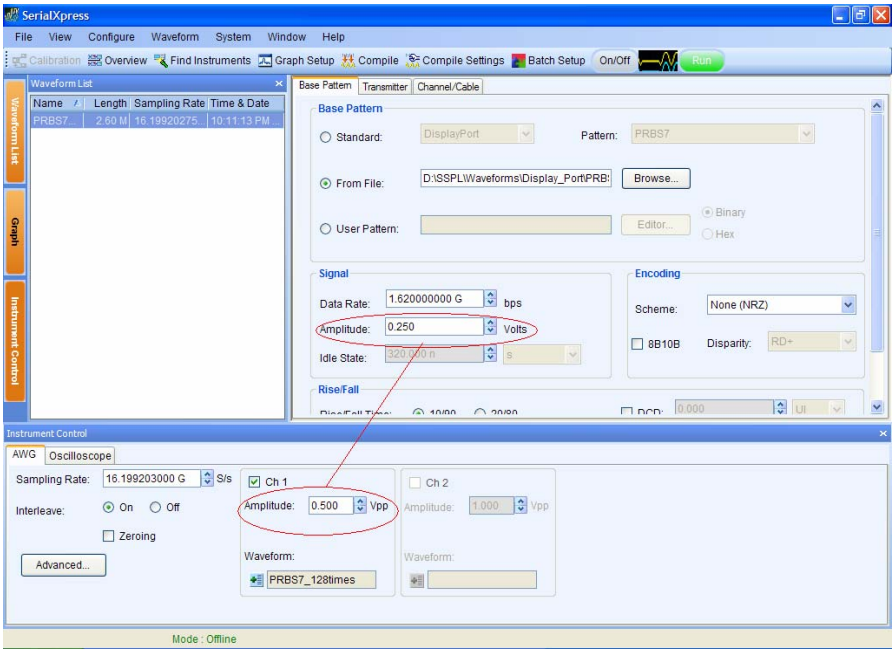
12. Calibration results are applied automatically when waveforms are compiled
13. Click **Apply** and **OK**

Jitter and EYE Height Calibration

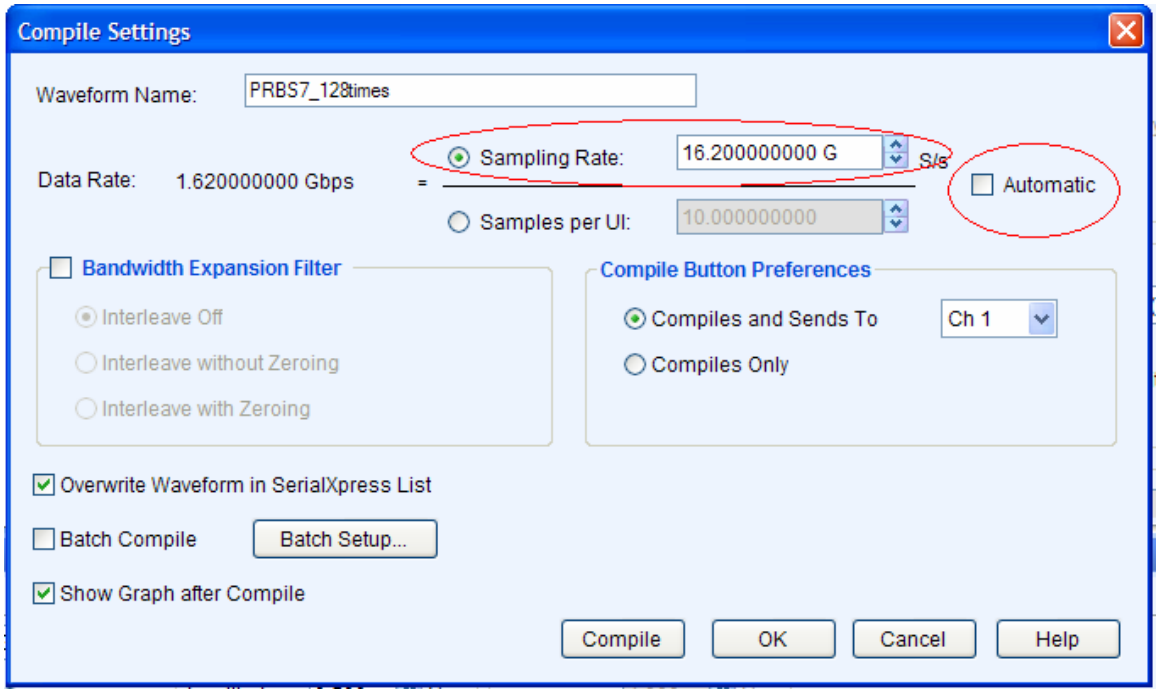
14. Go the **Base pattern Tab**
15. Input PRBS7_128times.txt (or) Freq_Lock_128times (or) Symbol_Lock_128times as appropriate as shown below
16. Ensure that the **Rise / Fall time** are set at minimum as shown below (should be 62psec)



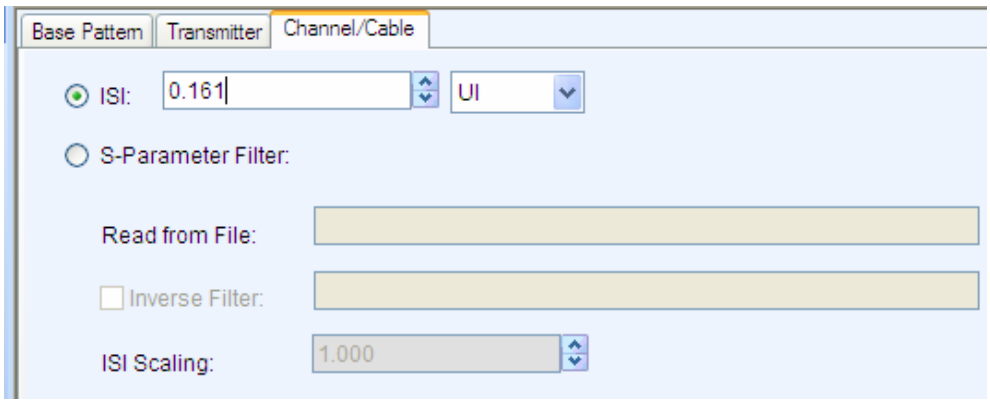
17. With AWG amplitude and SerialXpress amplitude settings, you can reach as low as 125mV for AWG7102 with opt 06. SerialXpress amplitude get multiplied with AWG amplitude setting. For e.g. when AWG amplitude is set to 500 mV and SerialXpress amplitude at 0.250 V, then the actual amplitude generated out AWG would be 125mV. Use appropriate attenuators for smaller amplitudes than 125 mV



18. From the toolbar, click **Compile Settings**
19. Uncheck **Automatic**
20. Enter **Sampling Rate** as 16.2 Gbps



21. Enter Rj and ISI values as given in the Jitter table



22. The SJ is now added so as to measure the required Tj value as given in the tables below for the respective DP data rates.

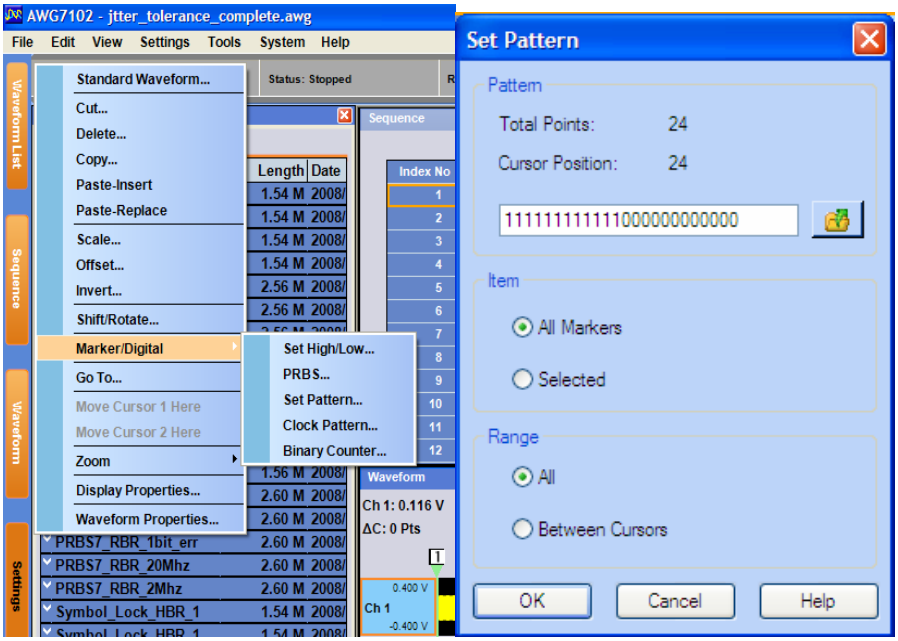
f(Sj)	Tj(JTRBRrx)	ISI	RJ(RMS)	SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1075	570	7.9	408
10	748	570	7.9	81
20	741	570	7.9	74

Table 4-2: Jitter Component Settings for Reduced Rate

Table 4-3: Jitter Component Settings for High Rate

f(Sj)	Tj(JTHBRrx)	ISI	RJ(RMS)	SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	816	161	13.2	493
10	489	161	13.2	166
20	482	161	13.2	159
100	482	161	13.2	159

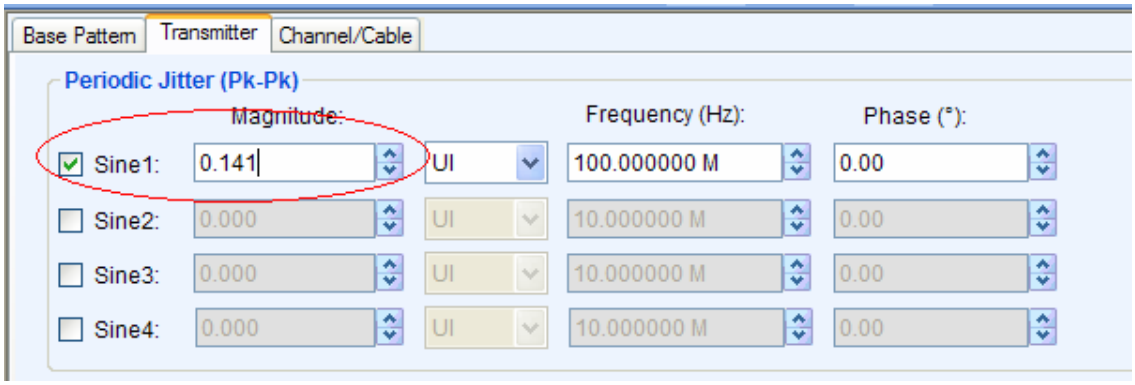
23. Press **Compile**
24. Go to the AWG User Interface
25. Right on the CH1 **M1 1 -> Marker/Digital -> Set Pattern**
26. Type "**11111111111111111111000000000000000000000000**" (20 "ones" and 20 "zeros")for RBR and "**111111111110000000000000**" (12 "ones" and 12 "zeros") for HBR as shown below



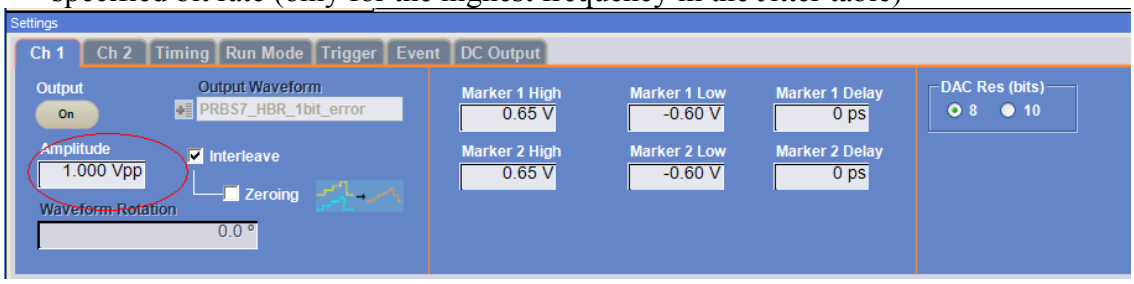
27. This would generate a half rate clock pattern (e.g. D24.3) out of the marker signals which is used as cross talk input to DUT
28. If you are using DPOJET, then the following setup files can be recalled

    i. dp-rbr-frequency-lock.set
    ii. dp-rbr-symbol-lock.set
    iii. dp-rbr-prbs7-lock.set
    iv. dp-hbr-frequency-lock.set
    v. dp-hbr-symbol-lock.set
    vi. dp-hbr-prbs7-lock.set

29. In order to achieve Tj with the aggressor signal turned on, ISI and RJ shall be calibrated to the given value and then SJ shall be increased until Tj is achieved.



30. Recompile with appropriate Sj value until the Tj value is achieved.
31. Adjust the amplitude in the AWG until you get the EYE height for the specified bit rate (only for the highest frequency in the Jitter table)

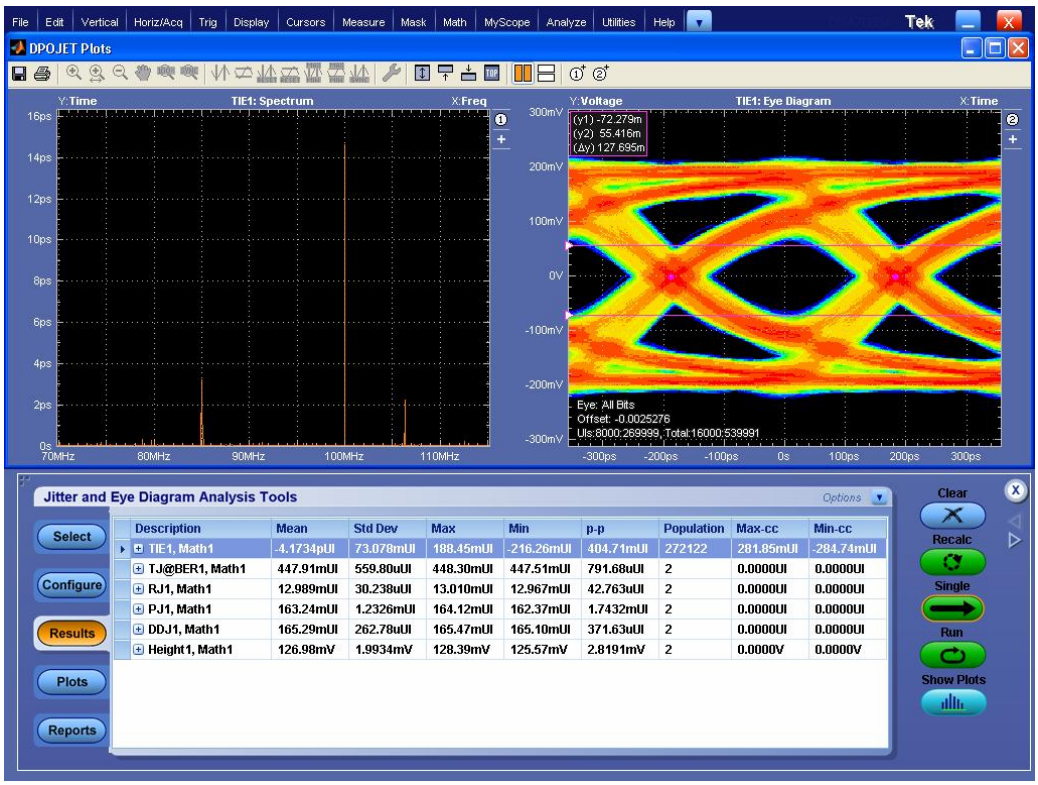


High Bit Rate: voltage = 150mVolts peak-peak (Table 3-16 of VESA DisplayPort Standard Ver. 1.1a)

Reduced Bit Rate: voltage = 46mVolts peak-peak. (Table 3-17 of VESA DisplayPort Standard Ver. 1.1a)

Note – EYE height is calibrated only for the highest Sj frequencies at all date rates supported.

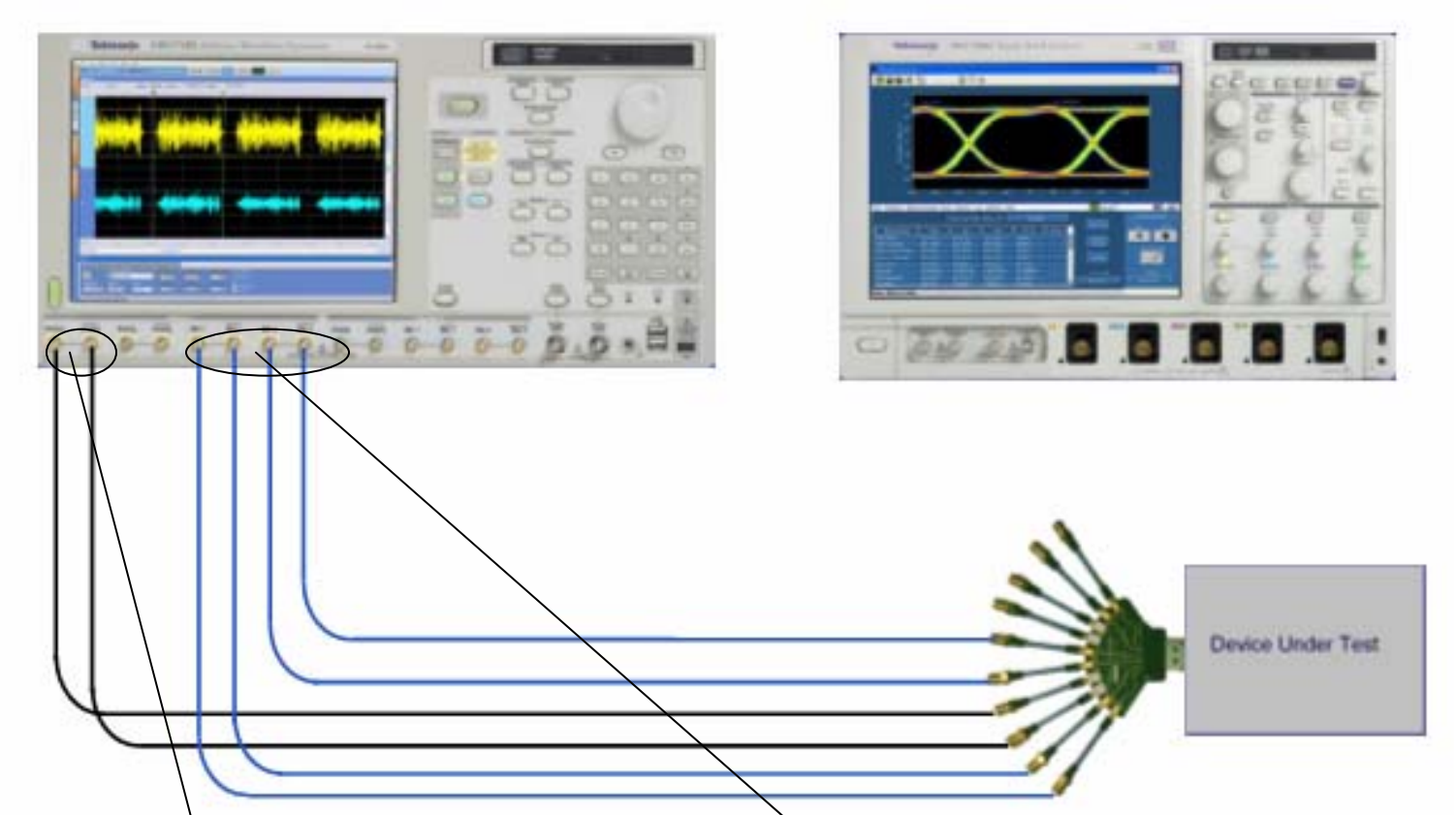
For e.g. 100 Mhz for the HBR as shown below



32. The calibrated jittered wfms are saved to the AWG DP setup folder.
33. Repeat this steps 14 – 30 for the various Sj frequencies Freq_Lock and Symbol lock patterns
34. Then these files are sequenced in AWG

4.4 APPENDIX B:

Connection Diagram for Receiver Test setup:



(Rise time filters, DC block and attenuators not shown in the connection diagram) Rise time filters and attenuators (4 nos) to be added to the output of **AWG Markers** , DC blocks and attenuators (2 nos) to the **Analog output** of CH1 and CH1 $\overline{\ }$.

Efficere DisplayPort fixture pin assignment table:

Connector Pin Assignments

Display Port Plug & Receptacle Pin Assignments		
Pin Description	Connector Pin Number	Destination Number
ML_Lane 0 (p) - Source ML_Lane 3 (n) - Sink	1	J1
Ground	2	Ground
ML_Lane 0 (n) - Source ML_Lane 3 (p) - Sink	3	J2
ML_Lane 1 (p) - Source ML_Lane 2 (n) - Sink	4	J3
Ground	5	Ground
ML_Lane 1 (n) - Source ML_Lane 2 (p) - Sink	6	J4
ML_Lane 2 (p) - Source ML_Lane 1 (n) - Sink	7	J5
Ground	8	Ground
ML_Lane 2 (n) - Source ML_Lane 1 (p) - Sink	9	J6
ML_Lane 3 (p) - Source ML_Lane 0 (n) - Sink	10	J7
Ground	11	Ground
ML_Lane 3 (n) - Source ML_Lane 0 (p) - Sink	12	J8
Ground	13	Ground
Ground	14	Ground
AUX_CH (p) - Source AUX_CH (p) - Sink	15	J9
Ground	16	Ground
AUX_CH (n) - Source AUX_CH (n) - Sink	17	J10
Hot Plug Detect	18	P2 Pin 1
Return DP_PWR	19	P2 Pin 3
DP_PWR	20	P2 Pin 2
Ground	2, 5, 8, 11, 13, 14, 16	P2 Pin 4

Connector End View
Looking into connector