

## Introduction to Logic Gates

### Materials:

- [2 Series Mixed Series Oscilloscope \(MSO\)](#)
- Direct current (DC) power supply: [2230 High Power Programmable Power Supply](#)
- AND gate (1)
- NAND gate (1)
- OR gate (1)
- NOR gate (1)
- XOR gate (1)
- Breadboard
- Jumper wires

### Procedure:

#### Task 1: Exploring Basic Logic Gates

1. Place the AND gate chip on the breadboard. Use the 2230 power supply to supply power to the chip. Connect the first input ( $b_0$ ) to the 0 bit on the PG output that is to the left of the AFG output. Connect the second input ( $b_1$ ) to the 1 bit on the PG output. Connect the channel 1 probe to the first input ( $b_0$ ), channel 2 probe to the second input ( $b_1$ ) and channel 3 probe to the output (X) on the 2 Series MSO. Turn all three channels on by clicking the colored channel buttons on the right panel. Double tap the oscilloscope screen to pull up the "WAVEFORM VIEW" menu. Under "Display Mode" select "Stacked" to view the three channels stacked on top of each other.
2. Use the 2 Series MSO pattern generator to fill out the truth table in Table 1. for the AND gate. To configure the pattern generator, click the "AFG/PG" button on the bottom of the screen. Select "PG" to pull up the menu. Use bits 0 and 1 to test the output of the AND gate (X). Select "High" for "1" inputs and "Low" for "0" inputs. Set the Amplitude to 3.3 V and the Bit Rate to 1 kb/s. Once bits 0 and 1 are configured, click the "Continuous" button to turn the pattern generator on. Record the output on channel 3 into Table 1. Repeat for all bit combinations in the table.

AND gate PN: 74LS08

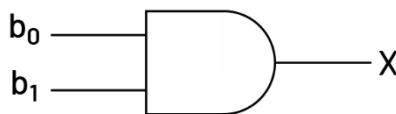


Figure 1. AND gate diagram.





$b_0$	$b_1$	X
0	0	
1	0	
0	1	
1	1	

Table 1. AND gate truth table.

- Repeats step 2 for the rest of the logic gates in Figures 2-4. Analyze the NAND, OR, and NOR gates. What is the relationship between the NAND and AND gates? What about the NOR and OR gates?

NAND gate PN: 74LS00

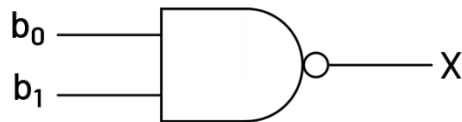


Figure 2. NAND gate diagram.

$b_0$	$b_1$	X
0	0	
1	0	
0	1	
1	1	

Table 2. NAND gate truth table.

OR gate PN: 74LS32

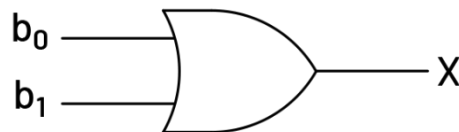


Figure 3. OR gate diagram.

$b_0$	$b_1$	X
0	0	
1	0	
0	1	
1	1	

Table 3. OR gate truth table.





NOR gate PN: 74LS02

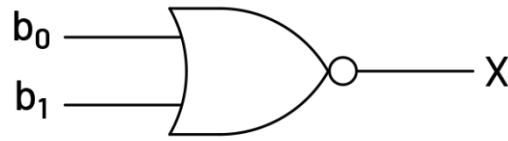


Figure 4. NOR gate diagram.

$b_0$	$b_1$	X
0	0	
1	0	
0	1	
1	1	

Table 4. NOR gate truth table.

Task 2: Exploring the Exclusive OR Gate

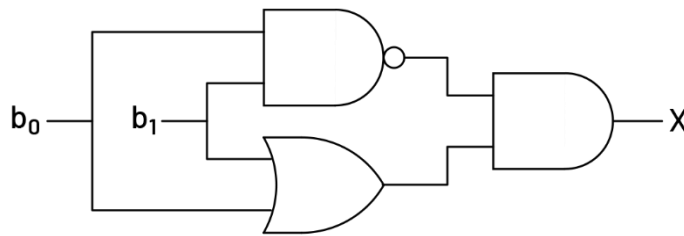


Figure 5. Combination of logic gates diagram.

1. Build the logic gates diagram in Figure 5. Use the Pattern Generator on the 2 Series MSO to generate the different bit combinations for  $b_0$  and  $b_1$ . Record the measurements from the output (X) in Table 5.

$b_0$	$b_1$	X
0	0	
1	0	
0	1	
1	1	

Table 5. Combination of logic gates truth table.

2. Repeat the Step 1 for the exclusive OR (XOR) gate in Figure 6. And record the measured outputs in Table 6. Compare Tables 5 and 6. What conclusions can be drawn from the similarities to the logic gate configuration in Figure 5 to the XOR gate in Figure 6?





PN: 74LS86

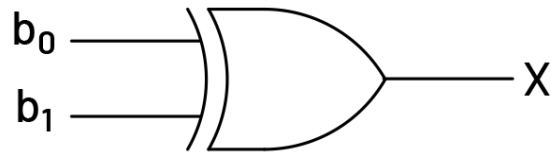


Figure 6. XOR gate diagram.

$b_0$	$b_1$	$X$
0	0	
1	0	
0	1	
1	1	

Table 6. XOR gate truth table.

Instructor Notes:

Answer key to logic gate truth tables:

$b_0$	$b_1$	$X$
0	0	0
1	0	0
0	1	0
1	1	1

Table 1. AND gate truth table.

$b_0$	$b_1$	$X$
0	0	1
1	0	1
0	1	1
1	1	0

Table 2. NAND gate truth table.

$b_0$	$b_1$	$X$
0	0	0
1	0	1
0	1	1
1	1	1

Table 3. OR gate truth table.





$b_0$	$b_1$	X
0	0	1
1	0	0
0	1	0
1	1	0

Table 4. NOR gate truth table.

$b_0$	$b_1$	X
0	0	0
1	0	1
0	1	1
1	1	0

Table 5. Combination of logic gates truth table.

$b_0$	$b_1$	X
0	0	0
1	0	1
0	1	1
1	1	0

Table 6. XOR gate truth table.

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