D Flip-flop Latch

Materials:

- 2 Series Mixed Series Oscilloscope (MSO)
- Direct current (DC) power supply: 2230 High Power Programmable Power Supply
- D – Flip-flop Latch (1)
- Breadboard
- Jumper wires

Procedure:

D Flip-Flop PN: 74LS74

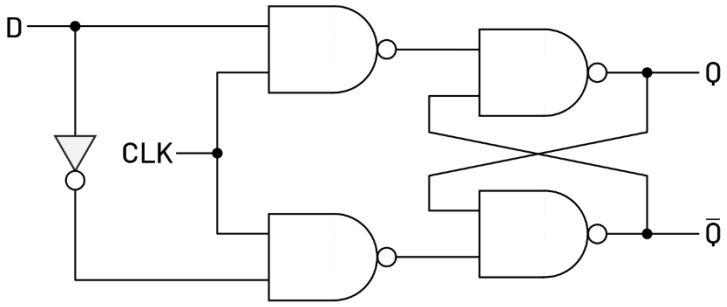

Figure 1. D flip-flop latch diagram.

1. To test the D flip-flop gate, place the chip on the bread board. Use the DC power supply to supply the require voltage to the chip and connect the chip's ground to the power supply ground. Connect the PRESET and CLEAR pins on the chip to the same input voltage to deactivate the pins. Make sure to use the correct pinout diagram for the chip to avoid damaging the latch.

2. To generate a clock signal, use either an external AFG or the internal AFG on the 2 Series MSO. Generate a square wave with an amplitude of 2 V and a 1 V offset. Set the frequency of the square wave to 50 Hz. Connect this signal to the CLK pin of the flip-flop. For the data pin (D), use the built-in pattern generator on the oscilloscope. Connect the b_0 bit to the data pin of the chip. Make sure to tie both the AFG, pattern generator and power supply grounds together.

3. To observe the behavior of the D flip-flop, connect the data input (D) to channel 1 of the 2 Series MSO and the CLK input to channel 2. Connect the outputs to channels 3 and 4. Turn all four channels on by using the colored channel buttons on the right-side panel. Tap and hold onto the oscilloscope's screen and tap "Stacked Display Mode" to see all four channels.

4. Turn on the AFG and power supply. Observe the waveforms with the data input (D) low. Does the Q or the $\bar{Q}$ output change? Now set the data input (D) high by tapping the "PG" button at the bottom of the screen near the AFG button. Once the menu is opened, set the first bit (b_0) to "High". Do the outputs change?

5. Now, remove the clock signal by turning off the AFG. Select the "Toggle" option for b_0 in the pattern generator menu. Set the bit frequency to 50 b/s and observe the outputs. Since the data input is switching between high and low, are the outputs also switching? Why or why not are the outputs changing?

6. Turn back on the AFG clock signal and keep the data input the same as the previous step. Observe the outputs on channels 3 and 4 compared to the inputs. When do the outputs change in relation to the clock input (Channel 2)? Do your observations match the truth table shown in Table 1.

CLK	D	Q	$\bar{Q}$	Description
0	X	Q_0	$\bar{Q}_0$	Memory
0→1(↑)	0	0	1	Set
0→1(↑)	1	1	0	Set

Table 1. D flip-flop latch truth table.

Instructor Notes:

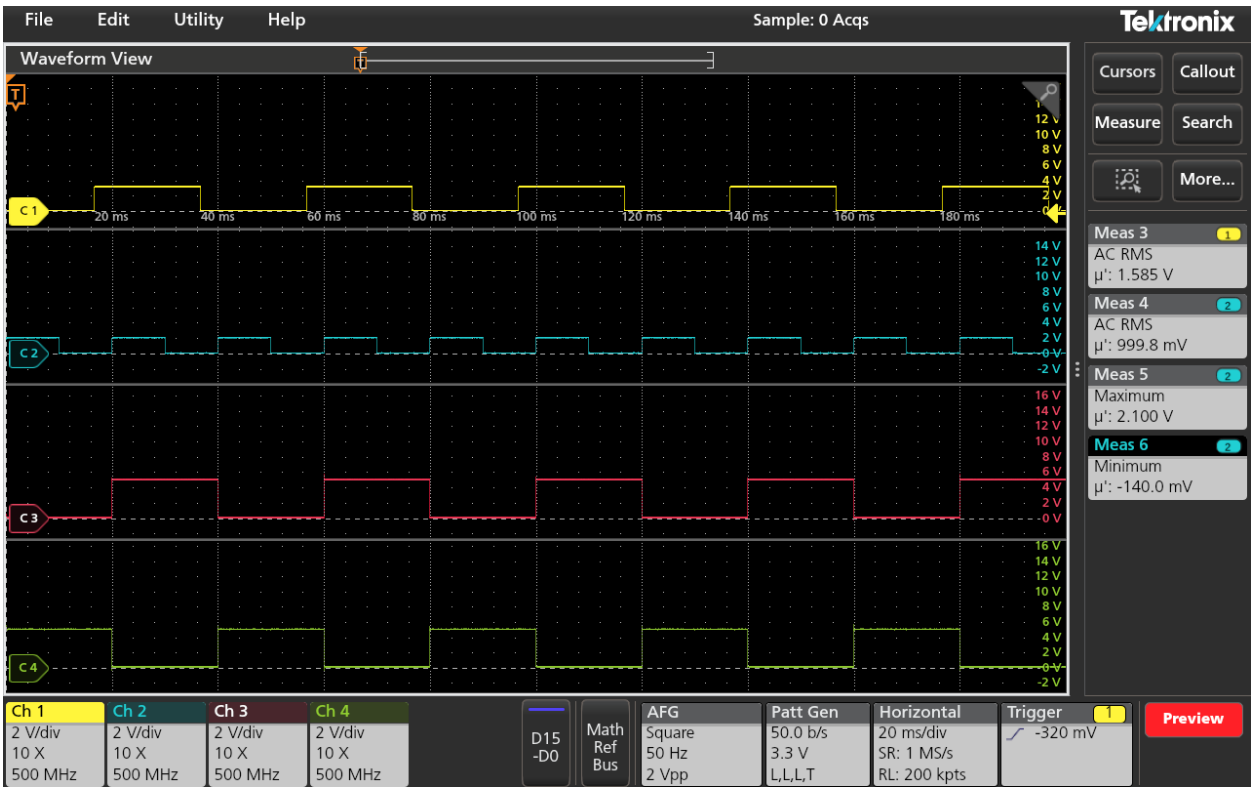

Figure 2. Waveforms from Task 1, step 6. Channel 1 is the data input, channel 2 the CLK, channel 3 is the Q output and channel 4 is the $\bar{Q}$ output.

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