

# Tektronix Innovation Forum

Enabling Innovation in the Digital Age

工业界最新高速接口测试方案

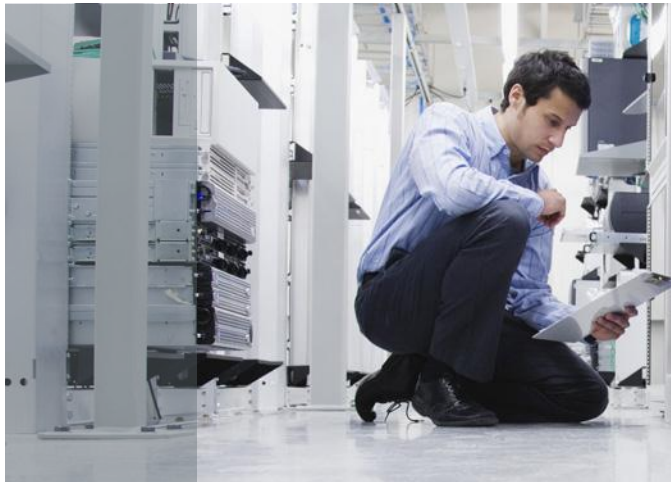
Presenter: Cyphei Chang

**Tektronix**<sup>®</sup>

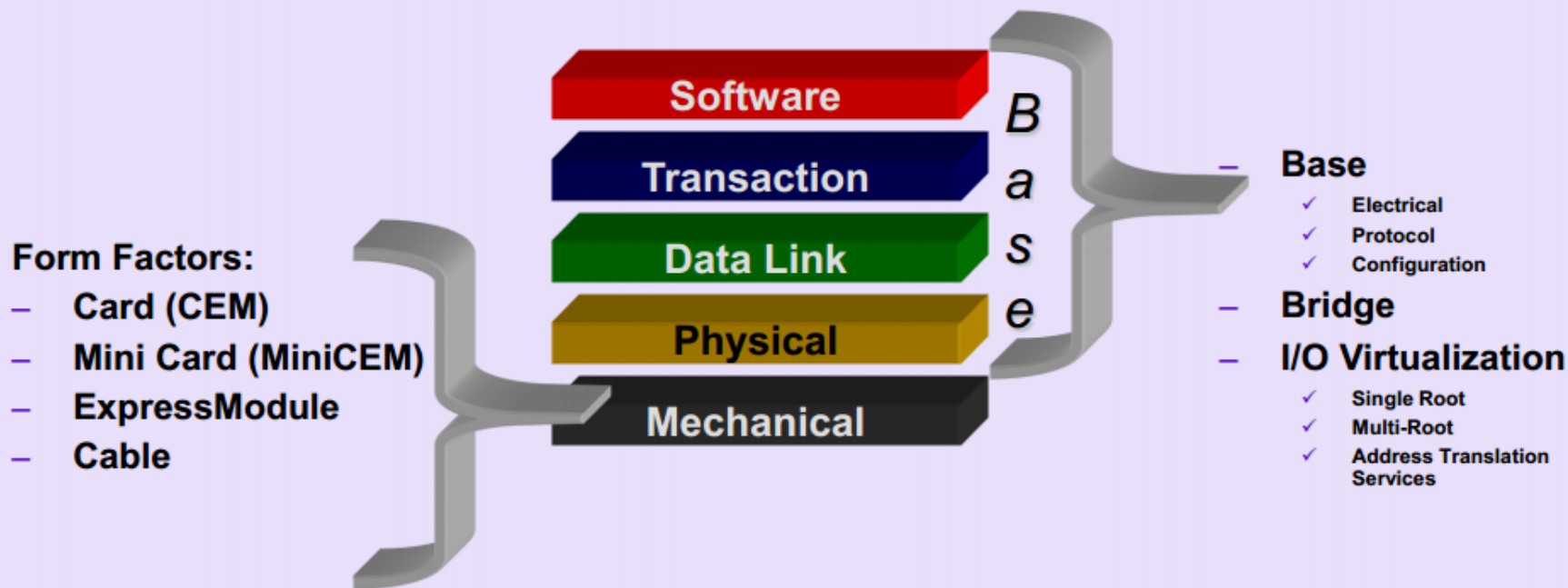


# PCIe Gen3 Tx Solutions

AE University – July 2013

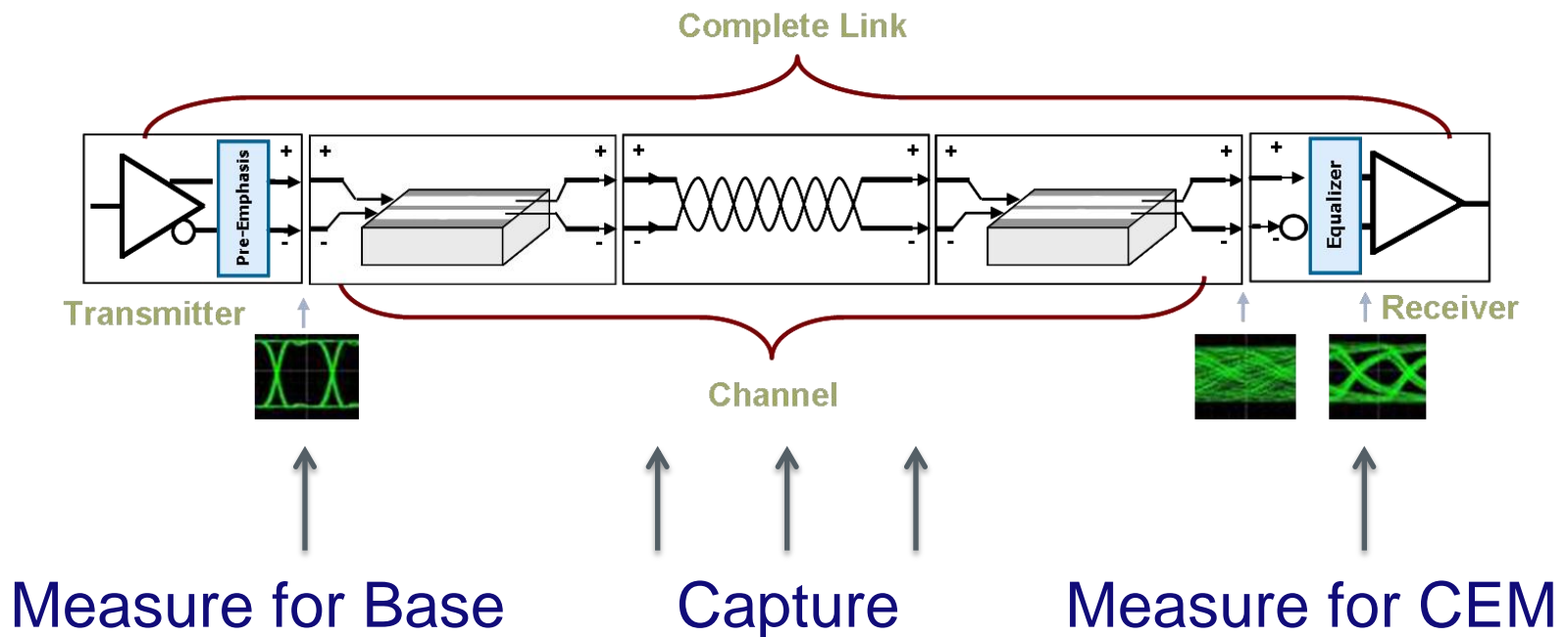


# PCIe Specifications



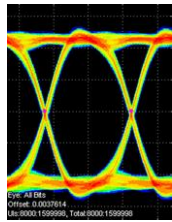
# PCIe Base vs CEM Testing

- What test point each type of testing addresses?
- How do we get to see the signal at the point of interest?

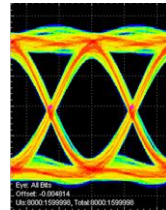


# System (Base Spec) Tx Testing

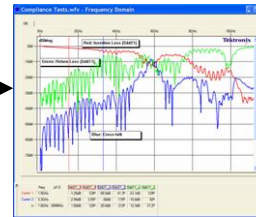
- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not possible
- De-embedding is required to see what the signal looks like at the pins of the TX, without the added effects of the channel
- S-Parameters are acquired on the replica channel



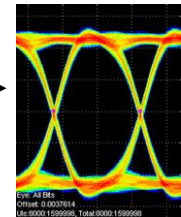
Signal at Tx Pins



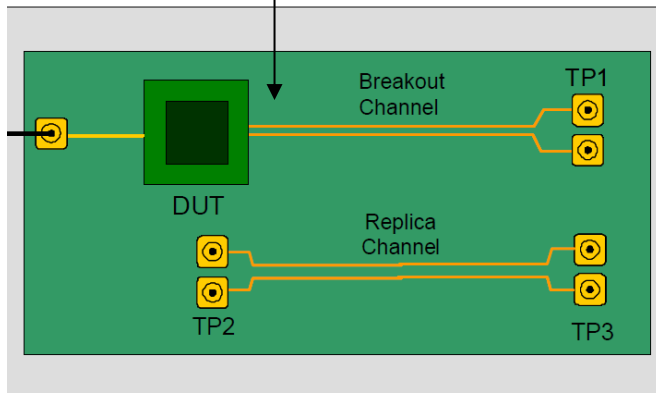
Measured Signal at TP1



De-embed using S-Parameters

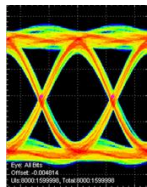


Signal with Channel Effects Removed

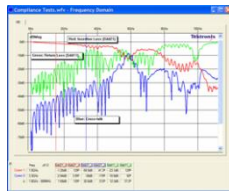


# Add-In Card (CEM Spec) Tx Testing

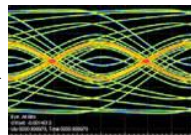
- CEM Specification Measurements are defined at the slicer of a receiver
- Signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements



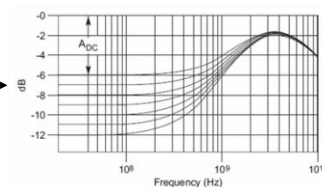
Signal Acquired from Compliance Board



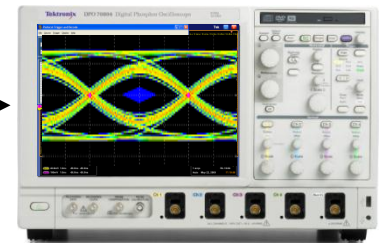
Embed Compliance Channel and Package



Closed Eye due to the Channel



Apply CTLE + DFE

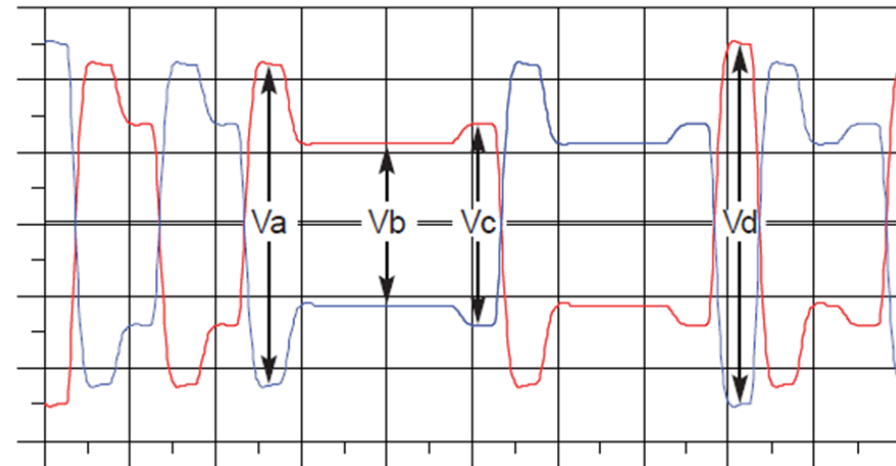


Open Eye for Measurements

# Compliance Patterns

- Once in compliance mode, bursts of 100MHz clock can be used to cycle through various settings of compliance patterns to perform, Jitter, voltage, timing measurements.

Data Rate	Preshoot	De-emphasis
2.5 GT/s,		-3.5 dB
5.0 GT/s,		-3.5 dB
5.0 GT/s,		-6.0 dB
8.0 GT/s,	P0 = 0.0	-6.0±1.5dB
8.0 GT/s,	P1 = 0.0	-3.5±1.5dB
8.0 GT/s,	P2 = 0.0	-4.4±1.5dB
8.0 GT/s,	P3 = 0.0	-2.5±1dB
8.0 GT/s,	P4 = 0.0	0.0dB
8.0 GT/s,	P5 = 1.9±1dB	0.0dB
8.0 GT/s,	P6 = 1.9±1dB	0.0dB
8.0 GT/s,	P7 = 1.9±1dB	-6.0±1.5dB
8.0 GT/s,	P8 = 1.9±1dB	-3.5±1dB
8.0 GT/s,	P9 = 1.9±1dB	0.0dB
8.0 GT/s,	P10 = 1.9±1dB	Test Max Boost Limit



$$\text{De-emphasis} = 20\log_{10} Vb/Va$$

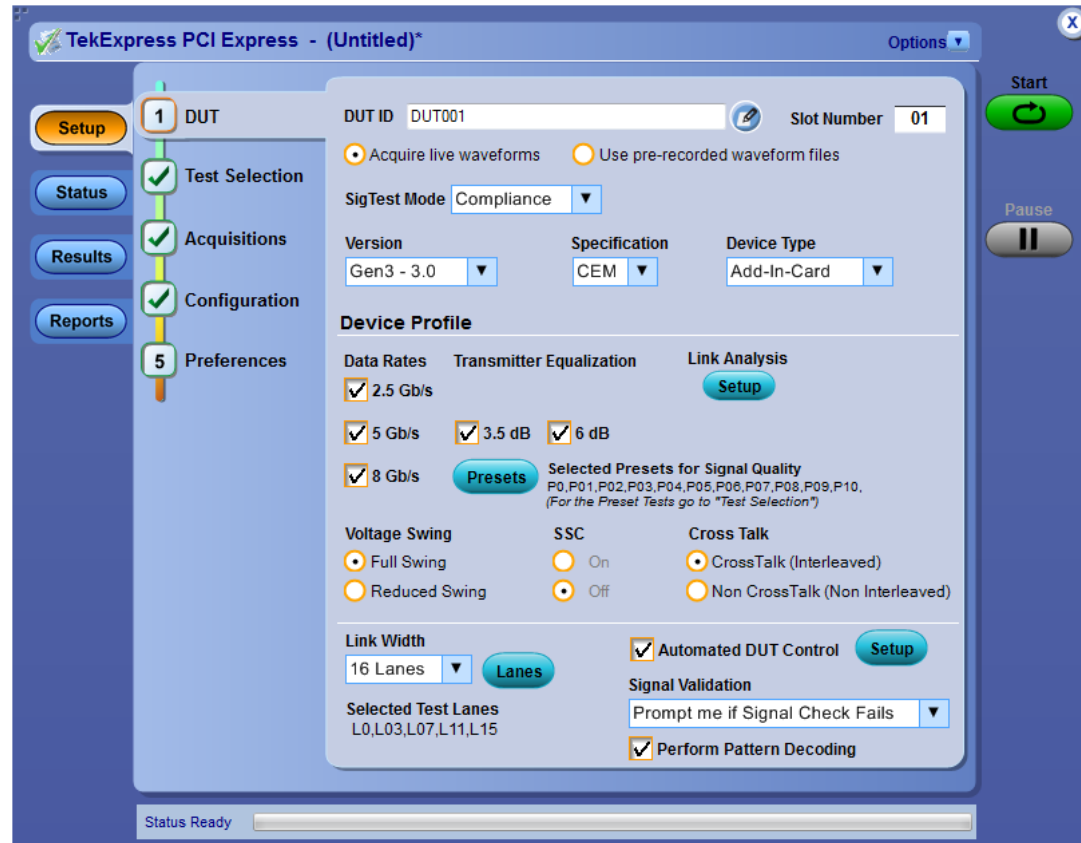
$$\text{Preshoot} = 20\log_{10} Vc/Vb$$

$$\text{Boost} = 20\log_{10} Vd/Vb$$

# Introducing the NEW Opt PCE3

- TekExpress Automation for Tx Compliance with unique features including:

- ✓ Sets up the Scope and DUT for testing
- ✓ Toggles thru and verifies the different Presets and Bit Rates
- ✓ Tests multiple slots and lanes
- ✓ Acquires the data
- ✓ Processed with PCI-SIG SigTest
- ✓ Provides custom reporting





# What's New in Option PCE3 Release 2?

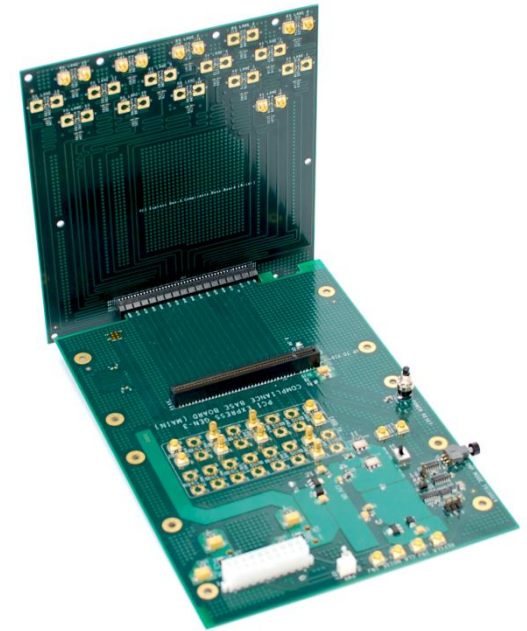
- Supports a faster, Python-based sequencer
  - Much faster program launch with the test time reduced by ~50%
  - 64-bit only application (requires 70K C/D oscilloscopes with Win7 64-bit)
    - Will maintain earlier 32-bit release for 70K A/B oscilloscopes with WinXP 32-bit on [www.tek.com](http://www.tek.com)
  - Smaller installer
- SigTest.exe (Command-Line) integration
  - Supports PCI-SIG recommended SigTest.exe testing
  - User can switch between DLL and Command-Line (.exe) modes
  - All result are populated in Tektronix result/report format in command line mode
- Support multiple versions of SigTest
  - User option to select required version and run
- Broader AWG/AFG support for automatic DUT toggle (*Min 2ch & 100MHz Burst mode*)
  - AFG3252/C
  - AWG5002B/C, AWG5012B/C, AWG5014B/C
  - AWG7082B/C, AWG7122B/C
  - AWG70001A/2A
- Incorporates customer & field feedback
  - Crosstalk option is added
  - Gen2 System-Board limit issue fixed
  - Addresses 6 customer-reported issues & ~30 PCIe Workshop-reported issues

# Automation Simplifies Tx Testing

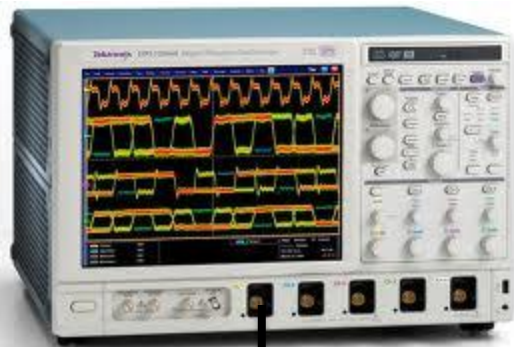
- While convenient single capture capability is essential, automation makes the testing practical
- Iterate over multiple presets and lanes
- Gather results in a single report
- Provide means for quick switch to debugging and additional measurements
- Remove test fixture effects by using de-embedding

# Add-In Card Test Fixture

- Compliance Base Board (CBB)
  - Used for Testing Add-In cards
  - All Tx / Rx Lanes are routed to SMP
  - Compliance Mode Toggle Switch
  - Low Jitter Clean Reference Clock
  - Separate CBB for Gen 1/2/3



Compliance Base Board (CBB)



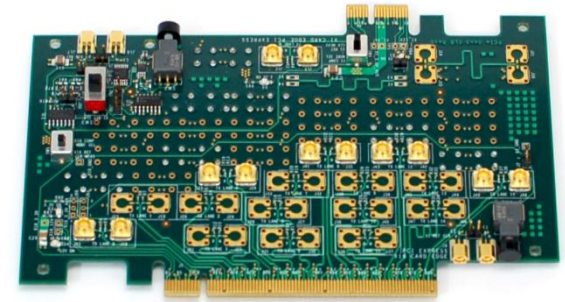
Data

Add-In  
Card

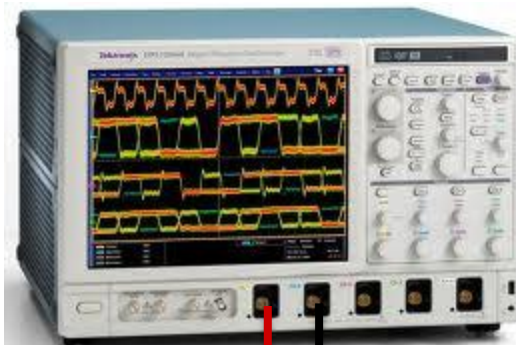
CBB with Multiple Slots of different widths and toggle switch

# System Test Fixtures

- Compliance Load Board (CLB)
  - Used for testing System Boards
  - All Tx / Rx Lanes and Ref Clk routed to SMP
  - Compliance Mode Toggle Switch
  - Various types of Edge Connectors to support different types of Slots on System Boards
  - Separate CLB's for Gen1/2/3



Compliance Load Board (CLB)



Data

Ref Clk

CLB  
with  
toggle  
switch

System Board / Mother Board with Multiple Slots

# TekExpress Automation for Tx Compliance - Setup

The screenshot shows the TekExpress PCI Express software interface. On the left, a navigation pane includes buttons for Setup, Status, Results, and Reports, and a vertical progress indicator with steps 1 (DUT), Test Selection, Acquisitions, Configuration, and 5 (Preferences). The main area is divided into several sections:

- DUT Section:** DUT ID: DUT001, Slot Number: 01. Radio buttons for "Acquire live waveforms" (selected) and "Use pre-recorded waveform files".
- SigTest Mode:** Compliance (dropdown).
- Version/Specification/Device Type:** Gen3 - 3.0, CEM, Add-In-Card.
- Device Profile:** Data Rates (2.5, 5, 8 Gb/s), Transmitter Equalization (3.5 dB, 6 dB), Link Analysis (Setup button), Voltage Swing (Full/Reduced), SSC (On/Off), Cross Talk (CrossTalk/Non CrossTalk).
- Link Width:** 16 Lanes, Lanes button.
- Selected Test Lanes:** L0,L03,L07,L11,L15.
- Automation:** Automated DUT Control (checked), Signal validation (Prompt me if Signal Check Fails), Perform Pattern Decoding (checked).

On the right side of the interface are Start and Pause buttons. Four callout boxes point to specific features:

- Run Analysis on Live or Pre-Recorded Data:** Points to the radio buttons for waveform acquisition.
- Type of test / device selection:** Points to the Version, Specification, and Device Type dropdowns.
- Test selection:** Points to the SigTest Mode dropdown.
- Automate DUT control:** Points to the Automated DUT Control checkbox.

# TekExpress Automation for Tx Compliance – Test

The screenshot displays the TekExpress PCI Express software interface. The main window title is "TekExpress PCI Express - (Untitled)\*". On the left, a vertical navigation pane shows five steps: 1. DUT (checked), 2. Test Selection (highlighted), 3. Acquisitions, 4. Configuration, and 5. Preferences. The main area is titled "PCIe : System-Board : Gen3 - 3.0 : CEM". It features a "Signal Test" tab and a "Preset Test" tab. Below these are three buttons: "Deselect All", "Select Required", and "Select All". A list of tests is shown with checkboxes, all of which are checked:

- 2.5Gbps
- 5Gbps
- 8Gbps
  - Unit Interval
  - Mask Hits (All Bits)
  - Composit Eye Height
  - Transition Eye Diagram
  - Non Transition Eye Diagram
  - Min Eye Width
  - Min Time Between Crossovers
  - TJ @ E-12
  - Dj\_dd
  - RJ(RMS)
  - Peak to Peak Jitter

Below the list is a "Test Description" section with a text area and two buttons: "Show MOI" and "Schematic". On the right side of the main window, there are "Start" and "Pause" buttons. A red box highlights the test selection area, and a line connects it to a separate box labeled "Test Selection".

Test Selection

# TekExpress Automation for Tx Compliance – Reports

TekExpress PCI Express - (Untitled)\*     Options ▾

Overall Test Result ✔ Pass     Preferences ▾

Signal Test Preset Test

Setup  
Status  
Results  
Reports

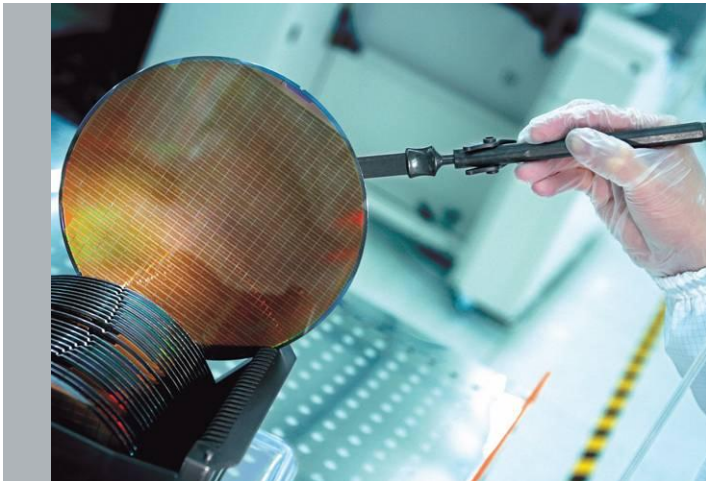
Description	Details	Generation	Pass/Fail	Value	Margin
▶ Lane0			✔ Pass		
- Unit Interval	Mean Unit Interval	8Gbps P07	✔ Pass	125.0090 ps	L: 0.0465 ps H: 0.0235 ps
- High Limit			✔ Pass	125.0325	
- Low Limit			✔ Pass	124.9625	
+ Mask Hits(All Bits)	Mask Hits	8Gbps P07	✔ Pass	0.0000 hits	H: 0.0000 hits
+ Composit Eye Height	Composit Eye Height	8Gbps P07	✔ Pass	105.7689 mV	L: 71.7689 mV
+ Transition Eye Diagram	Min Transition Eye Height	8Gbps P07	Informative	107.2269 mV	N.A
+ Transition Eye Diagram	Min Transition Voltage	8Gbps P07	✔ Pass	-0.1264 mV	L: 599.8736 mV
+ Transition Eye Diagram	Max Transition	8Gbps P07	✔ Pass	0.1289 mV	H: 599.8711 mV
+ Transition Eye Diagram	Min Transition Top Margin	8Gbps P07	✔ Pass	0.0259 mV	L: 0.0259 mV
+ Transition Eye Diagram	Min Transition Bottom Margin	8Gbps P07	✔ Pass	-0.0314 mV	H: 0.0314 mV
+ Transition Eye Diagram	Transition Eye Mask Hits	8Gbps P07	✔ Pass	0.0000 hits	H: 0.0000 hits
+ Non Transition Eye Diagram	Min Non Transition Eye Height	8Gbps P07	Informative	112.3181 mV	N.A
+ Non Transition Eye Diagram	Min Non Transition	8Gbps P07	✔ Pass	-0.1274 mV	L: 599.8726 mV

Status Completed.

Start  
Pause  
Clear

# PCIe Gen3 Rx Solutions

AE University – July 2013



**Tektronix**<sup>®</sup>



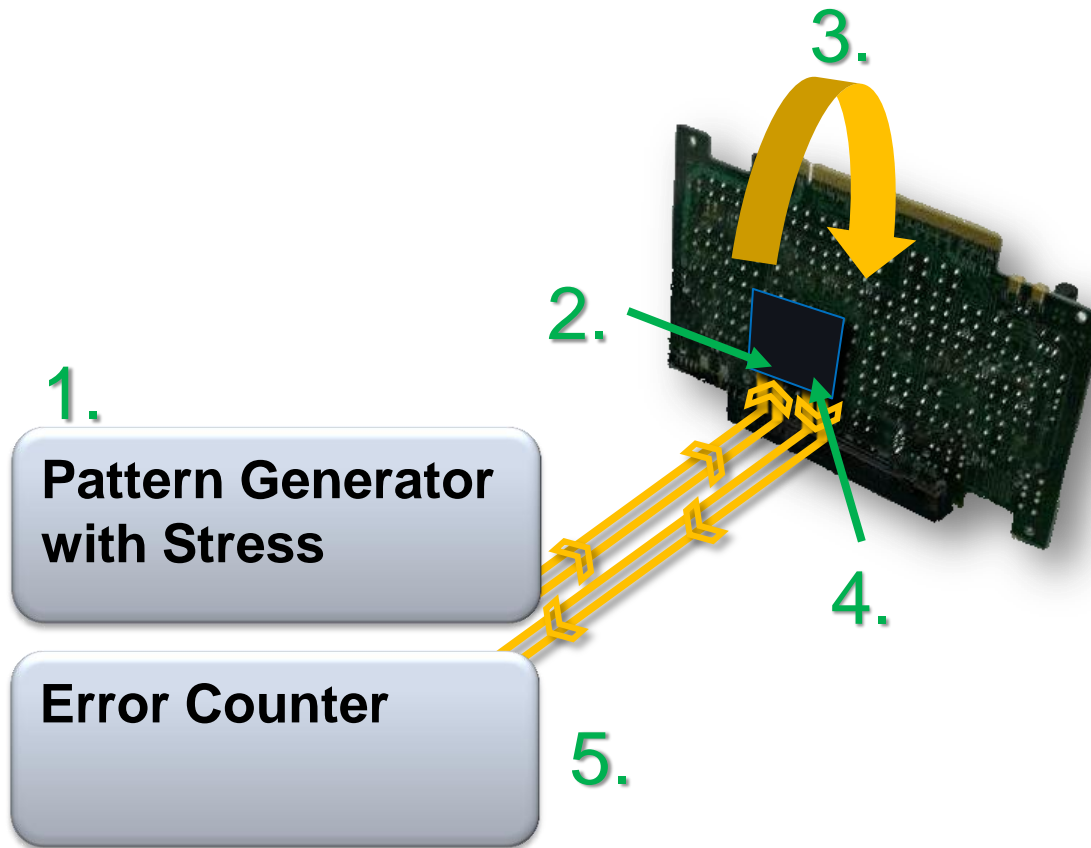
# Essentials of Rx Testing

- PCIe 3.0 introduced formal Rx testing
- Based on stress testing of the DUT in loopback
  - Looped back signal must be the same as stressed signal
- DUT must support loopback initialization and training
- Impairments in stress must be controlled and repeatable
- DUT must receive stressed signals without errors (errors below specified ratio  $10^{-12}$ )

# Testing Challenges in Rx

- Rx: Support of loopback
  - ✓ Loopback initialization
  - ✓ Proper training conditions
  - ✓ Correct stress and signal impairment levels
- How to achieve required confidence level and beyond?
  - ✓ Length of test (Rx)

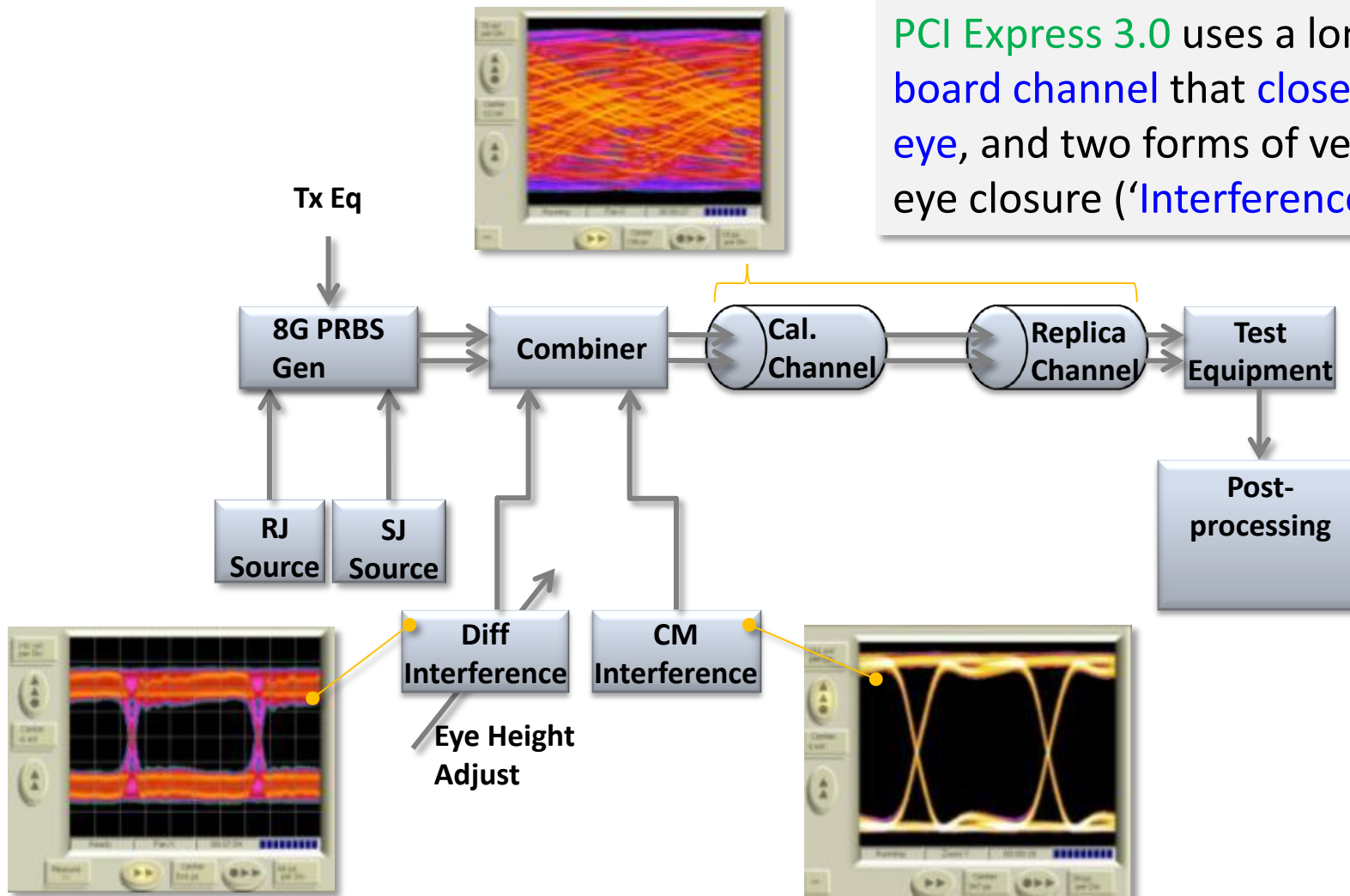
# Basic Receiver Testing



At the simplest level, receiver testing is composed of:

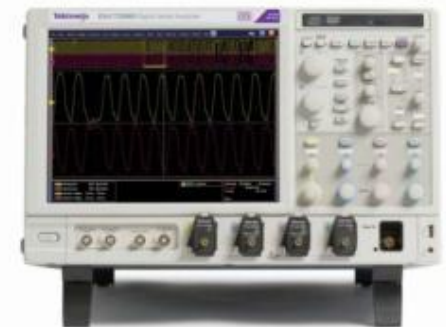
1. Send **impaired signal** to the receiver under test
2. The **receiver decides** whether the incoming bits are a one or a zero
3. The chip **loops back** the bit stream to the transmitter
4. The **transmitter sends out** exactly the bits it received
5. An **error counter** compares the bits to the expected signal and looks for mistakes (errors)

# Stress Composition

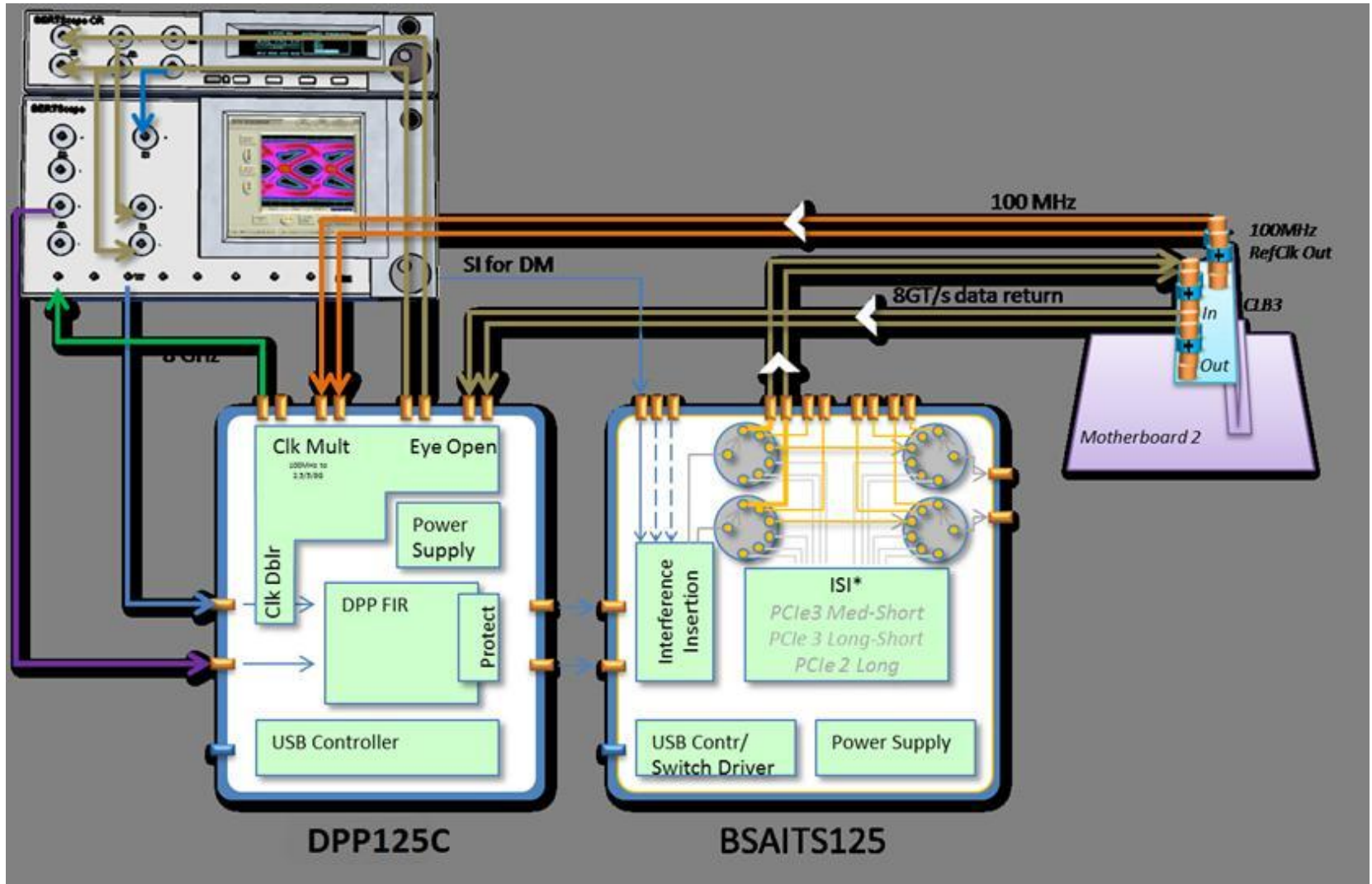


# Components of a PCIe3 Receiver Test Solution

- BERTScope C Model
  - PG, stressed eye sources, ED
- New! DPP125C Option ECM
  - Eye opener, Clock doubler/Multiplier
- New! BSAITS125
  - CM/DM interference
  - ISI for Gen2 & Gen3
  - Option EXP for variable ISI
- New! CR125A Opt PCIE8G
  - PLL analysis for Gen1/2/3
- New! BSAPCI3 SW
  - Auto calibration, Link training, and test
- Cables, adapters, compliance boards
- DSA/DPO/MSO70K Series Oscilloscope
  - Stressed Eye Calibration



# Typical PCIe3 Rx Test Configuration



# Automatic Calibration

- Due to complex test setup and variations in DUTs and test equipment just dialing up the settings on the signal source is not sufficient
- Stress must be measured and adjusted
- Automatic calibration is used to achieve the right amount of stress
- Margin testing complements the compliance testing
  - Help understand your device's margins.
  - How much additional stress does it tolerate?

# Stressed Eye Calibration Setup


The screenshot displays the 'PCIe 3.0 Receiver Testing, 0.54' software interface. On the left is a navigation menu with sections: Preferences (Start Connect, Help), Calibrations (DPP, Amplitudes, Stressed Eye), Execute Tests (Preset Test, BER Test), and View Test Results (BER Test). At the bottom are status indicators: No BSC, No DPP, No CR, No Scope, and No Sigtest.

The main window is titled 'EYE Calibration' and shows a 'Cabling Diagram'. The diagram illustrates the signal path for calibration. It includes an 'SI Combiner' connected to an 'SI Out (Rear)' port of a device. The signal path involves 'Gen 3 CBB (Main)' and 'Gen 3 CBB (Riser)' components, with 'RX Lane 0' and 'TX Lane 0 (Out) (Rear)' connections. A green line indicates the signal path leading to an 'RT Scope for Calibration'. Other components shown include 'Gen 3 CLB', 'Digital Pre-Emphasis', 'Eye Opener', and 'Reference Clock Multiplier'.



# Navigate Presets in Rx Testing

BER Test



**Configure BER Sweep**

FS  Boost Limit  dB Click individual cells or row/column headers to select

Select
  P0
  P1
  P2
  P3
  P4
  P5
  P6
  P7
  P8

PS	DE	C+1																	
		Boost	0/24	1/24	2/24	3/24	4/24	5/24	6/24	7/24	8/24								
0/24		0.0	0.0	0.0	-0.8	0.0	-1.6	0.0	-2.5	0.0	-3.5	0.0	-4.7	0.0	-6.0	0.0	-7.6	0.0	-9.5
	P4	0.0		0.8	P3	1.6	P3	2.5	P1	3.5	P2	4.7	P0	6.0		7.6		9.5	
1/24		0.8	0.0	0.8	-0.8	0.9	-1.7	1.0	-2.8	1.2	-3.9	1.3	-5.3	1.6	-6.8	1.9	-8.8		
			0.8		1.6		2.5		3.5		4.7		6.0		7.6		9.5		
2/24		1.6	0.0	1.7	-0.9	1.9	-1.9	2.2	-3.1	2.5	-4.4	2.9	-6.0	3.5	-8.0				
	P5	1.6		2.5		3.5		4.7		6.0	P7	7.6		9.5					
C-1 3/24		2.5	0.0	2.8	-1.0	3.1	-2.2	3.5	-3.5	4.1	-5.1	4.9	-7.0						
	P6	2.5		3.5		4.7		P8	6.0	P7	7.6		9.5						
4/24		3.5	0.0	3.9	-1.2	4.4	-2.5	5.1	-4.1	6.0	-6.0								
	P9	3.5		4.7		6.0		7.6		9.5									
5/24		4.7	0.0	5.3	-1.3	6.0	-2.9	7.0	-4.9										
			4.7		6.0		7.6		9.5										
6/24		6.0	0.0	6.8	-1.6	8.0	-3.5												
			6.0		7.6		9.5												

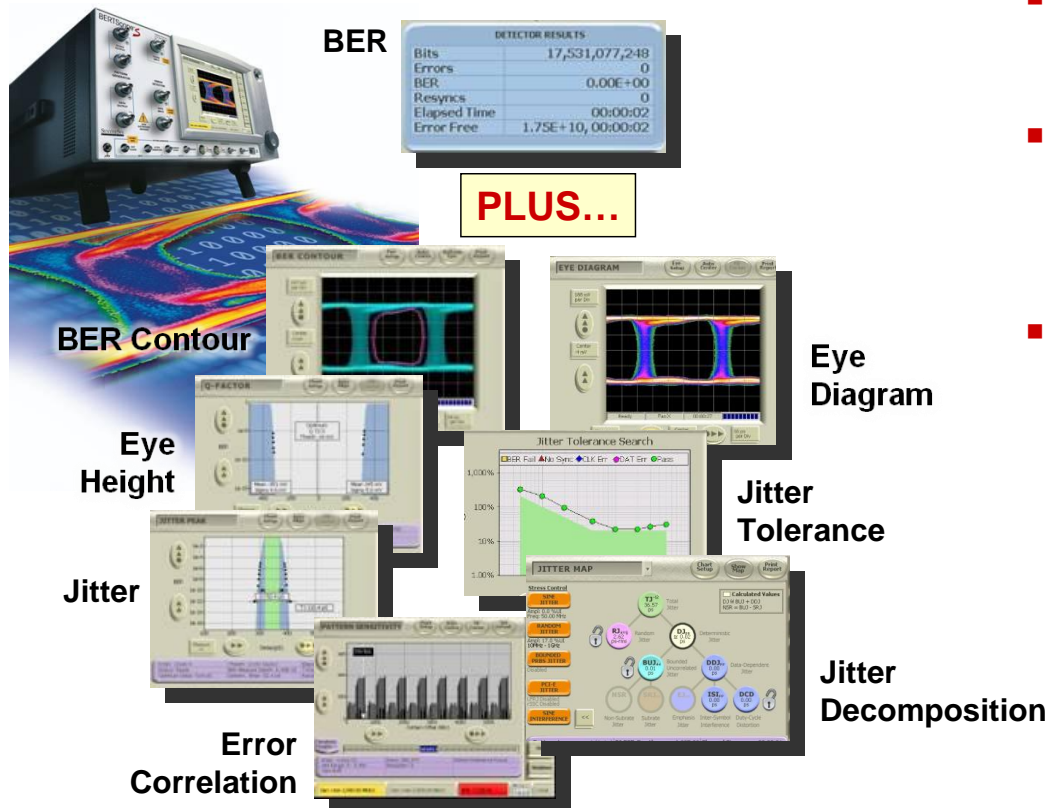
< Back    Next >    Cancel

# Rx Testing Summary

- Certainly the most complex type of testing
  - Due to complexity of equipment and procedures
- Extensive correlation studies in PCI-SIG have helped to streamline solutions
  - Similar stress signals
  - Guided calibration and test execution
  - Good correlation on the latest workshop
- Successful Rx compliance and margin test gives you the confidence that the device passes on the workshop

# Beyond Compliance: BERTScope Analysis Tools

- Besides being a BERT, the BERTScope's **“Scope” functionality** brings benefits that complement those of the Tektronix scopes
- Analysis tools are full featured and easy to use



- Frees up the scope for other tasks
- **Eye diagram for quick diagnosis** of synchronization and BER failure issues
- **Debug** challenging **signal integrity problems**
  - Error Location Analysis
  - Pattern Capture
  - Jitter Map
  - BER Contour

# PCIe Gen4 Update




# Gen4 Update

- Key attributes/requirements of PCIe 4.0
  - 16 GT/s, using scrambling, same as 8 GT/s, no encoding change
  - Maintains compatibility w/ PCIe installed base
  - Connector enhanced electrically (no mechanical changes)
  - Limited channel: ~12", 1 connector; repeater for longer reach
- Uniform measurement methodology applied across all data rates
- New 'SRIS' independent RefClk modes
  - SRIS – Separate RefClk Independent SSC Architecture
- Rev 0.3 Base spec just introduced in PCI-SIG (June 2013)
  - Rev 0.9 no earlier than 1H/2015
  - Rev 1.0 no earlier than 2H/2015

# Gen4 Update


- Tx Jitter – Analysis solution available today with PCE3.
- Tx EQ – CEM and Embedded will have limited change. Base might require Sampling solution.
- Rx – Similar approach at 16Gb/s.



## Transmitter Jitter Spec

- PCIe 4.0 uses same jitter parameters as PCIe 3.0
  - ✓  $T_{TX-UPW-TJ}$ ,  $T_{TX-UPW-DJDD}$ ,  $T_{TX-DDJ}$ ,  $T_{TX-UTJ}$  and  $T_{TX-UDJDD}$
  - ✓ Jitter will need to scale approximately with bitrate
  - ✓ De-embedding approach will likely remain the same
- PCIe 1.x and PCIe 2.x jitter parameters will be recast into the same form as the PCIe 3.0 parameters
  - ✓ Backward compatibility will be guaranteed
  - ✓ Some PCIe 1.x/2.x parameters will be effectively tightened
  - ✓ Example: PCIe 2.x  $T_{MIN-PULSE}$  parameter will be converted into  $T_{TX-UPW-TJ}$  and  $T_{TX-UPW-DJDD}$


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## PCIe 4.0 Rx Specification

- Will continue to rely upon a stressed eye approach where both EH and EW are stressed
  - ✓ Calibration channels IL will need to be reduced to yield ~24 dB at 8 GHz
  - ✓ Behavioral package model needs to comprehend reduced  $C_{PAD}$  or include T-coil models
  - ✓ Behavioral DFE model to have increased number of taps, at least 2
  - ✓ More capable CTLE model

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## Transmitter Equalization

- Max PCIe 4.0 channel IL remains approx the same as for PCIe 3.0
- Plan is to retain same equalization presets
  - ✓ Training will require that only a subset of the presets be used (P7 and P8)
- Equalization coefficient range and resolution also are intended to remain unchanged
- EIEOS signaling will likely change such that no TxEQ is applied during the EIEOS interval

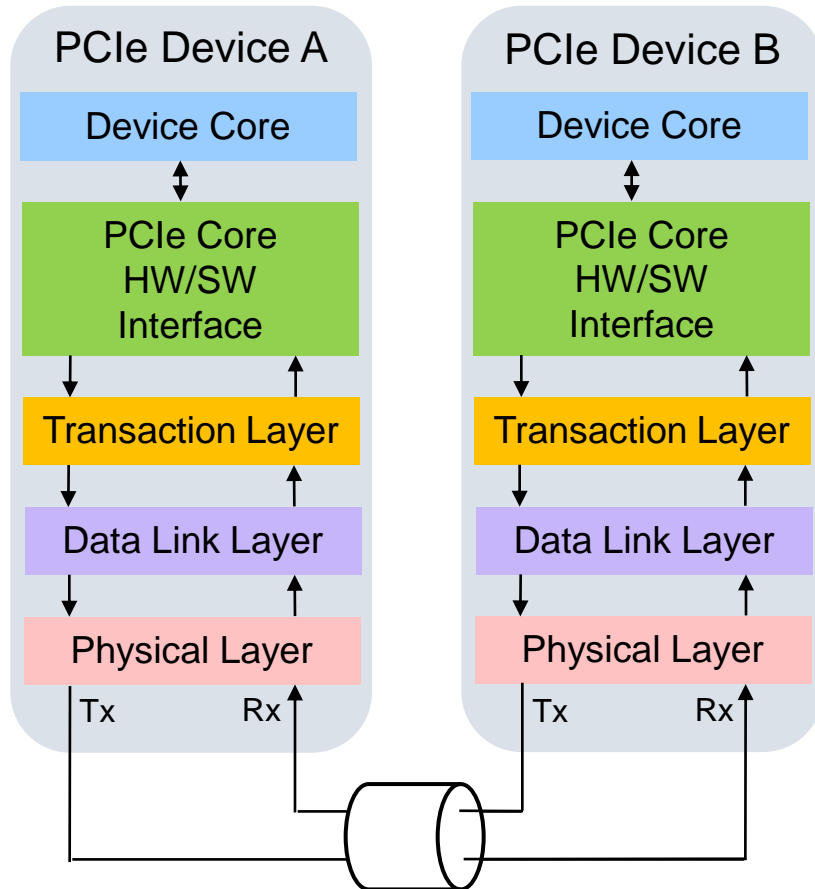
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# PCIe 3.0 Protocol Solutions

Supplemental



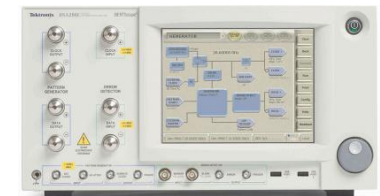
# Testing Challenges with PCI Express 3.0



Logic Protocol Analyzer



Oscilloscope  
Tx

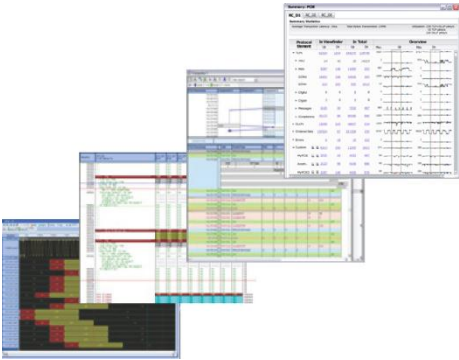


BERTScope  
Rx



# PCI Express Protocol Test Solution

## Software



- Module setup & trigger
- PCIe decoders
- Data windows:
  - Summary Profile
  - Transaction with BEV Flow control
  - Listing
  - Waveform

## Modules



- 8, 5, 2.5 GTs
- x8 & x4
- 8 State Triggering
- 8 GB memory
  - 16 GB for x16
- OpenEYE
- FastSYNC

## Probes



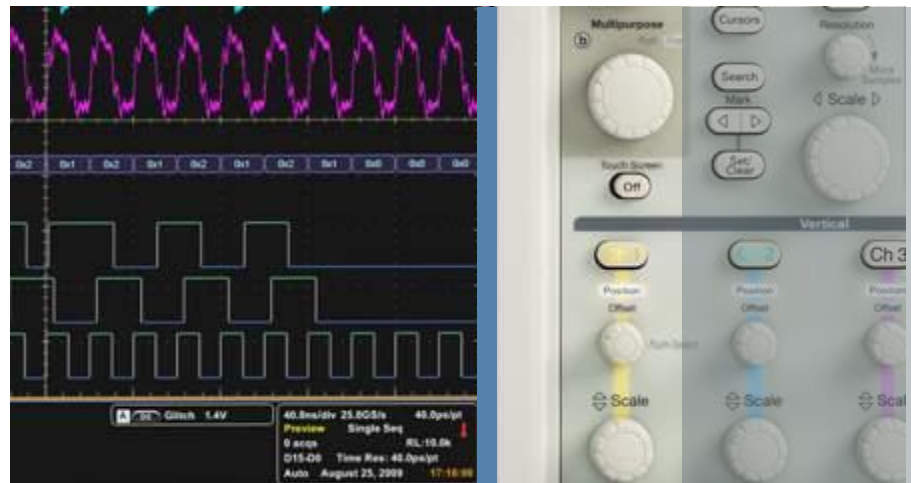
- x8 & x4 midbus
- x16, x8, x4, x1 slot interposers with Lane Converters
- Solder-down probe
- Gen2 probes for x8 & x4 midbus footprints rated to 5 GTs
- All probes rated to 8 GTs
- 6' probe cables
- ScopePHY

## Mainframes

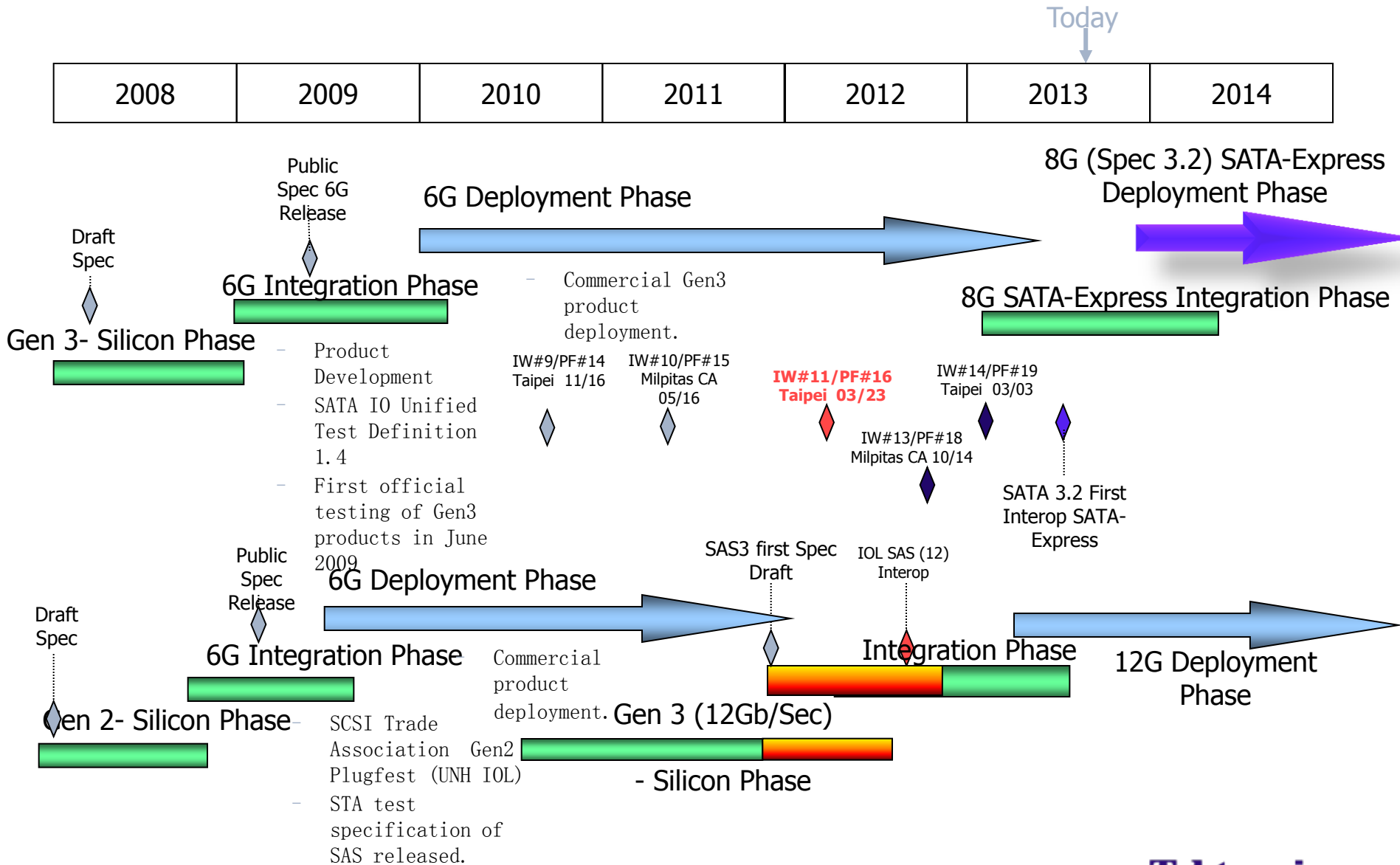


- 2 module portable mainframe with integrated 15" display & PC controller
- 6 module benchtop with GbE controller (requires PC)
- Single GUI & frame for system level debug of multi-buses

# SAS PHY Test Solutions

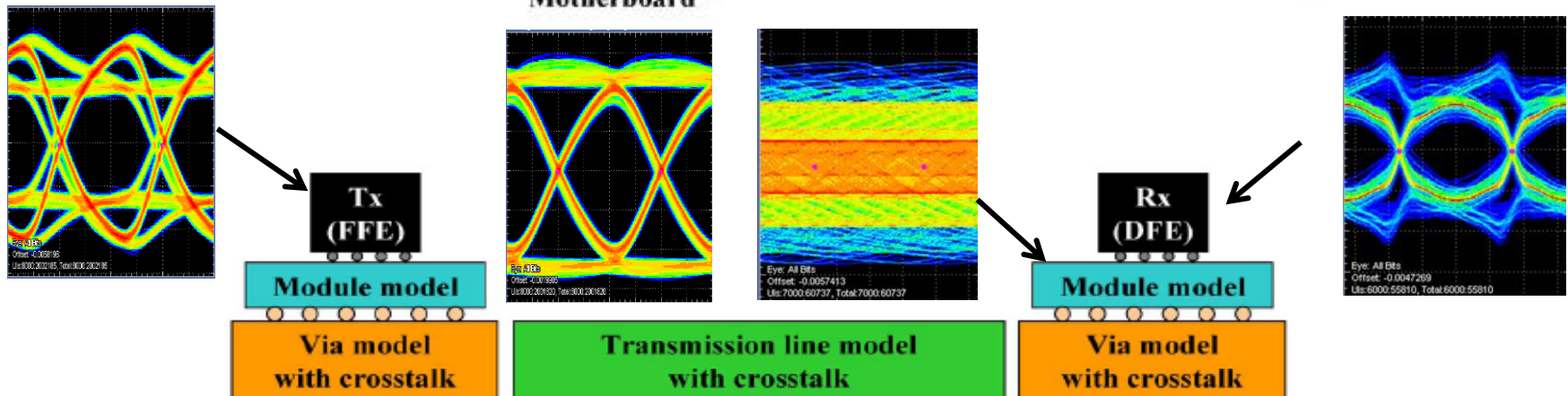
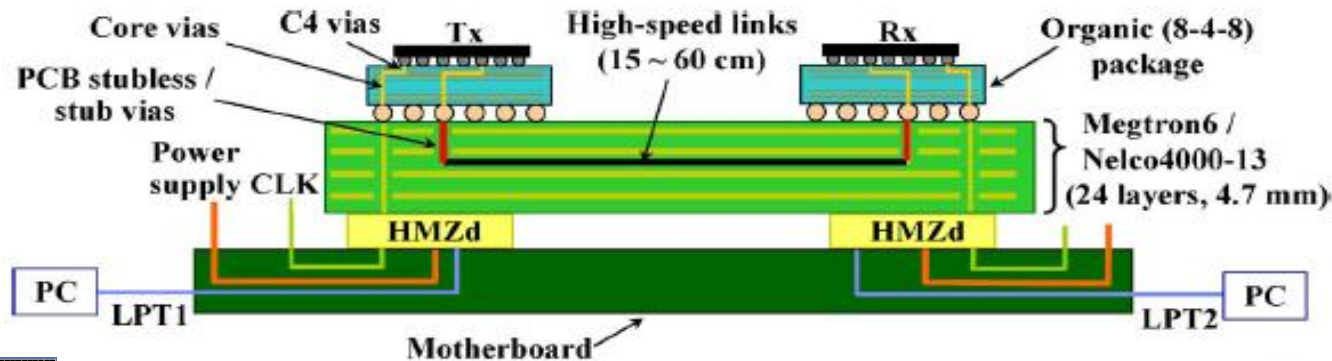


# Storage Timelines and Solutions Development

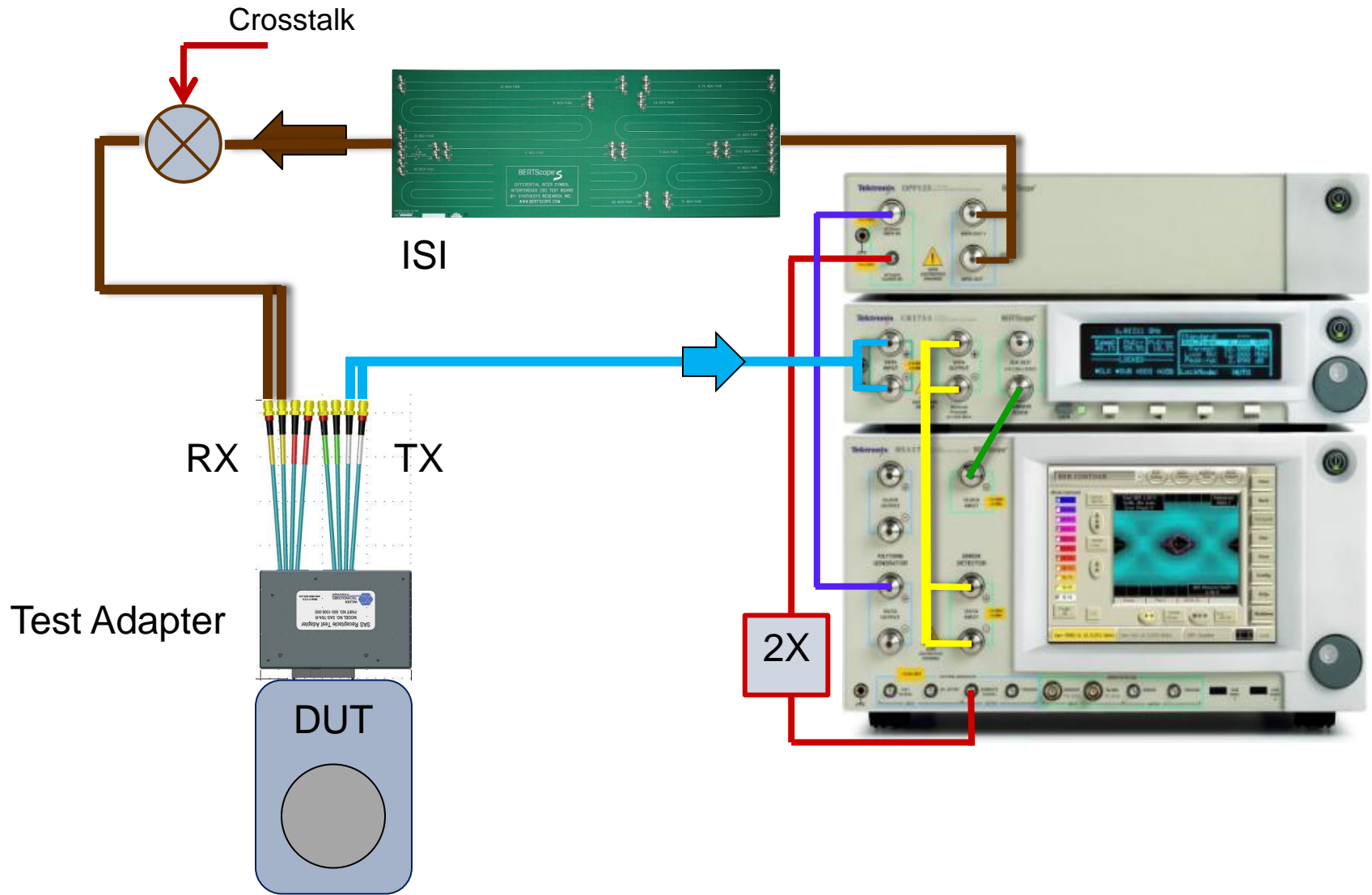


# 12G+ Design Problem: 1000mV, FFE, Crosstalk, DFE, 50mV

- Crosstalk and signal loss problems are the largest design challenge today.
- Significant advances in high tap count Decision Feedback Equalization are key to operating at 12G+.



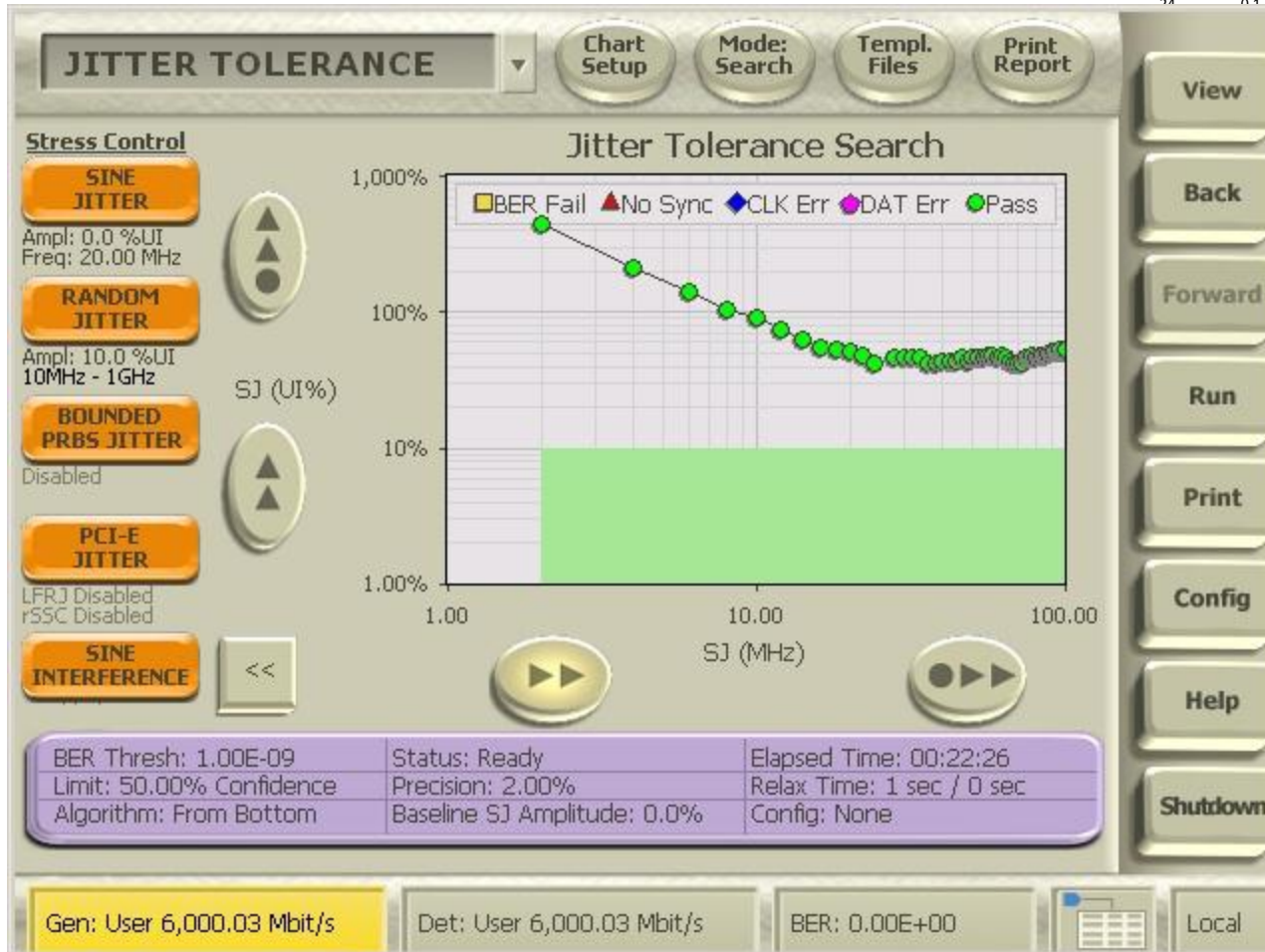
# SAS 12G Rx Equipment



# Rx Results (BERTScope)

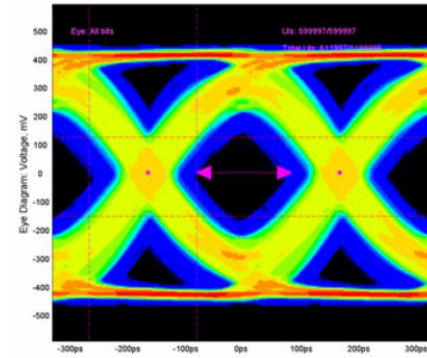
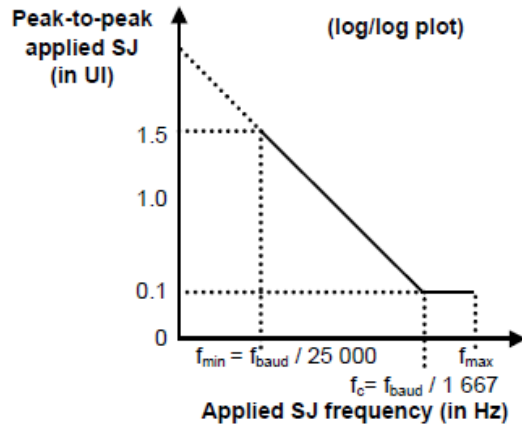
- Automated Scan from 10 Hz to 100 MHz
- SAS-3 (6/12 Gb/s) spec requires 97, 240 kHz & 2.06, 3.6 and 15 MHz

DATA	T-MHz	T-SJ	SJ	Bits	Errors	BER	Status	ThreshVX	DelayPS
	2	0.1	0.1	4.52	6E+08	0	0.00E+00 PASSED	0	267.531
	4	0.1	0.1	2.1	6E+08	0	0.00E+00 PASSED	0	266.451
	6	0.1	0.1	1.42	6E+08	0	0.00E+00 PASSED	0	266.451
	8	0.1	0.1	1.04	6E+08	0	0.00E+00 PASSED	-2	266.451
	10	0.1	0.1	0.9	6E+08	0	0.00E+00 PASSED	0	266.451
	12	0.1	0.1	0.74	6E+08	0	0.00E+00 PASSED	0	266.451
	14	0.1	0.1	0.64	6E+08	0	0.00E+00 PASSED	-2	266.451
	16	0.1	0.1	0.56	6E+08	0	0.00E+00 PASSED	0	266.451
	18	0.1	0.1	0.54	6E+08	0	0.00E+00 PASSED	1	266.451
	20	0.1	0.1	0.52	6E+08	0	0.00E+00 PASSED	0	266.451
	22	0.1	0.1	0.48	6E+08	0	0.00E+00 PASSED	0	266.451
	24	0.1	0.1	0.42	6E+08	0	0.00E+00 PASSED	0	266.451
	0.46			0.46	6E+08	0	0.00E+00 PASSED	0	267.531
	0.46			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
	0.46			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
	0.46			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
	0.42			0.42	6E+08	0	0.00E+00 PASSED	0	266.451
	0.42			0.42	6E+08	0	0.00E+00 PASSED	0	266.451
	0.44			0.44	6E+08	0	0.00E+00 PASSED	0	266.451
	0.44			0.44	6E+08	0	0.00E+00 PASSED	0	266.451
	0.44			0.44	6E+08	0	0.00E+00 PASSED	0	266.451
	0.46			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
	0.46			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
	0.46			0.46	6E+08	0	0.00E+00 PASSED	-2	267.531
	0.46			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
	0.48			0.48	6E+08	0	0.00E+00 PASSED	1	267.531
	0.48			0.48	6E+08	0	0.00E+00 PASSED	0	266.451
	0.46			0.46	6E+08	0	0.00E+00 PASSED	-2	267.531
	0.48			0.48	6E+08	0	0.00E+00 PASSED	0	266.451
	0.46			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
	0.44			0.44	6E+08	0	0.00E+00 PASSED	-1	267.531
	0.42			0.42	6E+08	0	0.00E+00 PASSED	-3	267.531
	0.42			0.42	6E+08	0	0.00E+00 PASSED	0	266.451
	0.42			0.42	6E+08	0	0.00E+00 PASSED	0	266.451
	0.46			0.46	6E+08	0	0.00E+00 PASSED	0	266.451
	0.46			0.46	6E+08	0	0.00E+00 PASSED	-2	267.531
	0.48			0.48	6E+08	0	0.00E+00 PASSED	0	266.451
	0.46			0.46	6E+08	0	0.00E+00 PASSED	-1	267.531
	0.48			0.48	6E+08	0	0.00E+00 PASSED	0	266.451
	0.48			0.48	6E+08	0	0.00E+00 PASSED	-2	267.531
	0.48			0.48	6E+08	0	0.00E+00 PASSED	0	266.451
	0.5			0.5	6E+08	0	0.00E+00 PASSED	0	266.451
	0.52			0.52	6E+08	0	0.00E+00 PASSED	-2	267.531
	0.52			0.52	6E+08	0	0.00E+00 PASSED	0	266.451
	0.52			0.52	6E+08	0	0.00E+00 PASSED	-1	267.531
	0.54			0.54	6E+08	0	0.00E+00 PASSED	0	267.531
	0.52			0.52	6E+08	0	0.00E+00 PASSED	0	266.451
							LIMIT		
	0.54			0.54	6E+08	0	0.00E+00 REACHED	0	266.451

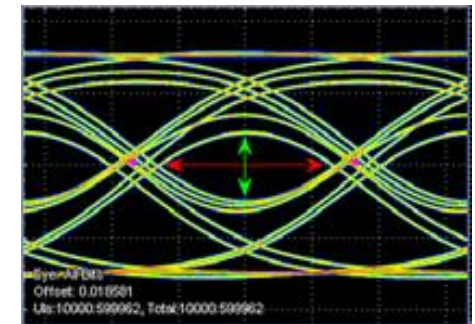
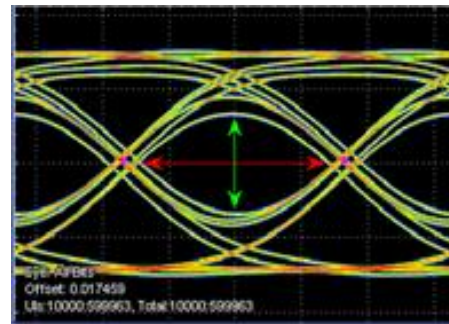
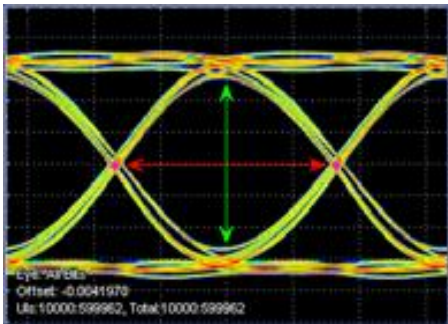


# Need for Precise ISI generation

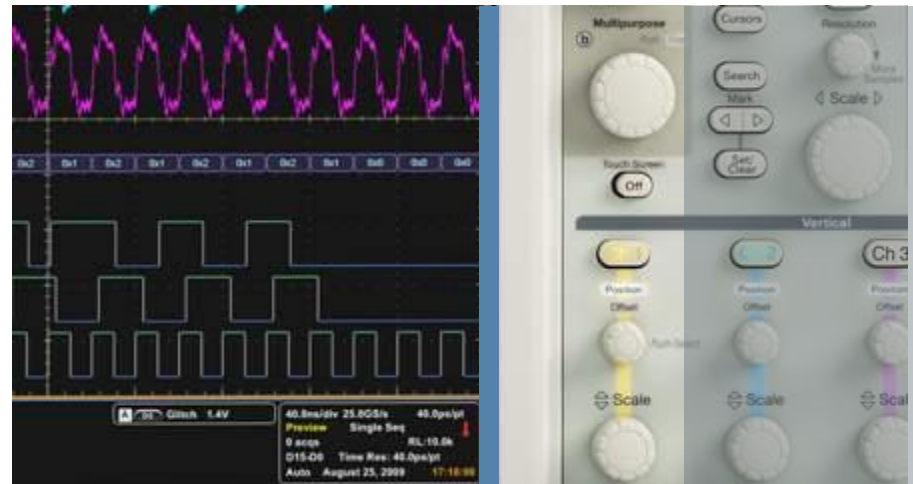
- Device margin testing against variable magnitude sinusoidal test vectors has been foundation of receiver characterization.



- Current PHY designs use sophisticated CTLE and/or DFE architectures, where tolerance and margining against DDJ is more important than SJ.



# SATA PHY Test Solutions





It's the measurements ..

# SATA UTD 1.4.2 Test Requirements

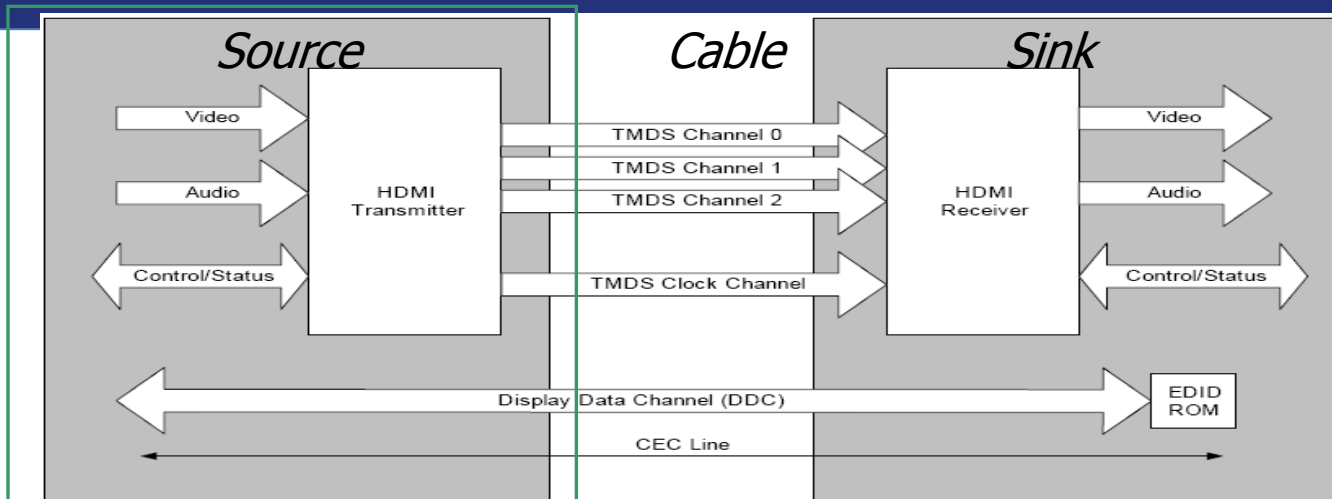
Phy Transmit Signal Requirements	SI General Requirements
TSG-01 : Differential Output Voltage	SI-1:8 : Cable Characterization
TSG-02 : Rise/Fall Time <b>revised</b>	SI-09 : Inter-Symbol Interference
TSG-03 : Differential Skew	Phy General Requirements
TSG-04 : AC Common Mode Voltage <b>revised</b>	PHY-01 : Unit Interval
TSG-05 : Rise/Fall Imbalance	PHY-02 : Frequency Long Term Stability
TSG-06 : Amplitude Imbalance <b>obsolete</b>	PHY-03 : Spread-Spectrum Modulation Frequency
TSG-07 : Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, fBAUD/10	PHY-04 : Spread-Spectrum Modulation Deviation
TSG-08: Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, fBAUD/10	Phy OOB Requirements
TSG-09 : Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, fBAUD/500	OOB-01 : OOB Signal Detection Threshold
TSG-10 : Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, fBAUD/500	OOB-02 : UI During OOB Signaling
TSG-11 : Gen2 (3Gb/s) TJ at Connector, Clock to Data, fBAUD/500	OOB-03 : COMINIT/RESET and COMWAKE Transmit Burst Length
TSG-12 : Gen2 (3Gb/s) DJ at Connector, Clock to Data, fBAUD/500	OOB-04 : COMINIT/RESET Transmit Gap Length
TSG-13: Gen3 (6Gb/s) Transmit Jitter w/wo CIC <b>revised</b>	OOB-05 : COMWAKE Transmit Gap Length
TSG-14 : Gen3 (6Gb/s)TX Maximum Differential Voltage Amplitude	Phy Receiver/Transmitter Channel Reqs
TSG-15 : Gen3 (6Gb/s) TX Minimum Differential Voltage Amplitude <b>ECN-50 Revised</b>	RX/TX-01 : Pair Differential Impedance
TSG-16 : Gen3 (6Gb/s) Tx AC Common Mode Voltage <b>revised</b>	RX/TX-02 : Single-Ended Impedance (Obsolete)
Phy Receive Signal Requirement	RX/TX-03 : Gen2 (3Gb/s) Differential Mode Return Loss
RSG-01 : Gen1 (1.5Gb/s) Receiver Jitter Tolerance Test (Normative)	RX/TX-04 : Gen2 (3Gb/s) Common Mode Return Loss
RSG-02 : Gen2 (3Gb/s) Receiver Jitter Tolerance Test (Normative)	RX/TX-05 : Gen2 (3Gb/s) Impedance Balance
RSG-03 : Gen3 (6Gb/s) Receiver Jitter <b>ECN-50/ECN-51 Revised</b>	RX/TX-06 : Gen1 (1.5Gb/s) Differential Mode Return Loss
RSG-05 : Gen1 Asynchronous Receiver Stress Test at +350ppm	RX/TX-07 : Gen3 (6Gb/s) Differential Mode Return Loss
RSG-06 : Gen1 Asynchronous Receiver Stress Test With SSC	RX/TX-08 : Gen3 (6Gb/s) Impedance Balance

## SATA Measurement Legends:

- No change from previous UTD 1.3 spec version
- Revised methodology from UTD1.3 to UTD 1.4
- New test definitions in UTD 1.4
- Obsolete

Summary: TSG05/06 have been classified as EMI related and moved to an obsolete status. TSG15 will use an eye height methodology and will have different limits depending on the DUT being a Host or Device

# HDMI Source Testing



- Rise/Fall Time
  - Inter-pair Skew
  - Clock Duty Cycle
  - Clock Jitter
  - Eye Diagram
  - Voltage VL
  - Intra-pair Skew
- Differential
- Single-ended

# System recommendation for HDMI 2.0 for Source measurement

# AppsU

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Table 4-24 Source AC Characteristics at TP1

Item	Value
Rise time / fall time (20%-80%)	<u>if attached Sink supports &lt; 340MHz</u> <u>75psec ≤ Rise time / fall time</u> <u>if attached Sink supports &gt; 340MHz and transmitted TMDs Character Rate &gt; 340MHz</u> <u>42.5psec ≤ Data Rise time / Data fall time</u> <u>75psec ≤ Clock Rise time / Clock fall time</u>

Table 4-30 TP7 Direct Attach AC Characteristics at 6Gbps

Item	Value
Rise time / fall time (20%-80%)	<u>if attached Sink supports &gt; 340MHz and transmitted TMDs Character Rate &gt; 340MHz</u> <u>42.5psec ≤ Data Rise time / Data fall time</u> <u>75psec ≤ Clock Rise time / Clock fall time</u>

- HDMI 1.4b, should be capable of measuring 75 psec, but no word about the System Rise time.
- **HDMI 2.0 should be capable of measuring 42.5 psec, but no word about System Rise time.**
- The Error contribution of RT measurement due to System and DUT generally not accounted when we refer to specification

# What is the system bandwidth needed to measure 42.5 (20-80% )psec or less DUT Rise time

- System bandwidth should be around  $(42.5/1.5)$  28psec
- Scope bandwidth of 16 Ghz and 16 Ghz DSP enhanced probe has System Rise time of about 23 psec. It can measure the DUT Rise time of 42.5 psec with error of 1%. And can measure DUT Rise time of 37 psec with error of 7%.
- We can indicate Pass or fail confidently only when the System band. width is close to 16 Ghz scope .
- Is it fact for all scope vender ??
  - Spec says it should not be less than 42.5psec.
  - Max Rise time is limited by Eye diagram slope.
  - Both scope and Probe rise time cannot be less or equal to the DUT rise time because it can measure the signal rise time accurately only if DUT RT is slower than system rise time by 1.5 X times.
- How it is handled in HDMI 1.4b today???
  - We recommend 8Ghz scope and 13 Ghz probe, then system rise time is 38 psec which is close 2X faster than 75 psec

- 16GHz BW scope will give 1% error and hence is recommended for HDMI 2.0 testing.
- HDMI 2.0 RT/FT (20%-80%) data signals is 42.5ps



Eye Diagram test is changed

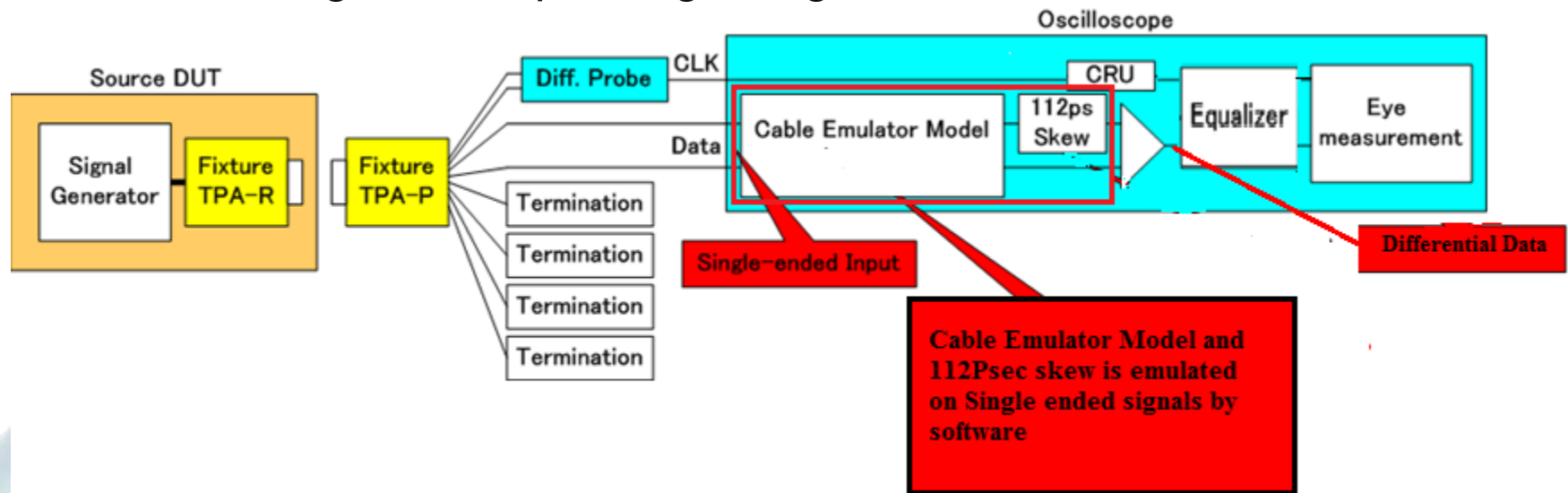
Rest of the tests is same

1.4b CTS test is a pre-requisite for HDMI 2.0

Min 8GHz scope to 16GHz scope

Fixtures and Probes

- Most Source tests are likely to be same as HDMI 1.4b but for Eye Diagram test.
- Source Eye Diagram test is measured at TP2\_EQ.
- TP2 is the signal after passing along a worst cable.

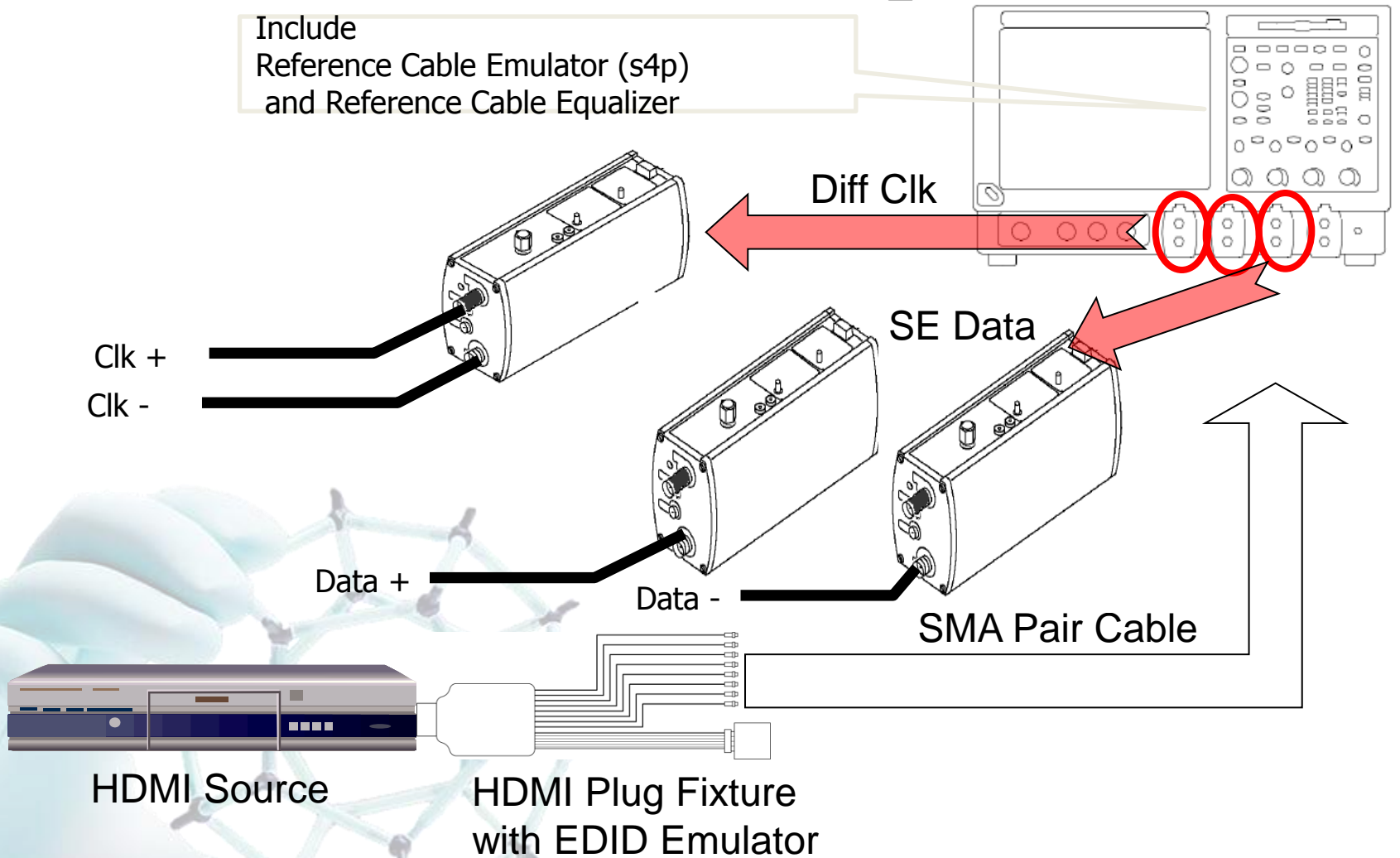




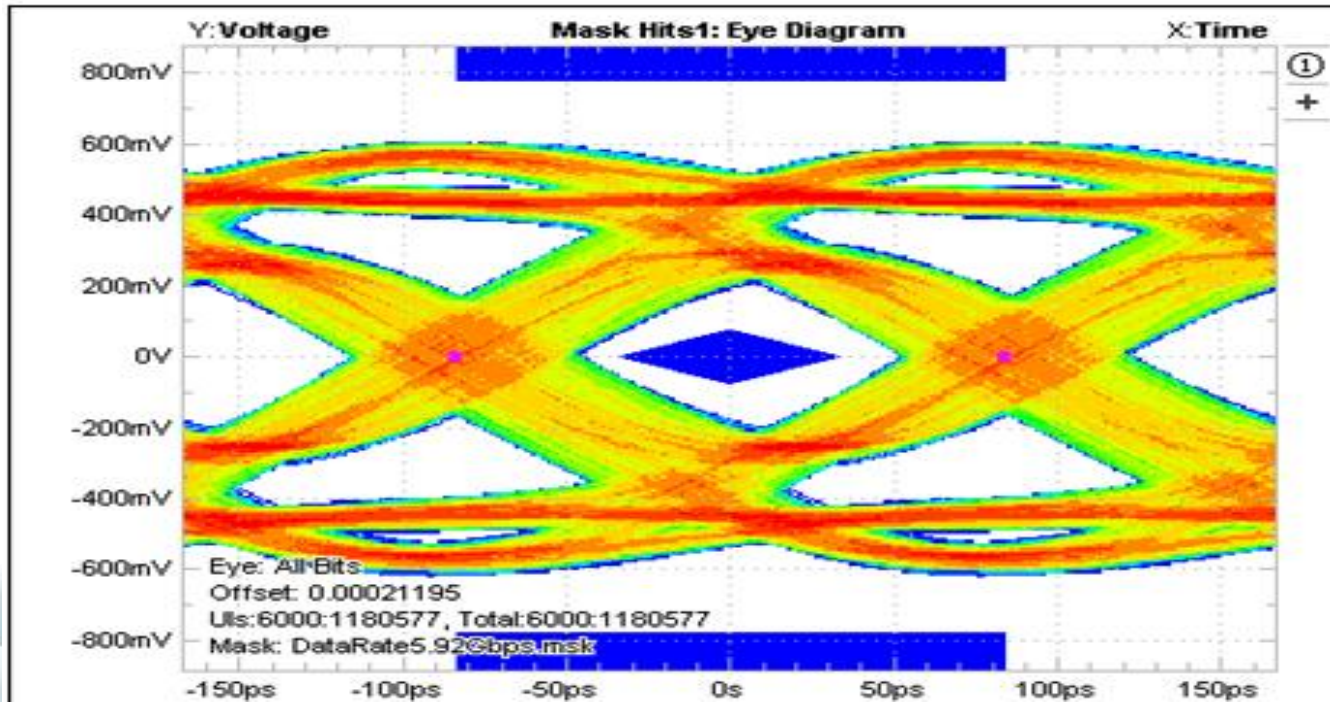
# Source Eye Diagram Test

Tektronix Oscilloscope  
DPO/DSA/MSO70000 Series  
≥ 16GHz

Include  
Reference Cable Emulator (s4p)  
and Reference Cable Equalizer



# TP2 Source Eye for HDMI 2.0 6G signal



Single End Input eye rendered at Tek lab

# HDMI 2.0 Tx Compliance Software

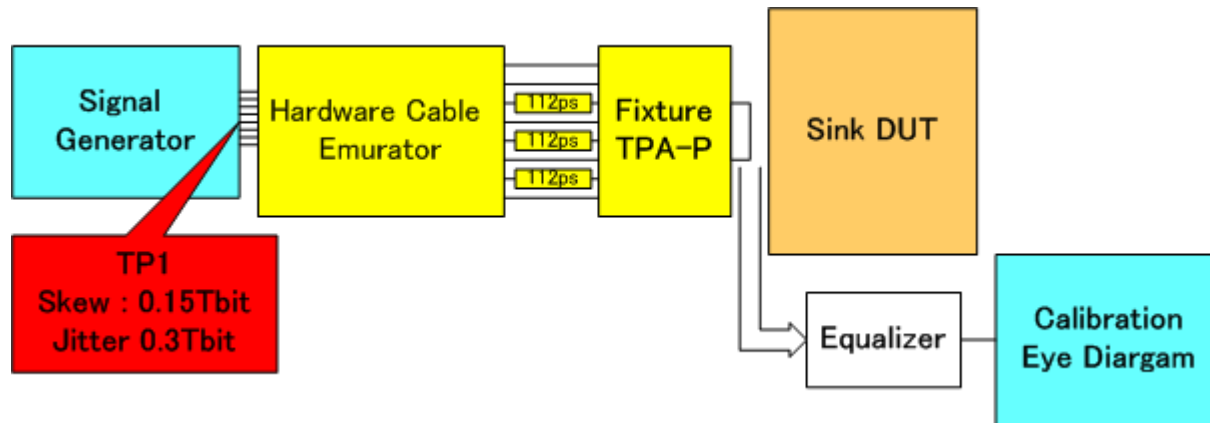
Test Name	Details	TBit	Value	Units	Pass/Fail	Margin
1.2 TMDS TRise TFall	Clock Rise Time	168.3498	38.7089	ps	Fail	-36.2911
1.2 TMDS TRise TFall	Clock Fall Time	168.3498	38.1015	ps	Fail	-36.8985
1.5 TMDS ClockDutyCycle	Maximum Duty Cycle	168.3498	50.01	%	Pass	-9.99
1.5 TMDS ClockDutyCycle	Minimum Duty Cycle	168.3498	49.99	%	Pass	9.99
1.6 TMDS Clock Jitter	TMDS Clock Jitter	168.3498	40.1239	ps	Pass	-1.9635
1.6 TMDS Clock Jitter	TMDS VSwing	168.3498	64.7812	mV	Fail	-335.22 & 1135.22
1.1 TMDS V Low	TMDS VLow for	168.3498	3.2822	V	Fail	0.9822 & -0.1822
1.1 TMDS V Low	TMDS VLow for	168.3498	3.1738	V	Fail	0.8738 & -0.0738
1.4 TMDS Intra-Pair Skew	TMDS Intra-Pair Skew for Clock	168.3498	9.7096	ps	Pass	-15.5429
<b>D0</b>						
1.2 TMDS TRise TFall	D0 Rise Time	168.3498	60.6379	ps	Pass	18.1379
1.2 TMDS TRise TFall	D0 Fall	168.3498	58.5778	ps	Pass	16.0778
1.1 TMDS V Low	TMDS VLow for	168.3498	3.1720	V	Fail	0.8720 & -0.2720

# Sink Tests

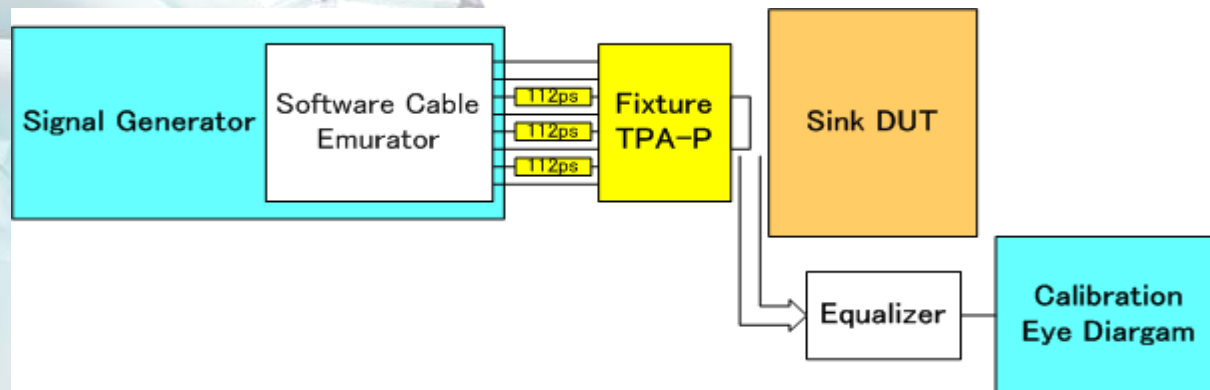


# Requirement for Signal generation

## Cable Emulation and Skew by Hardware



## Hardware Skew and Software Cable Emulation



# Likely Sink Electrical tests

**Test ID HF2-1: Sink TMDS Electrical – 340-600Mcsc – Min/Max Differential Swing Tolerance**

**Test ID HF2-2: Sink TMDS Electrical – 340-600Mcsc – Intra-Pair Skew**

**Test ID HF2-3: Sink TMDS Electrical – 340-600Mcsc – Jitter Tolerance**

**Test ID HF2-4: Sink TMDS Electrical – 340-600Mcsc – Differential Impedance**



# Sink Test

Tektronix AFG3000  
(Synchronize two AWGs)

Tektronix Oscilloscope  
DPO/DSA/MSO70000 Series  
(Synchronize two AWGs  
and Automation Test)

Tektronix AWG70002A HDM

Include  
Reference Cable Emulator (s2p)

112ps Delay Line  
(Emulate Cable Skew)

SMA Pair Cable

HDMI Plug Fixture

HDMI Sink

# Sink Testing 1.4b Vs 2.0

Jitter Tolerance test needs +ve and -ve lanes tested with 112ps delay line

Rest of the tests is same

1.4b CTS test is a pre-requisite for HDMI 2.0

Need AWG70K series for HDMI 2.0 as against AWG7K.

Min 8GHz scope to 16GHz scope

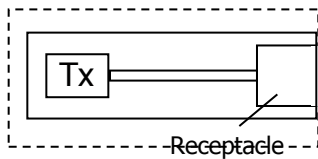
Fixtures and Probes



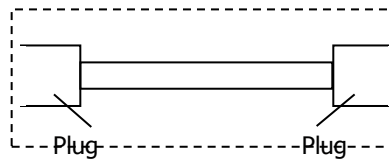
# MHL Ecosystem and Tektronix Solution



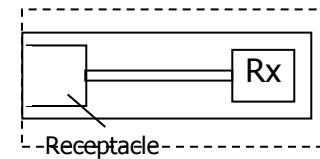
Source Devices



Cable Assemblies

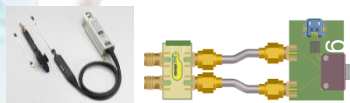


Sink Devices

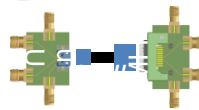
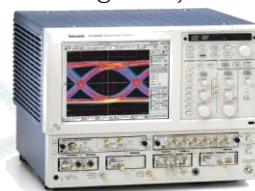


Source: MHL.org

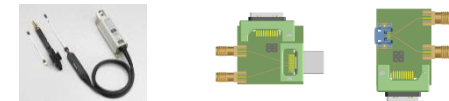
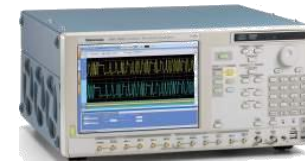
- Mobile Devices, STBs



- Dongles, Cables



- TVs, Monitors, ..

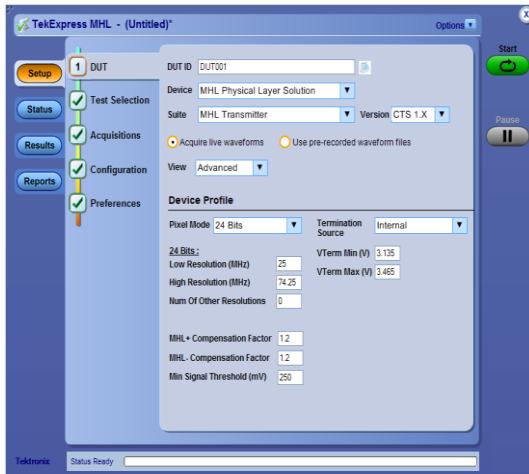


Electrical and Protocol

Electrical and Protocol

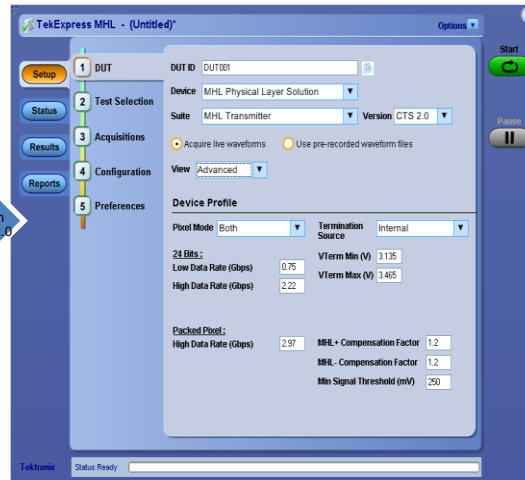
# Tektronix MHL Transmitter Solution

- Tektronix has worked closely with MHL consortium to define the next CTS version 2.1 and MHL 2.1 TX SW.



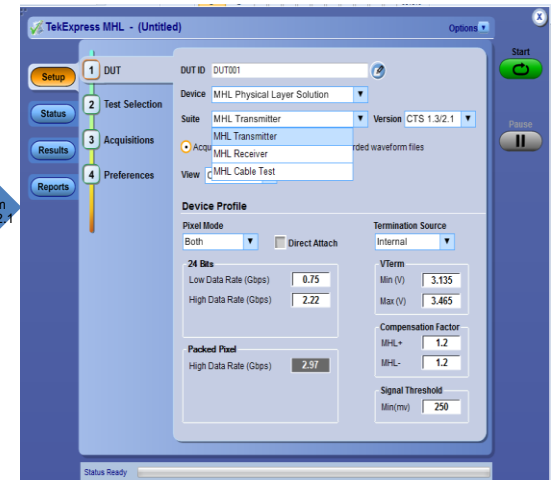
CTS 1.x

Switch from CTS 1.x to 2.0



CTS 2.0

Switch from CTS 2.0 to 2.1



CTS 2.1

- MHL Protocol Analyzer SW is MHL 2.1 version available
- MHL 2.1 Sink Patterns for Direct Attach Device testing is available
- MHL 2.1 Cable Electrical testing patterns are available
- **New Python sequencing –faster speed**
- **No Excel dependency.**
- **No changes in test gear for MHL 2.1 only new feature support.**

- DPO/DSA/MSO 70804B/C Series Real Time Oscilloscope with BW  $\geq$  8GHz
- MHL Compliance Software – Option MHD
- Innovative MHL Protocol Software from Third party – TEK-PGY-MHL-PA-SW
- Probes – P7313SMA (two) and P7240 (one)
- MHL Test Fixture including Direct Attach Fixture – Available from Tektronix.
- AWG7122C with Opt 01,02 or 06 and 08 for the innovative direct Synthesis based MHL Rx/Dongle testing.
- C-Bus Sink and Source board is needed and is available from Tektronix
- DSA8200 or Equivalent with 80E03/80E04 and I-Connect Software for MHL cable testing ( performed manually using MOIs)

Please contact local Tektronix account managers for further details.

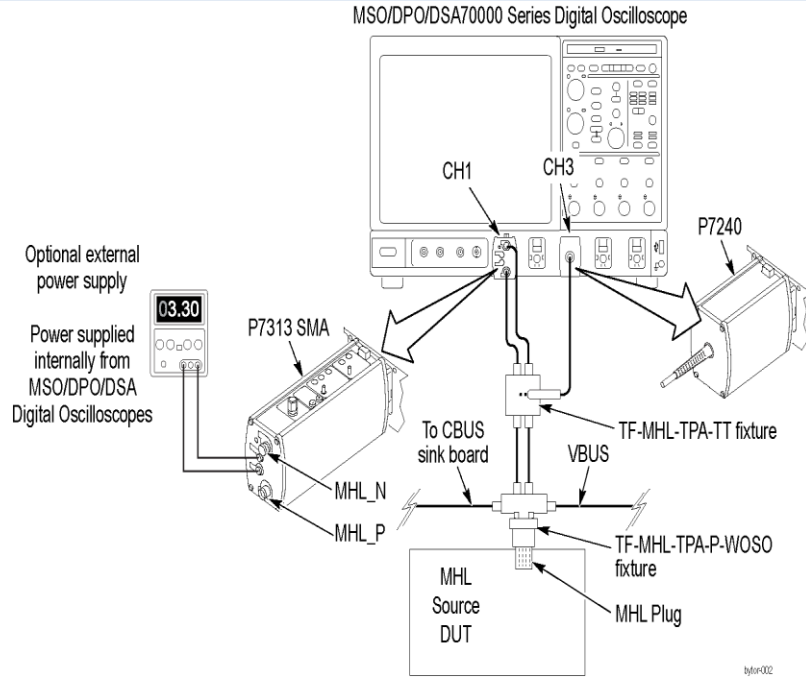
# Tektronix MHL 2.1 Tx Solution with Direct Attach test support

The screenshot shows the TekExpress MHL software interface. The main window is titled "TekExpress MHL - (Untitled)\*" and has an "Options" dropdown in the top right. On the left, there is a navigation pane with buttons for "Setup", "Status", "Results", and "Reports". A vertical progress indicator shows four steps: 1. DUT (highlighted in orange), 2. Test Selection (checked), 3. Acquisitions, and 4. Preferences. The "Setup" section is active, displaying the following configuration:

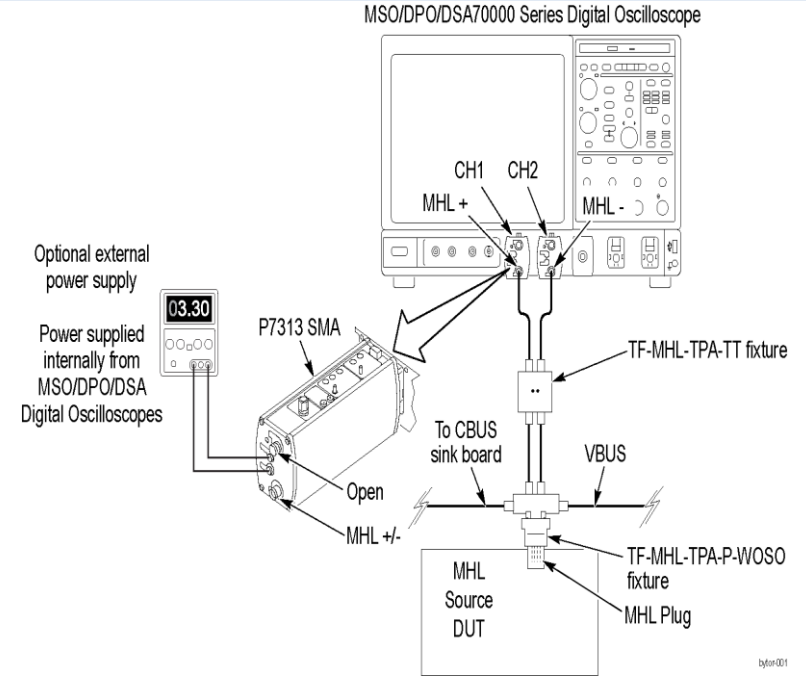
- DUT ID: DUT001
- Device: MHL Physical Layer Solution
- Suite: MHL Transmitter
- Version: CTS 1.3/2.1
- Acquire live waveforms (selected) / Use pre-recorded waveform files
- View: Compliance
- Device Profile:
  - Pixel Mode: Both
  - Direct Attach (checked)
  - Termination Source: Internal
  - 24 Bits:
    - Low Data Rate (Gbps): 0.75
    - High Data Rate (Gbps): 2.22
  - Packed Pixel:
    - High Data Rate (Gbps): 2.97
  - VTerm:
    - Min (V): 3.135
    - Max (V): 3.465
  - Compensation Factor:
    - MHL+: 1.2
    - MHL-: 1.2
  - Signal Threshold:
    - Min(mv): 250

At the bottom left, a status bar shows "Status Ready". On the right side of the interface, there are "Start" and "Pause" buttons.

# Tektronix MHL Tx Setup



**MHL Differential and CM Test Setup**  
6 tests



**Single Ended and Intra Pair Skew Test Setup**  
6Tests

**Also same setup is used for MHL Protocol Testing**

\*\* C-Bus Sink and Source Board is needed for hand shaking and is available from Tektronix

# MHL 2.1 Compliance Software for Automated Tx Tests: Option MHD

The screenshot displays the TekExpress MHL software interface. The main window title is "TekExpress MHL - (Untitled)". On the left, a vertical navigation bar contains buttons for "Setup", "Status", "Results", and "Reports". A central column shows a progress indicator with four steps: "1 DUT" (checked), "2 Test Selection" (highlighted), "3 Acquisitions", and "4 Preferences". The main area is titled "MHL Physical Layer Solution : MHL Transmitter : CTS 1.3/2.1" and contains a tree view of test items. The "MHL Clock" category is expanded, showing several sub-items, with "3.1.1.5 Common-mode Output Swing Voltage-V\_CMSWING (Low)" selected. Below the tree view is a "Test Description" box containing the text: "This test confirms that common-mode output voltage swing amplitude is within the specified limits when the source device operates in normal mode." To the right of the description are "Schematic" and "Configure" buttons. On the far right, there are "Start" and "Pause" buttons. The status bar at the bottom indicates "Status Ready".

TekExpress MHL - (Untitled) Options

Start

Pause

MHL Physical Layer Solution : MHL Transmitter : CTS 1.3/2.1

Deselect All Select All

- MHL Clock
  - 3.1.1.1 Standby Output Voltage-VOFF
  - 3.1.1.5 Common-mode Output Swing Voltage-V\_CMSWING (Low)
  - 3.1.1.7 Common-mode Rise and Fall Times-TR\_CM, TF\_CM (High)
  - 3.1.1.10 MHL Clock Duty Cycle in Normal Mode (High)
  - 3.1.1.14 MHL Clock Duty Cycle in PackedPixel Mode (High)
  - 3.1.1.17 TP2 Clock Jitter in Normal Mode (Low, High)
  - 3.1.1.19 TP2 Clock Jitter in PackedPixel Mode (High)
- MHL Data
  - 3.1.1.2 Single-ended High Level Voltage-VSE\_HIGH (Low)
  - 3.1.1.3 Single-ended Low Level Voltages-VSE\_LOW (Low)
  - 3.1.1.4 Differential Output Swing Voltage-VDF\_SWING (Low)
  - 3.1.1.6 Differential Rise and Fall Times-TR\_DF, TF\_DF (High)
  - 3.1.1.18 TP2 Eye Diagram in Normal Mode (Low, High)
  - 3.1.1.20 TP2 Eye Diagram in PackedPixel Mode (High)

**Test Description**

This test confirms that common-mode output voltage swing amplitude is within the specified limits when the source device operates in normal mode.

Schematic

Configure

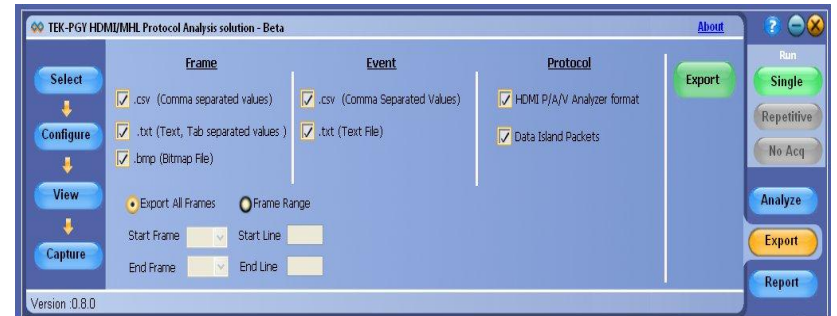
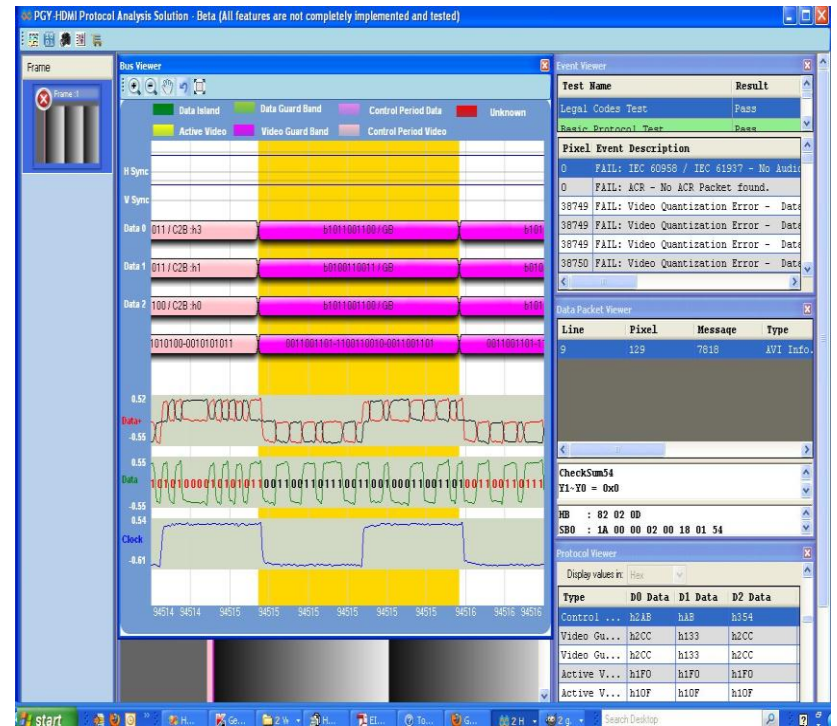
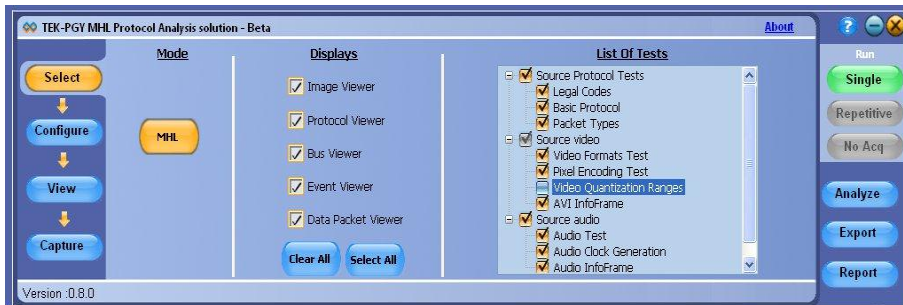
Status Ready

# MHL 2.1 tests- Detailed information on Protocol tests(no Changes)

- MHL Protocol Analysis software running on the Tektronix REAL TIME Oscilloscope
  - Unique value proposition as the same real time scope is used for both Physical layer testing and Protocol testing.
  - Gives the seamless transition from Phy layer to Protocol.
  - Cost effective solution.
- Features
  - Multi View support
    - Bus Analysis
    - Frame Viewer
    - Event Viewer
    - Protocol Viewer
    - Linked to the analog waveform
  - Tektronix Nomenclature – TEK-PGY-MHL-PA-SW



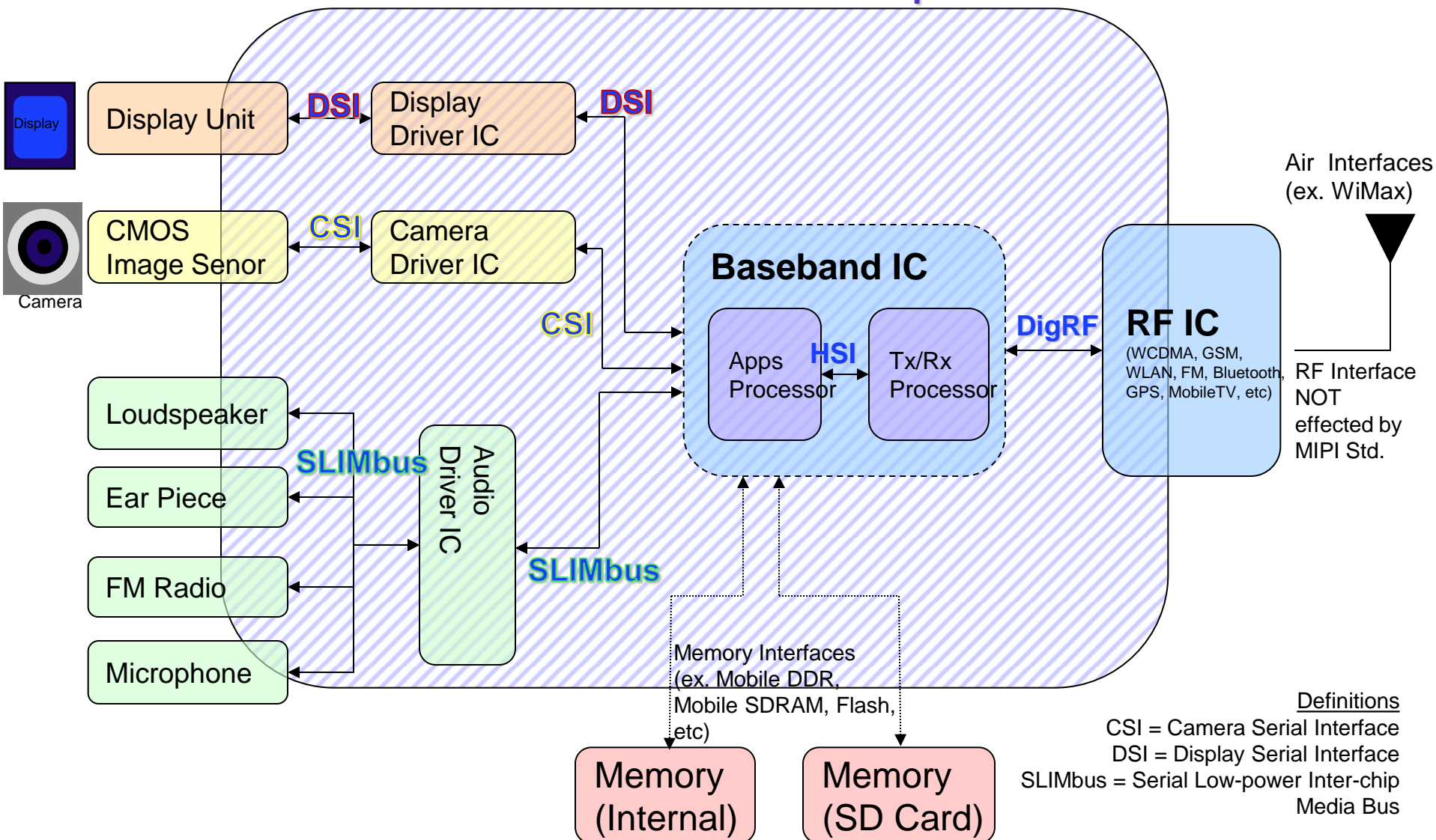
# Tektronix MHL Protocol Analyzer: Seamless PHY and Link Layer Testing



# MIPI Standards Overview

## Example Mobile Device Block Diagram

### MIPI Specific Standards



# Tek Tools are listed on MIPI Alliance Webpage and CTS



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**MIPI Alliance Testing Program**  
Version 1.00  
30-August 2010

**MIPI Alliance Testing Program  
User's Manual, Method of Implementation (MOI), and  
Tutorial Documentation for  
D-PHY Physical Layer Transmitter Conformance Tests,  
Using Agilent, LeCroy, and Tektronix Real-Time DSOs, and  
DPHYGUI TX Conformance Software (v20100830)**

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# Tek MIPI setup used by UNH-IOL



InterOperability Laborator... x +

www.iol.unh.edu/services/testing/mipi/equipment.php

Through a collaborative agreement with Tektronix, the UNH-IOL is using the Tektronix DSA72004B Digital Serial Analyzer for MIPI testing. Combined with UNH-IOL's D-PHYGUI software, this platform provides the ability to capture and analyze D-PHY signalling, in order to perform the UNH-IOL D-PHY Transmitter Physical Layer Conformance Test Suite.

For more information on the Tektronix DSA72004B please visit <http://www.tek.com>

The Moving Pixel Company P331 MIPI D-PHY Probe is used to implement many protocol layer tests for both CSI-2 and DSI for up to 4 lanes.

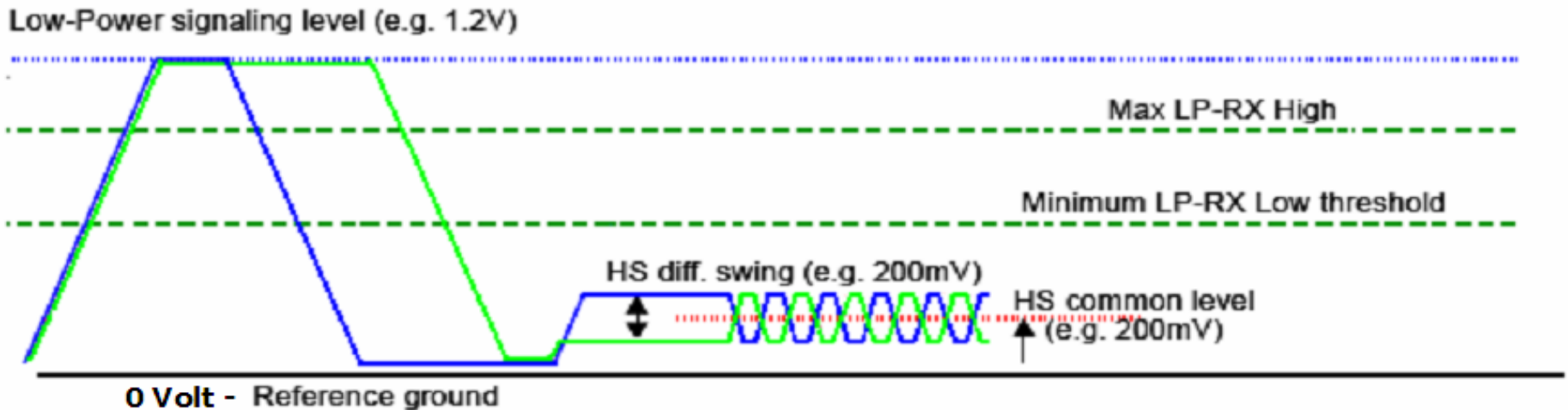
For more information on the P331 MIPI D-PHY Probe, visit <http://www.movingpixel.com/main.pl?products.html>

Waiting for www.iol.unh.edu...

UNH-IOL (University of New Hampshire) is a 3<sup>rd</sup> party test house for MIPI testing

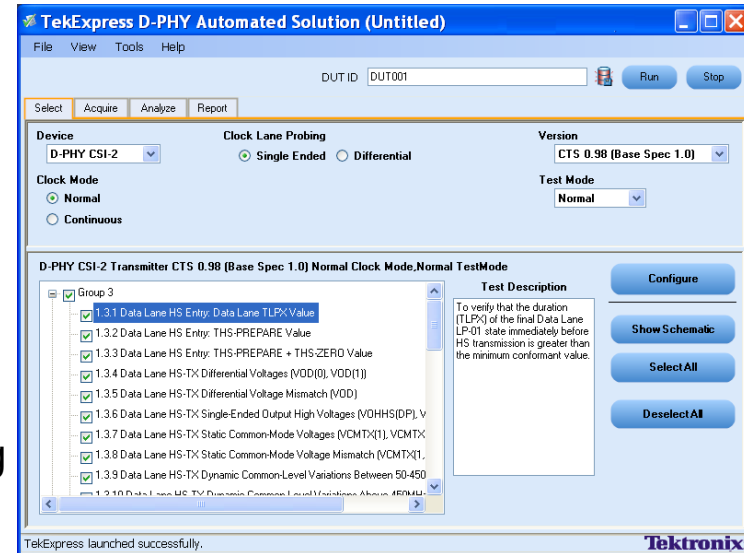
# What is D-PHY ?

- It's a PHY standard for interfacing Camera (CSI) & Display (DSI)
- Two modes of transmission
  - High Speed (HS) and Low Power (LP)
- Modes are mixed during the operation
  - Transitions from LP to HS and back to LP on the fly
- Maximum Data Rate
  - High Speed mode: 80 Mbps – 1.5 Gbps, Typically at ~500 Mbps.
  - Low Power mode: Up to 10 Mbps
- Bus termination
  - 50 ohms in HS
  - Hi-Z in LP



# D-PHY Tx : Opt.D-PHYTX Conformance Test Solution

- Opt.D-PHYTX : D-PHY Automated Solution
  - TekExpress option for Fully-Automated testing
  - Provides Conformance and Characterization Testing
  - Based on D-PHY Base Spec v1.0 and UNH's Conformance Test Suite v0.98.
  - Runs on 7K/C and 70K/B/C scopes
- Opt.TEKEXP is Pre-Requisite
- Differentiation
  - Un-parallel Automation
    - Using Automatic cursor finding of Test Regions
  - 100% Widest Test Coverage
  - For Conformance testing to Latest CTS (v0.98)
  - Based on Latest Base spec (v1.0)
  - Fully-Automated Temperature Chamber testing
- Value proposition
  - Custom-limits/ Limits-Editing on the fly
  - Test Reports
    - Pass/Fail Summary with Margin details & Zoom-in waveform captures
  - Tek 3.5GHz scope is the minimal configuration for accurate testing



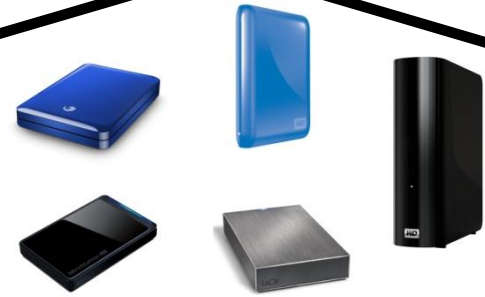
# USB 3.0 Physical Layer Testing



# USB Usage Model



**HDDs**



**Devices**

**Thumbdrives**



**A to Std B**



**Hubs**



**A to μB**



**Tablets**



**Video Adapters**



Goal: Any certified host works with any certified hub or device.



# Interoperability Challenge

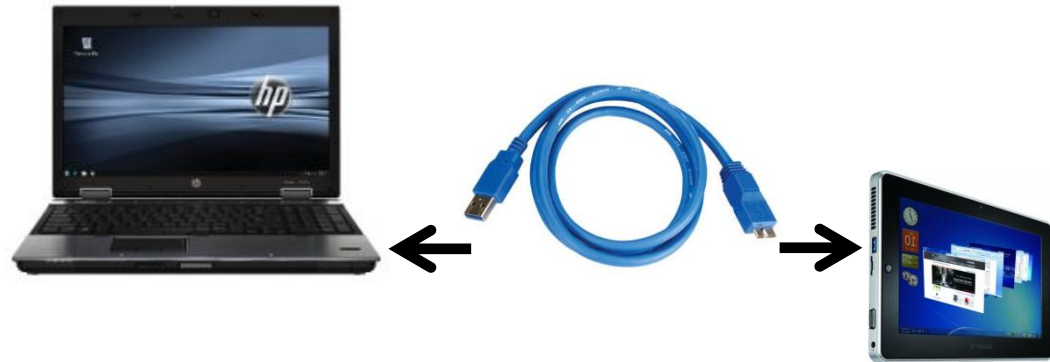
## Short Channel

- 1" host PCB route
- ¼" device PCB route
- Direct plug



## Long Channel

- 10" host PCB route
- 4" device PCB route
- 3m cable



SuperSpeed USB must accommodate a wide range of interconnect channels (loss, crosstalk, reflections).

# USB 3.0 Key Considerations

- Receiver testing now required
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues
- Channel considerations
  - Need to consider transmission line effects
  - Software channel emulation for early designs
- New Challenges
  - 12" Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx
- Test strategy
  - Cost-effective tools
  - Flexible solutions

## 6 Physical Layer

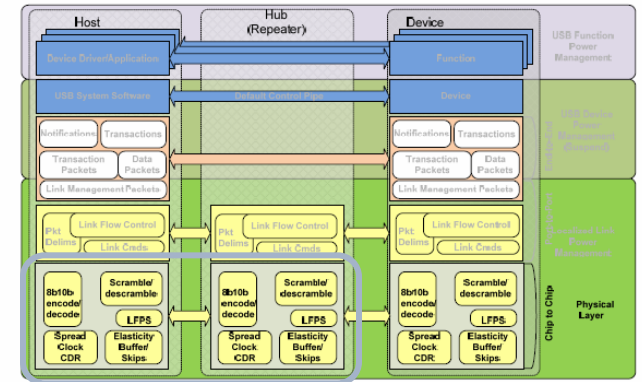
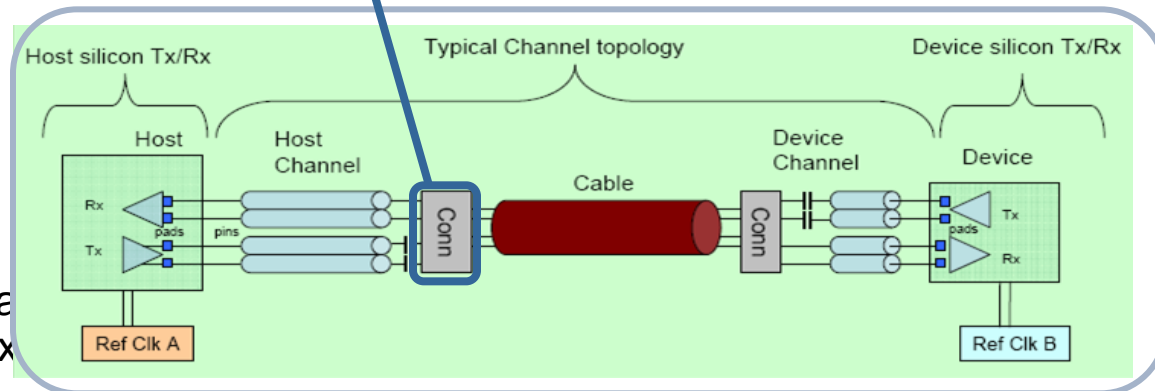
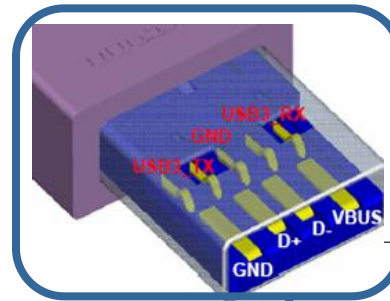


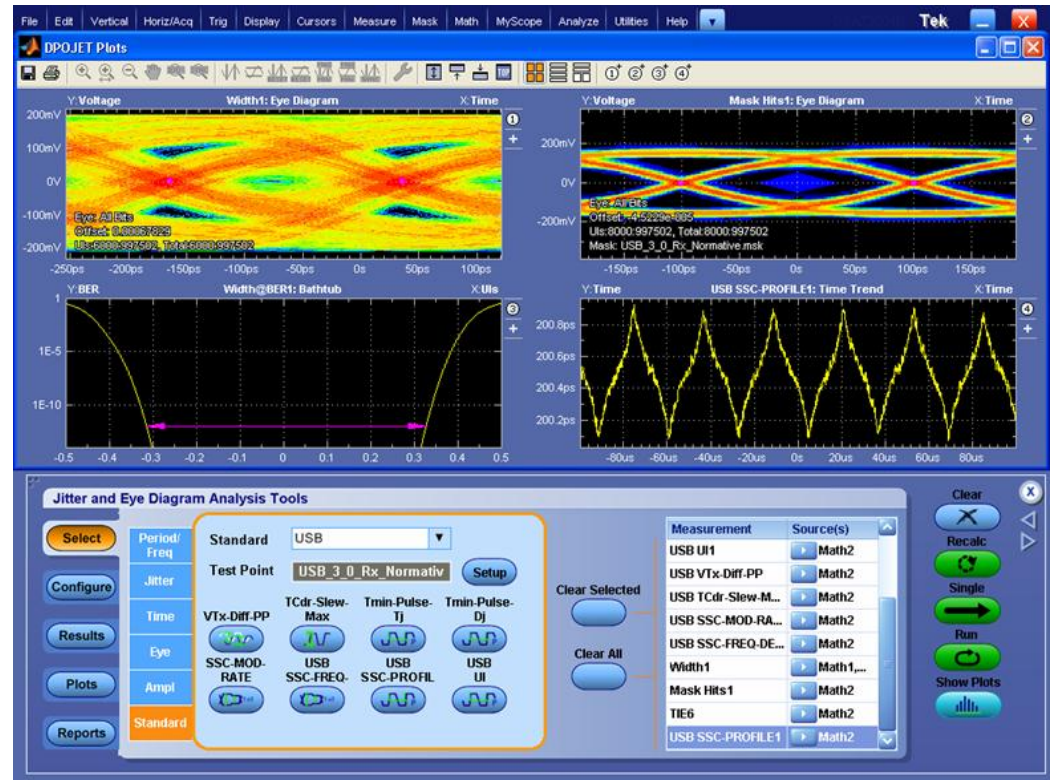
Figure 6-1. Super Speed Block Diagram: Physical



Source: USB 3.0 Rev 1.0 Specification

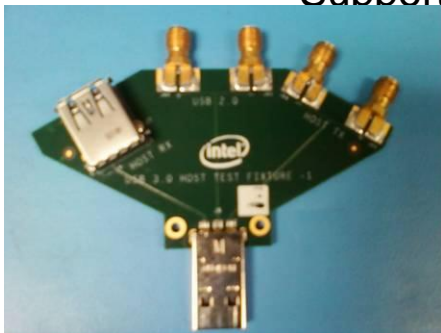
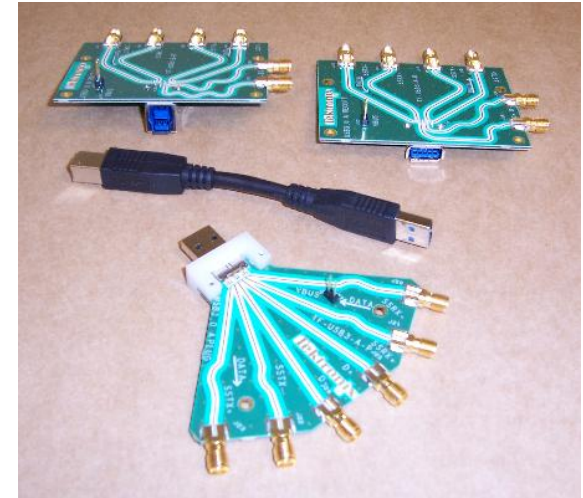
# USB 3.0 Transmitter Measurement Overview

- Voltage and Timing
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate
- Low Frequency Periodic Signaling (LFPS)
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod
- SSC
  - Modulation Rate
  - Deviation



# USB 3.0 Test Fixtures

- Two options for USB 3.0 Test Fixtures
  - Tektronix supplied fixtures
    - Enables SW channel emulation for TX and RX testing
    - Published electrical specifications
    - Supports TX, RX, and Cable testing
    - Available from Tektronix
  - USB-IF supplied fixtures and cables (shown below)
    - Used for compliance testing
    - Enables SW channel emulation for TX only
    - Supports TX and RX testing



# NEW Debug and Analysis Tools

- USB3 Decode with Hierarchical Bus display
- Includes Digital, 8b10b, PHY, LINK, and Transaction layers
- Enables decode, search and trigger, available with option SR-USB

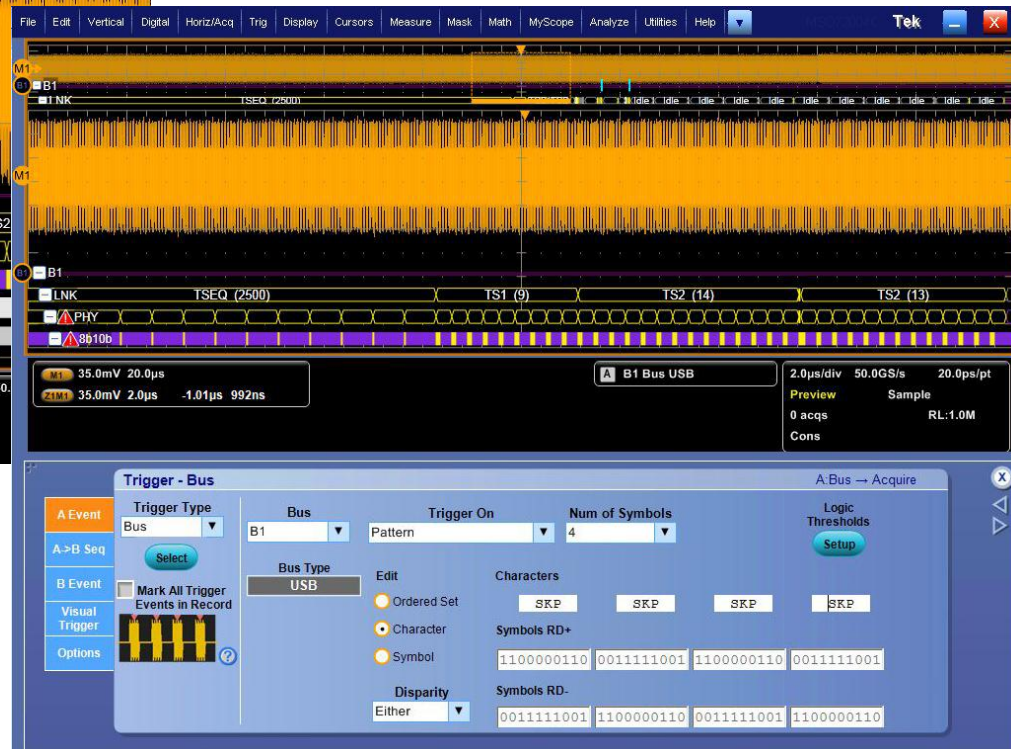


# Decode and Trigger Examples

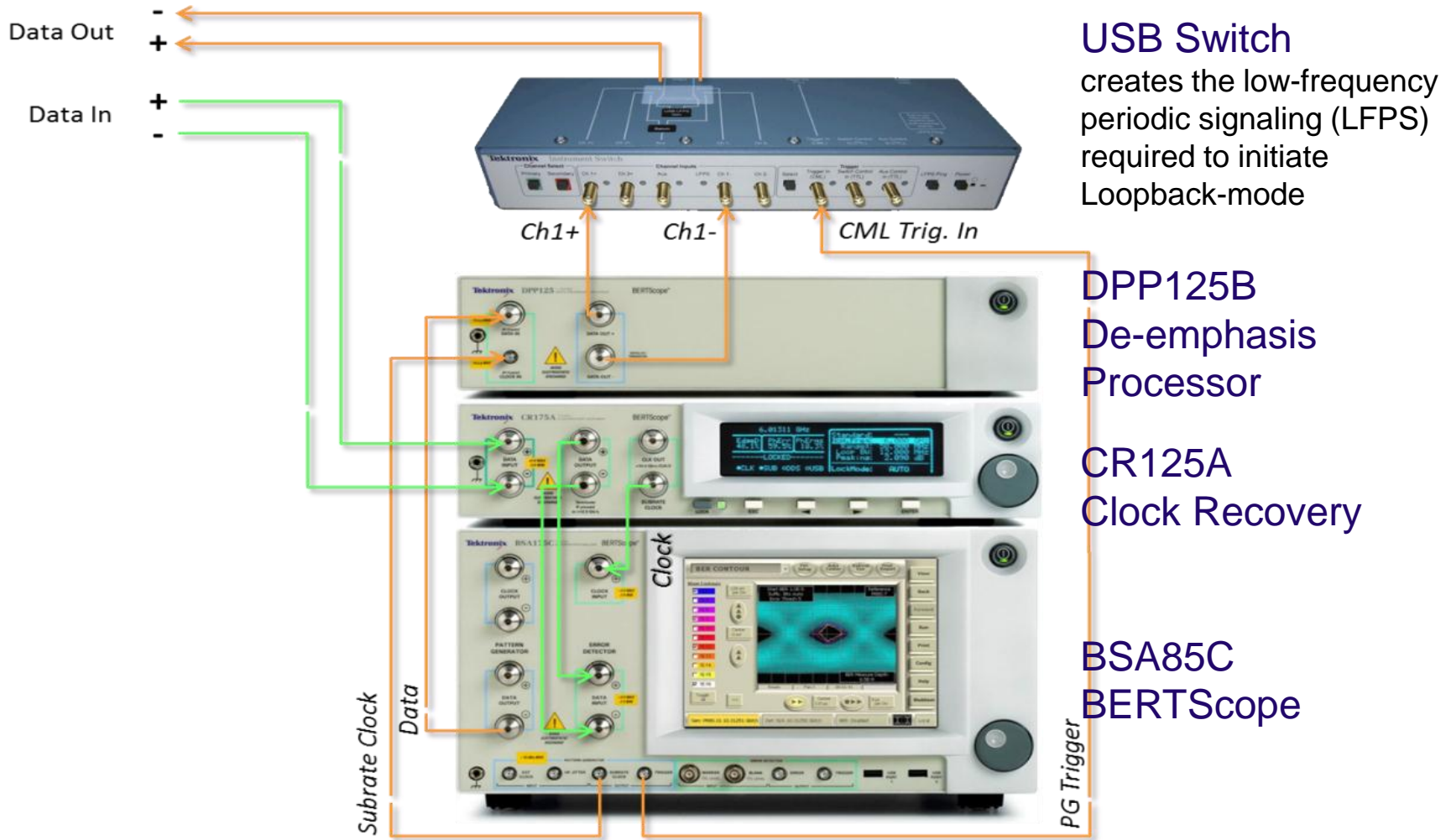
## USB3 Link Training



## USB3 Trigger Setup

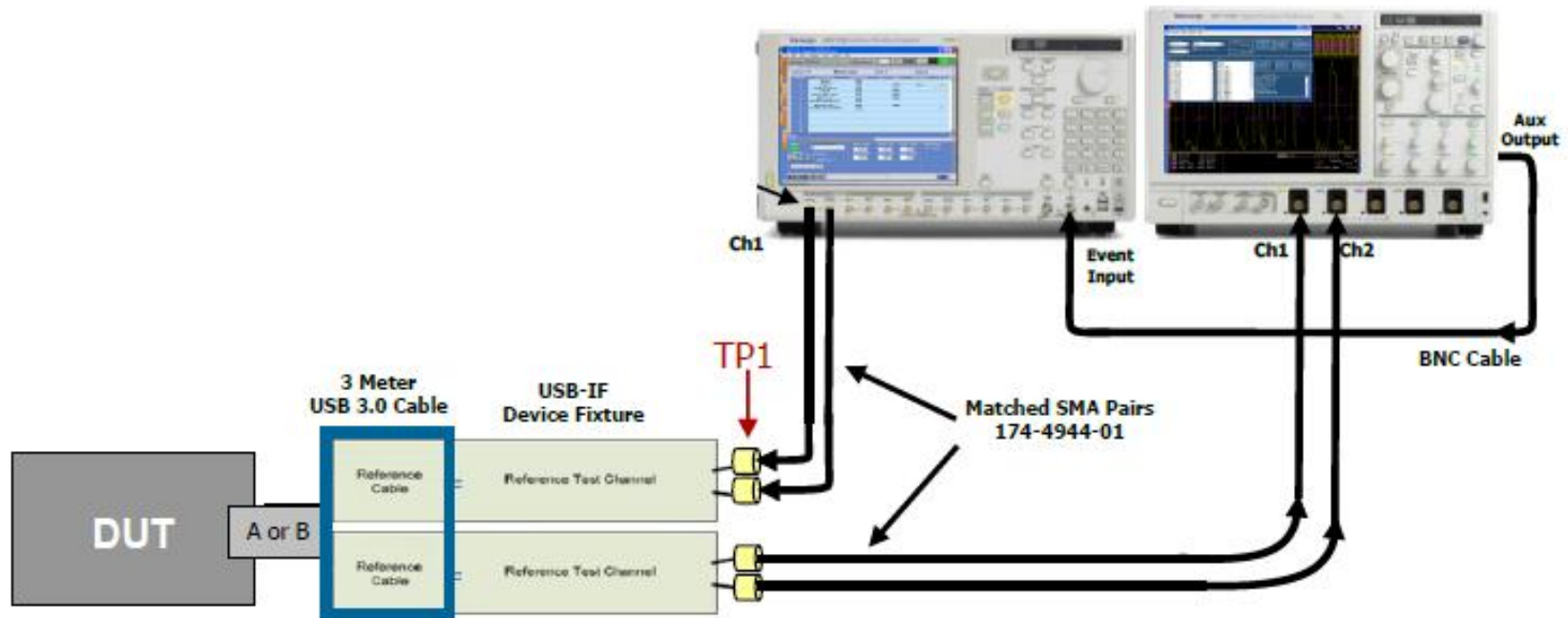


# BERTScope USB 3.0 RX Test Configuration



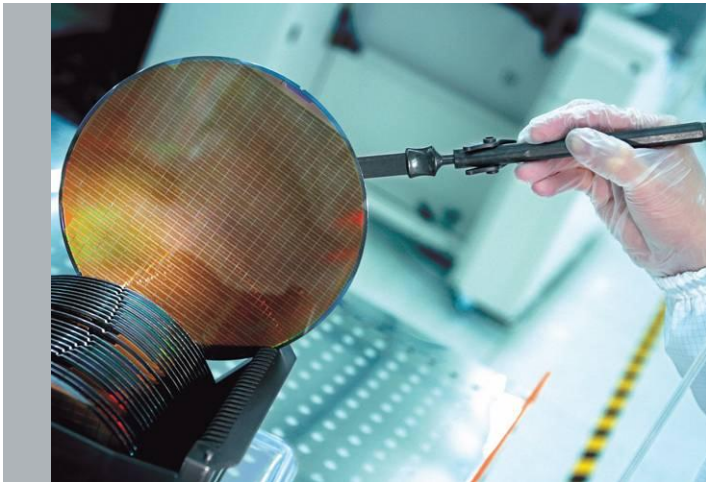
# AWG USB 3.0 RX/TX Test Configuration

- Only test equipment setup with a common configuration for Receiver and Transmitter Testing
- All Signal Impairments including channel impairments generated by the AWG
- No need for external error detectors
  - Only Oscilloscope based bit or symbol error detection solution (Ellisys Protocol Analyzers also supported)





# Introduction to USB 3.0 SuperSpeedPlus

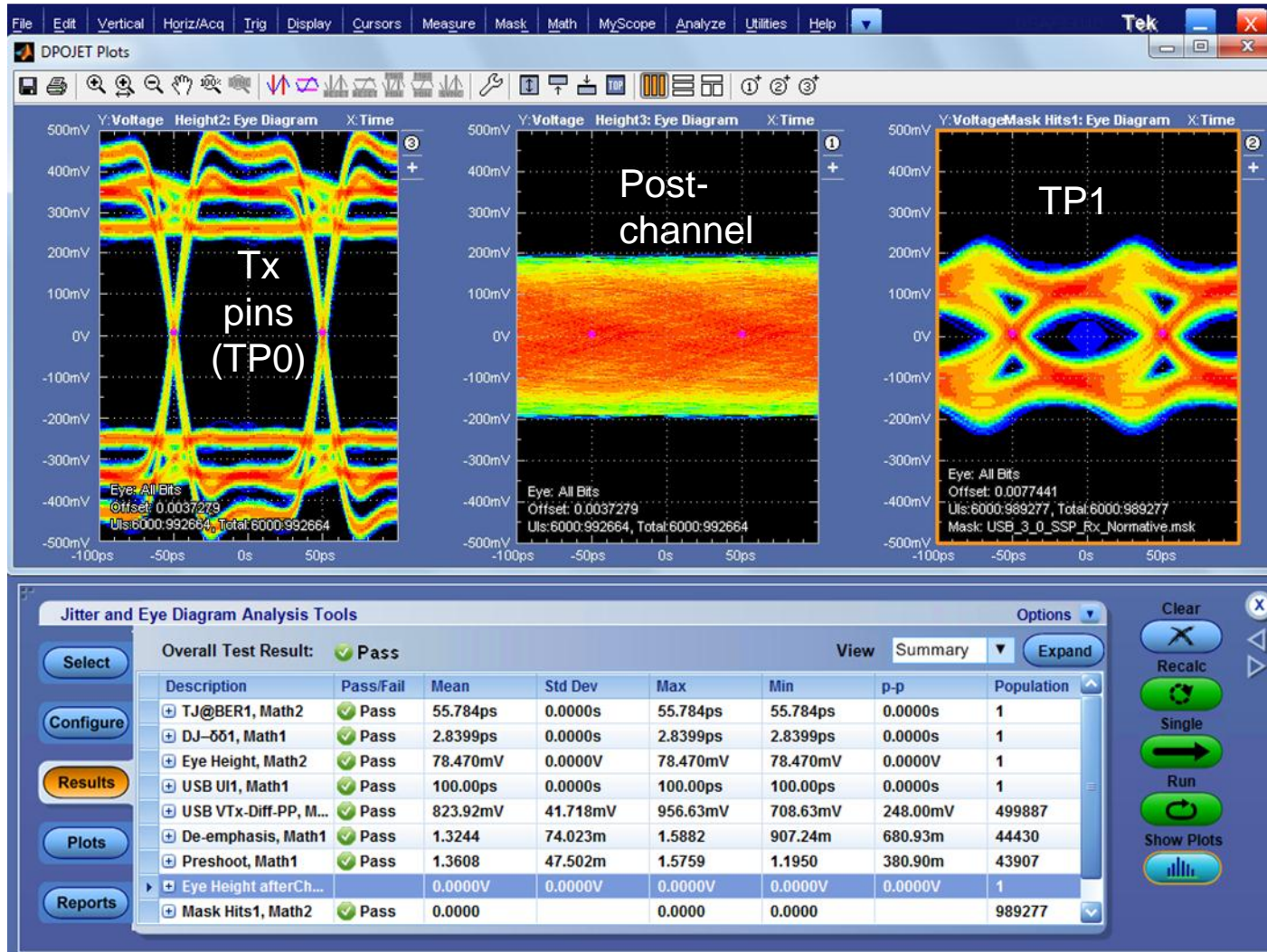


# USB 3.0 Comparison

	SuperSpeed	SuperSpeedPlus
Data Rate	5 Gb/s	10 Gb/s
Encoding	8b/10b	128b/132b
Target Channel	3m + Host/Device channels (-17dB, 2.5 GHz)	1m + board ref channels (-20dB, 5 GHz)
LTSSM	LFPS, TSEQ, TS1, TS2	LFPSPlus, SCD, TSEQ, TS1, TS2,
Reference Tx EQ	De-emphasis	3-tap (Preshoot/De-emphasis)
Reference Rx EQ	CTLE	CTLE + 1-tap DFE
JTF Bandwidth	4.9 MHz	7.5 MHz
Eye Height (TP1)	100 mV	70 mV
TJ@BER	132 ps (0.66 UI)	71 ps (0.714 UI)
Backwards compatibility	Y	Y
Connector	Std A	Improved Std A with insertion detect

# Transmitter Validation Example – DPOJET

- Measure Eye height and jitter at TP1

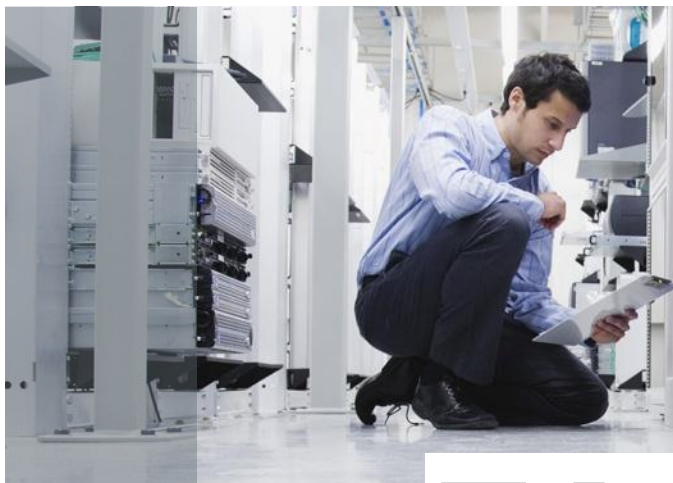


## Recommended Transmitter Solution

- $\geq 20$  GHz BW, 100 GS/sec preferred
  - DSA72004C or higher recommended
- $>10$ M minimum record length allows capture of 1M UI at 100 GS/sec, no interpolation. Increase memory depth if interpolation will be enabled, or if  $>1$ MUI captures are desired.
- Option DJA Advanced DPOJET required, signal analysis
- Option SLA Advanced SDLA required, cycle through 7 CTLE/1 DFE settings
- Option SSP, provides USB3 10G specific measurements

For instrument bandwidth, consider factors such as edge rate, reflections, SNR (de-embedding), and launch characteristics.

感谢您的关注！



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