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Tektronix Method of Implementation for PCI Express Gen 4.0 TX CEM Test Procedure

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MODIFICATION RECORD

Version	Date	Changes done
0.1 Draft	07-Jan-2019	All
0.2 Draft	08-Jan-2019	Section 4
0.3 Draft	17-Jan-2019	All
0.4 Draft	04-Feb-2019	All
0.5 Draft	06-Feb-2019	All
0.6 Draft	07-Feb-2019	All
0.7 Draft	07-Feb-2019	All
1.0	12-Feb-2019	All

References

The following documents are referenced in this document:

- *PCI Express® Architecture PHY Test Specification Revision 4.0, Version 0.9*

Software

- TekScope Firmware v10.8 or above
- DPOJET v10.0.6 or above
- DPOJET PCIE v10.4.2 or above
- TekExpress PCI Express v10.4.4 or above
- SIGTEST Post processing analysis tools (4.0.42) / (4.0.45) as on 12-Feb-2019
- Check for latest SigTest versions on the Intel website

REQUIRED EQUIPMENTS

Equipment	Details	Qty	P/N	Vender
Gen4 CEM Fixture	CBB/CLB/ISI Board of PCIE 4.0 Rev2.0	1	NA	PCI-SIG
SMA-SMA Cable	1m SMA-SMA Phase Matched Cable Pair	1	PMCABLE1M	Tektronix
SMA-SMP Cable	1m SMA-SMP Phase Matched Cable Pair (1 pair needed without toggle automation and 2 pairs needed with)	2 (pairs)	174-6659-01	Tektronix
SMA-SMP short cable	SMA - SMP cable pair, 2.5 inches, <1psec skew	1 (pair)	80350960	Huber-Suhner
SMP-SMP Cable	SMP-SMP cable pair, 12 inches, <1psec skew	1 (pair)	80345501	Huber-Suhner
SMP-F 50 Ohm terminator	Some Add-In Card require termination for unused lanes.	6/14/30	ST2645	Fairview Microwave
ATX Power Supply	Any ATX Power Supply >=750W	1	NA	Any
Real Time Oscilloscope	DPO73304SX/DPS75002SX DPS75902SX/DPS77002SX	1	NA	Tektronix
AFG/AWG with BNC to SMA adaptors	Optional Equipment – Needed if toggle automation is to be utilized. DC blocks can optionally be added.	1	AWG7122C or AFG (check with rep for PN)	Tektronix
SMA Probes	TCA-SMA-292D	4		Tektronix
Differential Probes	P7625/P7633	2		Tektronix

1. Introduction

This Method of Implementation (MOI) provides direction for testing PCIe Gen4 CEM Tx using a Tektronix Real Time Oscilloscope with the TekExpress PCI Express automation software. This document provides a list of test equipment, connection diagrams, and procedures per the PCI Express Architecture PHY Test Specification Revision 4.0. Following are the five tests which are required for Gen4 CEM Tx.

1. Add-in Card Transmitter Signal Quality Test for 16 GT/s
2. Add-in Card Transmitter Preset Test for 16 GT/s
3. Add-in Card Transmitter Pulse Width Jitter Test for 16 GT/s
4. System Board Transmitter Signal Quality Test for 16 GT/s
5. System Board Transmitter Preset Test for 16 GT/s

2. Probe Support

Tektronix supports both SMA (direct) probes and Differential probes for PCI Express Gen4 Transmitter testing. Add-In Cards require only a Data signal and Systems require both Data and Clock signal for Transmitter testing, so the probe configuration is different between Add-In Cards and Systems.

Refer to the table below for recommended scope and probe configurations:

DUT Type	Probe Type	Scope Model	Note
Add-In Card/ Non-Root	2 x SMA Probe	MSO/DPO72504DX MSO/DPO73304DX DPO73304SX	Use the alternate channel on the scope Ex. Ch1 and Ch3 or Ch2 and Ch4
	1 x Differential Probe	MSO/DPO72504DX MSO/DPO73304DX DPO73304SX	
System/Host/Root	4 x SMA Probe	DPS73308SX DPS75004SX	Use the Master unit TekConnect channels for Data signal and Extension unit TekConnect channels for Clock signal
	2 x Differential Probe	MSO/DPO72504DX MSO/DPO73304DX DPO73304SX	Use the alternate channel on the scope Ex. Ch1 and Ch3 or Ch2 and Ch4

Tektronix Probe P/N:

- SMA Probe: TCA-SMA-292D
- Differential Probe: P7625 or P7633

3. CONNECTION DIAGRAM

This section provides connection diagrams for all Tx tests as descripted in the PCI Express Architecture PHY Test Specification executed with a Tektronix oscilloscope and manually toggling the DUT through the compliance mode patterns.

3.1 Tx Signal Quality Test for Add-In-Card – DUT Toggle in Manual Mode

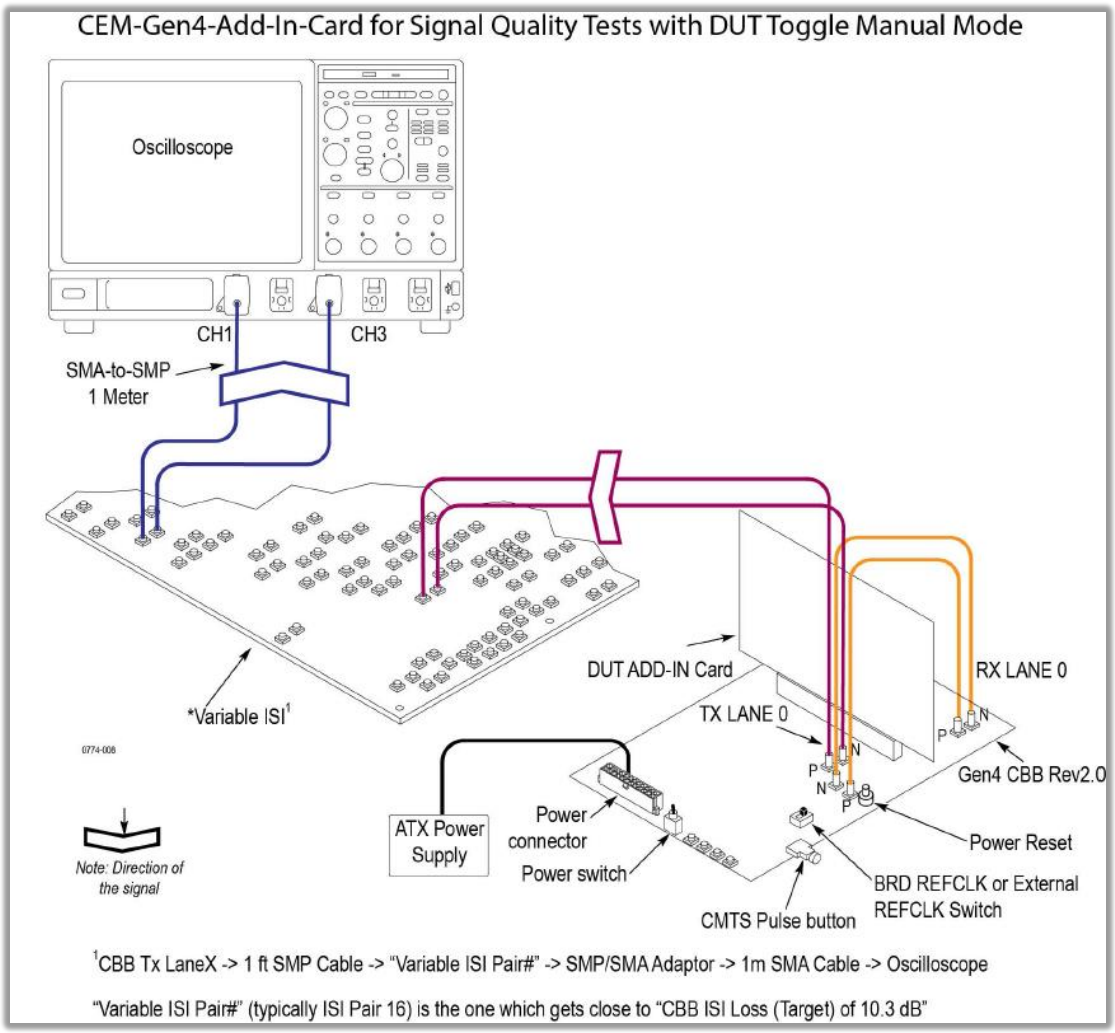


Figure 1 Tx Signal Quality Test for Add-In-Card – DUT Toggle in Manual Mode

LEGEND

2.5" SMP-SMA Cable connected with SMA-SMA 1 Meter Phase Matched Cable from "Variable ISI Pair#16" P and N to Oscilloscope CH1 and CH3

12" SMP-SMP Cable from Gen4 CBB Rev2 TX Lane0 to "Variable ISI Pair#16" P and N

12" SMP-SMP Cable from J5/J85 on the Gen4 CBB Rev2 to RX Lane0 P and N

Brd Ref Clk or External Ref Clk Switch - Ensure it is set towards 'Brd Ref Clk' side for TX Tests

CMTS Pulse button - Compliance Mode Toggle Switch

Note: Variable ISI pair#16 is nominal, but to ensure correct loss follow the VNA based measurements described in the test fixture characterization

3.2 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle in Manual Mode

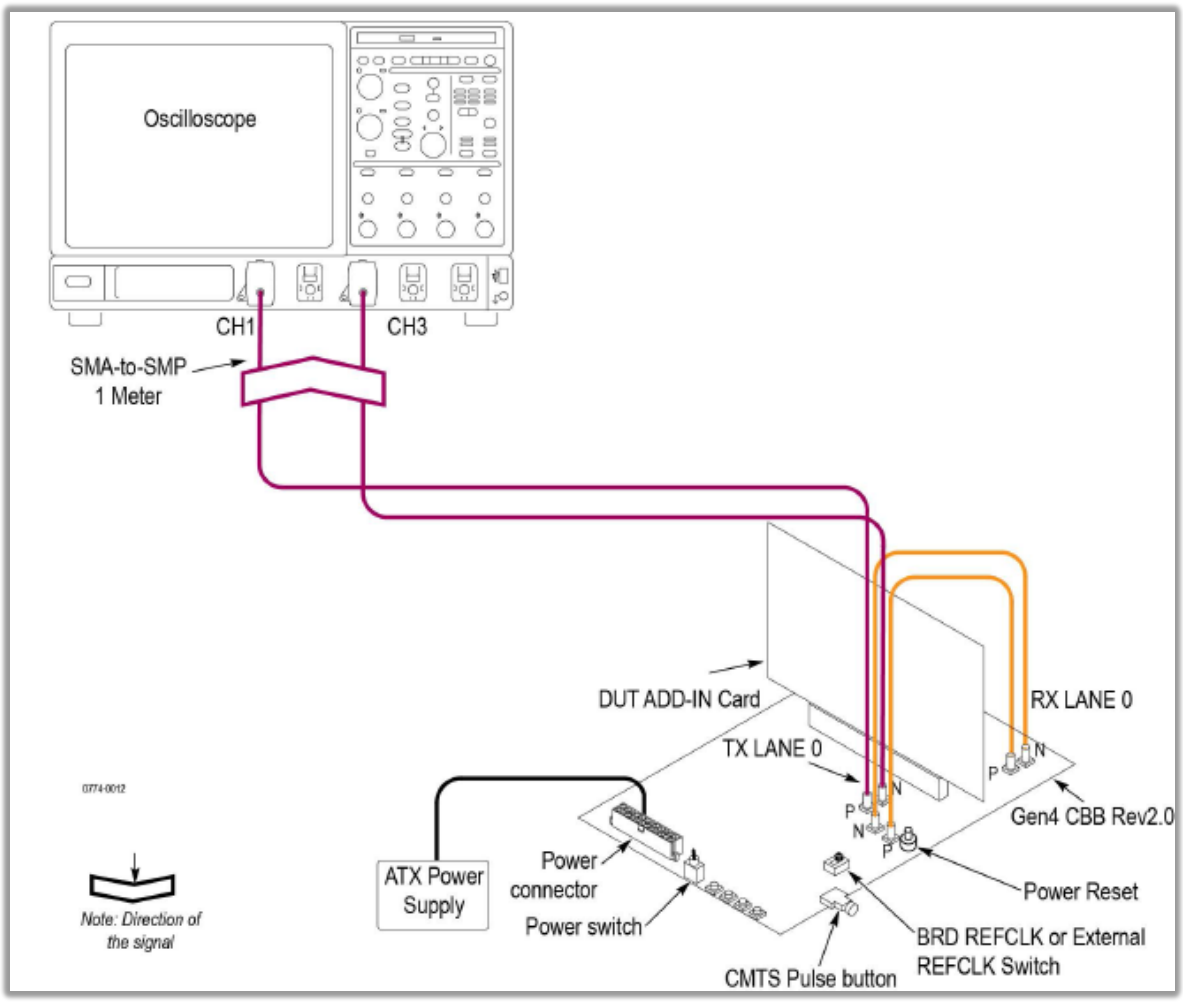


Figure 2 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle in Manual Mode

LEGEND

2.5" SMP-SMA Cable connected with SMA-SMA 1 Meter Phase Matched Cable from Gen4 CBB Rev2 TX Lane0 P and N connected to Oscilloscope CH1 and CH3

12" SMP-SMP Cable from J5/J85 on the Gen4 CBB Rev2 to RX Lane0 P and N

Brd Ref Clk or External Ref Clk Switch - Ensure it is set towards 'Brd Ref Clk' side for TX Tests

CMTS Pulse button - Compliance Mode Toggle Switch

3.3 Tx Signal Quality Test for System-Board – DUT Toggle in Manual Mode

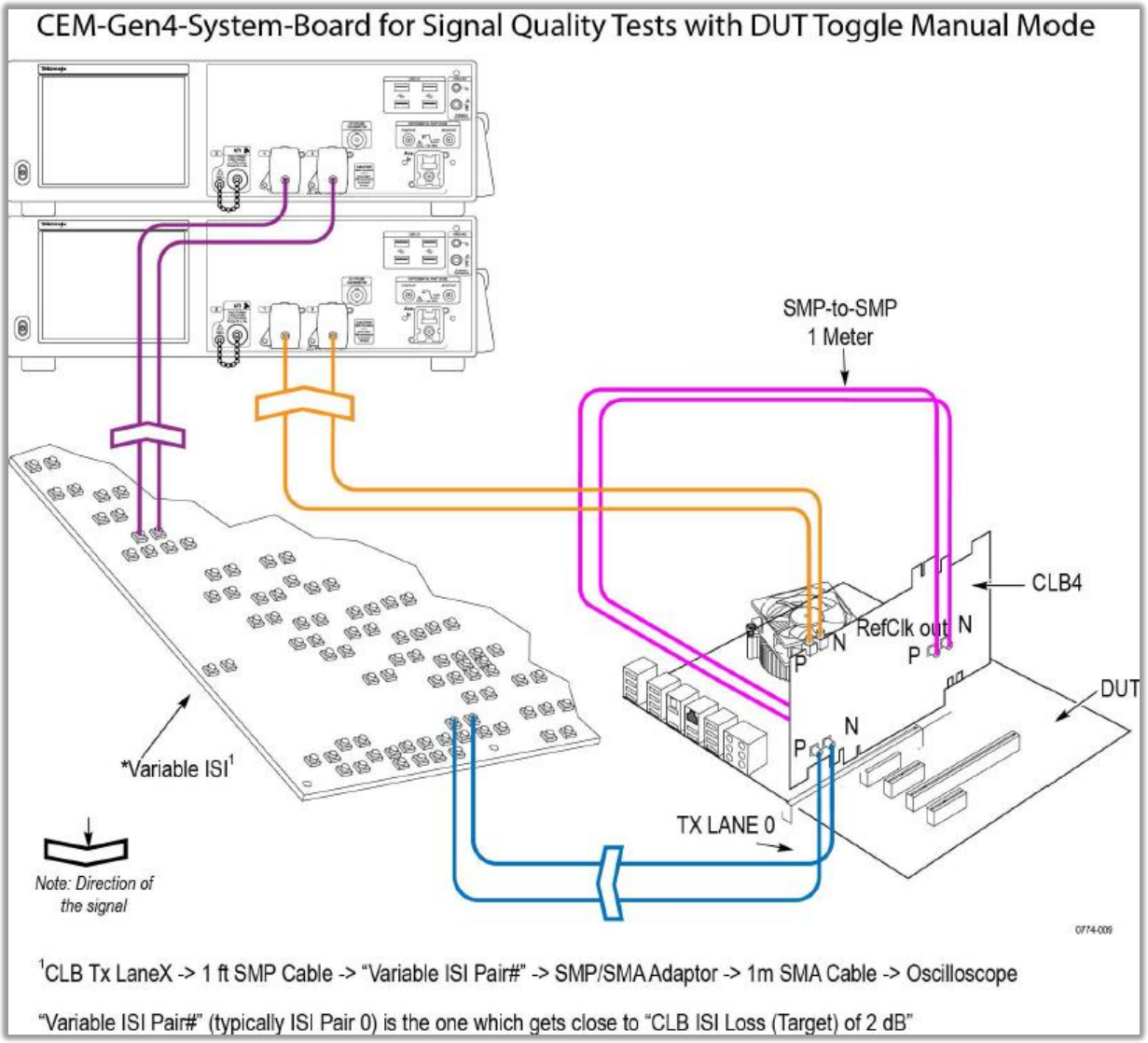


Figure 3 Tx Signal Quality Test for System-Board – DUT Toggle in Manual Mode

LEGEND

- 12" SMP-SMP Cable from Gen4 CLB Rev2 TX Lane0 P and N to "Variable ISI Pair#0" P and N
- 2.5" SMP-SMA Cable connected with SMA-SMA 1 Meter Phase Matched Cable from "Variable ISI Pair#0" P and N connected to Oscilloscope CH1 and CH3
- SMA-SMP 1 Meter Cable from Gen4 CLB Rev2 Ref Clk P and N to Oscilloscope CH2 and CH4
- 12" SMP-SMP Cable from J5/J85 on the CBB Rev2 to RX Lane0 P and N

Note: Variable ISI pair#0 is nominal, but to ensure correct loss follow the VNA based measurements described in the test fixture characterization

3.4 Tx Preset Test for System-Board – DUT Toggle in Manual Mode

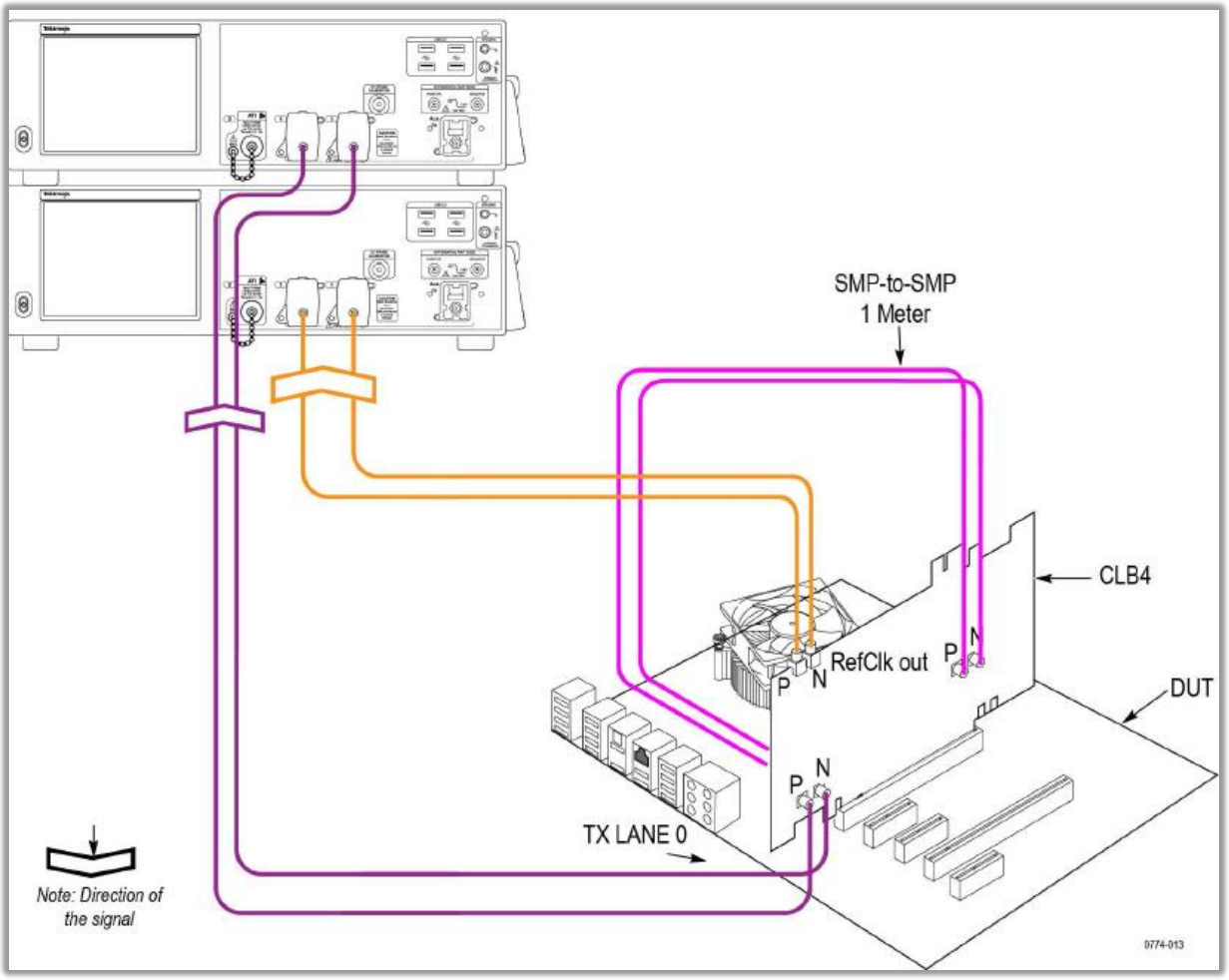


Figure 4 Tx Preset Test for System-Board – DUT Toggle in Manual Mode

LEGEND

2.5" SMP-SMA Cable connected with SMA-SMA 1 Meter Phase Matched Cable from Gen4 CLB Rev2 TX Lane0 P and N to Oscilloscope CH1 and CH3

SMA-SMP 1 Meter Cable from Gen4 CLB Rev2 Ref Clk P and N to Oscilloscope CH2 and CH4

12" SMP-SMP Cable from J5/J85 on the CBB Rev2 to RX Lane0 P and N

3.5 Tx Signal Quality Test for Add-In-Card – DUT Toggle Automation

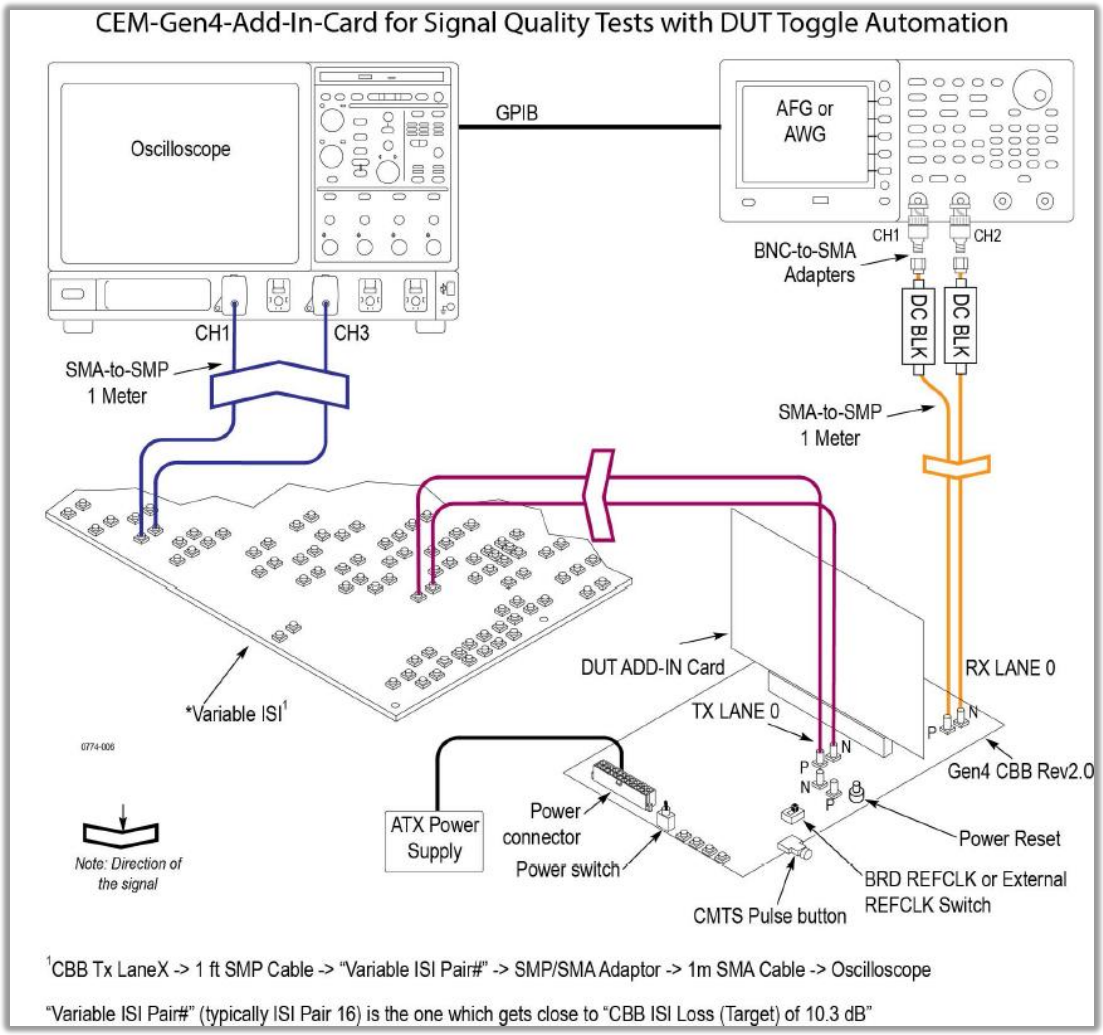


Figure 5 Tx Signal Quality Test for Add-In-Card – DUT Toggle Automation

LEGEND

2.5" SMP-SMA Cable connected with SMA-SMA 1 Meter Phase Matched Cable from "Variable ISI Pair#16" P and N to Oscilloscope CH1 and CH3

12" SMP-SMP Cable from Gen4 CBB Rev2 TX Lane0 to "Variable ISI Pair#16" P and N

SMA-SMP 1 Meter Cable from AWG/AFG on the Gen4 CBB Rev2 to RX Lane0 P and N

Note:
If you are using AFG for DUT toggle automation, DC blocks are optional. They are not required for AWG.

Brd Ref Clk or External Ref Clk Switch - Ensure it is set towards 'Brd Ref Clk' side for TX Tests

CMTS Pulse button - Compliance Mode Toggle Switch

Note: Variable ISI pair#16 is nominal, but to ensure correct loss follow the VNA based measurements described in the test fixture characterization

3.6 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle Automation

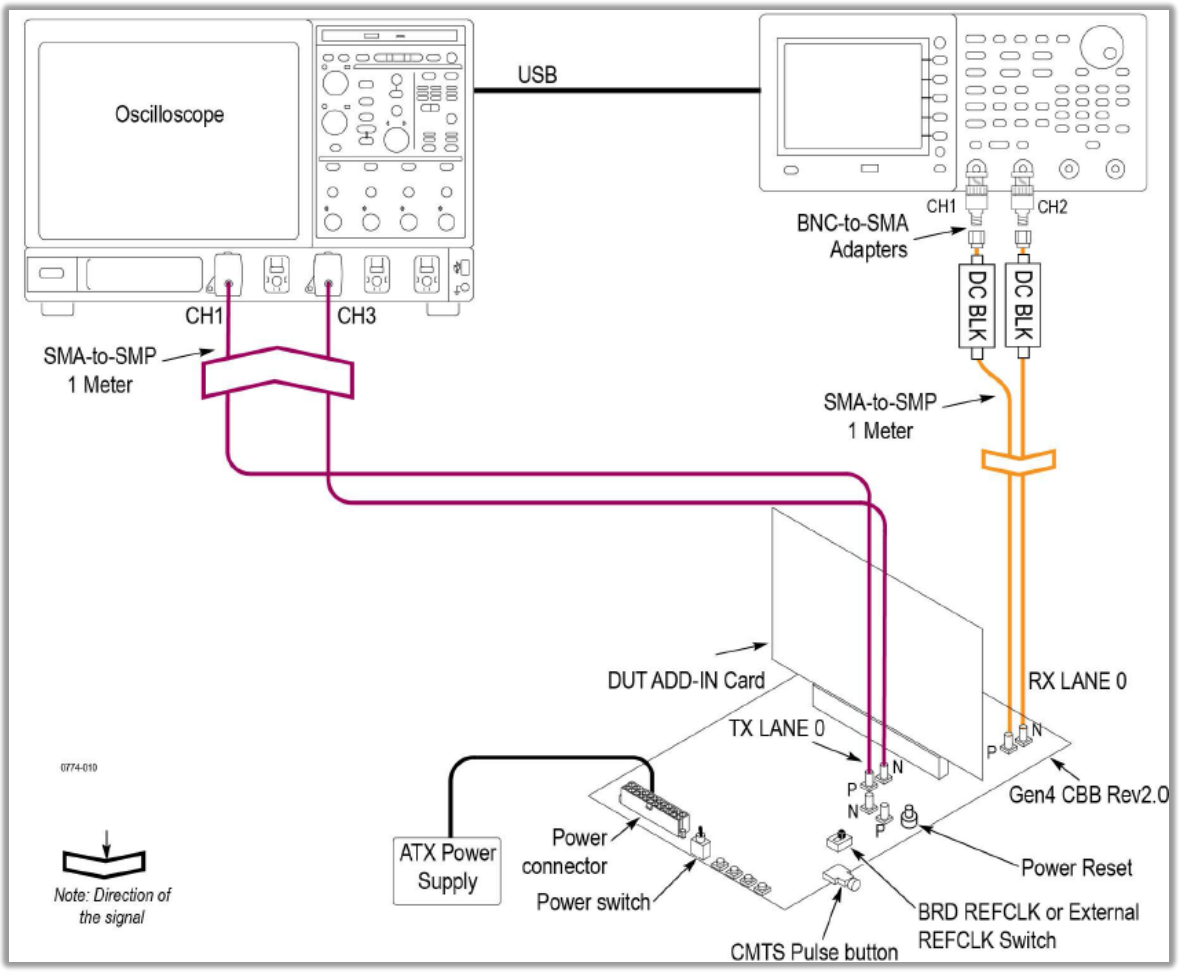


Figure 6 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle Automation

LEGEND

2.5" SMP-SMA Cable connected with SMA-SMA 1 Meter Phase Matched Cable from Gen4 CBB Rev2 TX Lane0 P and N connected to Oscilloscope CH1 and CH3

SMA-SMP 1 Meter Cable from AWG/AFG on the Gen4 CBB Rev2 to RX Lane0 P and N
Note:
If you are using AFG for DUT toggle automation, DC blocks are optional. They are not required for AWG.

Brd Ref Clk or External Ref Clk Switch - Ensure it is set towards 'Brd Ref Clk' side for TX Tests

CMTS Pulse button - Compliance Mode Toggle Switch

3.7 Tx Signal Quality Test for System-Board – DUT Toggle Automation

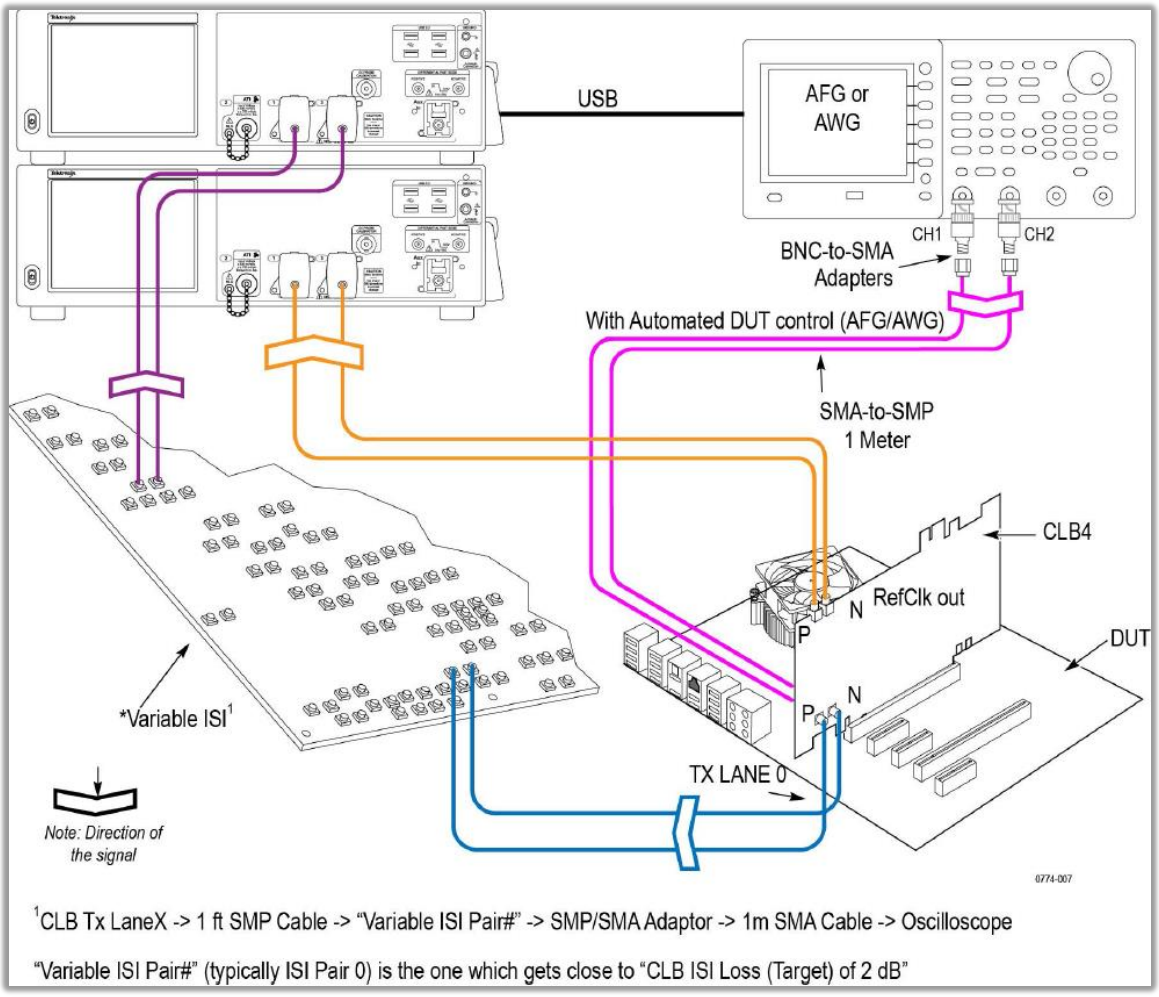


Figure 7 Signal Quality Test for System-Board – DUT Toggle Automation

LEGEND

12" SMP-SMP Cable from Gen4 CLB Rev2 TX Lane0 P and N to "Variable ISI Pair#0" P and N

2.5" SMP-SMA Cable connected with SMA-SMA 1 Meter Phase Matched Cable from "Variable ISI Pair#0" P and N connected to Oscilloscope CH1 and CH3

SMA-SMP 1 Meter Cable from Gen4 CLB Rev2 Ref Clk P and N to Oscilloscope CH2 and CH4

SMA-SMP 1 Meter Cable from AWG/AFG on the Gen4 CLB Rev2 to RX Lane0 P and N

Note:
If you are using AFG for DUT toggle automation, DC blocks are optional. They are not required for AWG.

Note: Variable ISI pair#0 is nominal, but to ensure correct loss follow the VNA based measurements described in the test fixture characterization

3.8 Tx Preset Test for System-Board – DUT Toggle Automation

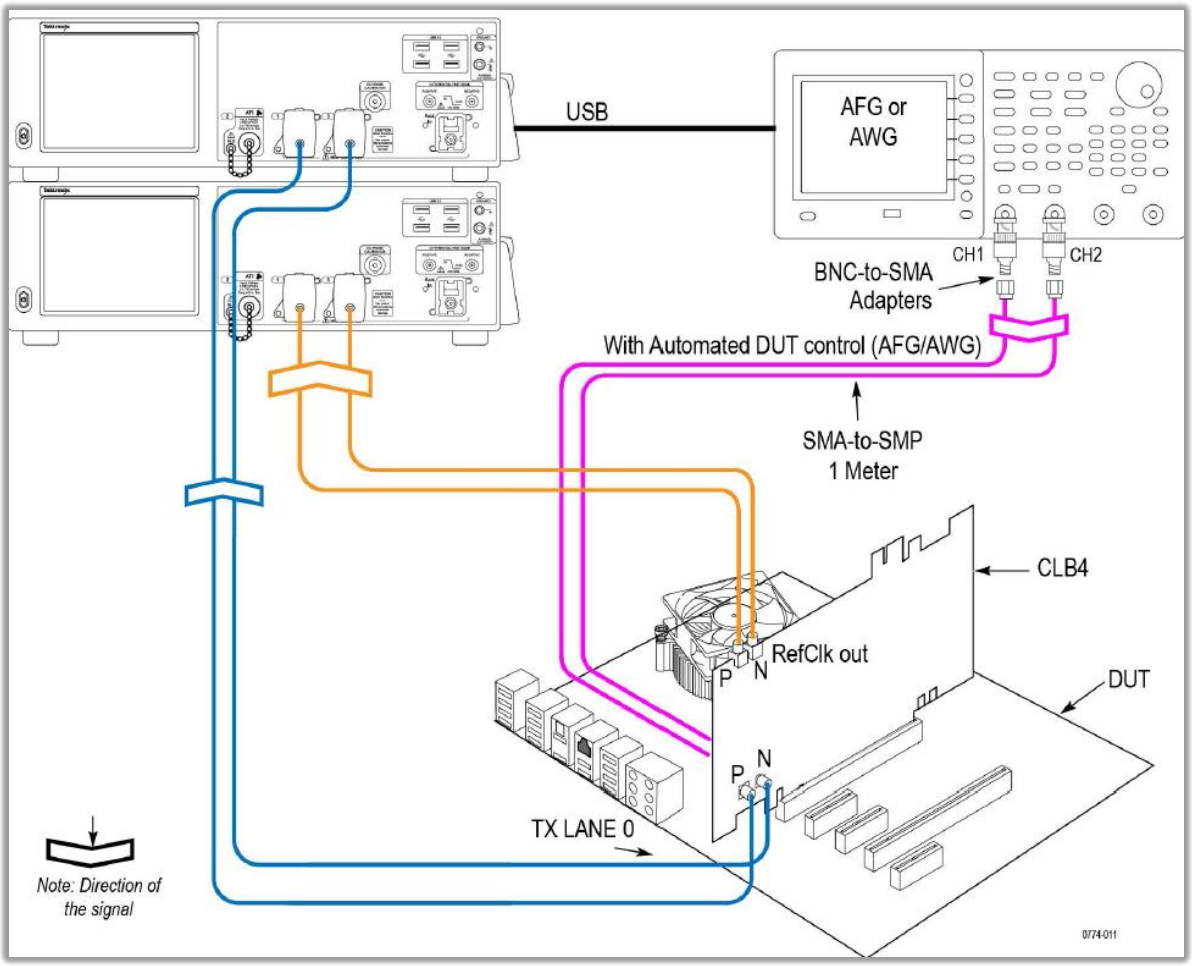


Figure 8 Tx Preset Test for System-Board – DUT Toggle Automation

LEGEND

2.5" SMP-SMA Cable connected with SMA-SMA 1 Meter Phase Matched Cable from Gen4 CLB Rev2 TX Lane0 P and N to Oscilloscope CH1 and CH3

SMA-SMP 1 Meter Cable from Gen4 CLB Rev2 Ref Clk P and N to Oscilloscope CH2 and CH4

SMA-SMP 1 Meter Cable from AWG/AFG on the Gen4 CLB Rev2 to RX Lane0 P and N

Note:
If you are using AFG for DUT toggle automation, DC blocks are optional. They are not required for AWG.

4. Tests

Following are the five tests that are recommended for Gen4 CEM Tx.

1. Add-In-Card Transmitter Signal Quality Test for 16 GT/s
2. Add-In-Card Transmitter Preset Test for 16 GT/s
3. Add-In-Card Transmitter Pulse Width Jitter Test for 16 GT/s
4. System-Board Transmitter Signal Quality Test for 16 GT/s
5. System-Board Transmitter Preset Test for 16 GT/s

4.1 Add-In-Card Transmitter Signal Quality Test for 16GT/s

This is referred to as "Add-In-Card Transmitter Electrical Compliance Test for 16.0 GT/s" in *PCI Express® Architecture PHY Test Specification Revision 4.0, Version 0.9*. This test is run on all card electromechanical (CEM) form factor add-in cards. This test verifies the Tx signal of the system at 16 GT/s meets the minimum eye diagram requirements with at least one Tx equalization preset.

1. Insert the Add-In Card under test into a compliance base board (CBB) 4.0 without power.
2. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
3. Launch TekExpress PCI Express Application from TekScope → Analyze menu.
4. Select the configuration in the application as per the figure below.

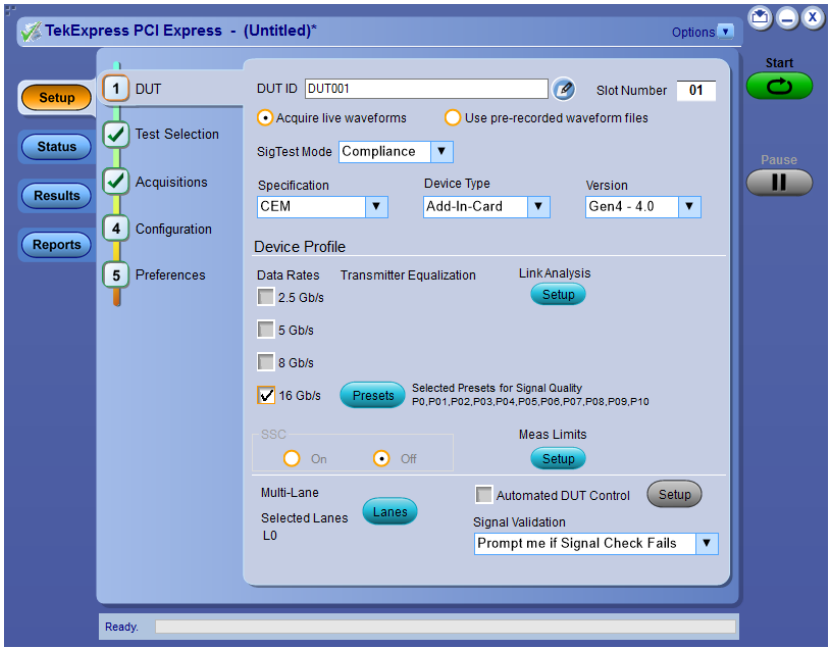


Figure 9 TekExpress PCI Express Add-In-Card Signal Quality Test Selection 1

5. Go to Test Selection panel and observe that Signal Test of 16Gbps are selected. By default, 'Uncorrelated PWJ TJ @E-12 Gen4' test is in unchecked state as physical connections are different and the procedure is explained in another section.

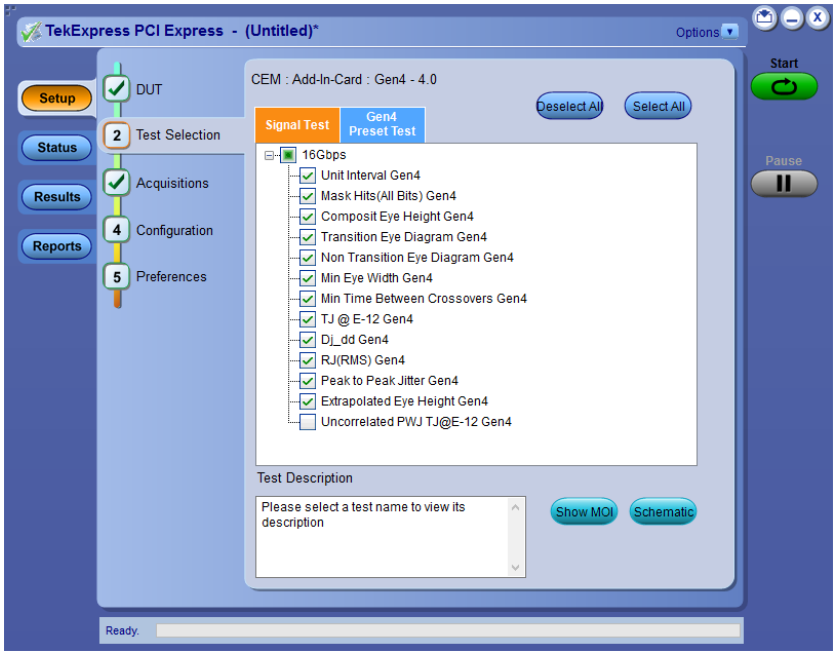


Figure 10 TekExpress PCI Express Add-In-Card Signal Quality Test Selection 2

6. Go to Acquisition panel and set the source of Lane0 Date+ to CH1 and Data- to CH3. Set the No of Acquisitions to '3' as we need to capture three 2.0M UI (Gen4 Compliance Pattern) differential waveforms for every Tx EQ Preset.

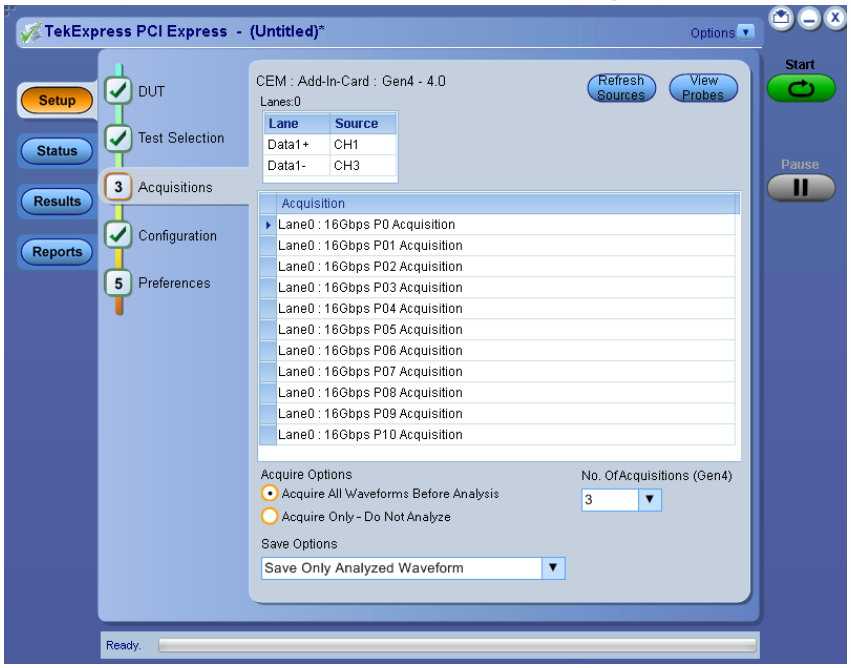


Figure 11 TekExpress PCI Express Add-In-Card Signal Quality Test Acquisitions

7. For the Tx Signal Quality Test for Add-In-Card in automated procedure we are using TekExpress PCI Express with automated DUT toggle option using AWG7122C. User can use AFG/AWG/GRL PCIE Controller for automated DUT toggle option. Refer the 'Appendix Section#5.3.1' for manual DUT toggle option.

8. Go to Configuration panel and select the 'Signal Source for DUT Automation' [AWG7122 in this case] and select the check box 'Automated DUT Control'.

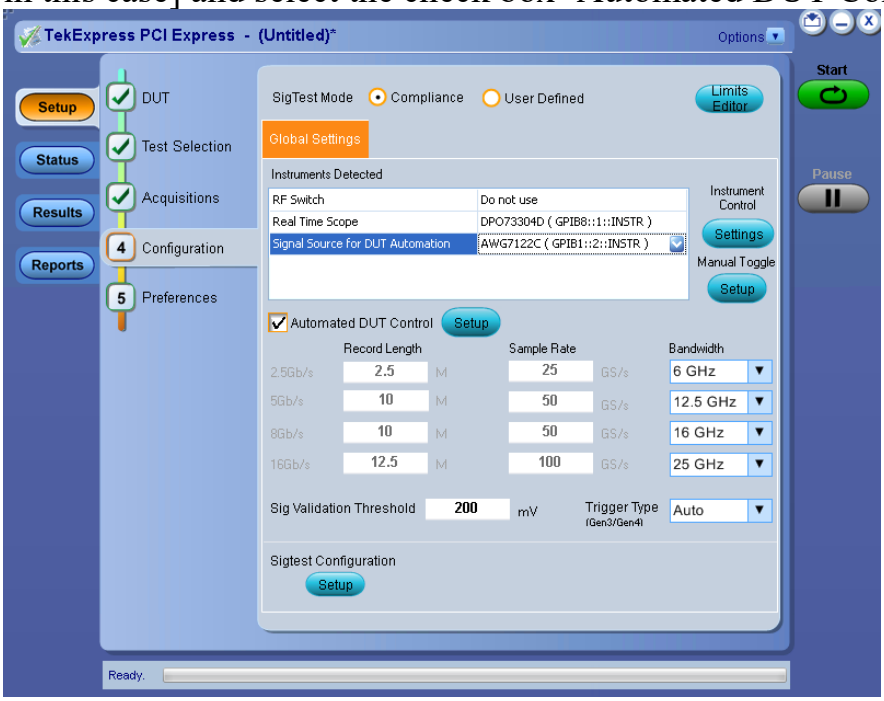


Figure 12 TekExpress PCI Express Add-In-Card Signal Quality Test Configuration

9. Click on SigTest configuration 'Setup' and observe the SigTest version and templates used for this test.

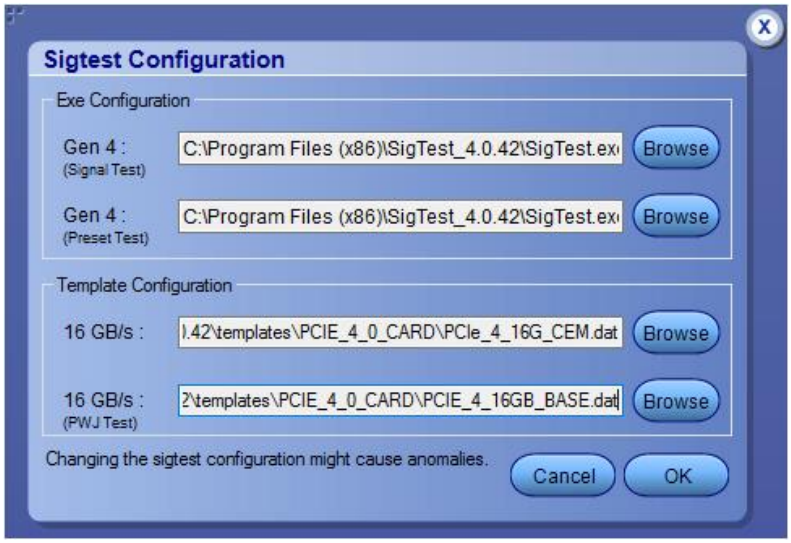


Figure 13 TekExpress PCI Express Add-In-Card Signal Quality Test SigTest Configuration

10. Click on 

to run the test.
11. Make the connection as per section#3.5 (Figure 5 Tx Signal Quality Test for Add-In-Card – DUT Toggle Automation) and verify that it as per the connection diagram that is prompted by application up during the run, Power ON the DUT and click OK to continue.
12. Observe that the DUT will be toggled automatically from Gen1 to Gen4 Preset P0
    And will start acquisition, observe that Package model embedded on the scope (refpkg_rootcomplex_5db_thru.s4p) gets applied and three waveforms of each preset are saved.

Figure 14 TekExpress PCI Express Add-In-Card Signal Quality Test applying package model

13. All acquired waveforms will be processed with SigTest using the "PCIe_4_16G_CEM.dat" template file which performs CTLE optimization. If all Tx EQ presets fail with this approach, you can configure the SigTest Setup (step #9) to run each CTLE individually using the "PCIe_4_16G_CEM_CTLE_6dB.dat through PCIe_4_16G_CEM_CTLE_12dB.dat" template files. A passing result with either case is allowed per the PCI Express Architecture PHY Test specification.

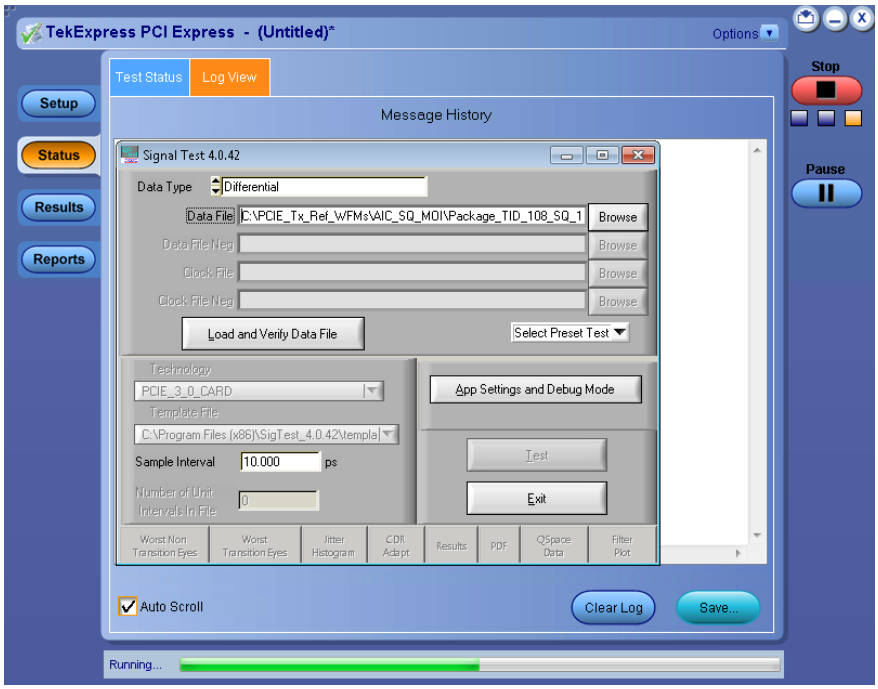


Figure 15 TekExpress PCI Express Add-In-Card Signal Quality Test SigTest Analysis

14. Observe the test results in TekExpress Results panel and once all the results are updated a test report will be generated. Additional information is provided beyond the compliance test criteria of passing the Min Eye Width and Extrapolated Eye Height measurements.

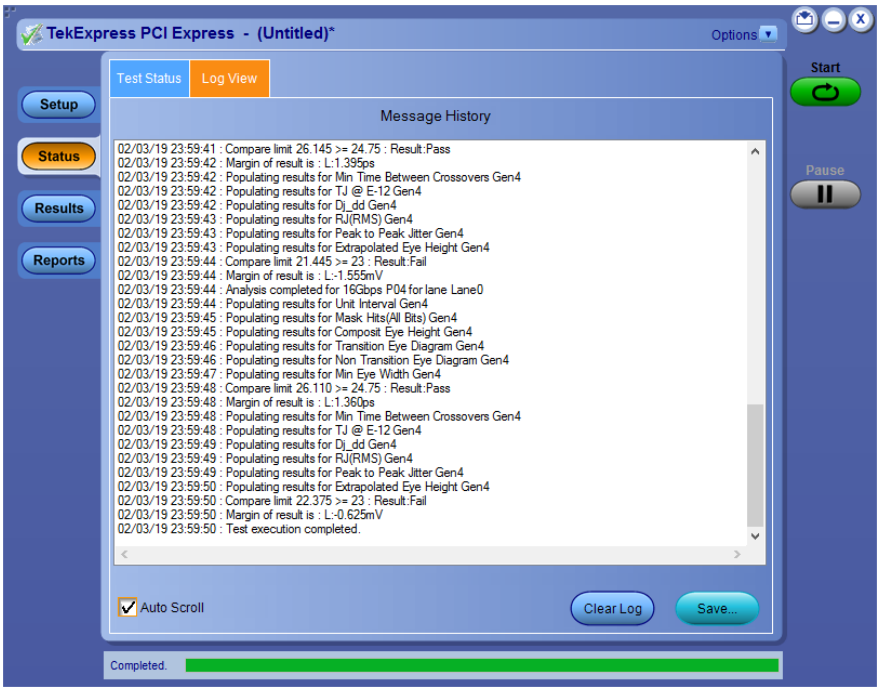


Figure 16 TekExpress PCI Express Add-In-Card Signal Quality Test Status

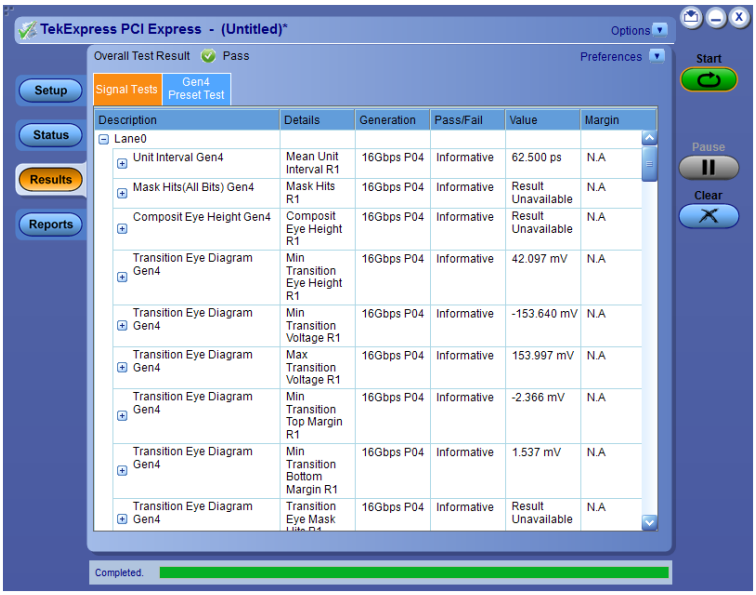


Figure 17 TekExpress PCI Express Add-In-Card Signal Quality Test Results

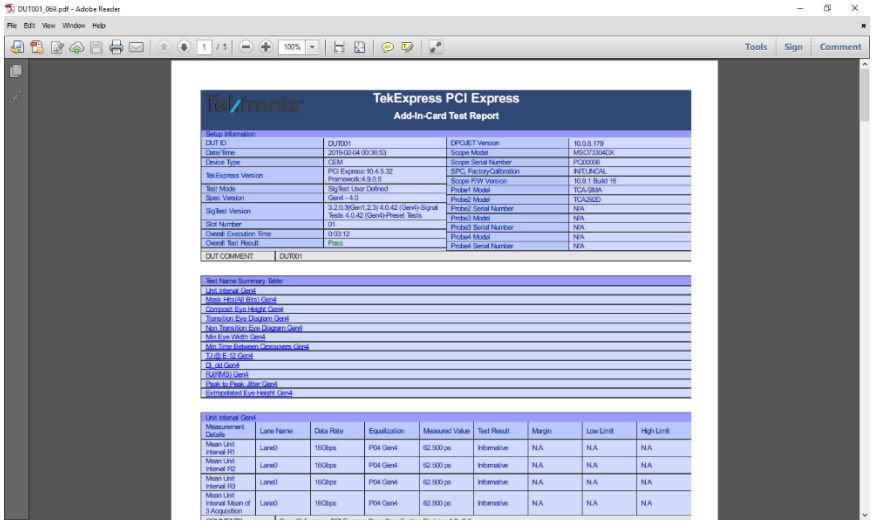


Figure 18 TekExpress PCI Express Add-In-Card Signal Quality Test Report

15. Once test report is generated you can save the Test Session in TekExpress, Options → Save Test Setup → Tek_Gen4_AIC_SQ_MOI (Example of session name). The saved data can be found in the location X:\PCI Express\Tek_Gen4_AIC_SQ_MOI\DUT001.

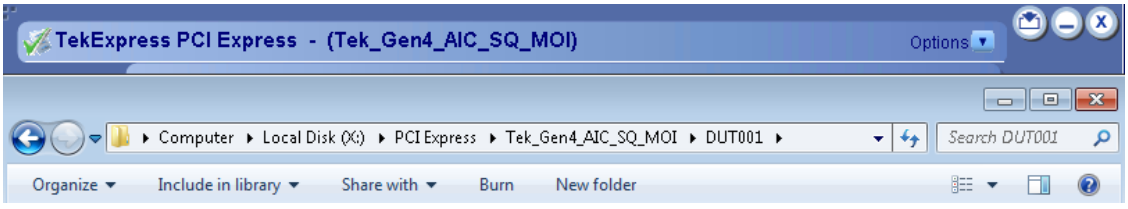


Figure 19 TekExpress PCI Express Add-In-Card Signal Quality Test Session Saved

4.2 Add-In-Card Transmitter Preset Test for 16 GT/s

This is referred as "Add-In-Card Transmitter Preset Test for 16.0 GT/ s" in *PCI Express® Architecture PHY Test Specification Revision 4.0*. This test is run on all card electromechanical form factor add-in cards that operate at 16.0 GT/s. The test verifies that the add-in card produces the correct transmitter equalization values for each preset in the set of 11 presets.

1. Insert the Add-In Card under test into a compliance base board (CBB) without power. A CBB revision 4.0 must be used at all data rates if 16 GT/s is supported.
2. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
3. Launch TekExpress PCI Express Application from TekScope → Analyze menu.
4. Select the configuration in the application as per the figure below.

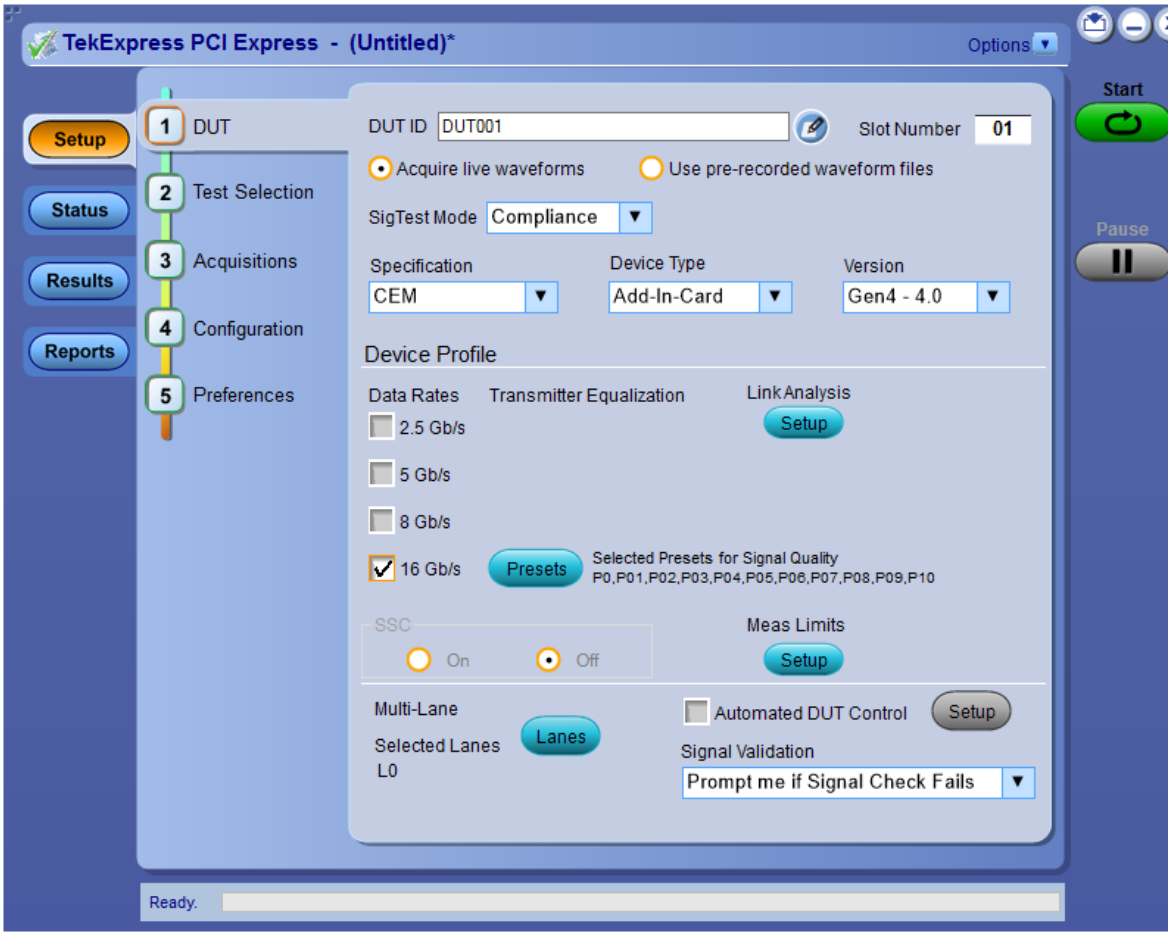


Figure 20 TekExpress PCI Express Add-In-Card Preset Test

5. Go to Test Selection panel and uncheck all the ‘Signal Tests’ in the 16Gbps tree node in the ‘Signal Test’ tab, then go to ‘Gen4 Preset Test’ tab and click on ‘Select All’ so that all the presets get selected.

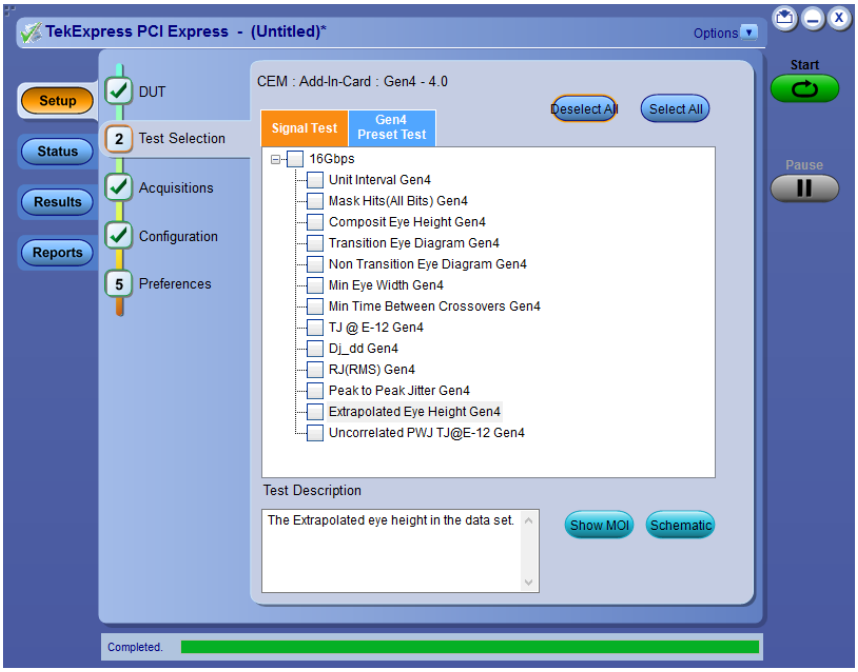


Figure 21 TekExpress PCI Express Add-In-Card Preset Test Selection 1

Figure 22 TekExpress PCI Express Add-In-Card Preset Test Selection 2

6. Go to Acquisition panel and set the source of Lane0 Date+ to CH1 and Data- to CH3. By default, one differential waveforms for every Tx EQ Preset is captured and saved by TekExpress.

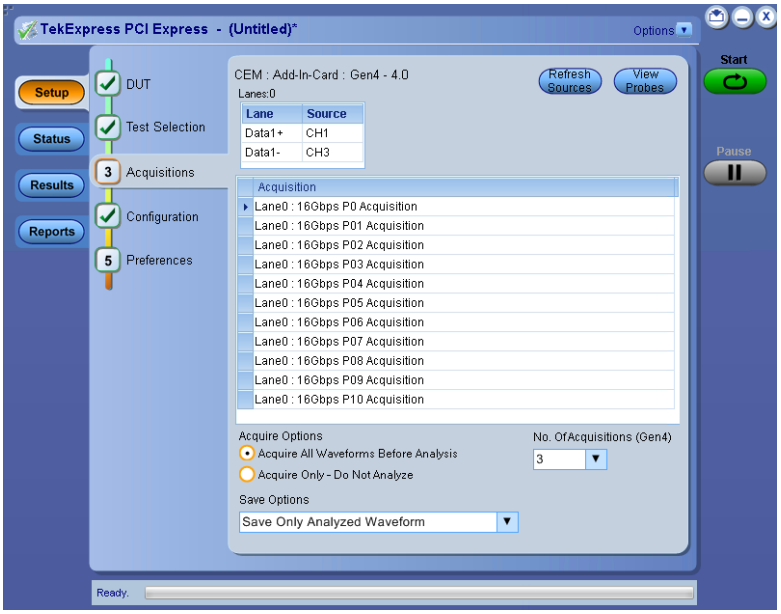


Figure 23 TekExpress PCI Express Add-In-Card Preset Test Acquisitions

7. For the Tx Preset Test for Add-In-Card in automated procedure we are using TekExpress PCI Express with automated DUT toggle option using AWG7122C. User can use AFG/AWG/GRL PCIE Controller for automated DUT toggle option. Refer the 'Appendix Section#5.3.2' for manual DUT toggle option.
8. Go to Configuration panel and select the 'Signal Source for DUT Automation' [AWG7122 in this case] and select the check box 'Automated DUT Control'.

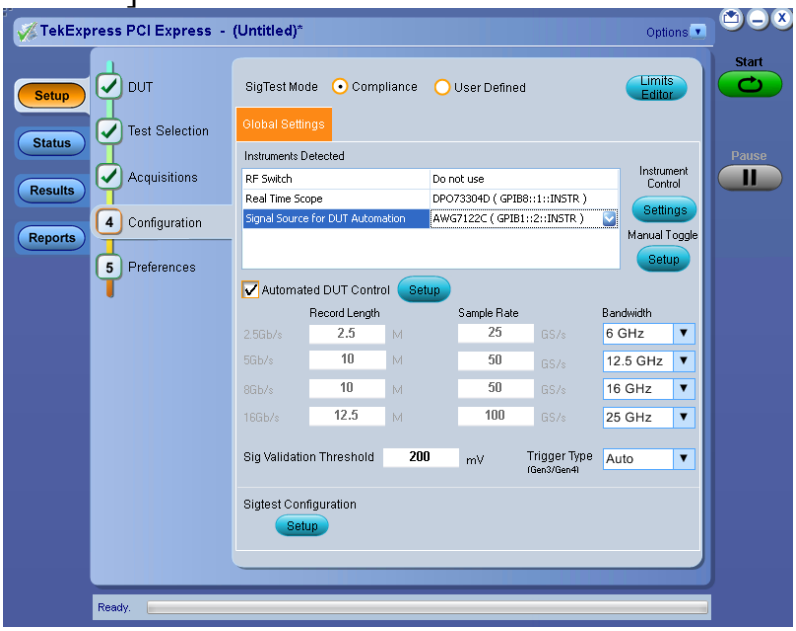


Figure 24 TekExpress PCI Express Add-In-Card Preset Test Configuration

9. Click on SigTest configuration ‘Setup’ and observe the SigTest version used for this test.

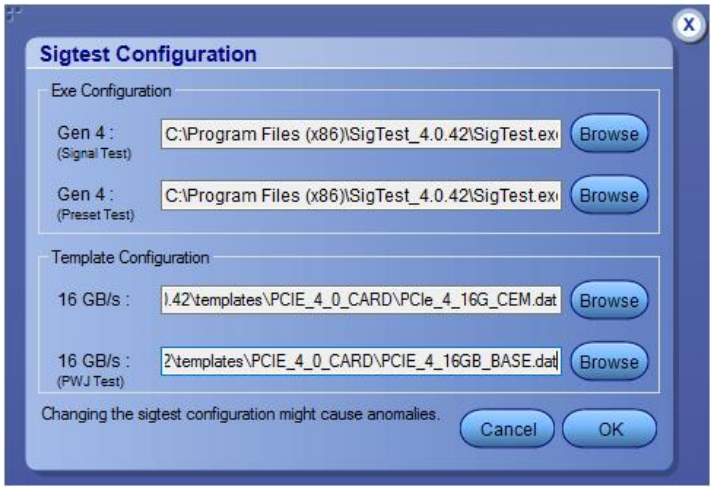


Figure 25 TekExpress PCI Express Add-In-Card Preset Test SigTest Configuration

10. Click on 

to run the test.
11. Make the connection as per section#3.6 (Figure 6 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle Automation) and verify that it as per the connection diagram that is prompted by application up during the run, Power ON the DUT and click OK to continue.
12. Observe that the DUT will be toggled automatically from Gen1 to Gen4 Preset P0 And will start the acquisition, observe that Package model is NOT embedded on the scope and the waveforms of each preset are saved.

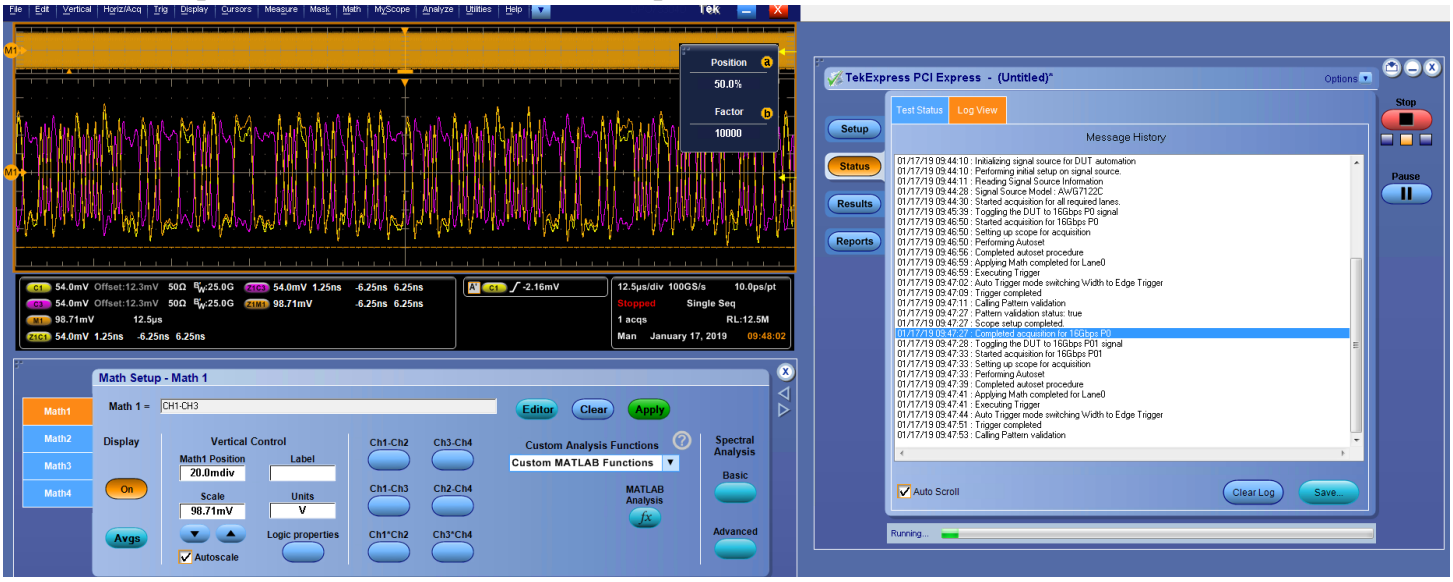


Figure 26 TekExpress PCI Express Add-In-Card Preset Test NO package model applied

13. After acquiring of all the waveforms, they will be post-processed using SigTest.

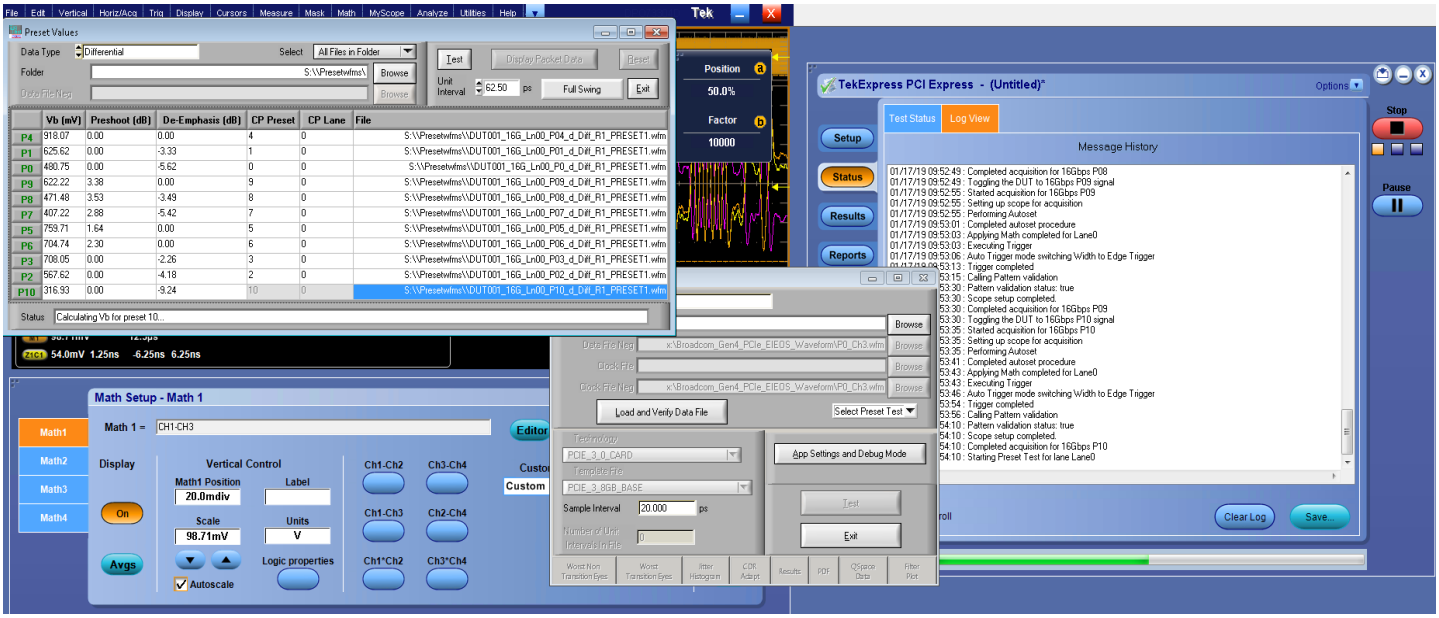


Figure 27 TekExpress PCI Express Add-In-Card Preset Test Analysis

14. Observe the test results in TekExpress Results panel and once all the results are updated a test report will be generated.

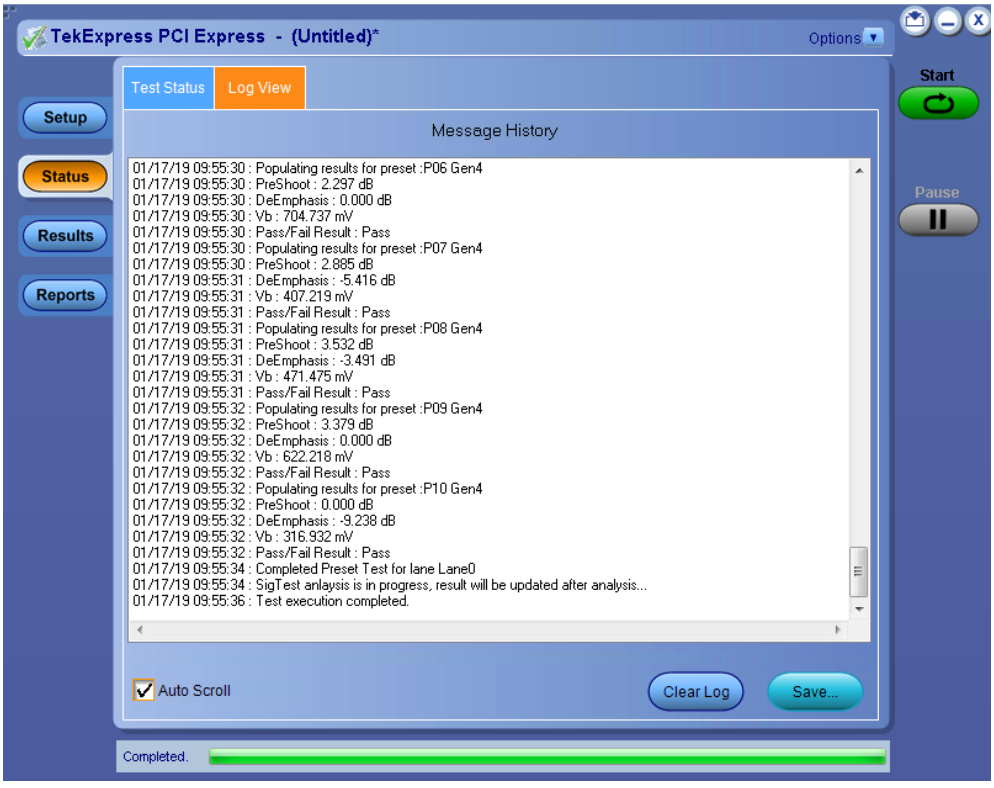


Figure 28 TekExpress PCI Express Add-In-Card Preset Test Status

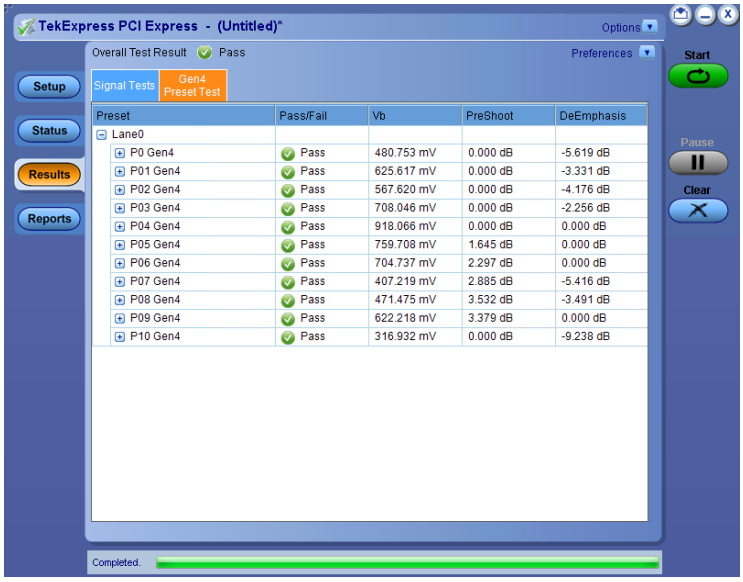


Figure 29TekExpress PCI Express Add-In-Card Preset Test Results

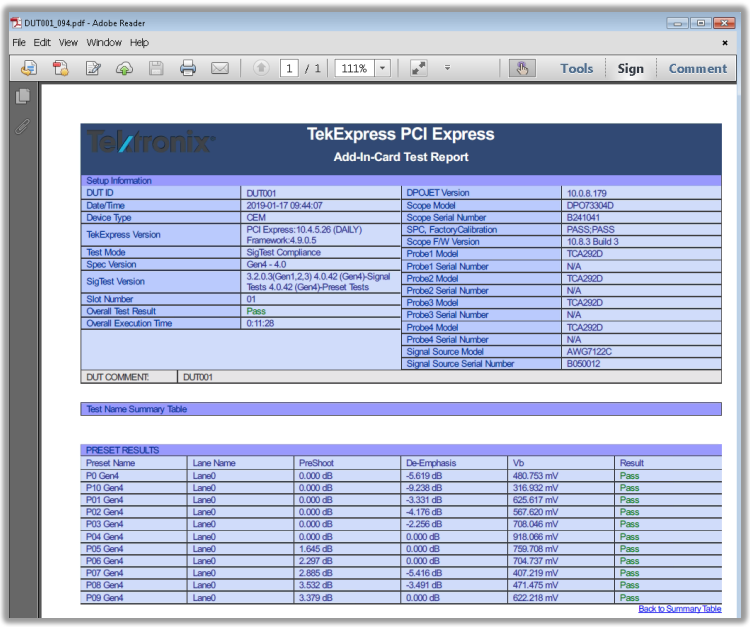


Figure 30 TekExpress PCI Express Add-In-Card Preset Test Report

15. Once test report is generated you can save the Test Session in TekExpress, Options → Save Test Setup → Tek_Gen4_AIC_Preset_MOI (Example of session name). The saved data can be found in the location X:\PCI Express\Tek_Gen4_AIC_Preset_MOI\DUT001.

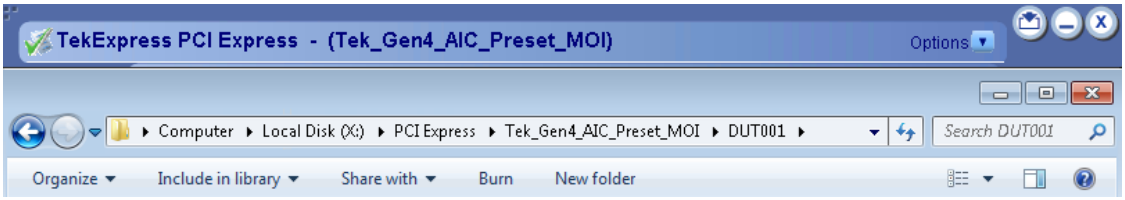


Figure 31 TekExpress PCI Express Add-In-Card Preset Test Session Saved

4.3 Add-In-Card Transmitter Pulse Width Jitter Test for 16 GT/s

This is referred as "Add-In-Card Transmitter Pulse Width Jitter Test at 16 GT/s" in *PCI Express® Architecture PHY Test Specification Revision 4.0*. This test is run on all card electromechanical form factor add-in cards that operate at 16.0 GT/s. This test verifies that the add-in card produces a Pulse Width Jitter (PWj) below the PCIe Base Specification limit.

1. Insert the Add-In Card under test into a compliance base board (CBB) 4.0 without power.
2. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
3. Launch TekExpress PCI Express Application from TekScope → Analyze menu.
4. Select the configuration in the application as per the figure below.

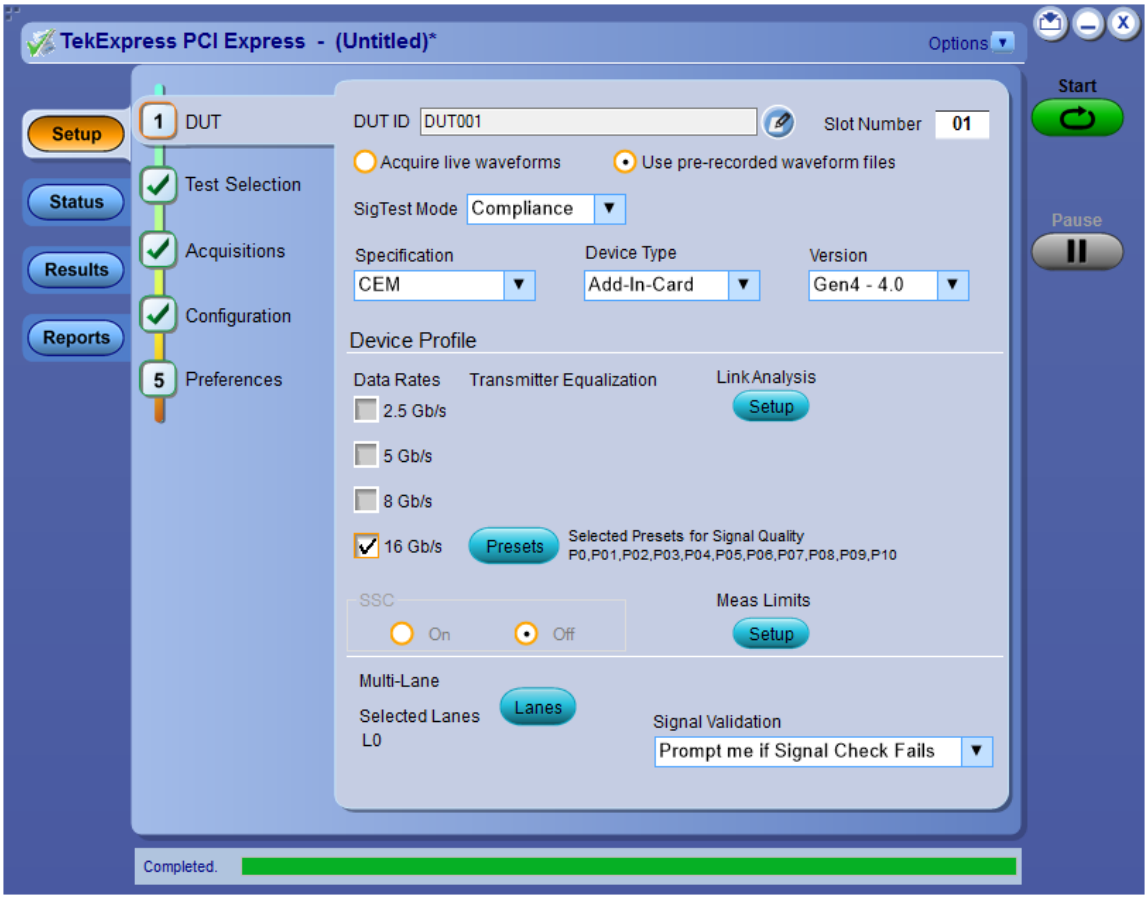


Figure 32 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test

5. Go to Test Selection panel and select Signal Test of 16Gbps, click on 'Deselect All' button which will uncheck all the tests. Now in the 16Gbps tree node select 'Uncorrelated PWJ TJ @E-12 Gen4' test.

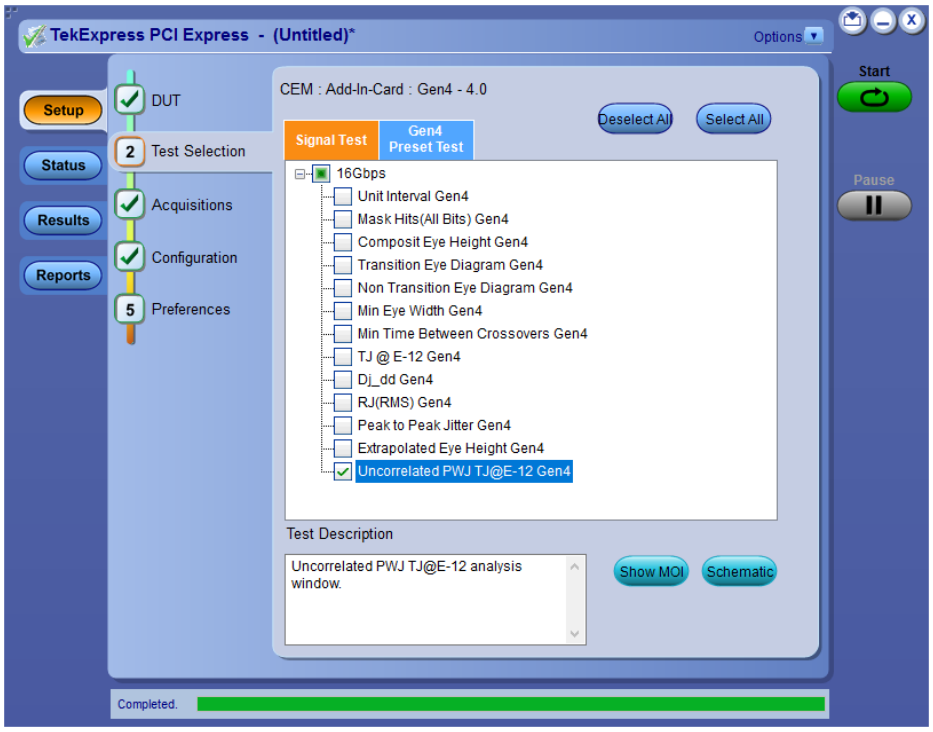


Figure 33 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Selection

6. Go to Acquisition panel and set the source of Lane0 Date+ to CH1 and Data- to CH3. Set the No of Acquisitions to '3' as we need to capture three 2.0M UI (Gen4 Compliance Pattern) differential waveforms for the data rate clock pattern.

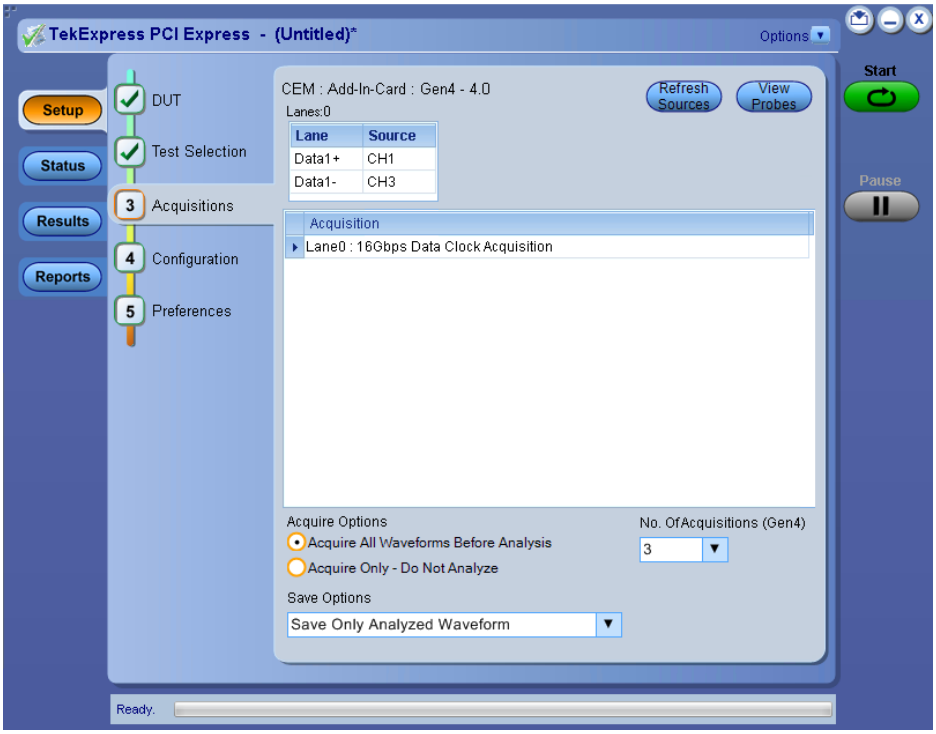


Figure 34 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Acquisitions

7. For the Tx Pulse Width Jitter Test for Add-In-Card in automated procedure we are using TekExpress PCI Express with automated DUT toggle option using AWG7122C. User can use AFG/AWG/GRL PCIE Controller for automated DUT toggle option. Refer the 'Appendix Section#5.3.3' for manual DUT toggle option.
8. Go to Configuration panel and select the 'Signal Source for DUT Automation' [AWG7122 in this case] and select the check box 'Automated DUT Control'.

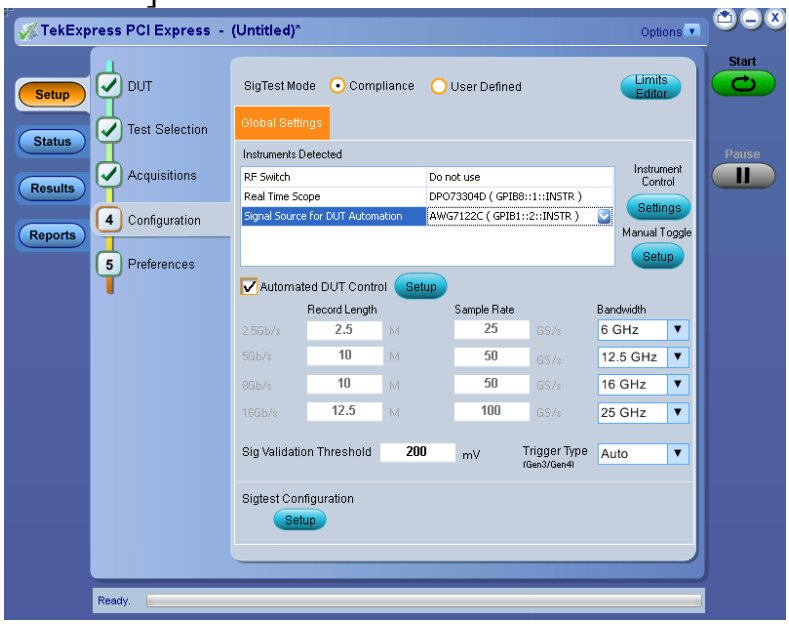


Figure 35 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Configuration

9. Click on SigTest configuration 'Setup' and observe the SigTest version and templates used for this test.

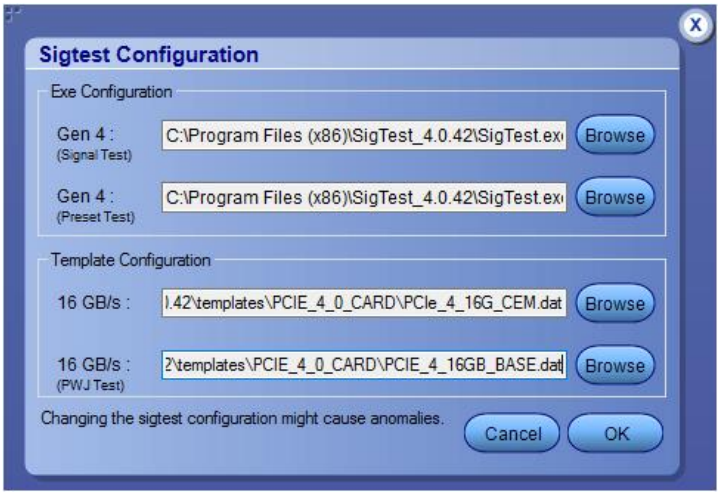


Figure 36 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test SigTest Configuration

10. Click on 

to run the test.

11. Make the connection as per section#3.6 (Figure 6 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle Automation) and verify that it as per the connection diagram that is prompted by application up during the run, Power ON the DUT and click OK to continue.
12. Observe that the DUT will be toggled automatically from Gen1 to the 16 GT/s Jitter Measurement Pattern (Lanes 0/8/16/24 – setting #27 in the 4.0 PCIe Base Specification) and will start the acquisition, observe that Package model is NOT embedded on the scope and the three waveforms of the Jitter Measurement Pattern are saved.

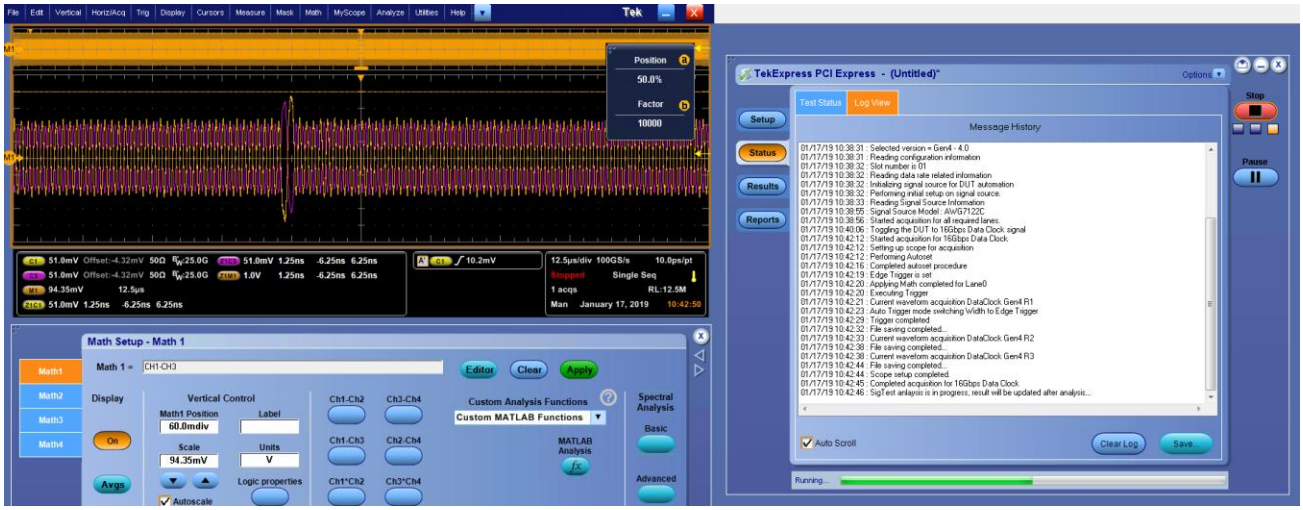


Figure 37 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test NO Package Model Applied

13. After acquiring all waveforms, they will be post-processed with SigTest. The Template File Technology Folder: PCIE_4_0_CARD and Template File Name: PCIe_4_16GB_BASE.dat

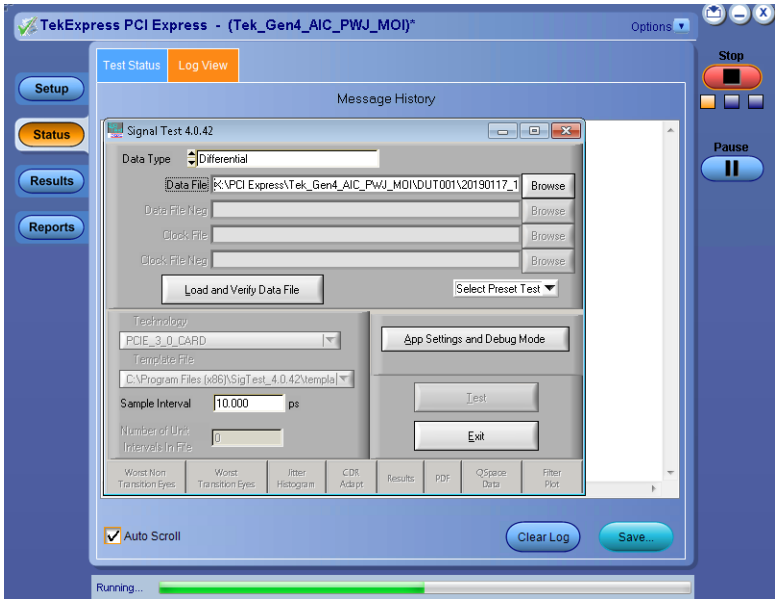


Figure 38 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test SigTest Analysis

14. Observe the test results in TekExpress Results panel and once all the results are updated a test report will be generated.

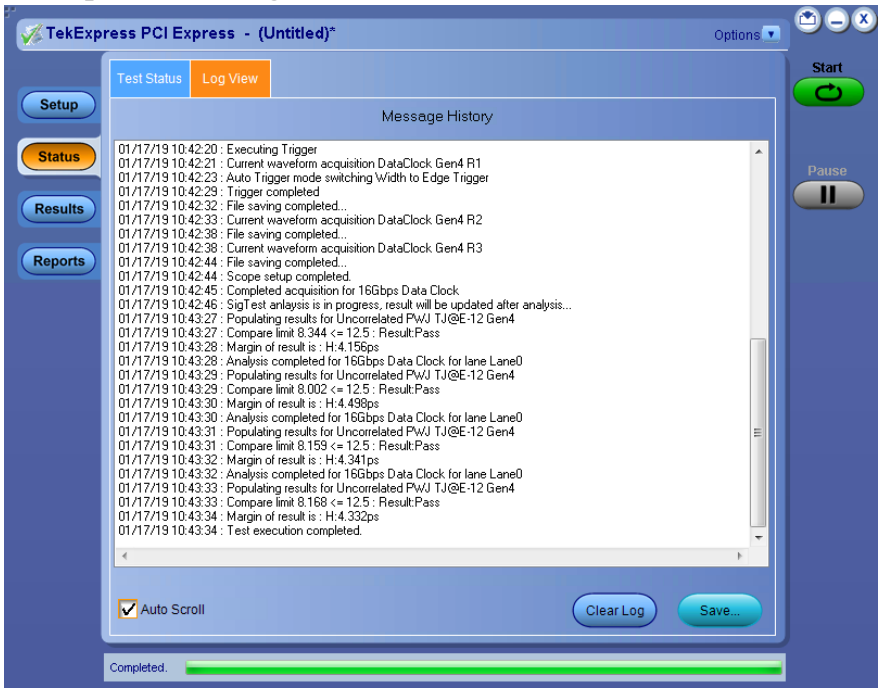


Figure 39 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Status

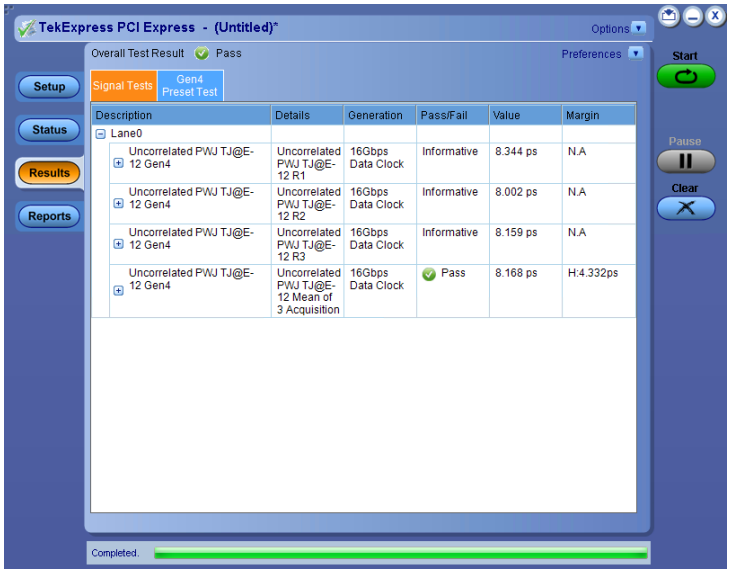


Figure 40 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Results

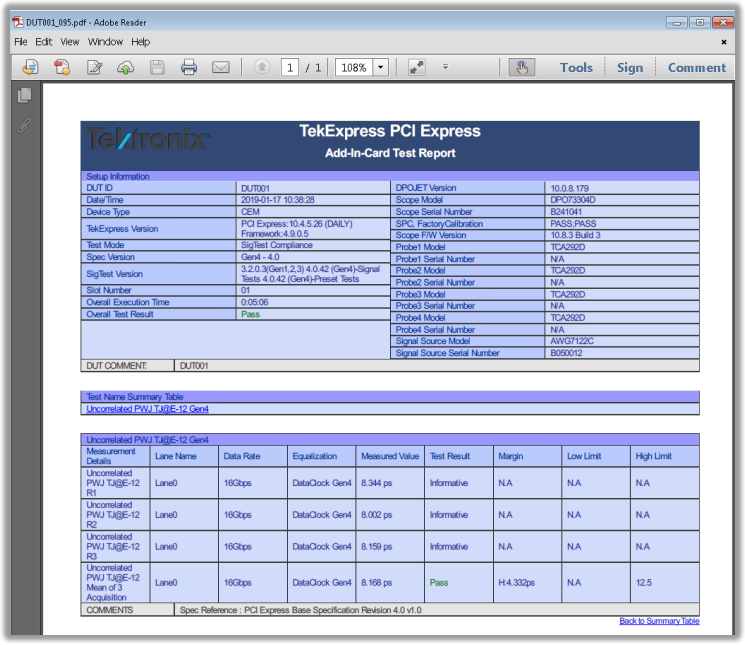


Figure 41 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Report

15. Once test report is generated you can save the Test Session in TekExpress, Options → Save Test Setup → Tek_Gen4_AIC_PWJ_MOI (Example of session name). The saved data can be found in the location X:\PCI Express\Tek_Gen4_AIC_PWJ_MOI\DUT001.

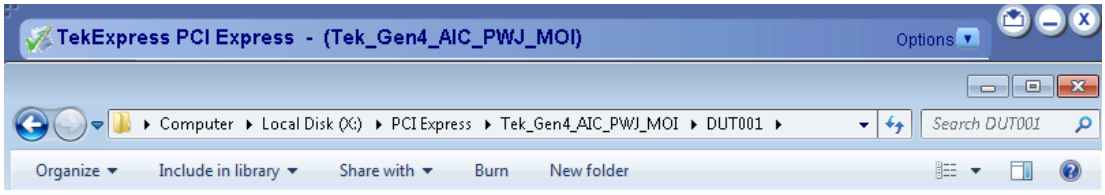


Figure 42 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Session Saved

4.4 System-Board Transmitter Signal Quality Test for 16 GT/s

This is referred as "System Board Transmitter Electrical Compliance Test for 16.0 GT/s" in *PCI Express® Architecture PHY Test Specification Revision 4.0*. This test is run on all card electromechanical form factor system boards. This test verifies the Tx signal of the system at 16 GT/s meets the minimum eye diagram requirements with at least one Tx equalization preset.

1. Power down the system under test and insert the compliance base board (CLB) 4.0 into the slot for test.
2. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
3. Launch TekExpress PCI Express Application from TekScope → Analyze menu.
4. Select the configuration in the application as per the figure below.

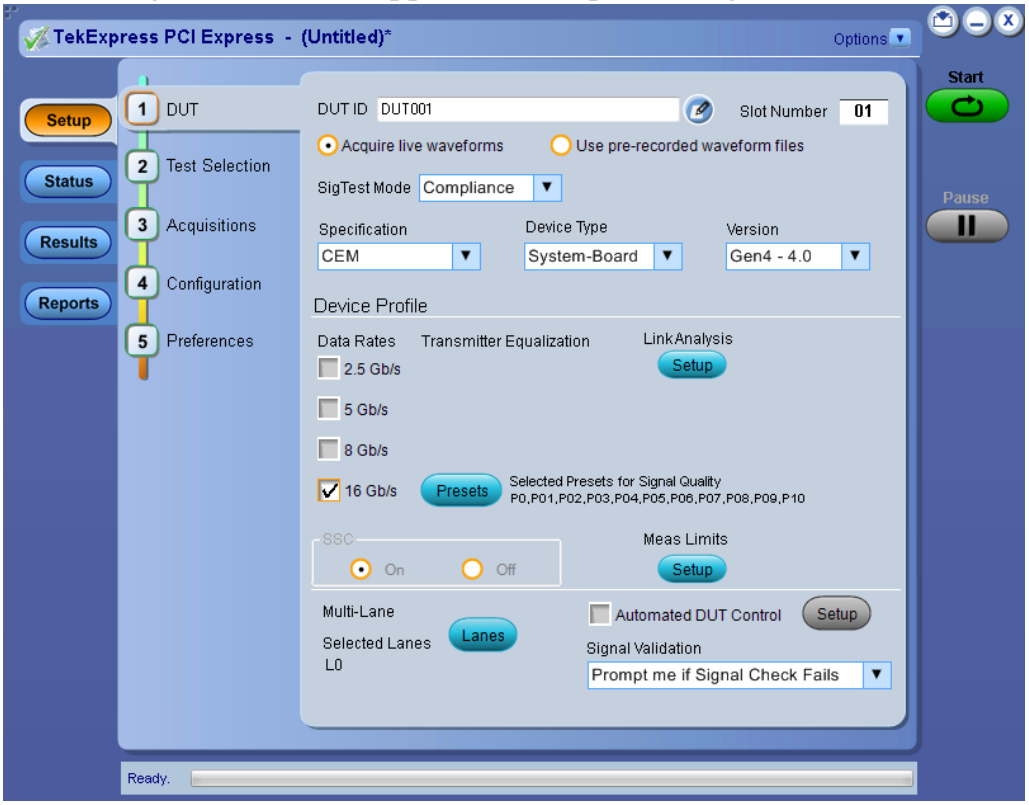


Figure 43 TekExpress PCI Express System-Board Signal Quality Test

5. Go to Test Selection panel and make sure all the tests are checked under the 16Gbps tree node in 'Signal Test'.

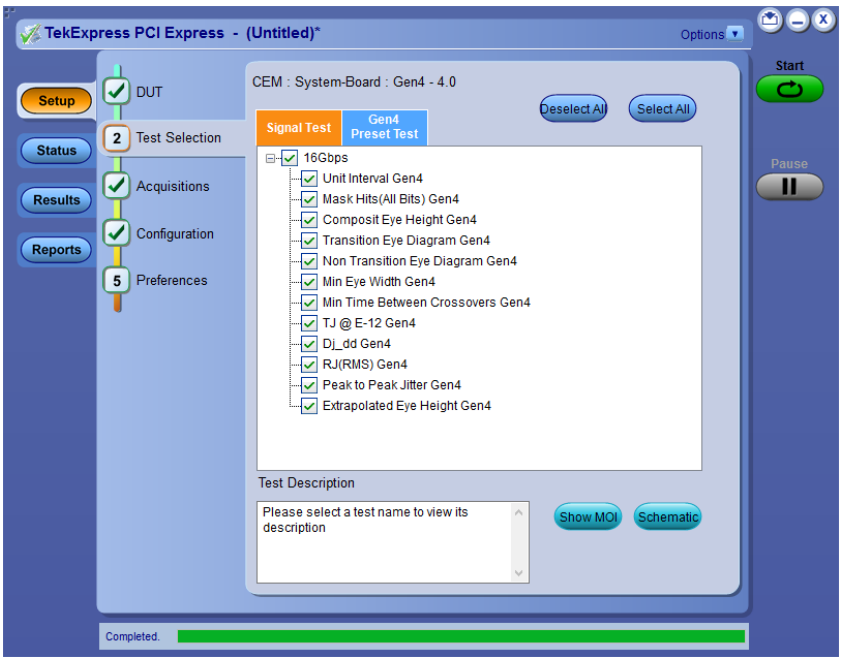


Figure 44 TekExpress PCI Express System-Board Signal Quality Test Selection

6. Go to Acquisition panel and set the source of Lane0 DATA to CH1 and CLOCK to CH3. We are using P7625 TriMode probe with tip P76CA-292C for DATA and P7313-SMA-Differential probe for CLOCK. Set the No of Acquisitions to '3' as we need to capture three 2.0M UI (Gen4 Compliance Pattern) differential waveforms for every Tx EQ Preset.

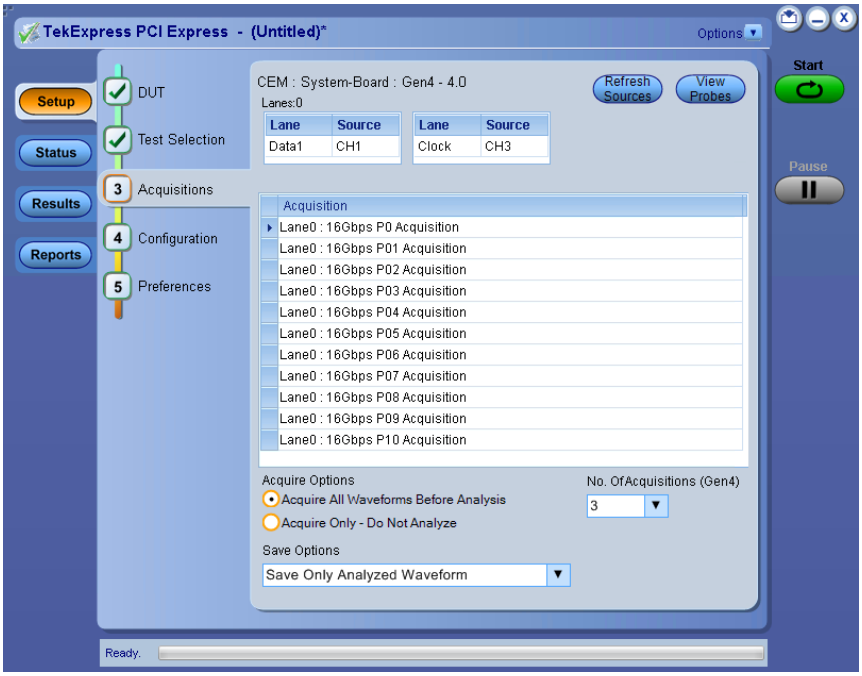


Figure 45 TekExpress PCI Express System-Board Signal Quality Test Acquisitions

7. For the Tx Signal Quality Test for System-Board in automated procedure we are using TekExpress PCI Express with automated DUT toggle option using AWG7122C. User can use AFG/AWG/GRL PCIE Controller for automated DUT toggle option. Refer the 'Appendix Section#5.3.4' for manual DUT toggle option.
8. Go to Configuration panel and select the 'Signal Source for DUT Automation' [AWG7122 in this case] and select the check box 'Automated DUT Control'.

Figure 46 TekExpress PCI Express System-Board Signal Quality Test Configuration

9. Click on SigTest configuration 'Setup' and observe the SigTest version and templates used for this test.

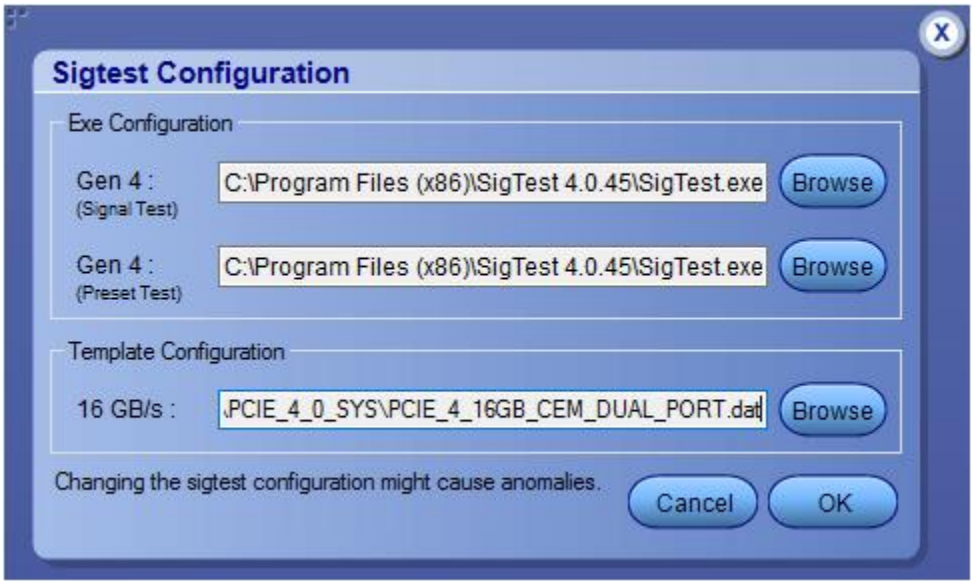


Figure 47 TekExpress PCI Express System-Board Signal Quality Test SigTest Configuration

10. Click on 

to run the test.
11. Make the connection as per section#3.7 (Figure 7 Signal Quality Test for System-Board – DUT Toggle Automation) and verify that it as per the connection diagram that is prompted by application up during the run, Power ON the DUT and click OK to continue.

12. Observe that the DUT will be toggled automatically from Gen1 to Gen4 Preset P0 And will start acquisition, observe that Package model embedded on the scope (refpkg_endpoint_3db_thru.s4p) gets applied and three waveforms of each preset are saved.

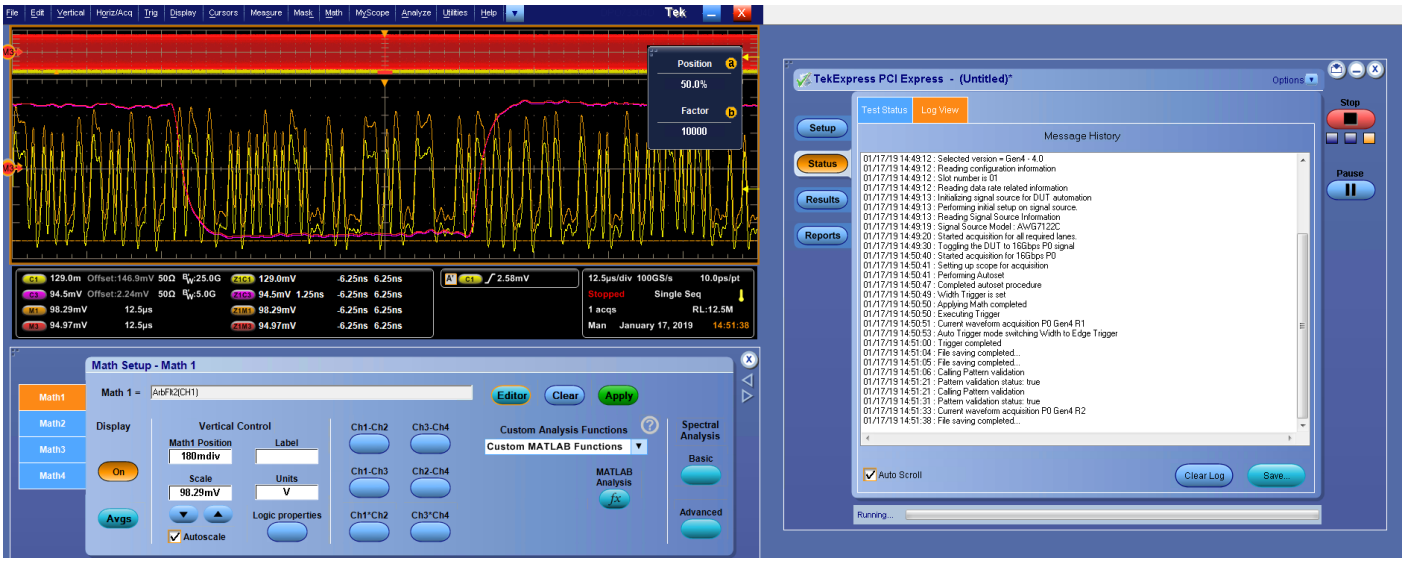


Figure 48 TekExpress PCI Express System-Board Signal Quality Test applying package model

13. All acquired waveforms will be processed with SigTest using the "PCIE_4_16GB_CEM_DUAL_PORT.dat" template file which performs CTLE optimization. If all Tx EQ presets fail with this approach, you can configure the SigTest Setup (step #9) to run each CTLE individually using the "PCIE_4_16GB_CEM_DUAL_PORT_CTLE_6dB.dat through PCIE_4_16GB_CEM_DUAL_PORT_CTLE_12dB.dat" template files. A passing result with either case is allowed per the PCI Express Architecture PHY Test specification.

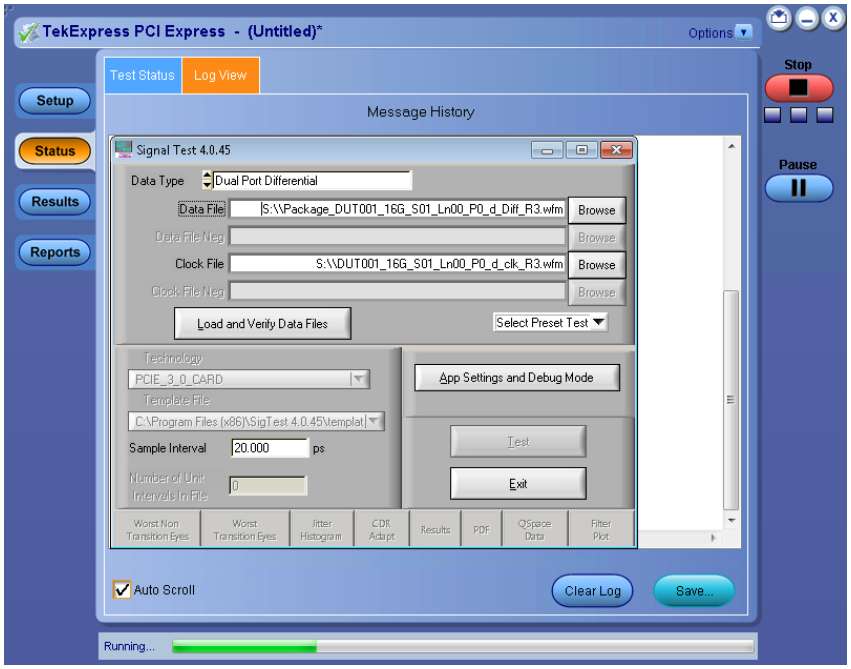


Figure 49 TekExpress PCI Express System-Board Signal Quality Test SigTest Analysis

14. Observe the test results in TekExpress Results panel and once all the results are updated a test report will be generated.

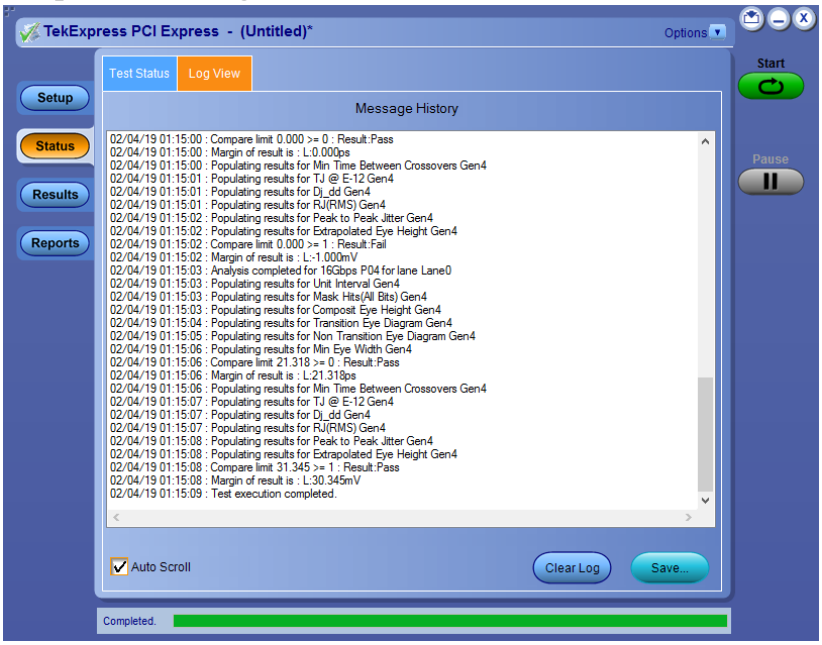


Figure 50 TekExpress PCI Express System-Board Signal Quality Test Status

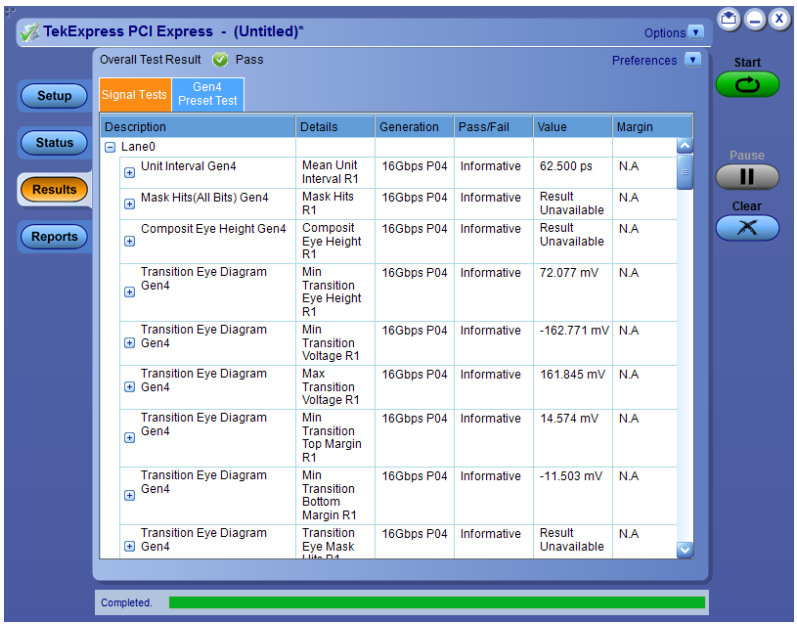


Figure 51 TekExpress PCI Express System-Board Signal Quality Test Results

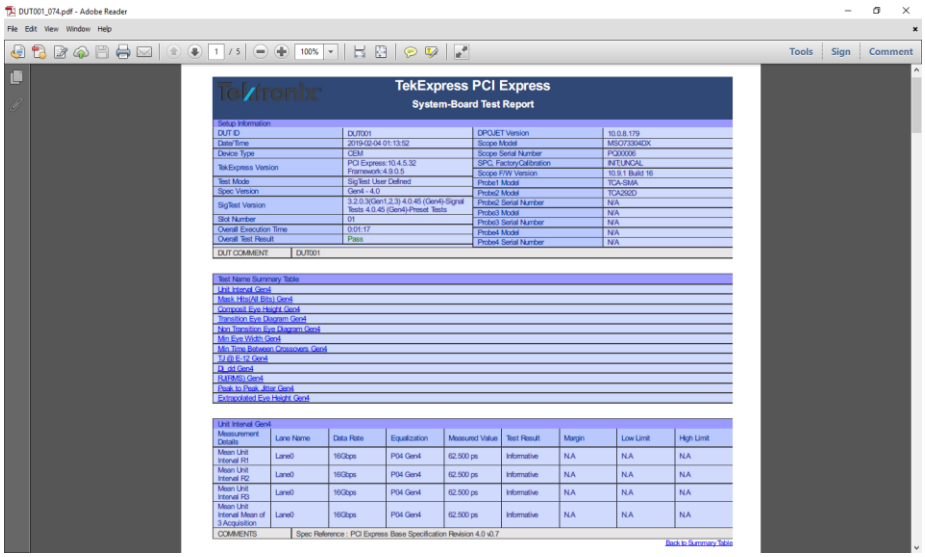


Figure 52 TekExpress PCI Express System-Board Signal Quality Test Report

15. Once test report is generated you can save the Test Session in TekExpress, Options → Save Test Setup → Tek_Gen4_SYS_SQ_MOI (Example of session name). The saved data can be found in the location X:\PCI Express\Tek_Gen4_SYS_SQ_MOI\DUT001.

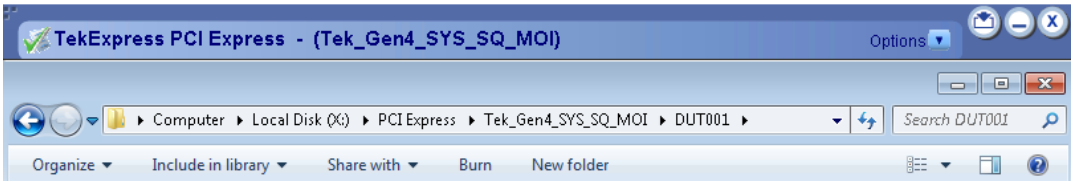


Figure 53 TekExpress PCI Express System-Board Signal Quality Test Session Saved

4.5 System-Board Transmitter Preset Test for 16 GT/s

This is referred as “System Board Transmitter Preset Test for 16.0 GT/s” in *PCI Express® Architecture PHY Test Specification Revision 4.0*. This test is run on all card electromechanical form factor system boards that operate at 16.0 GT/s. The test verifies that the system board produces the correct transmitter equalization values for each preset in the set of 11 presets.

1. Power down the system under test and insert the compliance base board (CLB) 4.0 into the slot for test.
2. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
3. Launch TekExpress PCI Express Application from TekScope → Analyze menu.
4. Select the configuration in the application as per the figure below.

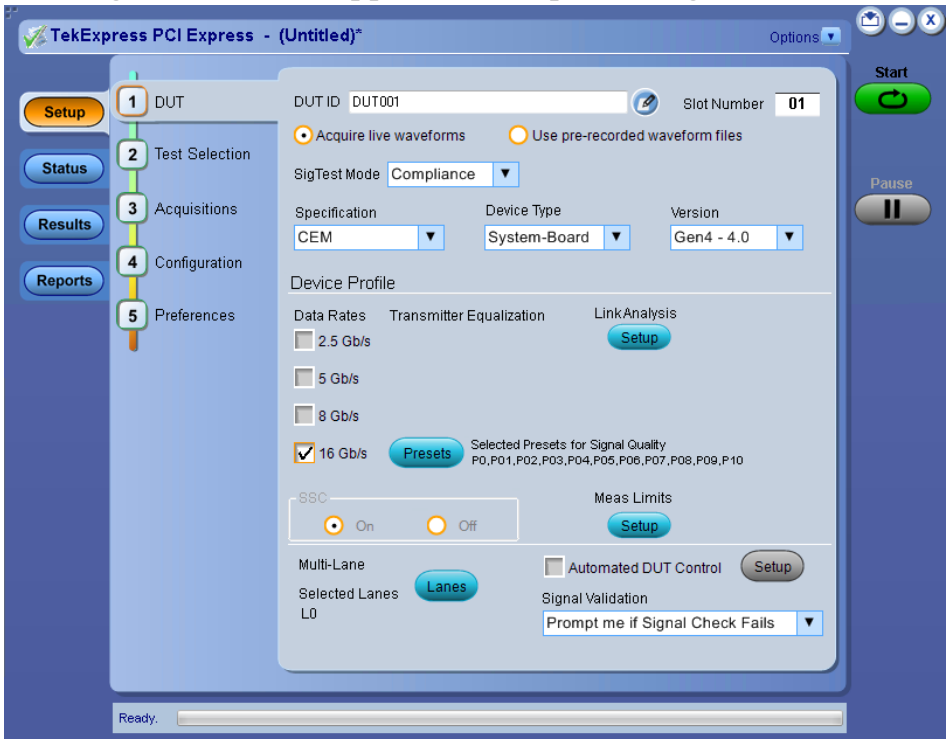


Figure 54 TekExpress PCI Express System-Board Preset Test

5. Go to Test Selection panel and make sure all the tests are un-checked under 16Gbps tree node in ‘Signal Test’ tab by clicking on ‘Deselect All’ button. Go to ‘Gen4 Preset Test’ tab and click on ‘Select All’ button.

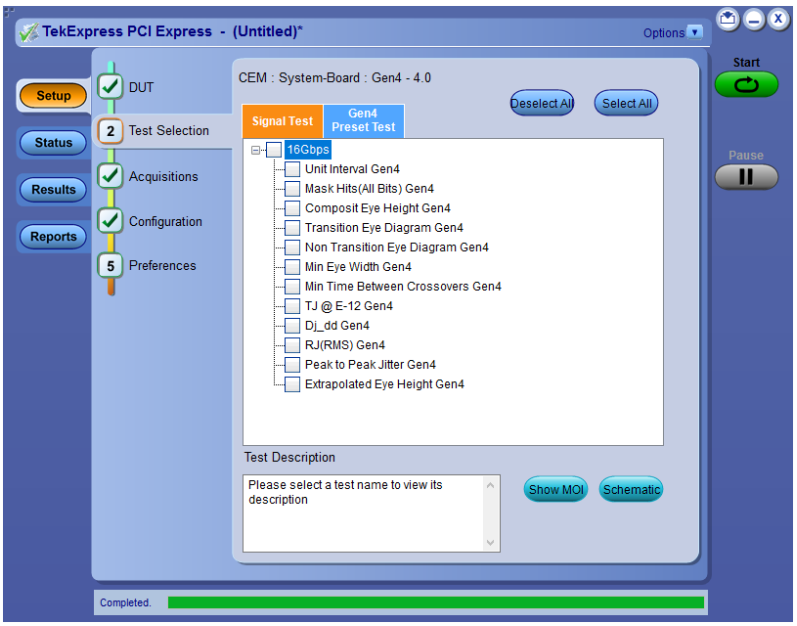


Figure 55 TekExpress PCI Express System-Board Preset Test Selection 1

Figure 56 TekExpress PCI Express System-Board Preset Test Selection 2

6. Go to Acquisition panel and set the source of Lane0 DATA to CH1 and CLOCK to CH3. We are using P7625 TriMode probe with tip P76CA-292C for DATA and P7313-SMA-Differential probe for CLOCK, to capture 2.0M UI (Gen4 Compliance Pattern) differential waveforms for every Tx EQ Preset.

   Note: We will not capture and save the CLOCK signal for this test, but the physical connection to the scope is required.

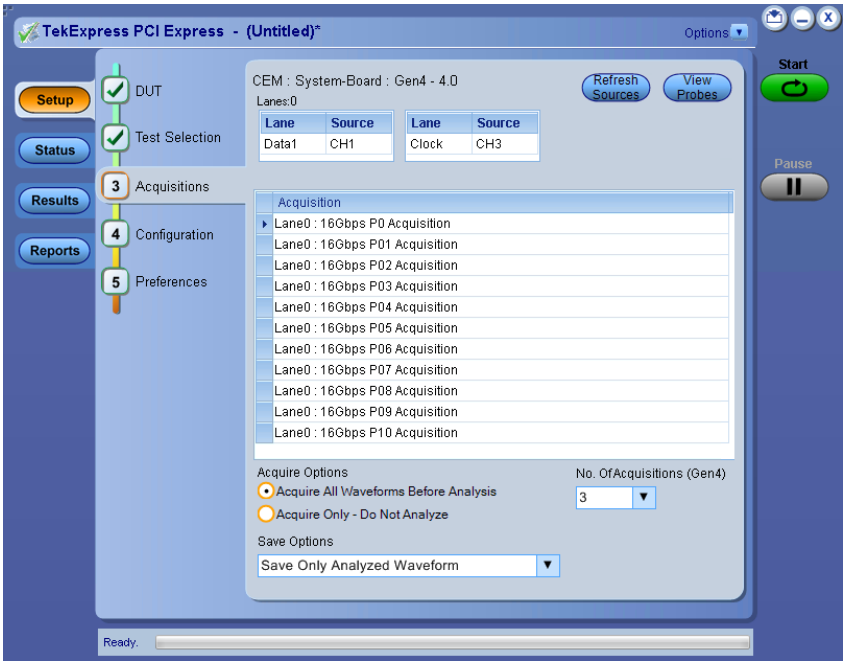


Figure 57 TekExpress PCI Express System-Board Preset Test Acquisitions

7. For the Tx Preset Test for System-Board in automated procedure we are using TekExpress PCI Express with automated DUT toggle option using AWG7122C. User can use AFG/AWG/GRL PCIE Controller for automated DUT toggle option. Refer the ‘Appendix Section#5.3.5’ for manual DUT toggle option.

8. Go to Configuration panel and select the ‘Signal Source for DUT Automation’ [AWG7122 in this case] and select the check box ‘Automated DUT Control’.

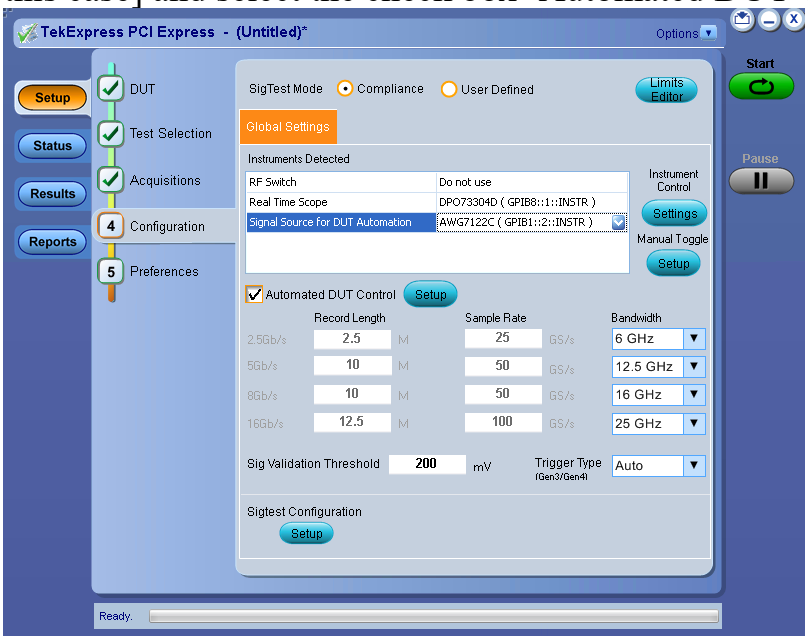


Figure 58 TekExpress PCI Express System-Board Preset Test Configuration

9. Click on SigTest configuration ‘Setup’ and observe the SigTest version used for this test.

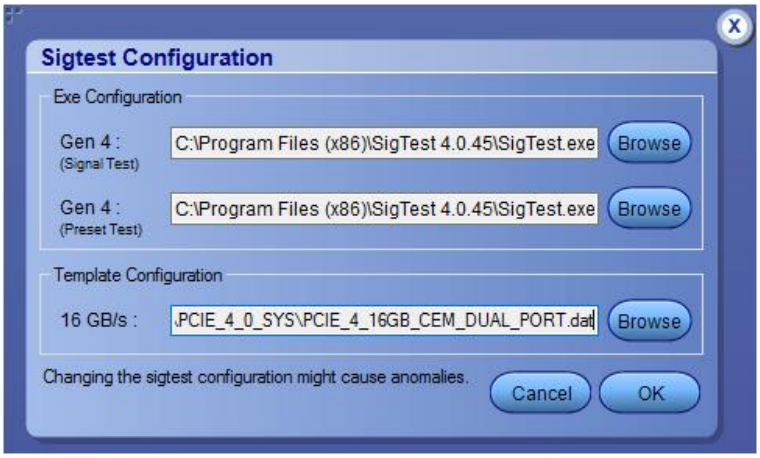


Figure 59 TekExpress PCI Express System-Board Preset Test SigTest Configuration

10. Click on 

to run the test.
11. Make the connection as per section#3.8 (Figure 8 Tx Preset Test for System-Board – DUT Toggle Automation) and verify that it as per the connection diagram that is prompted by application up during the run, Power ON the DUT and click OK to continue
12. Observe that the DUT will be toggled automatically from Gen1 to Gen4 Preset P0
    And will start acquisition, observe that Package model embedded on the scope (refpkg_endpoint_3db_thru.s4p) is not applied and waveform of each preset is saved.

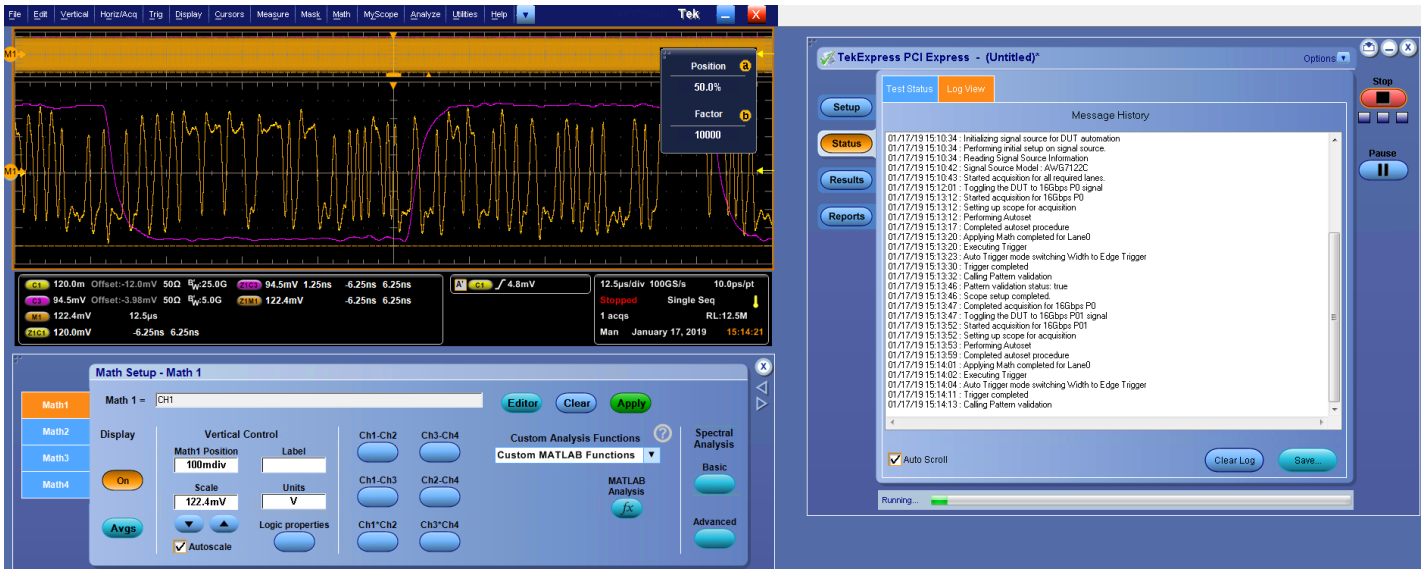


Figure 60 TekExpress PCI Express System-Board Preset Test NO Package Model applied

13. After acquiring the waveforms will be post-processed with SigTest.

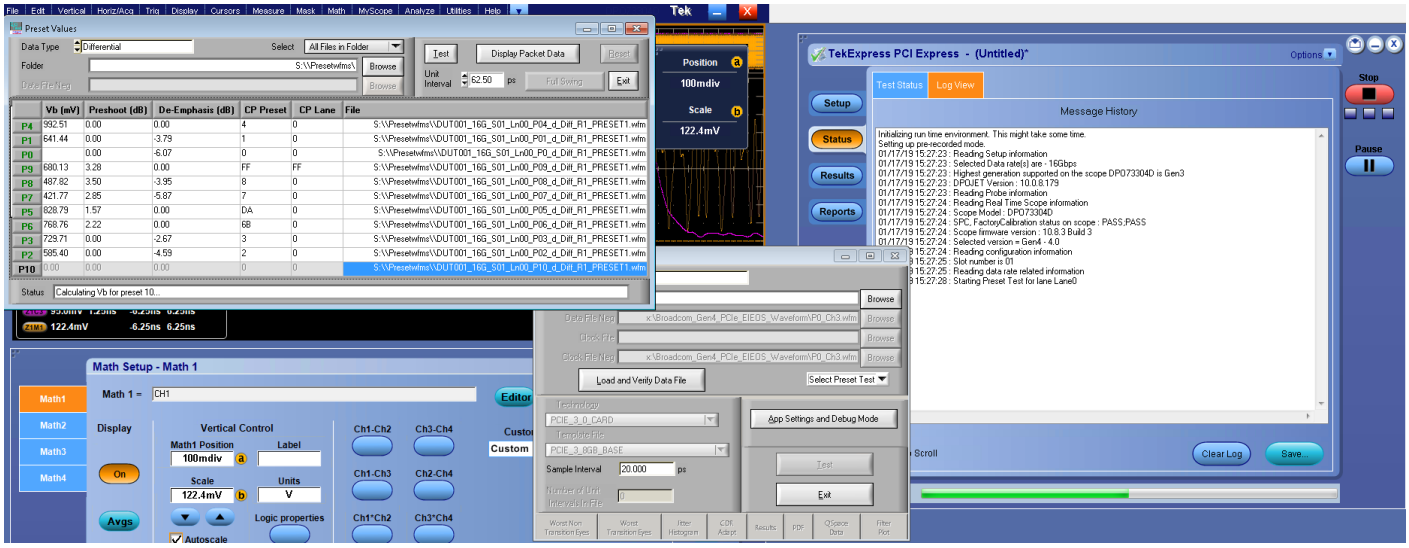


Figure 61 TekExpress PCI Express System-Board Preset Test SigTest Analysis

14. Observe the test results in TekExpress Results panel and once all the results are updated a test report will be generated.

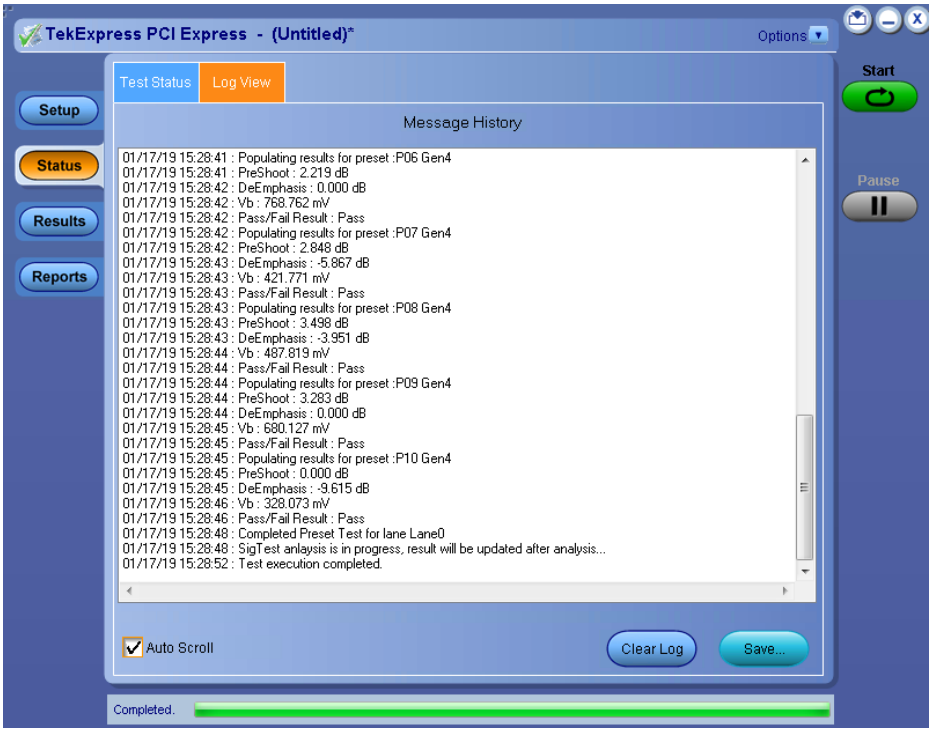
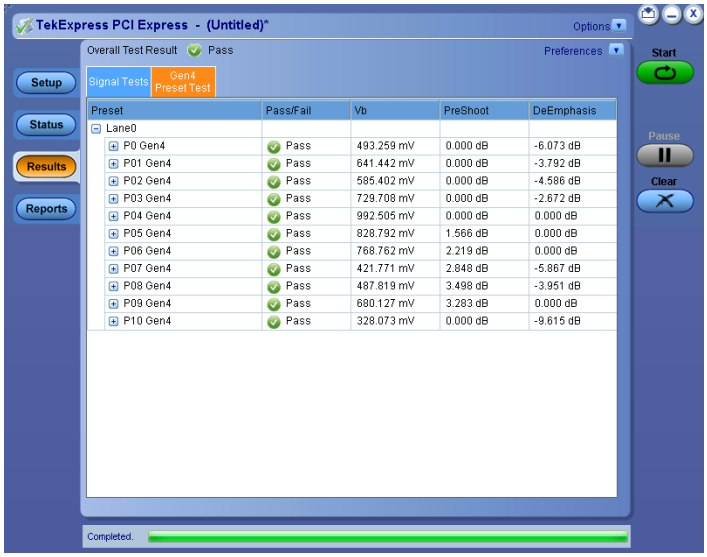
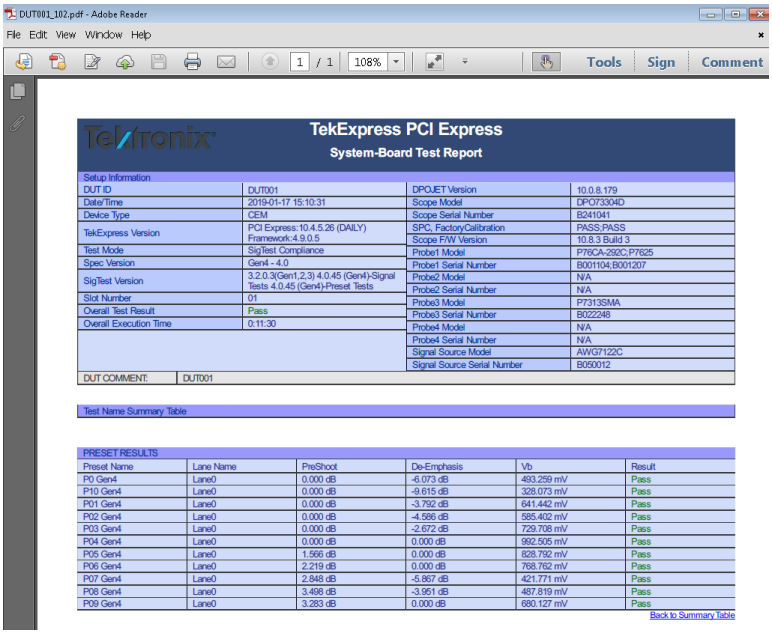


Figure 62 TekExpress PCI Express System-Board Preset Test Status



Preset	Pass/Fail	Vb	PreShoot	DeEmphasis
Lane0				
P0 Gen4	Pass	493.259 mV	0.000 dB	-6.073 dB
P01 Gen4	Pass	641.442 mV	0.000 dB	-3.792 dB
P02 Gen4	Pass	585.402 mV	0.000 dB	-4.586 dB
P03 Gen4	Pass	729.708 mV	0.000 dB	-2.672 dB
P04 Gen4	Pass	992.505 mV	0.000 dB	0.000 dB
P05 Gen4	Pass	828.792 mV	1.566 dB	0.000 dB
P06 Gen4	Pass	768.762 mV	2.219 dB	0.000 dB
P07 Gen4	Pass	421.771 mV	2.848 dB	-5.867 dB
P08 Gen4	Pass	487.819 mV	3.498 dB	-3.951 dB
P09 Gen4	Pass	680.127 mV	3.283 dB	0.000 dB
P10 Gen4	Pass	328.073 mV	0.000 dB	-9.615 dB

Figure 63 TekExpress PCI Express System-Board Preset Test Results



Setup Information			
DUT ID	DUT001	DPOJET Version	10.0.8.179
Date/Time	2019-01-17 15:10:31	Scope Model	DPO73304D
Device Type	CEM	Scope Serial Number	B241041
TekExpress Version	PCI Express:10.4.5.26 (DAILY) Framework:4.9.0.5	SPC, FactoryCalibration	PASS;PASS
		Scope F/W Version	10.8.3 Build 3
Test Mode	SigTest Compliance	Probe1 Model	P76CA-292C;P7625
Spec Version	Gen4 - 4.0	Probe1 Serial Number	B001104;B001207
SigTest Version	3.2.0.3(Gen1,2,3) 4.0.45 (Gen4)-Signal Tests 4.0.45 (Gen4)-Preset Tests	Probe2 Model	N/A
		Probe2 Serial Number	N/A
Slot Number	01	Probe3 Model	P7313SMA
Overall Test Result	Pass	Probe3 Serial Number	B022248
Overall Execution Time	0.11:30	Probe4 Model	N/A
		Probe4 Serial Number	N/A
		Signal Source Model	AWG7122C
		Signal Source Serial Number	B050012
DUT COMMENT:	DUT001		

Test Name Summary Table

PRESET RESULTS

Preset Name	Lane Name	PreShoot	De-Emphasis	Vb	Result
P0 Gen4	Lane0	0.000 dB	-6.073 dB	493.259 mV	Pass
P10 Gen4	Lane0	0.000 dB	-9.615 dB	328.073 mV	Pass
P01 Gen4	Lane0	0.000 dB	-3.792 dB	641.442 mV	Pass
P02 Gen4	Lane0	0.000 dB	-4.586 dB	585.402 mV	Pass
P03 Gen4	Lane0	0.000 dB	-2.672 dB	729.708 mV	Pass
P04 Gen4	Lane0	0.000 dB	0.000 dB	992.505 mV	Pass
P05 Gen4	Lane0	1.566 dB	0.000 dB	828.792 mV	Pass
P06 Gen4	Lane0	2.219 dB	0.000 dB	768.762 mV	Pass
P07 Gen4	Lane0	2.848 dB	-5.867 dB	421.771 mV	Pass
P08 Gen4	Lane0	3.498 dB	-3.951 dB	487.819 mV	Pass
P09 Gen4	Lane0	3.283 dB	0.000 dB	680.127 mV	Pass

Back to Summary Table

Figure 64 TekExpress PCI Express System-Board Preset Test Report

15. Once test report is generated you can save the Test Session in TekExpress, Options → Save Test Setup → Tek_Gen4_SYS_Preset_MOI (Example of session name). The saved data can be found in the location X:\PCI Express\Tek_Gen4_SYS_Preset_MOI\DUT001.

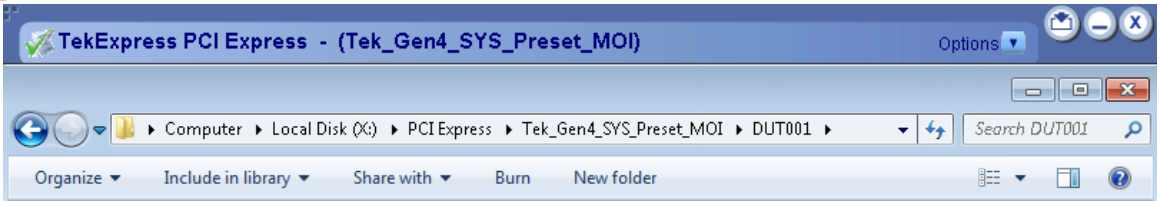


Figure 65 TekExpress PCI Express System-Board Preset Test Session Saved

5. Appendix

5.1 Channel Loss

All loss values are nominal differential insertions loss and actual loss values may vary with different cables, connectors, and board-to-board variation.

5.1.1 Channel Loss for Tx Signal Quality Test Add-In-Card

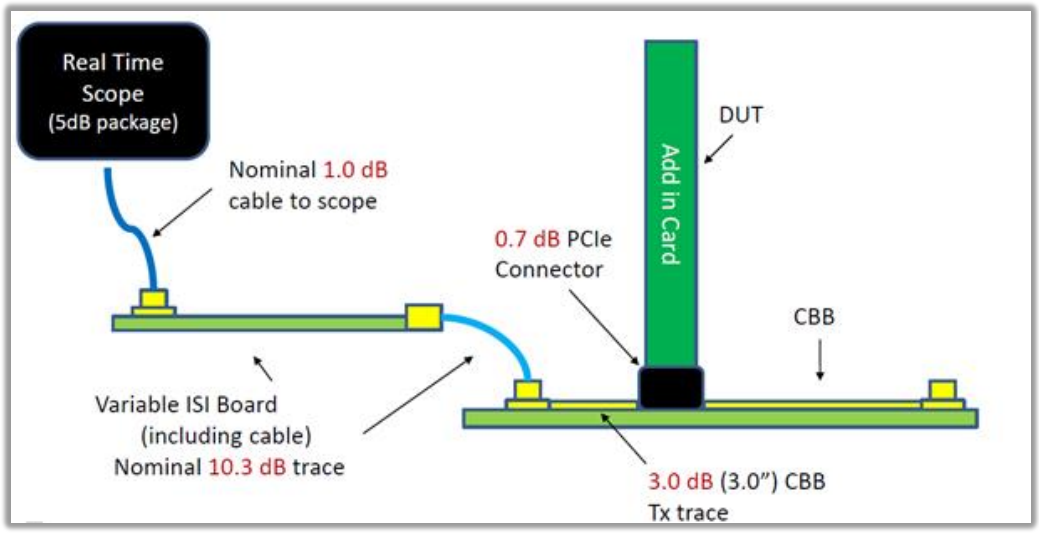


Figure 66 Channel Loss for Tx Signal Quality Test Add-In-Card

5.1.2 Channel Loss for Tx Preset Test Add-In-Card

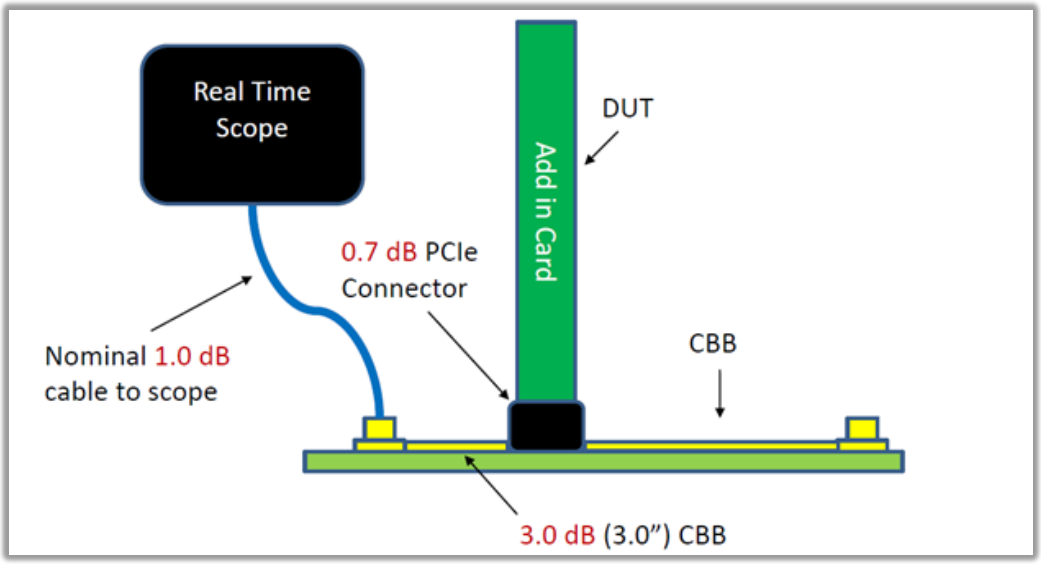


Figure 67 Channel Loss for Tx Preset Test Add-In-Card

5.1.3 Channel Loss for Tx Pulse Width Jitter Test Add-In-Card

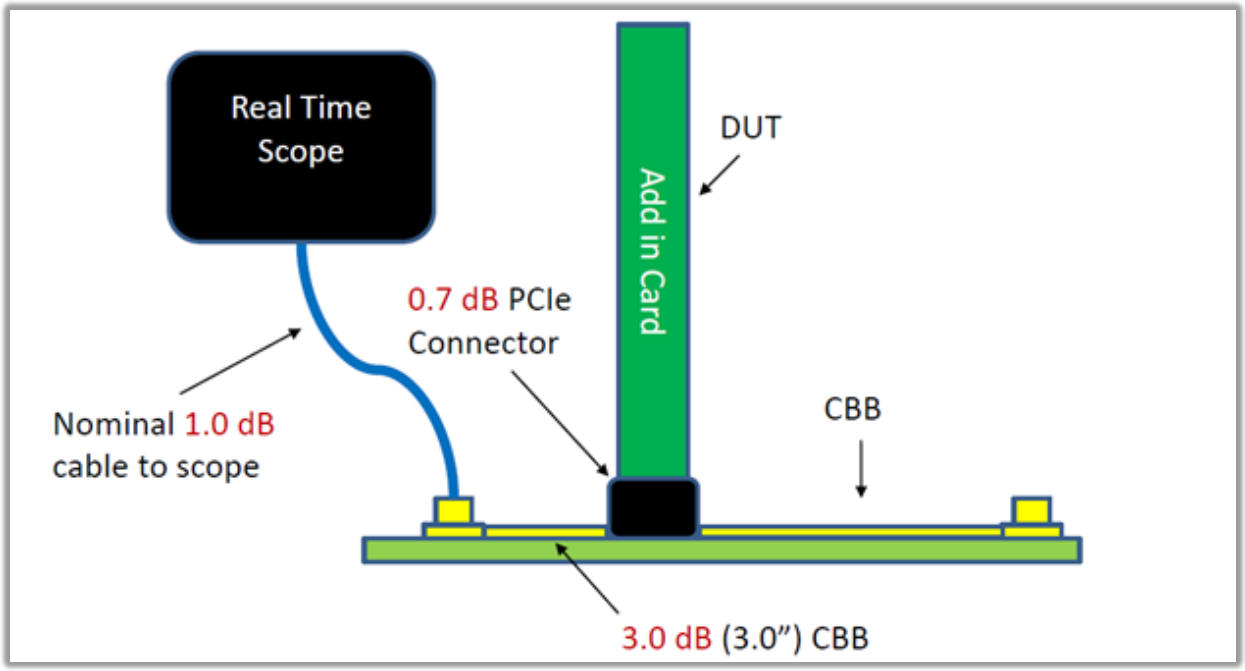


Figure 68 Channel Loss for Tx Pulse Width Jitter Test Add-In-Card

5.1.4 Channel Loss for Tx Signal Quality Test System-Board

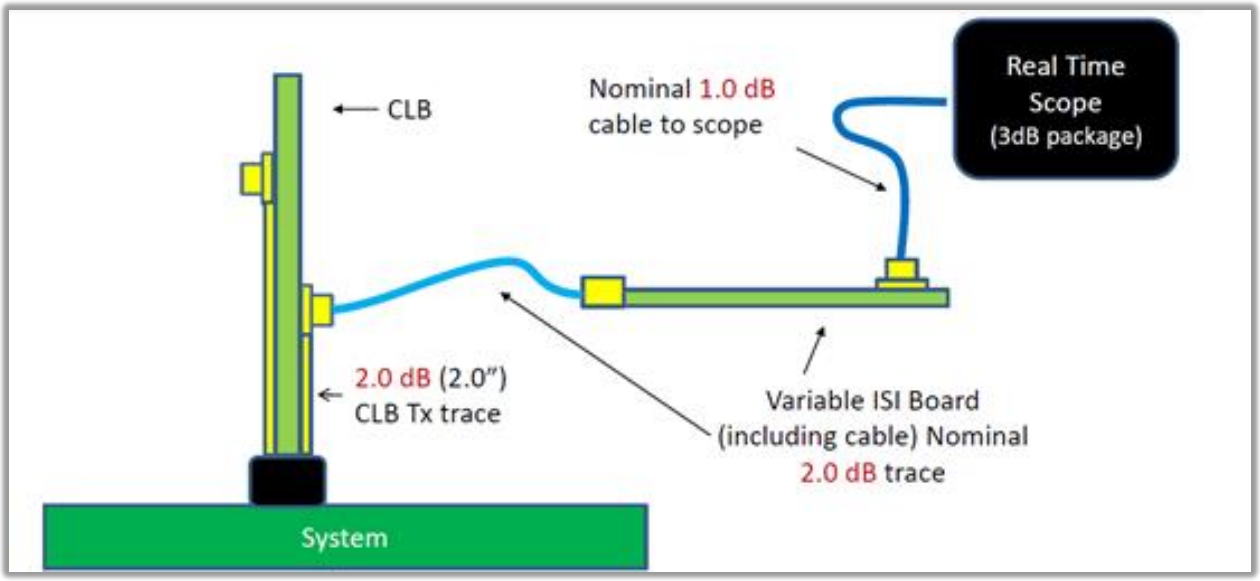


Figure 69 Channel Loss for Tx Signal Quality Test System-Board

5.1.5 Channel Loss for Tx Preset Test System-Board

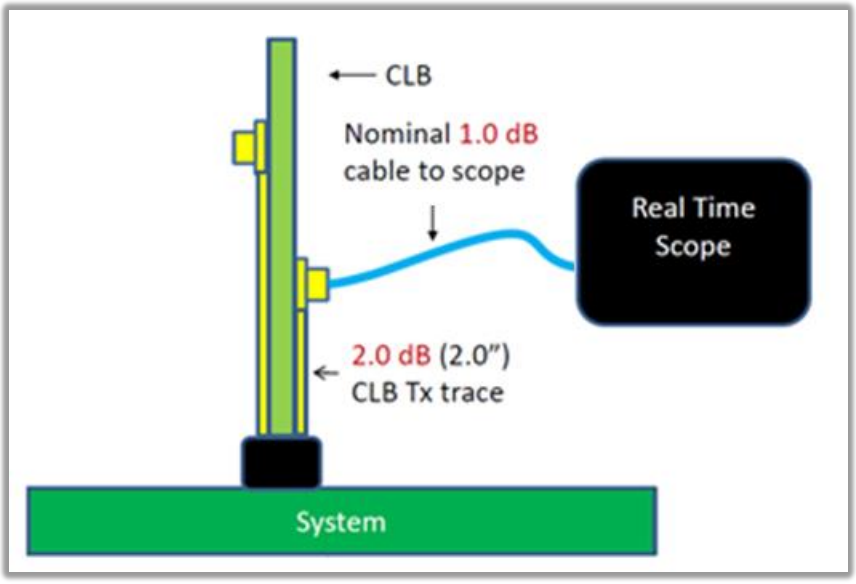


Figure 70 Channel Loss for Tx Preset Test System-Board

5.2 Fixture Characterization Preliminary

This document talks about Gen4 Fixture Characterization with measurement setups for Add-In-Card and System-Board.

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harcterization_Prelimir

5.3 DUT Toggle using Manual Mode

Ensure that in TekExpress PCI Express application you select ‘Do not use’ as ‘signal source for toggle’ in the configuration panel as show in the figure below.

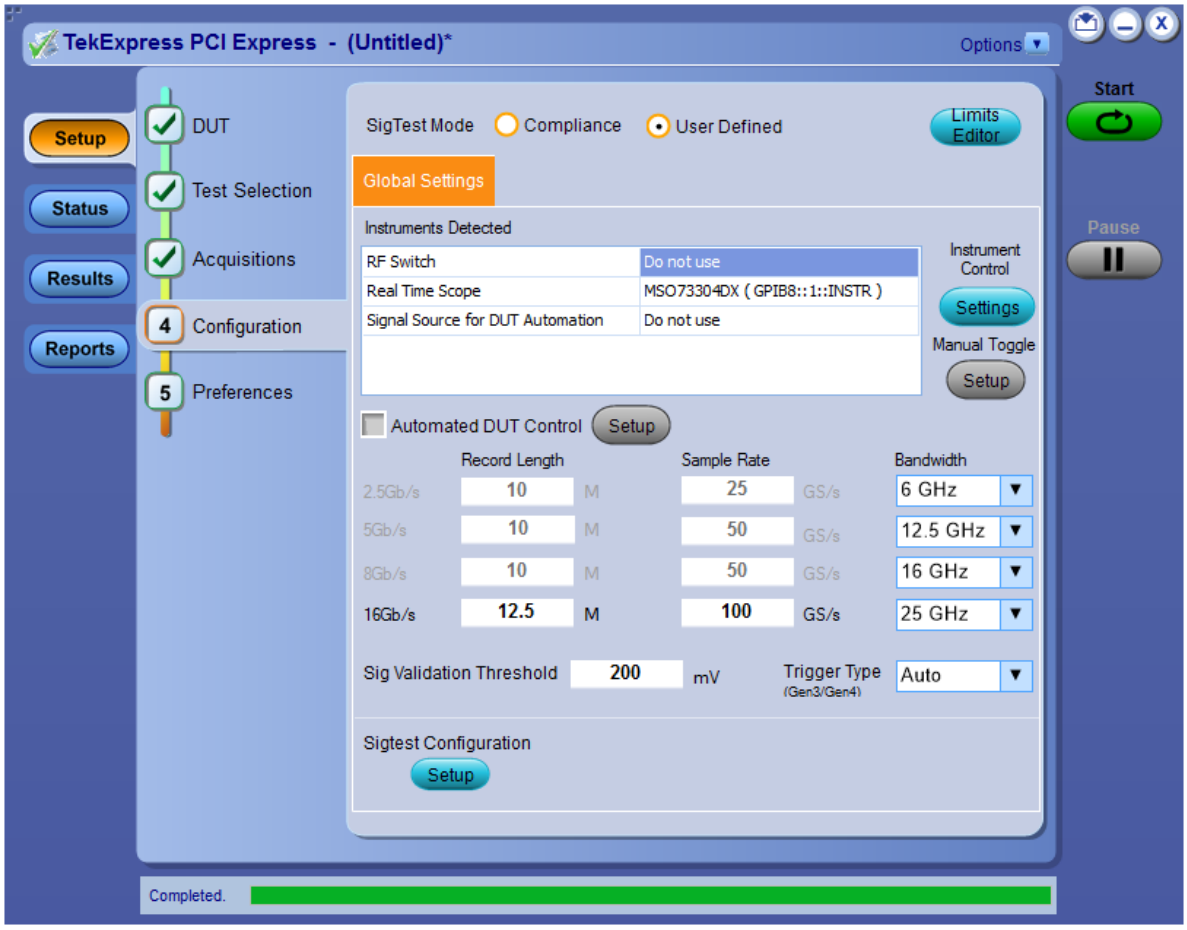

Figure 71 TekExpress PCI Express DUT Toggle in Manual Mode

5.3.1 Tx Signal Quality Test for Add-In-Card – DUT Toggle in Manual Mode

For Tx Signal Quality Test for Add-In-Card with DUT toggle in Manual Mode, make the connection as per section# 3.1 (Figure 1 Tx Signal Quality Test for Add-In-Card – DUT Toggle in Manual Mode) and start the test. User needs to push the ‘CMTS’ pulse button for 14 times to get to the Gen4 Preset0 pattern, post-acquisition of Gen4 Preset0, TekExpress application will prompt the user to send Gen4 Preset1 pattern then push the pulse button one time and click OK so that application will acquire. Continue this operation till Gen4 Preset10. The implementation method remains like section#4.1 exception point#8 is replaced with this step, where user selected ‘Do not use’ for ‘Signal Source for DUT Automation.

5.3.2 Tx Preset Test for Add-In-Card – DUT Toggle in Manual Mode

For Tx Signal Quality Test for Add-In-Card with DUT toggle in Manual Mode, make the connection as per section# 3.2 (Figure 2 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle in Manual Mode) and start the test. User needs to push the 'CMTS' pulse button for 14 times to get to the Gen4 Preset0 pattern, post-acquisition of Gen4 Preset0, TekExpress application will prompt the user to send Gen4 Preset1 pattern then push the pulse button one time and click OK so that application will acquire. Continue this operation till Gen4 Preset10. The implementation method remains like section#4.2 exception point#8 is replaced with this step, where user selected 'Do not use' for 'Signal Source for DUT Automation.

5.3.3 Tx Pulse Width Jitter Test for Add-In-Card – DUT Toggle in Manual Mode

For Tx Signal Quality Test for Add-In-Card with DUT toggle in Manual Mode, make the connection as per section# 3.2 (Figure 2 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle in Manual Mode) and start the test. User needs to push the 'CMTS' pulse button for 26 times to get to the Gen4 Preset0 pattern, post-acquisition of Gen4 Preset0, TekExpress application will prompt the user to send Gen4 Preset1 pattern then push the pulse button one time and click OK so that application will acquire. Continue this operation till Gen4 Preset10. The implementation method remains like section#4.3 exception point#8 is replaced with this step, where user selected 'Do not use' for 'Signal Source for DUT Automation.

5.3.4 Channel Tx Signal Quality Test for System-Board – DUT Toggle in Manual Mode

For Tx Signal Quality Test for System-Board with DUT toggle in Manual Mode, make the connection as per section# 3.3 (Figure 3 Tx Signal Quality Test for System-Board – DUT Toggle in Manual Mode) and start the test. User needs to push the 'CMTS' pulse button for 14 times to get to the Gen4 Preset0 pattern, post-acquisition of Gen4 Preset0, TekExpress application will prompt the user to send Gen4 Preset1 pattern then push the pulse button one time and click OK so that application will acquire. Continue this operation till Gen4 Preset10. The implementation method remains like section#4.4 exception point#8 is replaced with this step, where user selected 'Do not use' for 'Signal Source for DUT Automation.

5.3.5 Channel Tx Signal Quality Test for System-Board – DUT Toggle in Manual Mode

For Tx Preset Test for System-Board with DUT toggle in Manual Mode, make the connection as per section# 3.4 (Figure 4 Tx Preset Test for System-Board – DUT Toggle in Manual Mode) and start the test. User needs to push the 'CMTS' pulse button for 14 times to get to the Gen4 Preset0 pattern, post-acquisition of Gen4 Preset0, TekExpress application will prompt the user to send Gen4 Preset1 pattern then push the pulse button one time and click OK so that application will acquire. Continue this operation till Gen4 Preset10. The implementation method remains like section#4.5 exception point#8 is replaced with this step, where user selected 'Do not use' for 'Signal Source for DUT Automation.

5.4 Compliance Pattern Toggle Sequence

Toggle Sequence	*Setting#*	*Compliance Pattern from the DUT*	*Data Rate (GT/s)*
Power ON	1	Gen1	2.5
1	2	Gen2 - 3.5dB	5
2	3	Gen2 - 6.0dB	5
3	4	Gen3 - P0	8
4	5	Gen3 - P1	8
5	6	Gen3 - P2	8
6	7	Gen3 - P3	8
7	8	Gen3 - P4	8
8	9	Gen3 - P5	8
9	10	Gen3 - P6	8
10	11	Gen3 - P7	8
11	12	Gen3 - P8	8
12	13	Gen3 - P9	8
13	14	Gen3 - P10	8
14	**15**	**Gen4 - P0**	**16**
15	16	Gen4 - P1	16
16	17	Gen4 - P2	16
17	18	Gen4 - P3	16
18	19	Gen4 - P4	16
19	20	Gen4 - P5	16
20	21	Gen4 - P6	16
21	22	Gen4 - P7	16
22	23	Gen4 - P8	16
23	24	Gen4 - P9	16
24	25	Gen4 - P10	16
25	26	Jitter Measurement Pattern on all Lanes.	16
26	**27**	**Jitter Measurement Pattern on Lanes 0/8/16/24 and Compliance pattern on all other Lanes**	**16**
27	28	Jitter Measurement Pattern on Lanes 1/9/17/25 and Compliance pattern on all other Lanes	16
28	29	Jitter Measurement Pattern on Lanes 2/10/18/26 and Compliance pattern on all other Lanes	16
29	30	Jitter Measurement Pattern on Lanes 3/11/19/27 and Compliance pattern on all other Lanes	16
30	31	Jitter Measurement Pattern on Lanes 4/12/20/28 and Compliance pattern on all other Lanes	16
31	32	Jitter Measurement Pattern on Lanes 5/13/21/29 and Compliance pattern on all other Lanes	16
32	33	Jitter Measurement Pattern on Lanes 6/14/22/30 and Compliance pattern on all other Lanes	16
33	34	Jitter Measurement Pattern on Lanes 7/15/23/31 and Compliance pattern on all other Lanes	16

Figure 72 Compliance Pattern Toggle Sequence