Version 0.7 Feb-2019





Tektronix Method of Implementation for PCI Express Gen 4.0 TX CEM Test Procedure

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#### MODIFICATION RECORD

Version	Date	Changes done
0.1 Draft	07-Jan-2019	All
0.2 Draft	08-Jan-2019	Section 4
0.3 Draft	17-Jan-2019	All
0.4 Draft	04-Feb-2019	All
0.5 Draft	06-Feb-2019	All
0.6 Draft	07-Feb-2019	All
0.7 Draft	07-Feb-2019	All
1.0	12-Feb-2019	All

#### References

The following documents are referenced in this document:

• PCI Express® Architecture PHY Test Specification Revision 4.0, Version 0.9 Software

- TekScope Firmware v10.8 or above
- DPOJET v10.0.6 or above
- DPOJET PCIE v10.4.2 or above
- TekExpress PCI Express v10.4.4 or above
- SIGTEST Post processing analysis tools (4.0.42) / (4.0.45) as on 12-Feb-2019
- Check for latest SigTest versions on the Intel website

#### **REQUIRED EQUIPMENTS**

Equipment	Details	Qty	P/N	Vender
Gen4 CEM Fixture	CBB/CLB/ISI Board of PCIE 4.0	1	NA	PCI-SIG
	Rev2.0			
SMA-SMA Cable	1m SMA-SMA Phase Matched Cable	1	PMCABLE1M	Tektronix
	Pair			
SMA-SMP Cable	1m SMA-SMP Phase Matched Cable	2 (pairs)	174-6659-01	Tektronix
	Pair (1 pair needed without toggle			
	automation and 2 pairs needed with)			
SMA-SMP short	SMA - SMP cable pair, 2.5 inches,	1 (pair)	80350960	Huber-
cable	<1psec skew			Suhner
SMP-SMP Cable	SMP-SMP cable pair, 12 inches,	1 (pair)	80345501	Huber-
	<1psec skew			Suhner
SMP-F 50 Ohm	Some Add-In Card require	6/14/30	ST2645	Fairview
terminator	termination for unused lanes.			Microwave
ATX Power Supply	Any ATX Power Supply >=750W	1	NA	Any
Real Time	DPO73304SX/DPS75002SX	1	NA	Tektronix
Oscilloscope	DPS75902SX/DPS77002SX			
AFG/AWG with	Optional Equipment – Needed if	1	AWG7122C or	Tektronix
BNC to SMA	toggle automation is to be utilized.		AFG (check with	
adaptors	DC blocks can optionally be added.		rep for PN)	
SMA Probes	TCA-SMA-292D	4		Tektronix
Differential Probes	P7625/P7633	2		Tektronix

## 1. Introduction

This Method of Implementation (MOI) provides direction for testing PCIe Gen4 CEM Tx using a Tektronix Real Time Oscilloscope with the TekExpress PCI Express automation software. This document provides a list of test equipment, connection diagrams, and procedures per the PCI Express Architecture PHY Test Specification Revision 4.0. Following are the five tests which are required for Gen4 CEM Tx.

- 1. Add-in Card Transmitter Signal Quality Test for 16 GT/s
- 2. Add-in Card Transmitter Preset Test for 16 GT/s
- 3. Add-in Card Transmitter Pulse Width Jitter Test for 16 GT/s
- 4. System Board Transmitter Signal Quality Test for 16 GT/s
- 5. System Board Transmitter Preset Test for 16 GT/s

# 2. Probe Support

Tektronix supports both SMA (direct) probes and Differential probes for PCI Express Gen4 Transmitter testing. Add-In Cards require only a Data signal and Systems require both Data and Clock signal for Transmitter testing, so the probe configuration is different between Add-In Cards and Systems.

Refer to the table below for recommended scope and probe configurations:

DUT Type	Probe Type	Scope Model	Note
Add-In Card/ Non-	2 x SMA Probe	MSO/DPO72504DX MSO/DPO73304DX DPO73304SX	Use the alternate channel on the scope Ex. Ch1 and Ch3 or Ch2 and Ch4
Root	1 x Differential Probe	MSO/DPO72504DX MSO/DPO73304DX DPO73304SX	
System/Host/Root	4 x SMA Probe	DPS73308SX DPS75004SX	Use the Master unit TekConnect channels for Data signal and Extension unit TekConnect channels for Clock signal
	2 x Differential Probe	MSO/DPO72504DX MSO/DPO73304DX DPO73304SX	Use the alternate channel on the scope Ex. Ch1 and Ch3 or Ch2 and Ch4

Tektronix Probe P/N:

- SMA Probe: TCA-SMA-292D
- Differential Probe: P7625 or P7633

# 3. CONNECTION DIAGRAM

This section provides connection diagrams for all Tx tests as descripted in the PCI Express Architecture PHY Test Specification executed with a Tektronix oscilloscope and manually toggling the DUT through the compliance mode patterns.



#### 3.1 Tx Signal Quality Test for Add-In-Card – DUT Toggle in Manual Mode

Figure 1 Tx Signal Quality Test for Add-In-Card – DUT Toggle in Manual Mode





#### 3.2 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle in Manual Mode

Figure 2 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle in Manual Mode





#### 3.3 Tx Signal Quality Test for System-Board – DUT Toggle in Manual Mode

Figure 3 Tx Signal Quality Test for System-Board – DUT Toggle in Manual Mode





#### 3.4 Tx Preset Test for System-Board – DUT Toggle in Manual Mode

Figure 4 Tx Preset Test for System-Board – DUT Toggle in Manual Mode





#### 3.5 Tx Signal Quality Test for Add-In-Card – DUT Toggle Automation

Figure 5 Tx Signal Quality Test for Add-In-Card – DUT Toggle Automation





#### 3.6 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle Automation

Figure 6 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle Automation





## 3.7 Tx Signal Quality Test for System-Board – DUT Toggle Automation

Figure 7 Signal Quality Test for System-Board – DUT Toggle Automation

LEGEND	
	12" SMP-SMP Cable from Gen4 CLB Rev2 1X Laneo P and N to "Variable ISI Pair#0" P and N
	2.5" SMP-SMA Cable connected with SMA-SMA 1 Meter Phase Matched Cable from "Variable ISI
	Fail #0 F and N connected to Oschloscope CHT and CH5
	SMA-SMP 1 Meter Cable from Gen4 CLB Rev2 Ref Clk P and N to Oscilloscope CH2 and CH4
	SMA-SMP 1 Meter Cable from AWG/AFG on the Gen4 CLB Rev2 to RX Lane0 P and N
	Note:
	If you are using AFG for DUT toggle automation, DC blocks are optional. They are not required for AWG.
Note:	Variable ISI pair#0 is nominal, but to ensure correct loss follow the VNA based measurements described
	in the test fixture characterization



#### 3.8 Tx Preset Test for System-Board – DUT Toggle Automation

Figure 8 Tx Preset Test for System-Board – DUT Toggle Automation



## 4. Tests

Following are the five tests that are recommended for Gen4 CEM Tx.

- 1. Add-In-Card Transmitter Signal Quality Test for 16 GT/s
- 2. Add-In-Card Transmitter Preset Test for 16 GT/s
- 3. Add-In-Card Transmitter Pulse Width Jitter Test for 16 GT/s
- 4. System-Board Transmitter Signal Quality Test for 16 GT/s
- 5. System-Board Transmitter Preset Test for 16 GT/s

4.1 Add-In-Card Transmitter Signal Quality Test for 16GT/s

This is referred to as "Add-In-Card Transmitter Electrical Compliance Test for 16.0 GT/s" in *PCI Express*® *Architecture PHY Test Specification Revision 4.0, Version 0.9.* This test is run on all card electromechanical (CEM) form factor add-in cards. This test verifies the Tx signal of the system at 16 GT/s meets the minimum eye diagram requirements with at least one Tx equalization preset.

- 1. Insert the Add-In Card under test into a compliance base board (CBB) 4.0 without power.
- 2. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
- 3. Launch TekExpress PCI Express Application from TekScope  $\rightarrow$  Analyze menu.
- 4. Select the configuration in the application as per the figure below.



Figure 9 TekExpress PCI Express Add-In-Card Signal Quality Test Selection 1

5. Go to Test Selection panel and observe that Signal Test of 16Gbps are selected. By default, 'Uncorrelated PWJ TJ @E-12 Gen4' test is in unchecked state as physical connections are different and the procedure is explained in another section.

V TekExpress PCI Express	- (Untitled)* Option	s <b>- C</b>
Setup DUT	CEM : Add-In-Card : Gen4 - 4.0 Signal Test Preset Test	Start
Results Reports 5 Preferences	16Gbps     Unit Interval Gen4     Mask Hits(All Bits) Gen4     Gomposit Eye Height Gen4     Transition Eye Diagram Gen4     Min Eye Width Gen4     Min Eye Width Gen4     Min Time Between Crossovers Gen4     Jg E-12 Gen4     P J_d d Gen4     RJ(RMS) Gen4     Peak to Peak Jitter Gen4     Extrapolated Eye Height Gen4     Uncorrelated PWJ TJ@E-12 Gen4	Pause
	Test Description Please select a test name to view its description Show MOI Schematic	
Ready.		

Figure 10 TekExpress PCI Express Add-In-Card Signal Quality Test Selection 2

6. Go to Acquisition panel and set the source of Lane0 Date+ to CH1 and Data- to CH3. Set the No of Acquisitions to '3' as we need to capture three 2.0M UI (Gen4 Compliance Pattern) differential waveforms for every Tx EQ Preset.

V TekExpress PCI Express -	(Untitled)*	Options 💽 🧎	
Setup DUT Status Test Selection Besults 3 Acquisitions	CEM : Add-In-Card : Gen4 - 4.0 Lane::0 Data1 + CH1 Data1 - CH3	Refresh View Sources Probes	Start
Configuration	Lane0: 16Gbps P0 Acquisition     Lane0: 16Gbps P01 Acquisition     Lane0: 16Gbps P01 Acquisition		
5 Preferences	Lane0 : 166bps P03 Acquisition Lane0 : 166bps P04 Acquisition Lane0 : 166bps P05 Acquisition Lane0 : 166bps P06 Acquisition Lane0 : 166bps P07 Acquisition Lane0 : 166bps P08 Acquisition Lane0 : 166bps P10 Acquisition		
	Acquire Options • Acquire All Waveforms Before Analysis • Acquire Only - Do Not Analyze Save Options	No. OfAcquisitions (Gen4)	
Ready.	Save Only Analyzed Waveform		

Figure 11 TekExpress PCI Express Add-In-Card Signal Quality Test Acquisitions

- For the Tx Signal Quality Test for Add-In-Card in automated procedure we are using TekExpress PCI Express with automated DUT toggle option using AWG7122C. User can use AFG/AWG/GRL PCIE Controller for automated DUT toggle option. Refer the <u>'Appendix Section#5.3.1'</u> for manual DUT toggle option.
- 8. Go to Configuration panel and select the 'Signal Source for DUT Automation' [AWG7122 in this case] and select the check box 'Automated DUT Control'.

🌠 TekExp	ress PCI Express -	(Untitled)*						Opti	ons 💌	
Setup		SigTest Moo	le 💿 Comp	liance	0	Jser Defined		Edito		Start
Status	V lest Selection	Instruments D	etected							Pause
Results	Acquisitions	RF Switch Real Time Sco	pe		Do no DPO7	ot use 73304D ( GPIB8	::1::INSTR)	Instrur Cont	nent rol	
Reports	4 Configuration	Signal Source	for DUT Autom	ation	AWG	7122C ( GPIB1:	:2::INSTR )	Manual 1	ioaale	
Reports	5 Preferences	🗸 Automati	ed DUT Contro	ol Setu	qu			Setu	p	
			Record Length			Sample Rate		Bandwidth		
			2.5	М		25		6 GHz	•	
			10	М		50		12.5 GHz	•	
			10	М		50		16 GHz	Y	
			12.5	М		100		25 GHz	Y	
		Sig Validatio	n Threshold	200		mV	Trigger Type (Gen3/Gen4)	Auto	•	
		Sigtest Cont	iguration							
	Ready.									

Figure 12 TekExpress PCI Express Add-In-Card Signal Quality Test Configuration

9. Click on SigTest configuration 'Setup' and observe the SigTest version and templates used for this test.

Exe Configura	tion
Gen 4 : (Signal Test)	C:\Program Files (x86)\SigTest_4.0.42\SigTest.ex
Gen 4 : (Preset Test)	C:\Program Files (x86)\SigTest_4.0.42\SigTest.ex
Template Con	figuration
16 GB/s :	1.42\templates\PCIE_4_0_CARD\PCle_4_16G_CEM.dat
16 GB/s : (PWJ Test)	2\templates\PCIE_4_0_CARD\PCIE_4_16GB_BASE.dat Browse

Figure 13 TekExpress PCI Express Add-In-Card Signal Quality Test SigTest Configuration



- 10. Click on **to run the test**.
- 11. Make the connection as per <u>section#3.5 (Figure 5 Tx Signal Quality Test for Add-In-Card DUT Toggle Automation)</u> and verify that it as per the connection diagram that is prompted by application up during the run, Power ON the DUT and click OK to continue.
- 12. Observe that the DUT will be toggled automatically from Gen1 to Gen4 Preset P0 And will start acquisition, observe that Package model embedded on the scope (refpkg\_rootcomplex\_5db\_thru.s4p) gets applied and three waveforms of each preset are saved.



Figure 14 TekExpress PCI Express Add-In-Card Signal Quality Test applying package model

13. All acquired waveforms will be processed with SigTest using the "PCIe\_4\_16G\_CEM.dat" template file which performs CTLE optimization. If all Tx EQ presets fail with this approach, you can configure the SigTest Setup (step #9) to run each CTLE individually using the "PCIe\_4\_16G\_CEM\_CTLE\_6dB.dat through PCIe\_4\_16G\_CEM\_CTLE\_12dB.dat" template files. A passing result with either case is allowed per the PCI Express Architecture PHY Test specification.

	Test Status Log View		Sto
Setup	Message History		
Status	🕎 Signal Test 4.0.42	*	Davis
	Data Type 🗘 Differential		
Results	Data File C:\PCIE_Tx_Ref_WFMs\AIC_SQ_M0I\Package_TID_108_SQ_1 Browse		
Reports	Data File Neg		
iceports)	Clock File Browse		
	Clack File Neg		
	Load and Verify Data File Select Preset Test 🔻		
	Technology           PCIE_3_0_CARD            Template File		
	C/Program Files (x86)/SigT est_4.0.42\templa Sample Interval 10.000 ps		
	Number of Unit Intervals in File		
	Worst Non         Worst         Itter         CDR.         Results         PDF         QSpace         Filter           Transition Eyes         Transition Eyes         Histogram         Adapt         Results         PDF         Data         Port		
	Auto Scroll Clear Log	Save	

Figure 15 TekExpress PCI Express Add-In-Card Signal Quality Test SigTest Analysis

14. Observe the test results in TekExpress Results panel and once all the results are updated a test report will be generated. Additional information is provided beyond the compliance test criteria of passing the Min Eye Width and Extrapolated Eye Height measurements.

§ текехр	press PCI Express - (Untitled)*	Options 💌
	Test Status Log View	
Setup	Message History	
Status Results Reports	102/03/19 23:59.41. Compare Imit 26:145 >= 24.75. Result:Pass     102/03/19 23:59.42. Margin of result is: 1:1.395ps     102/03/19 23:59.42. Populating results for Mn Time Between Crossovers Gen4     102/03/19 23:59.42. Populating results for U fe E-12 Gen4     102/03/19 23:59.42. Populating results for U fe E-12 Gen4     102/03/19 23:59.43. Populating results for Plack to Peak Jitter Gen4     102/03/19 23:59.44. Populating results for Plack to Peak Jitter Gen4     102/03/19 23:59.44. Populating results for Plack to Peak Jitter Gen4     102/03/19 23:59.44. Populating results for Entropolated Eye Height Gen4     102/03/19 23:59.44. Populating results for Margin V     102/03/19 23:59.45. Populating results for Margin V     102/03/19 23:59.46. Populating results for Margin V     102/03/19 23:59.46. Populating results for Margin V     102/03/19 23:59.46. Populating results for Margin V     102/03/19 23:59.47. Populating results for Margin V     102/03/19 23:59.47. Populating results for Margin V     102/03/19 23:59.48. Populating results for Margin V     102/03/19 23:59.49. P	~
	<	>
	Auto Scroll	Clear Log Save

Figure 16 TekExpress PCI Express Add-In-Card Signal Quality Test Status

Signal Tests Gen4 Preset Test					Preierence
Description	Details	Generation	Pass/Fail	Value	Margin
🖃 Lane0					
🛨 Unit Interval Gen4	Mean Unit Interval R1	16Gbps P04	Informative	62.500 ps	N.A
Mask Hits(All Bits) Gen4	Mask Hits R1	16Gbps P04	Informative	Result Unavailable	N.A
Composit Eye Height Gen4	Composit Eye Height R1	16Gbps P04	Informative	Result Unavailable	N.A
Transition Eye Diagram Gen4	Min Transition Eye Height R1	16Gbps P04	Informative	42.097 mV	N.A
Transition Eye Diagram	Min Transition Voltage R1	16Gbps P04	Informative	-153.640 mV	N.A
Transition Eye Diagram Gen4	Max Transition Voltage R1	16Gbps P04	Informative	153.997 mV	N.A
Transition Eye Diagram Gen4	Min Transition Top Margin R1	16Gbps P04	Informative	-2.366 mV	N.A
Transition Eye Diagram	Min Transition Bottom Margin R1	16Gbps P04	Informative	1.537 mV	N.A
Transition Eye Diagram Gen4	Transition Eye Mask	16Gbps P04	Informative	Result Unavailable	N.A

Figure 17 TekExpress PCI Express Add-In-Card Signal Quality Test Results

2 🏟 💾 🖶 🖂 主 🖲	1/5	100% 💌	🗄 🖁 🔗 🖻 🖌	*					Tools 5	ign (	Comm
								_			
	— n .		TokEvprop								
	Tel/troi		TekExpres	s FOI Express							
			Add-In-Ca	rd Test Report							
	Setup Information		an amos	DOO ETTI Annian							
	Dotto		201001	DPOULT Version		10.8.179					
	Date Tree		2019/02/04/00/30:55	Scope Model	0	200733046/A					
	control type		PCI Example: 10.4.5.32	SPC FactoryCalibration		TUNCAL					
	TekExpress Version		Framework:4.9.0.5	Scope F/W Version	1	19.1 Build 16					
	Test Mode		SigTest User Defined	Probe1 Model	T	CA-SMA					
	Spec Version		Gent - 4.0	Probe2 Model	T	A292D					
	SigTest Version		3.2.0.3(Gen1,2,3) 4.0.42 (Gen4)-Signa	Probe2 Serial Number	N	A					
	(A. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.		Tests 4.0.42 (Gen4)-Preset Tests	Probe3 Model	N	A					
	Sidt Number		01	Probe3 Serial Number	N	A					
	Overall Execution time	0	Door 12	Probe4 Model	N	A					
	Chorder Hourt House		1000	Probed Siertal Number	I N	•					
	DUT COMMENT: Test Name Summary Te	DUT001				^					
	DUT COMMENT Test Name Summary IT Unit Internal Gen4 Mask Hts/All Bits/Gen Composit Eye Height O Transition Eye Daram Non Transition Eye Daram Non Transition Eye Daram Min Time Batesen Ore Tuff E-12 Gen4	DUTRO1 Table Conti In Gonti In Gonti In Gonti In Gonti In Gonti In Gonti In Gonti				A					
	DUT COMMENT: Test Name Summary To July Interest Cen4 Metek Htts/All Bits Cen4 Compose Test Helpfe C Tarasion Eye Daarm Non Transion Eye Daarm Min Eye Wath Cen4 Min Eye Wath Cen4 Min Eye Wath Cen4 D ad Gen4 D ad Gen4	DUTTO1 Table Conti n Gonti n Gonti surram Gonti zasouna Conti				A					
	DUT COMMENT: Test Name Summary Tr Unit Integrit Grad. Minis Hind (1818) Grad. Compast Eye Height C Tambion Eye Dagtorn Non Timmi Evenon Close Min Time Evenon Close Holl E-12 Grad. RUPINS) Grad. Berl Ministry Berl Closed. Berl Ministry Berl Closed.	DUTION Table Inf Gent Gent Mont Scores Gent Scores Gent Mont Scores Scor				A					
	DUT COMMENT: Test Name Summary II List integet Gen4 Mink Him/All Bind Cen Compare Lips Heart C Tarssion Eve Dasten Nm Transition Eve Dasten Nm Transition Eve Dasten Min Time Between Cen Tardin E-12 Cend D, ad Cend Pank Jo Pank Jiller Dath Center Eve Heart Dath Center Eve Heart Dath Center Eve Heart	DUTION Table Ind Canif In Gant In Gant Inscient Gant Inscient Gant Inscient Gant Inscient Gant				n 					
	DUT COMMENT: Test Name Summary Tr Juli Intradi Gani Minis Hini (1818) Gani Dimesi Ken Ken Dagan Mini Time Stere Dagan Stere Dagan Mini Time Stere Dagan Stere Dagan Stere Dagan Stere Dagan Stere Dagan Stere Dagan Stere Dagan Mini Time Stere Dagan Stere Dagan Mini Time Stere Dagan M	DUTION Table In Ganit In Ganit In Ganit In Ganit In Ganit In Ganit In Ganit In Ganit In Ganit				~ 					
	DUT COMMENT: Test Name Burmary Tr Job Introd Graf Mede Hind Italia Card Compani Eury Hagta C Dansilon Eve Dagant Non Tanuiton Eve Dagant Non Card Card Dad Card Data Card Data Card Eventoria Card	DUTION Table Each n.Gent again Gent again Gent assource Gent the Gent				^					
	DUT COMMENT: Test Name Summary Tr Jaki Virgest Gend Meter Handrick Ban Gen Dimonsh Eine Hagtro C Dimonsh Eine Nather Dimonsh Eine Nather Meter State States Meter Nather Did E-12 Cond Did E-12 Cond E-10 Cond E-10 Cond E-10 Kent Did E-12 Cond E-10 Kent Did E-12 Cond E-10 Kent Did E-12 Cond E-10 Kent E-10 Kent Did E-12 Cond E-10 Kent Did E-10 Ken	DUTION Table Ind Cansi In Gansi Second Secon				1					
	DUT COMMENT Test Name Summary Te Unit transf Earls Mest Hinkle Bits Carr Dampion Earls High Carr Dampion Earls High Carr Min Stev Math Card Min Stev Math Card Math	DUTTO! Teche and Canti azaran Canti azaran C	ta Ree Equilizión Mile	nund Value Test Result	Margin	Low Limit	Hgh Limit				
	DUT COMMENT Test Issen Surveys V International Content Mass Surveys V International Content Mass Surveys V International Content Instructional Content Instructional Content Instructional Content Instructional Content Instructional Content Mass Instruction Instructional Mass Instruction Instructional Instructi	DUTION Teles and Canti In Ganti Saram Ganti Teles Canti Inteles the Name Date Net Canti Net Canti Net Canti Net Canti	ta Refe Equilization Mee Obje Poli Gen4 (22.5	aured Value Test Result 20 ja Homative	Margin NA	Low Limit NA	Hgh Limit NA				
	DUT COMMENT Test Rever Surveys T List stream Surveys T Mass Hardwidth Social Sampas Sampas Sampas Mass Sampas Sampas Mark Sampas Samp	DUTDO1 Table Inti Ganti Canti	ta Refe Egustarion Mile Zite Poli Gent G2 Zite Poli Gent G25	aurol Vulue Tast Result 20 ps Hieranije 20 ps Hieranije	Margin NA NA	Low Limit NA NA	Hgh Limit NA NA				
	DUT COMMENT Test Same Summers T. 14th thread Same Summers T. 14th thread Same Summers T. 14th thread Same Same Same Same Same Same Same Same	DUTTON           Table           Canal           Canal<	а Яле Бранбалом Ми Окра (940 Gunk) 0.2. Окра (964 Gunk) 0.2. Окра (964 Gunk) 0.2.2	aurod Valauo II Test Pesual 1 20 ja Holomation 20 ja Holomation 20 ja Holomation	Mirgin NA NA NA	Low Limit NA NA NA	High Limit NA NA NA				

Figure 18 TekExpress PCI Express Add-In-Card Signal Quality Test Report

15.Once test report is generated you can save the Test Session in TekExpress, Options → Save Test Setup → Tek\_Gen4\_AIC\_SQ\_MOI (Example of session name). The saved data can be found in the location X:\PCI Express\Tek\_Gen4\_AIC\_SQ\_MOI\DUT001.

TekExpress PCI Express - (Tek_Gen4_AIC_SQ_MOI)	Options 🔽 😁 🗕 🗴
Organize   Include in library   Share with   Burn New folder	:= - 🔟 🔞

Figure 19 TekExpress PCI Express Add-In-Card Signal Quality Test Session Saved

### 4.2 Add-In-Card Transmitter Preset Test for 16 GT/s

This is referred as "Add-In-Card Transmitter Preset Test for 16.0 GT/ s" in *PCI Express*® *Architecture PHY Test Specification Revision 4.0*. This test is run on all card electromechanical form factor add-in cards that operate at 16.0 GT/s. The test verifies that the add-in card produces the correct transmitter equalization values for each preset in the set of 11 presets.

- 1. Insert the Add-In Card under test into a compliance base board (CBB) without power. A CBB revision 4.0 must be used at all data rates if 16 GT/s is supported.
- 2. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
- 3. Launch TekExpress PCI Express Application from TekScope  $\rightarrow$  Analyze menu.
- 4. Select the configuration in the application as per the figure below.

Setup       1       DUT       DUT ID       DUT01       Image: Status       I	V TekExpress PCI Express -	(Untitled)*	Options 💽 管
Results   3 Acquisitions   4 Configuration   5 Preferences     Device Profile   Data Rates   Transmitter Equalization   Link Analysis   2.5 Gb/s   5 Gb/s   8 Gb/s   1 16 Gb/s   Presets   Selected Presets for Signal Quality   PO,P01,P02,P03,P04,P05,P08,P09,P10     Multi-Lane   Selected Lanes   Lines   Lanes   Lanes   Signal Validation   Prompt me if Signal Check Fails	Setup 1 DUT Status 2 Test Selection	DUT ID DUT001 Slot Number • Acquire live waveforms Use pre-recorded waveform files SigTest Mode Compliance  •	r 01
S       Preferences       Data Rates       Transmitter Equalization       Link Analysis         S       2.5 Gb/s       Setup         S       5 Gb/s         8 Gb/s       8 Gb/s         16 Gb/s       Presets       Selected Presets for Signal Quality         Po,P01,P02,P03,P04,P05,P00,P07,P08,P09,P10       Meas Limits         SSC       Meas Limits         Selected Lanes       Lanes         L0       Signal Validation         Prompt me if Signal Check Fails       T	Results Acquisitions 4 Configuration	Specification     Device Type     Version       CEM     ▼     Add-In-Card     ▼     Gen4 - 4.0	
Multi-Lane Selected Lanes L0 Multi-Lane Signal Validation Prompt me if Signal Check Fails	5 Preferences	Device Profile         Data Rates       Transmitter Equalization         Link Analysis         2.5 Gb/s         5 Gb/s         8 Gb/s         ✓ 16 Gb/s         Presets       Selected Presets for Signal Quality P0,P01,P02,P03,P04,P05,P06,P07,P08,P09,P10         SSC       Meas Limits         On       Off	
		Multi-Lane Selected Lanes Lanes L0 Prompt me if Signal Check Fa	ils V

Figure 20 TekExpress PCI Express Add-In-Card Preset Test

5. Go to Test Selection panel and uncheck all the 'Signal Tests' in the 16Gbps tree node in the 'Signal Test' tab, then go to 'Gen4 Preset Test' tab and click on 'Select All' so that all the presets get selected.



Figure 21 TekExpress PCI Express Add-In-Card Preset Test Selection 1

🖉 TekExpr	ress PCI Express -	(Untitled)*				Options	
Setup	DUT	CEM : Add-	In-Card : Gen4 st Gen4 Preset Tes	- 4.0 st	Deselect A	) Select All	Start
Status	<u> </u>		Preset	Preshoot	Deemphasis	Dependencies	Pause
		•	PO	0.0 dB	-6.0 dB	P04	
Results		~	P01	0.0 dB	-3.5 dB	P04	
		✓	P02	0.0 dB	-4.4 dB	P04	
Reports			P03	0.0 dB	-2.5 dB	P04	
	– .		P04	0.0 dB	0.0 dB	-	
	5 Preferences		P05	1.9 dB	0.0 dB	P04	
			P06	2.5 dB	0.0 dB	P04	
		✓	P07	3.5 dB	-6.0 dB	P05,P02	
			P08	3.5 dB	-3.5 dB	P06,P03	
			P09	3.5 dB	0.0 dB	P04	
		~	P10	0.0 dB	-9.5 dB	P04	
		Lanes Selected I L0	anes		Show M	(O) (Schematic	
	Ready.						

Figure 22 TekExpress PCI Express Add-In-Card Preset Test Selection 2

6. Go to Acquisition panel and set the source of Lane0 Date+ to CH1 and Data- to CH3. By default, one differential waveforms for every Tx EQ Preset is captured and saved by TekExpress.

TekExpress PCI Express -	(Untitled)*	Options 💽 🖽 🤤	20
TekExpress PCI Express -       Setup     UT       Status     Test Selection       3 Acquisitions       Configuration       5 Preferences	(Untitled)*         CEM: Add-In-Card : Gen4 - 4.0         Lane: 0         Lane: 1         Otal + CH1         Data1 - CH3         Acquisition         Lane: 160bps P0 Acquisition         Lane: 160bps P01 Acquisition         Lane: 160bps P02 Acquisition         Lane: 160bps P03 Acquisition         Lane: 160bps P04 Acquisition         Lane: 160bps P10 Acquisition         Lane: 160bps P10 Acquisition         Caquire Options         O Acquire Options         Acquire Only- Do Not Analyze         Save Only Analyzed Waveform	No. OfAcquisitions (Gen4)	se
Ready			

Figure 23 TekExpress PCI Express Add-In-Card Preset Test Acquisitions

- 7. For the Tx Preset Test for Add-In-Card in automated procedure we are using TekExpress PCI Express with automated DUT toggle option using AWG7122C. User can use AFG/AWG/GRL PCIE Controller for automated DUT toggle option. Refer the <u>'Appendix Section#5.3.2'</u> for manual DUT toggle option.
- 8. Go to Configuration panel and select the 'Signal Source for DUT Automation' [AWG7122 in this case] and select the check box 'Automated DUT Control'.

					<u></u>			
Setup		Sig lest Mo	de 💽 Comp	iliance	User Define	ed	Edito	
	Test Selection	Global Setti	ngs					
Status		Instruments D	)etected					
	Acquisitions	RF Switch			Do not use		Instrur Cont	nent trol
results		Real Time Sc	ope		DPO73304D ( GPI	B8::1::INSTR )	Satti	nas
4	Configuration	Signal Source	e for DUT Autom	ation	AWG7122C ( GPI	B1::2::INSTR)		Igo I
Reports							Mariuari	Uggie
5	Preferences			_	~		Sett	
		🗸 Automat	ted DUT Contro	ol 🔇 Seti	up l			
			Record Length		Sample Rate	e	Bandwidth	
			2.5	М	25		6 GHz	•
			10	M	50		12.5 GHz	•
			10	м	50		16 GHz	•
			12.5	м	100		25 GHz	•
		Qia Validatio	on Throchold	200		Trigger Type	A	
		org validatio	Sir micshold	200	mV	(Gen3/Gen4)	Auto	
		Sigtest Con	figuration					
		Set	up					

Figure 24 TekExpress PCI Express Add-In-Card Preset Test Configuration

9. Click on SigTest configuration 'Setup' and observe the SigTest version used for this test.



Figure 25 TekExpress PCI Express Add-In-Card Preset Test SigTest Configuration



10. Click on **to run the test**.

- 11. Make the connection as per <u>section#3.6 (Figure 6 Tx Preset / Pulse Width Jitter Test</u> <u>for Add-In-Card – DUT Toggle Automation</u>) and verify that it as per the connection diagram that is prompted by application up during the run, Power ON the DUT and click OK to continue.
- 12. Observe that the DUT will be toggled automatically from Gen1 to Gen4 Preset P0 And will start the acquisition, observe that Package model is NOT embedded on the scope and the waveforms of each preset are saved.



Figure 26 TekExpress PCI Express Add-In-Card Preset Test NO package model applied



13. After acquiring of all the waveforms, they will be post-processed using SigTest.

Figure 27 TekExpress PCI Express Add-In-Card Preset Test Analysis

14. Observe the test results in TekExpress Results panel and once all the results are updated a test report will be generated.

K TekExp	ress PCI Express - (Untitled)*	Options 💌	
	Test Status Log View		Start
Setup	Message History		
Status       Results       Reports	01/17/19 09:55:30 : Populating results for preset :P06 Gen4 01/17/19 09:55:30 : PreShoot : 2.297 dB 01/17/19 09:55:30 : Vb : 704.737 mV 01/17/19 09:55:30 : Poss/Fail Result : Pass 01/17/19 09:55:30 : Poss/Fail Result : Pass 01/17/19 09:55:31 : Vb : 204.737 mV 01/17/19 09:55:31 : Vb : 204.738 mV 01/17/19 09:55:31 : Vb : 407.219 mV 01/17/19 09:55:31 : Vb : 407.219 mV 01/17/19 09:55:31 : Poss/Fail Result : Pass 01/17/19 09:55:32 : Poss/Fail Result : Pass 01/17/19 09:55:34 : SigTest anlaysis in progress, result will be updated after analysis 01/17/19 09:55:36 : Test execution completed.		Pause
		4	
	Auto Scroll Clear Log	Save	

Figure 28 TekExpress PCI Express Add-In-Card Preset Test Status

Gen4				Preferences
Signal Lests Preset Test				
Preset	Pass/Fall	αv	Preshoot	DeEmphasis
E Laneo	- Dava	400 750	0.000 40	5 C40 JD
P0 Gen4	Pass Pass	480.753 mV	0.000 dB	-5.0 19 GB
Blig Port Gen4	Pass Roop	667.620 mV	0.000 dB	-3.331 UB
P02 Gen4	Pass Pass	709.046 mV	0.000 dB	-4.170 dB
P04 Gen4	Pass	918.066 mV	0.000 dB	0.000 dB
P05 Gen4	Pass	759 708 mV	1.645 dB	0.000 dB
P06 Gen4	Pass	704 737 mV	2 297 dB	0.000 dB
P07 Gen4	Pass	407 219 mV	2.885 dB	-5 416 dB
P08 Gen4	Pass	471.475 mV	3.532 dB	-3.491 dB
P09 Gen4	Pass	622.218 mV	3.379 dB	0.000 dB
P10 Gen4	Pass	316.932 mV	0.000 dB	-9.238 dB

Figure 29TekExpress PCI Express Add-In-Card Preset Test Results

1_094.) 1_Vies	pdf - Adobe Reader w. Window, Helo								
-									
- 🔁	2 🏠 🗒			/ 1 111% -		1	Tools	Sign	Com
_									
				TekEynress	PCI Express	2			
				Add-In-Card	Test Report				
	Setup Information		an ann a'		000 571 (				
	DUTID		001001	0.44.07	DPCJET Version		10.0.8.179		
	Date/ Iime		2019-01-17 0	8:44:07	Scope Model		DP073304	0	
	Device type		DCI Evonee	10.4.5.28 (DAILV)	SDC EactoryCalibrati	~	D241041	19	
	TekExpress Version		Framework:4	1.9.0.5	Scope E/W Version		10.8.3 Buil	d 3	
	Test Mode		SigTest Com	pliance	Probe1 Model		TCA292D		
	Spec Version		Gen4 - 4.0		Probe1 Serial Number		NA		
	SinTest Version		3.2.0.3(Gen1	,2,3) 4.0.42 (Gen4)-Signal	Probe2 Model		TCA292D		
	oignost reionair		Tests 4.0.42	(Gen4)-Preset Tests	Probe2 Serial Number	• • • • • • • • • • • • • • • • • • •	N/A		
	Slot Number		01		Probe3 Model		TCA292D		
	Overall Test Result		Pass 0:11:29		Probe3 Serial Number		N/A		
	Overall Execution him	0	0.11.20		Probe4 Model		TCA292D		
					Probe4 Serial Number		NA		
					Signal Source Model	humber	AWG/122	U .	
	DI IT COMMENT	DI 0001			olgrai obulce certai r	vurriber	000012		
	DOT COMMENT.	001001							
	Test Name Summary	Table							
	PRESET RESULTS			B 01 1					
	Preset Name	Lane Name		PreShoot	De-Emphasis	Vb		Result	
	PU Gen4	Lane0		0.000 dB	-5.619 dB	480.753 mV		Pass	
	P10 Gen4	Laneu		0.000 dB	-9.230 UD	516.932 mV		Pass	_
	P01 Gen4	Lane0		0.000 dB	-4.176 dB	567 620 mV		Page	
	P03 Gen4	Lane0		0.000 dB	-2.256 dB	708.046 mV		Pass	_
	P04 Gen4	Lane0		0.000 dB	0.000 dB	918.066 mV		Pass	
	P05 Gen4	Lane0		1.645 dB	0.000 dB	759.708 mV		Pass	
	P06 Gen4	Lane0		2.297 dB	0.000 dB	704.737 mV		Pass	
	P07 Gen4	Lane0		2.885 dB	-5.416 dB	407.219 mV	·	Pass	
	P08 Gen4	Lane0		3.532 dB	-3.491 dB	471.475 mV		Pass	

Figure 30 TekExpress PCI Express Add-In-Card Preset Test Report

15. Once test report is generated you can save the Test Session in TekExpress, Options  $\rightarrow$  Save Test Setup  $\rightarrow$  Tek\_Gen4\_AIC\_Preset\_MOI (Example of session name). The saved data can be found in the location X:\PCI Express\Tek\_Gen4\_AIC\_Preset\_MOI\DUT001.

TekExpress PCI Express - (Tek_Gen4_AIC_Preset_MOI)	Options 💽 🖱 🗕 🙁
Computer → Local Disk (X:) → PCI Express → Tek_Gen4_AIC_Preset_MOI → DUT001 →	✓ Search DUT001
Organize   Include in library   Share with   Burn New folder	= - 1 0
Figure 31 TekExpress PCI Express Add-In-Card Preset Test Sess	ion Saved

## 4.3 Add-In-Card Transmitter Pulse Width Jitter Test for 16 GT/s

This is referred as "Add-In-Card Transmitter Pulse Width Jitter Test at 16 GT/s" in *PCI Express*® *Architecture PHY Test Specification Revision 4.0.* This test is run on all card electromechanical form factor add-in cards that operate at 16.0 GT/s. This test verifies that the add-in card produces a Pulse Width Jitter (PWj) below the PCIe Base Specification limit.

- 1. Insert the Add-In Card under test into a compliance base board (CBB) 4.0 without power.
- 2. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
- 3. Launch TekExpress PCI Express Application from TekScope  $\rightarrow$  Analyze menu.
- 4. Select the configuration in the application as per the figure below.

🕫 🎻 TekExp	oress PCI Express -	(Untitled)*	Options 🔽 🖄 🗕 🤇
Setup		DUT ID DUT001 Ø Slot Number	r 01 Start
Status	Test Selection	Acquire live waveforms     O Use pre-recorded waveform files SigTest Mode Compliance	Pause
Results	Acquisitions	SpecificationDevice TypeVersionCEMImage: Certain Control Certain	
Reports		Device Profile	
	5 Preferences	Data Rates Transmitter Equalization Link Analysis	
		5 Gb/s	
		8 Gb/s     Selected Presets for Signal Quality     Presets     Presets     Presets     Presets     Selected Presets for Signal Quality     P0,P01,P02,P03,P04,P05,P06,P07,P08,P09,P10	
		SSC Meas Limits	
		Multi-Lane Selected Lanes L0 Prompt me if Signal Check Fa	ils <b>T</b>
	Completed		
	completed.		

Figure 32 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test

5. Go to Test Selection panel and select Signal Test of 16Gbps, click on 'Deselect All' button which will uncheck all the tests. Now in the 16Gbps tree node select 'Uncorrelated PWJ TJ @E-12 Gen4' test.

V TekExpress PCI Express - (	Untitled)*		Options 💽 🕒 🔍
Setup DUT 2 Test Selection	CEM : Add-In-Card : Gen4 - 4.0 Signal Test Gen4 Preset Test	select Al) Sele	rct All
Reports Acquisitions Configuration 5 Preferences	Unit Interval Gen4     Mask Hits(All Bits) Gen4     Composit Eye Height Gen4     Transition Eye Diagram Gen4     Min Eye Width Gen4     Min Time Between Crossovers Gen4     D_dd Gen4     R1(RMS) Gen4     Peak to Peak Jitter Gen4     Extrapolated Eye Height Gen4     Uncorrelated PWJ TJ@E-12 Gen4		Pause
	Test Description Uncorrelated PWJ TJ@E-12 analysis window.	Show MOI Sch	ematic

Figure 33 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Selection

6. Go to Acquisition panel and set the source of Lane0 Date+ to CH1 and Data- to CH3. Set the No of Acquisitions to '3' as we need to capture three 2.0M UI (Gen4 Compliance Pattern) differential waveforms for the data rate clock pattern.

V TekExpress PCI Express -	(Untitled)*	Options	
Setup Status Results Reports DUT Test Selection 3 Acquisitions 4 Configuration 5 Preferences	CEM : Add-In-Card : Gen4 - 4.0 Lane:0 Data1 + CH1 Data1 - CH3 Acquisition > Lane0 : 16Gbps Data Clock Acquisition	Refresh Sources Probes	Pause
	Acquire Options • Acquire All Waveforms Before Analysis Acquire Only - Do Not Analyze Save Options Save Only Analyzed Waveform	No. OfAcquisitions (Gen4)	
Ready.			

Figure 34 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Acquisitions

- For the Tx Pulse Width Jitter Test for Add-In-Card in automated procedure we are using TekExpress PCI Express with automated DUT toggle option using AWG7122C. User can use AFG/AWG/GRL PCIE Controller for automated DUT toggle option. Refer the <u>'Appendix Section#5.3.3'</u> for manual DUT toggle option.
- 8. Go to Configuration panel and select the 'Signal Source for DUT Automation' [AWG7122 in this case] and select the check box 'Automated DUT Control'.

		SigTest Mo	de 💽 Complia	nce 🔿	User Definer		Limit		St
Setup	Test Selection	Global Setti	ngs				Edito		
Status	I	Instruments E	etected						
Besulte	<ul> <li>Acquisitions</li> </ul>	RF Switch		Dor	iot use		Instrur Cont	nent rol	
Results		Real Time Sc	ope	DPO	73304D ( GPIB	3::1::INSTR )	Setti	nas	
Reports	4 Configuration	Signal Source	e for DUT Automatio	AWO	57122C ( GPIB1	::2::INSTR )	Manual 1	oggle	
Kepona							Set		
	5 Preferences	🔽 Automat	ed DUT Control	Setup					
			Record Length		Sample Rate		Bandwidth	_	
			2.5		25	GS/s	6 GHz	<b>v</b>	
			10		50		12.5 GHz	•	
			<b>10</b> M		50		16 GHz	•	
			12.5		100		25 GHz	•	
		Sig Validatio	on Threshold	200	тV	Trigger Type (Gen3/Gen4)	Auto	•	
		Sigtest Con	figuration up						

Figure 35 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Configuration

9. Click on SigTest configuration 'Setup' and observe the SigTest version and templates used for this test.

exe Configura	tion
Gen 4 : (Signal Test)	C:\Program Files (x86)\SigTest_4.0.42\SigTest.ex  Browse
Gen 4 : (Preset Test)	C:\Program Files (x86)\SigTest_4.0.42\SigTest.ex
Template Con	figuration
16 GB/s :	1.42'templates\PCIE_4_0_CARD\PCIe_4_16G_CEM.dat Browse
16 GB/s : (PWJ Test)	2'templates\PCIE_4_0_CARD\PCIE_4_16GB_BASE.dat

Figure 36 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test SigTest Configuration



10. Click on **to run the test**.

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- 11. Make the connection as per <u>section#3.6 (Figure 6 Tx Preset / Pulse Width Jitter Test</u> <u>for Add-In-Card – DUT Toggle Automation</u>) and verify that it as per the connection diagram that is prompted by application up during the run, Power ON the DUT and click OK to continue.
- 12. Observe that the DUT will be toggled automatically from Gen1 to the 16 GT/s Jitter Measurement Pattern (Lanes 0/8/16/24 setting #27 in the 4.0 PCIe Base Specification) and will start the acquisition, observe that Package model is NOT embedded on the scope and the three waveforms of the Jitter Measurement Pattern are saved.



Figure 37 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test NO Package Model Applied

13. After acquiring all waveforms, they will be post-processed with SigTest. The Template File Technology Folder: PCIE\_4\_0\_CARD and Template File Name: PCIe\_4\_16GB\_BASE.dat

Test Status Log View		
	Message History	
Signal Test 4.0.42		*
Data Type 🗘 Differential		
Data File K:\PCI Express\Tek_Ge	en4_AIC_PWJ_MOI\DUT001\20190117_1 Browse	
Data File Neg	Browse	
Clock File	Browse	
Clock File Neg	Browse	
Load and Verify Data File	Select Preset Test 💌	
Technology		
PCIE_3_0_CARD	App Settings and Debug Mode	
C:\Program Files (x86)\SigTest_4.0.42\temp		
Sample Interval 10.000 ps	Lest	
Number of Unit Intervals In Fre	Exit	
Worst Non Worst Jitter Transition Eyes Transition Eyes Histogram	CDR Results PDF Data Plot	-
		,
Auto Scroll	Clearlog	Save

Figure 38 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test SigTest Analysis

14. Observe the test results in TekExpress Results panel and once all the results are updated a test report will be generated.

🌾 TekExpr	ress PCI Express - (Untitled)*	Options	
	Test Status Log View		Start
Setup	Message History		
Status Results Reports	01/17/1910.42.20 : Executing Trigger 01/17/1910.42.21 : Current waveform acquisition DataClock Gen4 R1 01/17/1910.42.23 : Auto Trigger mode switching Width to Edge Trigger 01/17/1910.42.23 : Cite Saring completed. 01/17/1910.42.33 : Cite saring completed. 01/17/1910.42.33 : Cite saring completed. 01/17/1910.42.34 : Cite saring completed. 01/17/1910.42.44 : File saring completed. 01/17/1910.42.45 : Comparing completed. 01/17/1910.42.45 : Complexity and		Pause
	Auto Scroll	Save	
	Completed.		

Figure 39 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Status

Description         Details         Generation         Pass/Fail         Value         Margin           C Lane0         Uncorrelated PWJ TJ@E- 212 Gen4         Uncorrelated 16Gbps PWJ TJ@E- 12 R1         Informative Data Clock         8.344 ps         N.A           Uncorrelated PWJ TJ@E- 12 R0         Uncorrelated 16Gbps PWJ TJ@E- 12 R0         Informative Data Clock         8.002 ps         N.A           Uncorrelated PWJ TJ@E- 12 R3         Uncorrelated 16Gbps PWJ TJ@E- 12 R3         Informative PWJ TJ@E- 12 R3         8.159 ps         N.A           Uncorrelated PWJ TJ@E- 12 R3         Uncorrelated 16Gbps PWJ TJ@E- Data Clock         Informative PWJ TJ@E- 12 R3         8.168 ps         H.4.332ps
Image: Second
Uncorrelated PWJ TJ@E-
Uncorrelated PWJ TJ@E- PWJ TJ@E- Uncorrelated PWJ TJ
Uncorrelated PWJ TJ@E- Uncorrelated 16Gbps Q Pass 8.168 ps H:4.332ps
Uncorrelated PWJ TJ@E- Uncorrelated 16Gbps 📀 Pass 8.168 ps H:4.332ps
12 Gen4     PWU 1/02E- Data Clock     12 Mean of     3 Acquisition

Figure 40 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Results

J95.pdf - Adobe Reader								
view Window Help	2							
🍐 📝 🚳			1 / 1 108	3% -		8	Tools	Sign Con
Tole			TekExp	ress PC	I Express			
IGXII			Add-I	n-Card Tes	t Report			
Setup Informatio	n							
DUTID		DUT001		DPC	JET Version	1	10.0.8.179	
Date/Time		2019-01-17 1	10:38:28	Soc	pe Model		DP073304D	
Device Type		CEM		Soc	pe Serial Number	1	B241041	
TeleTowney May		PCI Express	3:10.4.5.26 (DAJLY)	SPC	, FactoryCalibration	1	PASS;PASS	
IERCAPIESS VERO	ion	Framework:	4.9.0.5	Scc	pe F/W Version	1	10.8.3 Build 3	
Test Mode		SigTest Con	pliance	Pro	Je1 Model	1	TCA292D	
Spec Version		Gen4 - 4.0		Pro	e1 Serial Number	1	NA	
SigTest Version		3.2.0.3(Gen*	.1,2,3) 4.0.42 (Gen4)	-Signal Prof	xe2 Model		TCA292D	
orginal factor		Tests 4.0.42	4.0.42 (Gen4)-Preset Tests Probe2 Serial Number		/	N/A		
Slot Number		01		Pro	xe3 Model	1	TCA292D	
Overall Execution	a Time	0:05:06	J5:06 Probe3 Serial Number		/	N/A		
Overall Test Rest	jit	Pass		Prof	xe4 Model	1	TCA292D	
			Probe4 Serial Number		NA			
				Sig	al Source Model		AWG7122C	
				Sigr	al Source Serial Num	iber /	8050012	
DUT COMMENT:	DUT001							
Test Name Sum	mary Table			-				
Lincorrelated PV	UTV@E-12 Gen4							
Old Shaness	o tolger te same							
Uncorrelated PW	UTJ@E-12 Gen4					4		
Measurement Details	Lane Name	Data Rate	Equalization	Measured Val	ue Test Result	Margin	Low Limit	High Limit
Uncorrelated PWJ TJ@E-12	Lane0	16Gbps	DataClock Gen4	8.344 ps	Informative	NA	NA	NA
Uncorrelated								
PWJ TJ@E-12 R2	Lane0	16Gbps	DataClock Gen4	8.002 ps	Informative	NA	NA	NA
Uncorrelated PWJ TJ@E-12 R3	Lane0	16Gbps	DataClock Gen4	8.159 ps	Informative	NA	NA	NA
Uncorrelated PWLTJ/@E-12	Lane0	16Gbps	DataClock Gen4	8.168 ps	Pass	H:4.332ps	NA	12.5
Mean of 3 Acquisition				1 1				

Figure 41 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Report

15.Once test report is generated you can save the Test Session in TekExpress, Options → Save Test Setup → Tek\_Gen4\_AIC\_PWJ\_MOI (Example of session name). The saved data can be found in the location X:\PCI Express\Tek\_Gen4\_AIC\_PWJ\_MOI\DUT001.

V TekExpress PCI Express - (Tek_Gen4_AIC_PWJ_MOI)	Options 🔽 🌥 🗕 🗵
Computer → Local Disk (X:) → PCI Express → Tek_Gen4_AIC_PWJ_MOI → DUT001 →	Search DUT001 🔎
Organize  Include in library  Share with  Burn New folder	:= - 🔟 🔞
Figure 42 TekExpress PCI Express Add-In-Card Pulse Width Jitter Test Session	ı Saved

## 4.4 System-Board Transmitter Signal Quality Test for 16 GT/s

This is referred as "System Board Transmitter Electrical Compliance Test for 16.0 GT/s" in *PCI Express*® *Architecture PHY Test Specification Revision 4.0.* This test is run on all card electromechanical form factor system boards. This test verifies the Tx signal of the system at 16 GT/s meets the minimum eye diagram requirements with at least one Tx equalization preset.

- 1. Power down the system under test and insert the compliance base board (CLB) 4.0 into the slot for test.
- 2. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
- 3. Launch TekExpress PCI Express Application from TekScope  $\rightarrow$  Analyze menu.
- 4. Select the configuration in the application as per the figure below.

🧭 TekExpress PCI Express - (	Untitled)*	Options 💽 🗂 🗕 🙁
Setup 1 DUT 2 Test Selection 3 Acquisitions	DUT ID DUT001 Slot Number O Acquire live waveforms Use pre-recorded waveform files SigTest Mode Compliance Specification Device Type Version CEM System-Board Gen4 - 4.0	D1 Start Pause
Reports 4 Configuration	Device Profile	
5 Preferences	Data Rates       Transmitter Equalization       Link Analysis         2.5 Gb/s       Setup         5 Gb/s       Setup         4 G Gb/s       Presets         5 Gb/s       Setup         6 Gb/s       Presets         5 Gb/s       Setup         6 Gb/s       On         6 Gb/s       On         6 Gb/s       Presets         7 G Gb/s       Meas Limits         6 G Gb/s       On         6 G Gb/s       Off         6 G Gb/s       Setup         6 G Gb/s       Off         7 G G Gb/s       Setup         6 G Gb/s       Off         7 G G Gb/s       Setup         6 G G G G G G G G G G G G G G G G G G G	etup s
Ready.		

Figure 43 TekExpress PCI Express System-Board Signal Quality Test

5. Go to Test Selection panel and make sure all the tests are checked under the 16Gbps tree node in 'Signal Test'.

TekExpress PCI Express - (	(Untitled)*		Options	
Setup DUT	CEM : System-Board : Gen4 - 4.0 Signal Test Gen4 Preset Test	select Al	Select All	Start
Status Results Reports Configuration 5 Preferences	16Gbps     Junit Interval Gen4     Mask Hits(All Bits) Gen4     Gromposit Eye Height Gen4     Transition Eye Diagram Gen4     Mon Transition Eye Diagram Gen4     Min Eye Width Gen4     Junit Time Between Crossovers Gen4     Junit Cen4     Junit Gen4     Junit Gen4     Peak to Peak Jitter Gen4     V Extrapolated Eye Height Gen4			Pause
Combined	Test Description Please select a test name to view its description	Show MOI	Schematic	

Figure 44 TekExpress PCI Express System-Board Signal Quality Test Selection

6. Go to Acquisition panel and set the source of Lane0 DATA to CH1 and CLOCK to CH3. We are using P7625 TriMode probe with tip P76CA-292C for DATA and P7313-SMA-Differential probe for CLOCK. Set the No of Acquisitions to '3' as we need to capture three 2.0M UI (Gen4 Compliance Pattern) differential waveforms for every Tx EQ Preset.

V TekExpress PCI Express	(Untitled)*	Options 🔽 🔿 🔾
	CEM : System-Board : Gen4 - 4.0 Lanes:0	Refresh View Probes
Status Test Selection	Lane         Source           Data1         CH1	Damas
Reports 3 Acquisitions 4 Configuration 5 Preferences	Acquisition Lane0: 166bps P0 Acquisition Lane0: 166bps P02 Acquisition Lane0: 166bps P03 Acquisition Lane0: 166bps P03 Acquisition Lane0: 166bps P06 Acquisition Lane0: 166bps P06 Acquisition Lane0: 166bps P07 Acquisition Lane0: 166bps P07 Acquisition	
Featy	Lane0 : 186bps P09 Acquisition Lane0 : 186bps P10 Acquisition Acquire Options Acquire All Waveforms Before Analysis Acquire Only - Do Not Analyze Save Options Save Only Analyzed Waveform	No. OfAcquisitions (Gen4)

Figure 45 TekExpress PCI Express System-Board Signal Quality Test Acquisitions

- 7. For the Tx Signal Quality Test for System-Board in automated procedure we are using TekExpress PCI Express with automated DUT toggle option using AWG7122C. User can use AFG/AWG/GRL PCIE Controller for automated DUT toggle option. Refer the <u>'Appendix Section#5.3.4'</u> for manual DUT toggle option.
- 8. Go to Configuration panel and select the 'Signal Source for DUT Automation' [AWG7122 in this case] and select the check box 'Automated DUT Control'.

	SigTest Mo	ode 💿 Comp	liance (	User Define	ed	Limit	
Test Selection	Global Sett	ings					
	Instruments	Detected					
Acquisitions	RF Switch		D	o not use		Instrur Cont	nent rol (
	Real Time S	tope	D	PO73304D ( GP1	B8::1::INSTR )	Setti	ngs
4 Configuration	Signal Sourc	e for DUT Automa	ation A	WG7122C ( GPI	B1::2::INSTR)	Manual 1	loggle
						Set	
5 Preferences	🗸 Automa	ited DUT Contro	Setup				
		Record Length		Sample Rate	e	Bandwidth	
		2.5		25		6 GHz	v
		10	М	50		12.5 GHz	Y
		10		50		16 GHz	T
		12.5		100		25 GHz	Y
	Sig Validati	on Threshold	200	mV	Trigger Type (Gen3/Gen4)	Auto	•
	Sigtest Co	nfiguration					
			_				

Figure 46 TekExpress PCI Express System-Board Signal Quality Test Configuration

9. Click on SigTest configuration 'Setup' and observe the SigTest version and templates used for this test.

Gen 4 : (Signal Test)	C:\Program Files (x86)\SigTest 4.0.45\SigTest.exe Browse
Gen 4 : (Preset Test)	C:\Program Files (x86)\SigTest 4.0.45\SigTest.exe Browse
emplate Cor	figuration
16 GB/s :	PCIE_4_0_SYS\PCIE_4_16GB_CEM_DUAL_PORT.dat Browse

Figure 47 TekExpress PCI Express System-Board Signal Quality Test SigTest Configuration



- 10. Click on **to run the test**.
- 11. Make the connection as per <u>section#3.7 (Figure 7 Signal Quality Test for System-Board DUT Toggle Automation)</u> and verify that it as per the connection diagram that is prompted by application up during the run, Power ON the DUT and click OK to continue.
- 12. Observe that the DUT will be toggled automatically from Gen1 to Gen4 Preset P0 And will start acquisition, observe that Package model embedded on the scope (refpkg\_endpoint\_3db\_thru.s4p) gets applied and three waveforms of each preset are saved.



Figure 48 TekExpress PCI Express System-Board Signal Quality Test applying package model

13. All acquired waveforms will be processed with SigTest using the "PCIE\_4\_16GB\_CEM\_DUAL\_PORT.dat" template file which performs CTLE optimization. If all Tx EQ presets fail with this approach, you can configure the SigTest Setup (step #9) to run each CTLE individually using the "PCIE\_4\_16GB\_CEM\_DUAL\_PORT\_CTLE\_6dB.dat through PCIE\_4\_16GB\_CEM\_DUAL\_PORT\_CTLE\_12dB.dat" template files. A passing result with either case is allowed per the PCI Express Architecture PHY Test specification.

press PCI Express - (Untitled)"	Options 💌
Test Status Log View	
Message History	
🕎 Signal Test 4.0.45 👘 💼	× ^
Data Type Dual Port Differential	
Data File S:\\Package_DUT001_16G_S01_Ln00_P0_d_Diff_R3.wfm Brow	se
Data File Neg	se
Clock File S:\\DUT001_16G_S01_Ln00_P0_d_clk_R3.wfm Brow	se
Clock File Neg	se
Load and Verify Data Files Select Preset Test ▼	
Technology	
PCIE_3_0_CARD	
C:\Program Files (x86)\SigTest 4.0.45\templat	
Sample Interval 20.000 ps	
Number of Unit	
Intervals in File	
Worst Non Worst Jitter CDR Results PDF Q5pace Filt Transition Eyes Transition Eyes Histogram Adapt Pi	er 💌
Auto Scroll Clear	.og Save

Figure 49 TekExpress PCI Express System-Board Signal Quality Test SigTest Analysis

14. Observe the test results in TekExpress Results panel and once all the results are updated a test report will be generated.

🌾 TekExp	ress PCI Express - (Untitled)*	Options	
	Test Status Log View		Start
Setup	Message History		
Status Results Reports	1204/13 01:15:00         Compare limit 0.000 > 0 - 0 - Result Pass           1204/13 01:15:00         Magnin dresults in 1:0000 pe           1204/13 01:15:00         Hogin dresults in 1:000 pe           1204/13 01:15:00         Hogin dresults in 1:000 pe           1204/13 01:15:00         Hogin dresults in 1:000 pe           1204/13 01:15:01         Hoginal pesults for 10_et E-12 Gen4           1204/13 01:15:01         Hoginal pesults for 10_et Hoginal pesults for 1600 Pesults for 170 Pesults for 1600 Pesults for 1600 Pesults for 1600 Pesults for 170	*	Pause
	<	>	
	Auto Scroll Clear Log	Save	
	Completed.		

Figure 50 TekExpress PCI Express System-Board Signal Quality Test Status

) s	ignal Tests Gen4 Preset Test					Preferences
	escription	Details	Generation	Pass/Fail	Value	Margin
	J Lane0					<u> </u>
	+ Unit Interval Gen4	Mean Unit Interval R1	16Gbps P04	Informative	62.500 ps	N.A 😑
	Mask Hits(All Bits) Gen4	Mask Hits R1	16Gbps P04	Informative	Result Unavailable	N.A
	Composit Eye Height Gen4	Composit Eye Height R1	16Gbps P04	Informative	Result Unavailable	N.A
	Transition Eye Diagram	Min Transition Eye Height R1	16Gbps P04	Informative	72.077 mV	N.A
	Transition Eye Diagram Gen4	Min Transition Voltage R1	16Gbps P04	Informative	-162.771 mV	N.A
	Transition Eye Diagram	Max Transition Voltage R1	16Gbps P04	Informative	161.845 mV	N.A
	Transition Eye Diagram	Min Transition Top Margin R1	16Gbps P04	Informative	14.574 mV	N.A
	Transition Eye Diagram ⊕ Gen4	Min Transition Bottom Margin R1	16Gbps P04	Informative	-11.503 mV	N.A
	Transition Eye Diagram Gen4	Transition Eye Mask	16Gbps P04	Informative	Result Unavailable	N.A

Figure 51 TekExpress PCI Express System-Board Signal Quality Test Results

aw Window Help											
in million rep											
🎯 🏟 🗒 🖶 🖂 🌘 🖲	) 1 / 5   😑	100%	-   🗄 🛙	3   🔛 🐶	at a start					Tools Sigr	Commen
	Tol			TekExpre	ss PCI	Express					
	IGNI			System-	Roard Tes	t Report					
	Setup Information	1	I pumper		L ppp a	Thissian					
	Date/Terra		2010/01	05-13-62	DP00	ET Version		0.0.8.179			
	Davies Taxe		201902-04	01.13.02	Scope	Control Management		000008			
	Device type		PCI Exman	e-10.4.5.32	SPC I	Sena Number		ATUNCAL			
	TekExpress Vers	ion	Framework	4.9.0.5	Scope	F/W Version	1	0.9.1 Build 16			
	Test Mode		SigTest Use	er Defined	Probe	Model	1	CA-SMA			
	Spec Version		Gen4 - 4.0		Probes	2 Model	1	CA292D			
	SigTest Version		3.2.0.3(Gen	1,2,3) 4.0.45 (Gen4)-Si	nal Probel	2 Serial Number	N	7A			
	Clot Mumber		16515 4.0.40	5 (Gen4) Meset lests	Probe	3 Model	N	ίΑ.			
	Overall Execution	Time	0:01:17		Probec	3 Serial Number	N	7A			
	Overall Test Res	it.	Pass		Probe	Model	N	TA			
		a.	11000		Probe	Senal Number	N	IA			
	Composit Eye H Transition Eye D Non Transition E Min Eye Width G Min Time Betwee TJ 20 E-12 Con4 D, dd Gen4 RU(RMS) Gen4 Peak to Peak JE Estimaticat Exercisi	ischt Gent lagram Gent inn inn Crossovers Gen inn Crossovers Gen inn Gent ist Gent ist Gent	1								
	Unit Interval Gen	4									
	Measurement Dotails	Lane Name	Data Rate	Equalization N	leasured Value	Test Result	Margin	LowLimit	High Limit		
	Mean Unit Interval R1	Lane0	16Gbps	P04 Gen4 6	2.500 ps	Informative	NA	NA	NA		
	Mean Unit Interval R2	Lane0	16Gbps	P04 Gen4 6	2.500 ps	Informative	NA	NA	NA		
	Mexan Unit	Lane0	16Gbps	P04 Gen4 6	2.500 ps	Informative	NA	NA	NA		
	Interval R3										

Figure 52 TekExpress PCI Express System-Board Signal Quality Test Report

15.Once test report is generated you can save the Test Session in TekExpress, Options → Save Test Setup → Tek\_Gen4\_SYS\_SQ\_MOI (Example of session name). The saved data can be found in the location X:\PCI Express\Tek\_Gen4\_SYS\_SQ\_MOI\DUT001.



Figure 53 TekExpress PCI Express System-Board Signal Quality Test Session Saved

## 4.5 System-Board Transmitter Preset Test for 16 GT/s

This is referred as "System Board Transmitter Preset Test for 16.0 GT/s" in *PCI Express*® *Architecture PHY Test Specification Revision 4.0*. This test is run on all card electromechanical form factor system boards that operate at 16.0 GT/s. The test verifies that the system board produces the correct transmitter equalization values for each preset in the set of 11 presets.

- 1. Power down the system under test and insert the compliance base board (CLB) 4.0 into the slot for test.
- 2. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
- 3. Launch TekExpress PCI Express Application from TekScope  $\rightarrow$  Analyze menu.
- 4. Select the configuration in the application as per the figure below.

Setup 1 DUT DUT ID DUT 001 Image: Start	🥳 TekExpress PCI Express 🕞	(Untitled)*	Options 🔽 🗂 🖵 🖉
Multi-Lane Automated DUT Control Setup Selected Lanes Signal Validation	TekExpress PCI Express -       Setup     1     DUT       Status     2     Test Selection       3     Acquisitions       4     Configuration       5     Preferences	(Untitle d)*         DUT ID       DUT001       Image: Start Number of Start Number	Options   Start  Pause  Setup

Figure 54 TekExpress PCI Express System-Board Preset Test

5. Go to Test Selection panel and make sure all the tests are un-checked under 16Gbps tree node in 'Signal Test' tab by clicking on 'Deselect All' button. Go to 'Gen4 Preset Test' tab and click on 'Select All' button.

TekExpress PCI Expre	ess - (Untitled)*	Options 💽 🗂 🗕 🗶
Setup DUT	CEM : System-Board : Gen4 - 4.0 Signal Test Gen4 Preset Test	Select All
Results Reports S Preferences	s s n s n s n s n s n s n s n s n s n s	Pause
	Test Description Please select a test name to view its description	Of Schematic
Completed.		

Figure 55 TekExpress PCI Express System-Board Preset Test Selection 1

🗸 TekExp	ress PCI Express -	(Untitled)				Opti	ons 💽 管	
Setup	DUT	CEM : Sys	tem-Board : Gen4 est Gen4 Preset Tes	m4 - 4.0 st	Deselect A	Select All		Start
Status	<u> </u>		Preset	Preshoot	Deemphasis	Dependencies	Р	
	3 Acquisitions	▶ ✓	PO	0.0 dB	-6.0 dB	P04		
Results	<b>Y</b>	~	P01	0.0 dB	-3.5 dB	P04		
	Configuration		P02	0.0 dB	-4.4 dB	P04		
Reports	- Conliguration		P03	0.0 dB	-2.5 dB	P04		
			P04	0.0 dB	0.0 dB	-		
	5 Preferences		P05	1.9 dB	0.0 dB	P04		
			P06	2.5 dB	0.0 dB	P04		
			P07	3.5 dB	-6.0 dB	P05,P02		
			P08	3.5 dB	-3.5 dB	P06,P03		
			P09	3.5 dB	0.0 dB	P04		
		✓	P10	0.0 dB	-9.5 dB	P04		
		Lanes Selected L0	Lanes		Show	MOI) Schematic		
	Ready.							

Figure 56 TekExpress PCI Express System-Board Preset Test Selection 2

6. Go to Acquisition panel and set the source of Lane0 DATA to CH1 and CLOCK to CH3. We are using P7625 TriMode probe with tip P76CA-292C for DATA and P7313-SMA-Differential probe for CLOCK, to capture 2.0M UI (Gen4 Compliance Pattern) differential waveforms for every Tx EQ Preset.

Note: We will not capture and save the CLOCK signal for this test, but the physical connection to the scope is required.

Setup	DUT	CEM : Sy Lanes:0	stem-Board :	Gen4 - 4.0		Refresh View Probes	
	Test Selection	Lane	Source	Lane	Source		
Status		Data1	CH1	Clock	CH3		Bour
	Acquisitions	-					Pau
Results	Acquisitions	Acqui	sition				
		▶ Lane0	: 16Gbps P0 /	Acquisition			
Reports 4	Configuration	LaneO	: 16Gbps P01	Acquisition			
	L .	LaneO	: 16Gbps P02	Acquisition			
5	Preferences	LaneO	: 16Gbps P03	Acquisition			
		LaneO	: 16Gbps P04	Acquisition			
		LaneO	: 16Gbps P05	Acquisition			
		Lane0	: 16Gbps P06	Acquisition			
		Lane0	: 16Gbps P07	Acquisition			
		LaneO	: 16Gbps P08	Acquisition			
		LaneO	: 16Gbps P09	Acquisition			
		Lane0	:16Gbps P10	Acquisition			
		Acquire O	ntions			No. Of Acquisitions (Gen4)	
			e All Waveforr	ms Before Ana	lysis		
		Acquir	e Only - Do No	ot Analyze		3	
		Roup Onti	- 				
		Save Opti	uns			-	
		Save Or	ily Analyzed	Waveform		▼	

Figure 57 TekExpress PCI Express System-Board Preset Test Acquisitions

- 7. For the Tx Preset Test for System-Board in automated procedure we are using TekExpress PCI Express with automated DUT toggle option using AWG7122C. User can use AFG/AWG/GRL PCIE Controller for automated DUT toggle option. Refer the <u>'Appendix Section#5.3.5'</u> for manual DUT toggle option.
- 8. Go to Configuration panel and select the 'Signal Source for DUT Automation' [AWG7122 in this case] and select the check box 'Automated DUT Control'.



Figure 58 TekExpress PCI Express System-Board Preset Test Configuration

9. Click on SigTest configuration 'Setup' and observe the SigTest version used for this test.



Figure 59 TekExpress PCI Express System-Board Preset Test SigTest Configuration



- 10. Click on **to** run the test.
- 11. Make the connection as per <u>section#3.8 (Figure 8 Tx Preset Test for System-Board</u> <u>– DUT Toggle Automation)</u> and verify that it as per the connection diagram that is prompted by application up during the run, Power ON the DUT and click OK to continue
- 12. Observe that the DUT will be toggled automatically from Gen1 to Gen4 Preset P0 And will start acquisition, observe that Package model embedded on the scope (refpkg\_endpoint\_3db\_thru.s4p) is not applied and waveform of each preset is saved.



Figure 60 TekExpress PCI Express System-Board Preset Test NO Package Model applied



13. After acquiring the waveforms will be post-processed with SigTest.

Figure 61 TekExpress PCI Express System-Board Preset Test SigTest Analysis

14. Observe the test results in TekExpress Results panel and once all the results are updated a test report will be generated.

Setup       Test Status       Log view       Message History         Status       01/17/1915/2841 : PreShoot: 2219 dB       01/17/1915/2842 : PreShoot: 2219 dB       Press         01/17/1915/2842 : PreShoot: 2219 dB       01/17/1915/2842 : PreShoot: 2248 dB       01/17/1915/2843 : PreShoot: 2348 dB       01/17/1915/2843 : PreShoot: 3248 dB       01/17/1915/2843 : PreShoot: 3248 dB       01/17/1915/2843 : PreShoot: 3248 dB       01/17/1915/2844 : PreShoot: 3283 dB       01/17/1915/2844 : PreShoot: 3280 dB       01/17/1915/2844 : PreShoot: 3280 dB	🚀 TekExpi	ress PCI Express - (Untitled)*	Options	
Setup       Message History         Status       0/17/19 15:28.41 : Populating results for preset :P06 Ger4         0/17/19 15:28.41 : PreShoot : 2.213 dB       0/17/19 15:28.42 : DeEmphasis : 0.00 dB         0/17/19 15:28.42 : Pass/Fail Result : Pass       0/17/19 15:28.42 : Pass/Fail Result : Pass         0/17/19 15:28.42 : Pass/Fail Result : Pass       0/17/19 15:28.42 : Pass/Fail Result : Pass         0/17/19 15:28.42 : Pass/Fail Result : Pass       0/17/19 15:28.43 : Pass/Fail Result : Pass         0/17/19 15:28.43 : Pass/Fail Result : Pass       0/17/19 15:28.43 : Pass/Fail Result : Pass         0/17/19 15:28.43 : Pass/Fail Result : Pass       0/17/19 15:28.43 : Pass/Fail Result : Pass         0/17/19 15:28.44 : Pass/Fail Result : Pass       0/17/19 15:28.44 : Pass/Fail Result : Pass         0/17/19 15:28.44 : Pass/Fail Result : Pass       0/17/19 15:28.44 : Pass/Fail Result : Pass         0/17/19 15:28.44 : Pass/Fail Result : Pass       0/17/19 15:28.45 : Pass/Fail Result : Pass         0/17/19 15:28.45 : Pass/Fail Result : Pass       0/17/19 15:28.45 : Pass/Fail Result : Pass         0/17/19 15:28.45 : Pass/Fail Result : Pass       0/17/19 15:28.45 : Pass/Fail Result : Pass         0/17/19 15:28.45 : Pass/Fail Result : Pass       0/17/19 15:28.45 : Pass/Fail Result : Pass         0/17/19 15:28.45 : Pass/Fail Result : Pass       0/17/19 15:28.45 : Pass/Fail Result : Pass         0/17/19 15:28.45 : Pass/Fail Result : Pass       0/17/19 15:28.45 : Pass		Test Status Log View		Start
Status       01/17/19 15.28.41 : Propulating results for preset : P06 Gen4       Image: Status       Im	Setup	Message History		
	Status Results Reports	01/17/19 15:28.41 : Populating results for preset :P06 Gen4 01/17/19 15:28.42 : Def mpdssis : 0.000 dB 01/17/19 15:28.42 : Postphasis : 0.000 dB 01/17/19 15:28.42 : Postphasis : 0.000 dB 01/17/19 15:28.42 : Postphasis : -0.000 dB 01/17/19 15:28.42 : Postphasis : -0.867 dB 01/17/19 15:28.43 : Def mpdssis : -0.867 dB 01/17/19 15:28.43 : Def mpdssis : -0.867 dB 01/17/19 15:28.43 : Postphasis : -0.987 dB 01/17/19 15:28.44 : Postphasis : -0.000 dB 01/17/19 15:28.45 : Postphasis : -0.000 dB 01/17/19 15:28.45 : Postphasis : -0.010 dB 01/17/19 15:28.45 : Postphasis : -0.010 dB 01/17/19 15:28.45 : Postphasis : -0.010 dB 01/17/19 15:28.45 : Postphasis : -0.615 dB 01/17/19 15:28.46 : Postphasis : -0.615 dB 01/17/19 15:28.48 : SigT est analysis is in progress, result will be updated after analysis 01/17/19 15:28.48 : SigT est analysis is in progress, result will be updated after analysis 01/17/19 15:28.45 : Postphase : -0.615 dB 01/17/19 15:28.48 : SigT est analysis is in progress, result will be updated after analysis 01/17/19 15:28.45 : Postphase : -0.615 dB 01/17/19 15:28.45 : Postphase : -0.615 dB 01/17/19 15:28.45 : Postphase : -0.615 dB 01/17/19 15:28.45 : : Test execution completed.	E Save	Pause

Figure 62 TekExpress PCI Express System-Board Preset Test Status

Preset         Pass/Fail         Vb         PreShoot         DeEmphasis           • Lane0         •
Cane0         PO Gen4         Pass         493.259 mV         0.000 dB         -6.073 dB           G PO1 Gen4         Pass         641.442 mV         0.000 dB         -3.792 dB           G PO1 Gen4         Pass         561.442 mV         0.000 dB         -4.586 dB           G PO3 Gen4         Pass         729.709 mV         0.000 dB         -2.672 dB           G PO3 Gen4         Pass         729.709 mV         0.000 dB         -2.672 dB           G PO4 Gen4         Pass         925.056 mV         0.000 dB         -2.672 dB           G PO4 Gen4         Pass         922.505 mV         0.000 dB         0.000 dB           G PO5 Gen4         Pass         728.728 mV         1.566 dB         0.000 dB           G PO5 Gen4         Pass         728.72 mV         2.19 dB         0.000 dB           G PO7 Gen4         Pass         788.782 mV         2.19 dB         0.000 dB           G PO8 Gen4         Pass         487.819 mV         3.489 dB         -3.951 dB           G PO8 Gen4         Pass         680.127 mV         3.283 dB         0.000 dB           G P08 Gen4         Pass         328.073 mV         0.000 dB         -8.615 dB
9 P0 Gen4         Pass         493.259 mV         0.000 dB         -6.073 dB           9 P01 Gen4         Pass         641.442 mV         0.000 dB         -3.792 dB           9 P02 Gen4         Pass         658.402 mV         0.000 dB         -4.586 dB           9 P03 Gen4         Pass         729.708 mV         0.000 dB         -2.672 dB           9 P04 Gen4         Pass         925.055 mV         0.000 dB         0.000 dB           9 P05 Gen4         Pass         926.205 mV         0.000 dB         0.000 dB           9 P05 Gen4         Pass         926.705 mV         1.666 dB         0.000 dB           9 P05 Gen4         Pass         728.708 mV         2.219 dB         0.000 dB           9 P05 Gen4         Pass         748.762 mV         2.219 dB         0.000 dB           9 P05 Gen4         Pass         421.771 mV         2.248 dB         -5.867 dB           9 P05 Gen4         Pass         421.771 mV         3.283 dB         -3.951 dB           9 P05 Gen4         Pass         680.127 mV         3.283 dB         -3.851 dB           9 P05 Gen4         Pass         680.127 mV         3.283 dB         0.000 dB         -9.615 dB
9 P01 Gen4         Ø Pass         641.442 mV         0.000 dB         -3.792 dB           10 P02 Gen4         Ø Pass         565.402 mV         0.000 dB         -4.556 dB           10 P03 Gen4         Ø Pass         729.703 mV         0.000 dB         -2.672 dB           10 P03 Gen4         Ø Pass         925.505 mV         0.000 dB         0.000 dB         0.000 dB           10 P05 Gen4         Ø Pass         923.505 mV         0.000 dB         0.000 dB         0.000 dB           10 P05 Gen4         Ø Pass         828.792 mV         1.566 dB         0.000 dB         0.000 dB           10 P05 Gen4         Ø Pass         788.762 mV         2.110 dB         0.000 dB         0.000 dB           10 P05 Gen4         Ø Pass         421.711 mV         2.848 dB         -5.667 dB         0.000 dB           10 P05 Gen4         Ø Pass         487.819 mV         3.283 dB         0.000 dB         -3.951 dB           10 P05 Gen4         Ø Pass         580.127 mV         3.283 dB         0.000 dB         -9.615 dB           10 P05 Gen4         Ø Pass         328.073 mV         0.000 dB         -9.615 dB
• P02 Gen4               • Pass          585 402 mV          0.000 dB          -4.586 dB                 • P03 Gen4               • Pass          728 708 mV          0.000 dB          -2.672 dB                 • P04 Gen4               • Pass          925.055 mV          0.000 dB          -2.672 dB                 • P04 Gen4               • Pass          925.055 mV          0.000 dB          0.000 dB                 • P05 Gen4               • Pass          787.762 mV          1.566 dB          0.000 dB                 • P05 Gen4               • Pass          787.771 mV          2.219 dB          0.000 dB                 • P05 Gen4               • Pass          421.771 mV          3.498 dB          -3.951 dB                 • P05 Gen4               • Pass          680.127 mV          3.283 dB          0.000 dB                 • P10 Gen4                • P10 Gen4                • P10 Gen4                • Pass
9         P03 Gen4         Pass         729.708 mV         0.000 dB         -2.672 dB           9         P04 Gen4         Pass         992.505 mV         0.000 dB         0.000 dB           9         P05 Gen4         Pass         928.726 mV         1.666 dB         0.000 dB           9         P05 Gen4         Pass         768.762 mV         2.219 dB         0.000 dB           9         P07 Gen4         Pass         421.771 mV         2.248 dB         -5.867 dB           9         P03 Gen4         Pass         421.771 mV         3.486 dB         -3.951 dB           9         P03 Gen4         Pass         680.127 mV         3.283 dB         0.000 dB           9         P03 Gen4         Pass         580.127 mV         3.283 dB         0.000 dB           9         P10 Gen4         Pass         328.073 mV         0.000 dB         -8.615 dB
9 P04 Gen4         9 Pass         992.505 mV         0.000 dB         0.000 dB           9 P05 Gen4         9 Pass         928.792 mV         1.566 dB         0.000 dB           9 P05 Gen4         9 Pass         768.762 mV         2.116 dB         0.000 dB           9 P07 Gen4         9 Pass         421.771 mV         2.446 dB         -5.867 dB           9 P08 Gen4         9 Pass         421.771 mV         2.446 dB         -5.867 dB           10 P08 Gen4         9 Pass         421.771 mV         2.486 dB         -5.867 dB           10 P08 Gen4         9 Pass         487.819 mV         3.286 dB         -3.961 dB           10 P08 Gen4         9 Pass         487.819 mV         3.286 dB         0.000 dB           10 P08 Gen4         9 Pass         328.073 mV         0.000 dB         -9.615 dB
IP 05 Gen4         Image: Second
• P06 Gen4               • Pass          768.762 mV          2.219 dB          0.000 dB                 • P06 Gen4               • Pass          421.771 mV          2.284 dB          -5.867 dB                 • P03 Gen4               • Pass          421.771 mV          3.488 dB          -3.951 dB                 • P03 Gen4               • Pass          680.127 mV          3.488 dB          -3.951 dB                 • P03 Gen4               • Pass          680.127 mV          3.283 dB          0.000 dB                 • P10 Gen4               • Pass          328.073 mV          0.000 dB          -8.615 dB
In P07 Gen4         Image: Pass         421.771 mW         2.484 dB         -5.867 dB           Image: P08 Gen4         Image: Pass         487.819 mW         3.498 dB         -3.951 dB           Image: P08 Gen4         Image: Pass         487.819 mW         3.498 dB         -3.951 dB           Image: P08 Gen4         Image: Pass         680.127 mW         3.283 dB         0.000 dB           Image: P10 Gen4         Image: Pass         328.073 mV         0.000 dB         -9.615 dB
⊕ P08 Gen4         ⊘ Pass         487.819 mV         3.498 dB         -3.951 dB           ⊕ P09 Gen4         ⊘ Pass         680.127 mV         3.283 dB         0.000 dB           ⊕ P10 Gen4         ⊘ Pass         328.073 mV         0.000 dB         -9.615 dB
IP09 Gen4         Image: OP38         B80.127 mV         3.283 dB         0.000 dB           Image: OP10 Gen4         Image: OP38         328.073 mV         0.000 dB         -9.615 dB
🖸 P10 Gen4 🥑 Pass 328.073 mV 0.000 dB -9.615 dB

Figure 63 TekExpress PCI Express System-Board Preset Test Results

View	Window Help										
7	Dr 😱 🗒	- □		1 / 1 108% -	ur an	Ŧ	8	Tools	Sign	Con	
_											
	<b>— —</b> <i>4</i>	9		TekEvpress	PCI Ev	nrass					
	I EL/ITOP			TEREAPIESS		picaa					
				System-Boar	rd Test Re	port					
	Setup Information										
	DUTID		DUT001		DPOJET Ve	sion		10.0.8.179			
	Date/Time		2019-01-17 1	5:10:31	Scope Mode	ł		DP073304D			
	Device Type		CEM		Scope Seria	I Number		B241041			
	TIT		PCI Express	10.4.5.26 (DAJLY)	SPC, Facto	vCalibration		PASS:PASS			
	TekExpress Version		Framework:4	.9.0.5	Scope F/W	Version		10.8.3 Build 3	l.		
	Test Mode		SigTest Com	pliance	Probe1 Mod	el		P76CA-292C	P7625		
	Spec Version		Gen4 - 4.0		Probe1 Seria	al Number		B001104;B001207			
	SigTest Version		3.2.0.3(Gen1	,2,3) 4.0.45 (Gen4)-Signal	Probe2 Mod	el		NA	NA		
	Sigliest version		Tests 4.0.45	(Gen4)-Preset Tests	Probe2 Seria	al Number		NA			
	Slot Number		01		Probe3 Mod	el		P7313SMA			
	Overall Test Result		Pass		Probe3 Seria	al Number		B022248			
	Overall Execution Time		0:11:30		Probe4 Mod	el		NA			
					Probe4 Seria	al Number		N/A	A		
					Signal Source	e Model		AWG7122C	20		
					Signal Sour	e Serial Numbe	r	B050012			
	DUT COMMENT:	DUT001									
	Taet Nama Summary Tah	la									
	Toor Harris Comminary Too	10									
	DEFORT DECLUTE										
	Preset Namo	Lano Namo		Deschool	Do Emphaei		1/b		Docult		
	Pi Gen4	Lane		0.000 //B	-6.073.dB	0	403 250 mV		Daee		
	P10 Gen4	Lane0		0.000 dB	-0.073 dB		493.209 mV		Daee		
	P01 Gen4	LanaO		0.000 dB	3 702 dB		641 442 mV		Pasa		
	P01 Gen4	Lane0		0.000 dB	-3.792 dB		595.402 mV		Page		
	P02 Gen4	Lane0		0.000 dB	-2.672.dB		729 708 mV		Page		
	P04 Gen4	LaneO		0.000 dB	0.000.48		992 505 mV		Daee		
	P05 Gen4	Lane0		1.566 dB	0.000 dB		828.702 mV		Page		
	P06 Gen4	Lane0		2.219 dB	0.000 dB		768 762 mV		Pass		
	P07 Gen4	Lane0		2.848 dB	-5.867 dB		421 771 mV		Page		
	P08 Gen4	Lane0		3.498 dB	-3.951 dP		487 819 ml/		Page	_	
	TOO GOIN	Landu		0.400 00	-0.001 UB		407.0191110		1 000		
	P09 Gen4	ane()		3 283 68			P991127 mV		Pace		

Figure 64 TekExpress PCI Express System-Board Preset Test Report

15.Once test report is generated you can save the Test Session in TekExpress, Options → Save Test Setup → Tek\_Gen4\_SYS\_Preset\_MOI (Example of session name). The saved data can be found in the location X:\PCI Express\Tek\_Gen4\_SYS\_Preset\_MOI\DUT001.

<pre>% TekExpress PCI Express - (Tek_Gen4_SYS_Preset_MOI)</pre>	Options 💽 🔿 🏵
Computer → Local Disk (X:) → PCI Express → Tek_Gen4_SYS_Preset_MOI → DUT001 →	✓ ✓ ✓ Search DUT001
Organize ▼ Include in library ▼ Share with ▼ Burn New folder	:= 🕶 🔳 🔞

Figure 65 TekExpress PCI Express System-Board Preset Test Session Saved

# 5. Appendix

## 5.1 Channel Loss

All loss values are nominal differential insertions loss and actual loss values may vary with different cables, connectors, and board-to-board variation.

## 5.1.1 Channel Loss for Tx Signal Quality Test Add-In-Card



Figure 66 Channel Loss for Tx Signal Quality Test Add-In-Card

## 5.1.2 Channel Loss for Tx Preset Test Add-In-Card



Figure 67 Channel Loss for Tx Preset Test Add-In-Card



## 5.1.3 Channel Loss for Tx Pulse Width Jitter Test Add-In-Card

Figure 68 Channel Loss for Tx Pulse Width Jitter Test Add-In-Card



#### 5.1.4 Channel Loss for Tx Signal Quality Test System-Board

Figure 69 Channel Loss for Tx Signal Quality Test System-Board



## 5.1.5 Channel Loss for Tx Preset Test System-Board

Figure 70 Channel Loss for Tx Preset Test System-Board

#### 5.2 Fixture Characterization Preliminary

This document talks about Gen4 Fixture Characterization with measurement setups for Add-In-Card and System-Board.



#### 5.3 DUT Toggle using Manual Mode

Ensure that in TekExpress PCI Express application you select 'Do not use' as 'signal source for toggle' in the configuration panel as show in the figure below.

V TekExpress	s PCI Express - (	(Untitled)*						Opti	ons 💌	
Setup	рит	SigTest Mode O Compliance O User Defined								Start
Status	Test Selection	Global Settir								
Status		Instruments D	Pause							
Results	Acquisitions	RF Switch			Do no	otuse		Contr	rol	
	Configuration	Real Time Sco Signal Source	for DUT Autom	ation	MSO: Do no	73304DX (GPIB at use	8::1::INSTR)	Settir	ngs	
Reports 4	Configuration							Manual T	oggle	
5	Preferences							Setu	qu	
l i i i i i i i i i i i i i i i i i i i	,	Automat	ed DUT Contro	ol Setu	up					
			Record Length			Sample Rate		Bandwidth		
		2.5Gb/s	10	Μ		25	GS/s	6 GHz	Y	
			10	Μ		50	GS/s	12.5 GHz	•	
			10	М		50	GS/s	16 GHz	•	
		16Gb/s	12.5	м		100	GS/s	25 GHz	Y	
		Sig Validatio	n Threshold	200	)	mV .	Trigger Type	Auto	T	
							(Gen3/Gen4)			
		Sigtest Cont	figuration							
		Setu	q							
_										
Con	npleted.									

Figure 71 TekExpress PCI Express DUT Toggle in Manual Mode

#### 5.3.1 Tx Signal Quality Test for Add-In-Card – DUT Toggle in Manual Mode

For Tx Signal Quality Test for Add-In-Card with DUT toggle in Manual Mode, make the connection as per <u>section# 3.1 (Figure 1 Tx Signal Quality Test for Add-In-Card – DUT Toggle in Manual Mode)</u> and start the test. User needs to push the 'CMTS' pulse button for 14 times to get to the Gen4 Preset0 pattern, post-acquisition of Gen4 Preset0, TekExpress application will prompt the user to send Gen4 Preset1 pattern then push the pulse button one time and click OK so that application will acquire. Continue this operation till Gen4 Preset10. The implementation method remains like <u>section#4.1</u> exception point#8 is replaced with this step, where user selected 'Do not use' for 'Signal Source for DUT Automation.

## 5.3.2 Tx Preset Test for Add-In-Card – DUT Toggle in Manual Mode

For Tx Signal Quality Test for Add-In-Card with DUT toggle in Manual Mode, make the connection as per section# 3.2 (Figure 2 Tx Preset / Pulse Width Jitter Test for Add-In-Card – DUT Toggle in Manual Mode) and start the test. User needs to push the 'CMTS' pulse button for 14 times to get to the Gen4 Preset0 pattern, post-acquisition of Gen4 Preset0, TekExpress application will prompt the user to send Gen4 Preset1 pattern then push the pulse button one time and click OK so that application will acquire. Continue this operation till Gen4 Preset10. The implementation method remains like section#4.2 exception point#8 is replaced with this step, where user selected 'Do not use' for 'Signal Source for DUT Automation.

#### 5.3.3 Tx Pulse Width Jitter Test for Add-In-Card – DUT Toggle in Manual Mode

For Tx Signal Quality Test for Add-In-Card with DUT toggle in Manual Mode, make the connection as per <u>section# 3.2 (Figure 2 Tx Preset / Pulse Width Jitter Test</u> for Add-In-Card – DUT Toggle in Manual Mode) and start the test. User needs to push the 'CMTS' pulse button for 26 times to get to the Gen4 Preset0 pattern, post-acquisition of Gen4 Preset0, TekExpress application will prompt the user to send Gen4 Preset1 pattern then push the pulse button one time and click OK so that application will acquire. Continue this operation till Gen4 Preset10. The implementation method remains like <u>section#4.3</u> exception point#8 is replaced with this step, where user selected 'Do not use' for 'Signal Source for DUT Automation.

#### 5.3.4 Channel Tx Signal Quality Test for System-Board – DUT Toggle in Manual Mode

For Tx Signal Quality Test for System-Board with DUT toggle in Manual Mode, make the connection as per <u>section#3.3 (Figure 3 Tx Signal Quality Test for System-Board – DUT Toggle in Manual Mode)</u> and start the test. User needs to push the 'CMTS' pulse button for 14 times to get to the Gen4 Preset0 pattern, post-acquisition of Gen4 Preset0, TekExpress application will prompt the user to send Gen4 Preset1 pattern then push the pulse button one time and click OK so that application will acquire. Continue this operation till Gen4 Preset10. The implementation method remains like <u>section#4.4</u> exception point#8 is replaced with this step, where user selected 'Do not use' for 'Signal Source for DUT Automation.

#### 5.3.5 Channel Tx Signal Quality Test for System-Board – DUT Toggle in Manual Mode

For Tx Preset Test for System-Board with DUT toggle in Manual Mode, make the connection as per <u>section# 3.4 (Figure 4 Tx Preset Test for System-Board – DUT Toggle in Manual Mode)</u> and start the test. User needs to push the 'CMTS' pulse button for 14 times to get to the Gen4 Preset0 pattern, post-acquisition of Gen4 Preset0, TekExpress application will prompt the user to send Gen4 Preset1 pattern then push the pulse button one time and click OK so that application will acquire. Continue this operation till Gen4 Preset10. The implementation method remains like <u>section#4.5</u> exception point#8 is replaced with this step, where user selected 'Do not use' for 'Signal Source for DUT Automation.

Toggle Sequence	Setting#	Compliance Pattern from the DUT	Data Rate (GT/s)
Power ON	1	Gen1	2.5
1	2	Gen2 - 3.5dB	5
2	3	Gen2 - 6.0dB	5
3	4	Gen3 - PO	8
4	5	Gen3 - P1	8
5	6	Gen3 - P2	8
6	7	Gen3 - P3	8
7	8	Gen3 - P4	8
8	9	Gen3 - P5	8
9	10	Gen3 - P6	8
10	11	Gen3 - P7	8
11	12	Gen3 - P8	8
12	13	Gen3 - P9	8
13	14	Gen3 - P10	8
14	15	Gen4 - PO	16
15	16	Gen4 - P1	16
16	17	Gen4 - P2	16
17	18	Gen4 - P3	16
18	19	Gen4 - P4	16
19	20	Gen4 - P5	16
20	21	Gen4 - P6	16
21	22	Gen4 - P7	16
22	23	Gen4 - P8	16
23	24	Gen4 - P9	16
24	25	Gen4 - P10	16
25	26	Jitter Measurement Pattern on all Lanes.	16
26	27	Jitter Measurement Pattern on Lanes 0/8/16/24 and Compliance pattern on all other Lanes	16
27	28	Jitter Measurement Pattern on Lanes 1/9/17/25 and Compliance pattern on all other Lanes	16
28	29	Jitter Measurement Pattern on Lanes 2/10/18/26 and Compliance pattern on all other Lanes	16
29	30	Jitter Measurement Pattern on Lanes 3/11/19/27 and Compliance pattern on all other Lanes	16
30	31	Jitter Measurement Pattern on Lanes 4/12/20/28 and Compliance pattern on all other Lanes	16
31	32	Jitter Measurement Pattern on Lanes 5/13/21/29 and Compliance pattern on all other Lanes	16
32	33	Jitter Measurement Pattern on Lanes 6/14/22/30 and Compliance pattern on all other Lanes	16
33	34	Jitter Measurement Pattern on Lanes 7/15/23/31 and Compliance pattern on all other Lanes	16

#### 5.4 Compliance Pattern Toggle Sequence

Figure 72 Compliance Pattern Toggle Sequence