

70th
Anniversary
展望太克 榮耀70

2016太克科技 春季創新論壇



Tektronix®

Tektronix

70th
Anniversary
展望太克 榮耀70

Type-C Overview

Gary Simonton

Product Marketing Engineer, USB Solutions

20 MAY 2016



Agenda

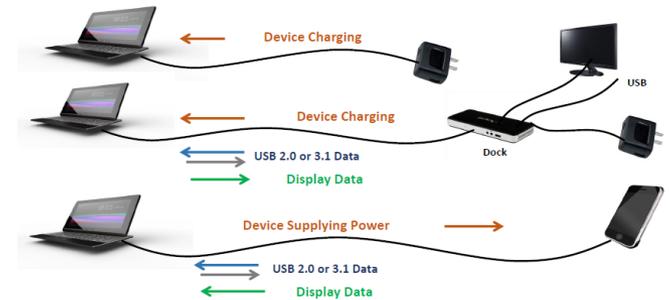
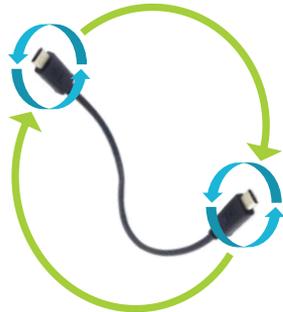
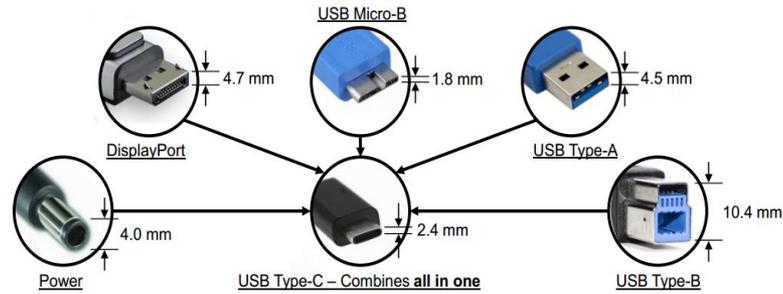
- Type-C Overview
- Specifications relevant to Type-C
- “Alt-Mode” Operation
- Test Fixtures
- Power Delivery Test
- Testing Challenges
- Tektronix Solutions for Type-C
- Summary



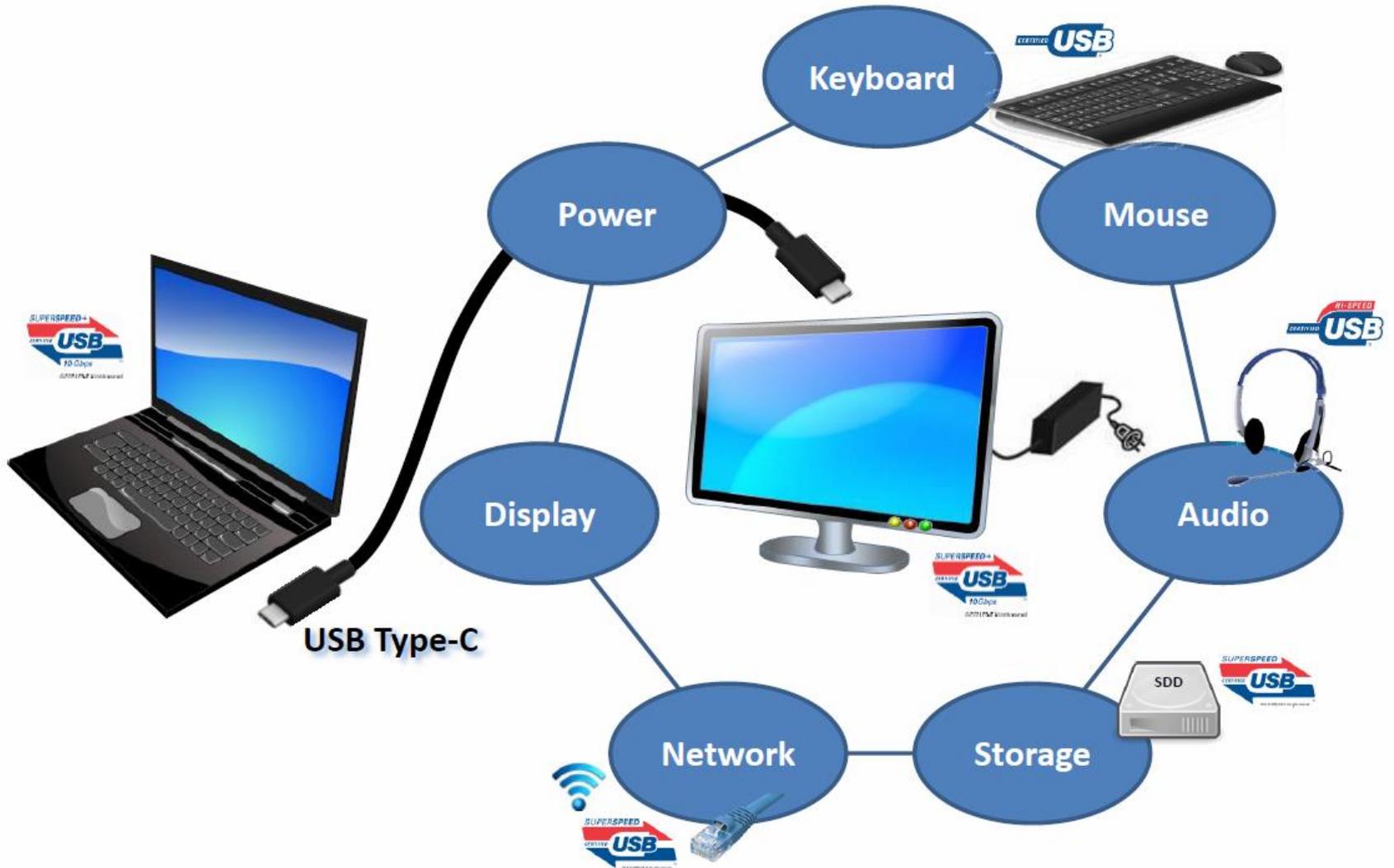
Type-C Overview

The background features several overlapping geometric shapes in various shades of blue and teal. A prominent feature is a large, tilted rectangular area filled with a fine halftone dot pattern. Other elements include solid-colored diagonal bars and overlapping trapezoidal shapes, creating a modern, layered aesthetic.

What is Type-C, why is it important?

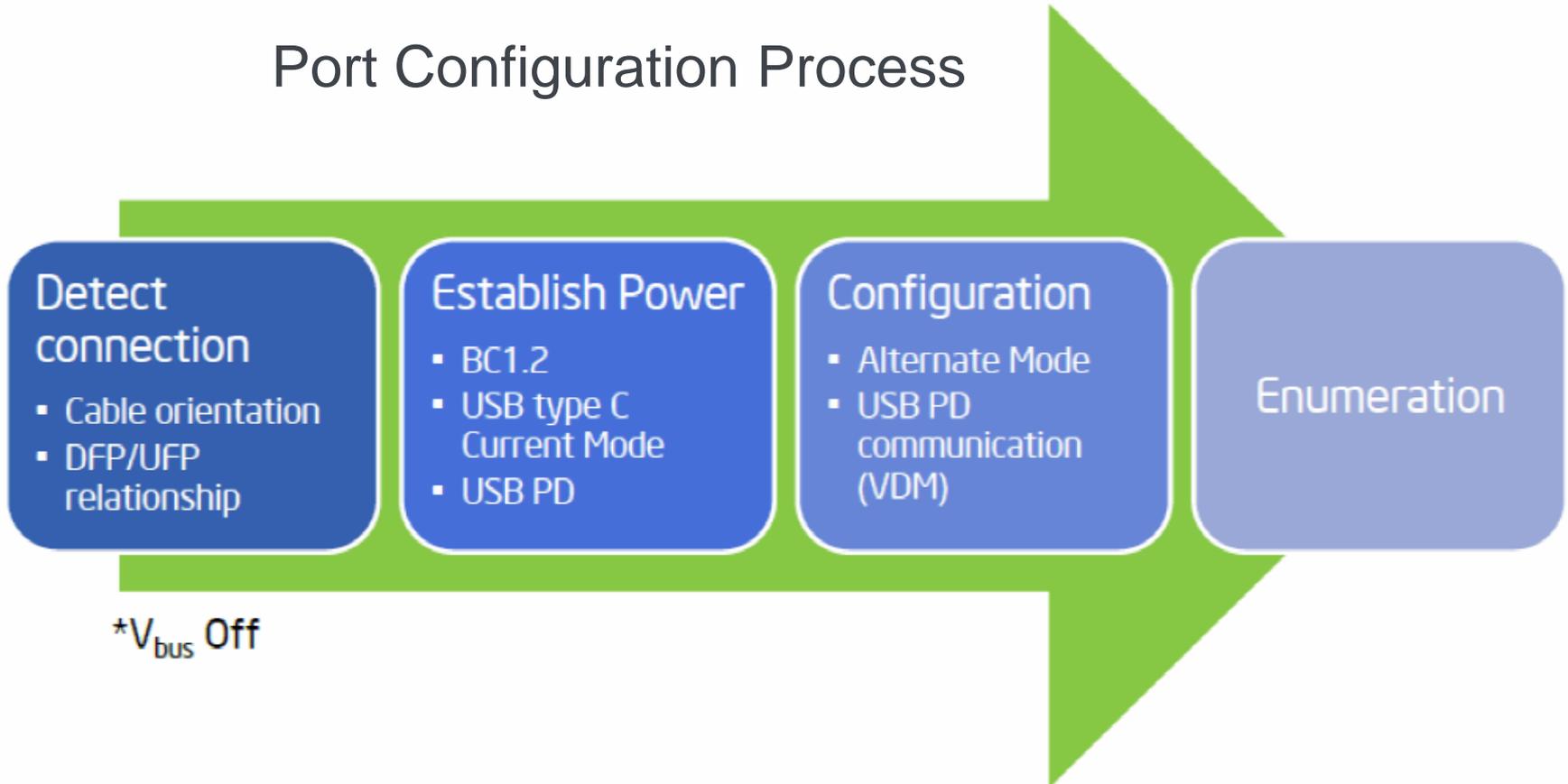


Single Connector Platform Model



USB = Data + Video + Power

Port Configuration Process

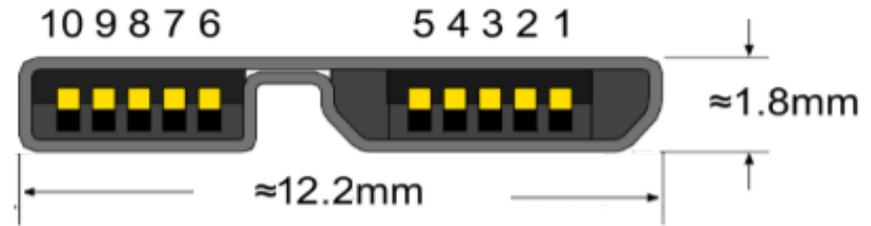


Source: Intel Corp.

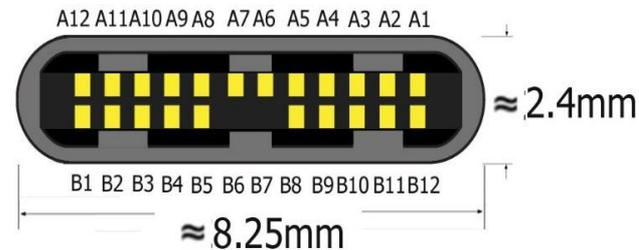
Type-C Comparison (*USB-C*)

- Rounded, reversible, flipable
- ~25% less width vs. μ B
- Signaling
 - Two SS differential pairs
 - Vbus power
 - Configuration Channel (CC)
 - USB 2.0 differential pair
 - Sideband Use (SBU)
 - Plug power (Vconn)

Micro B Plug



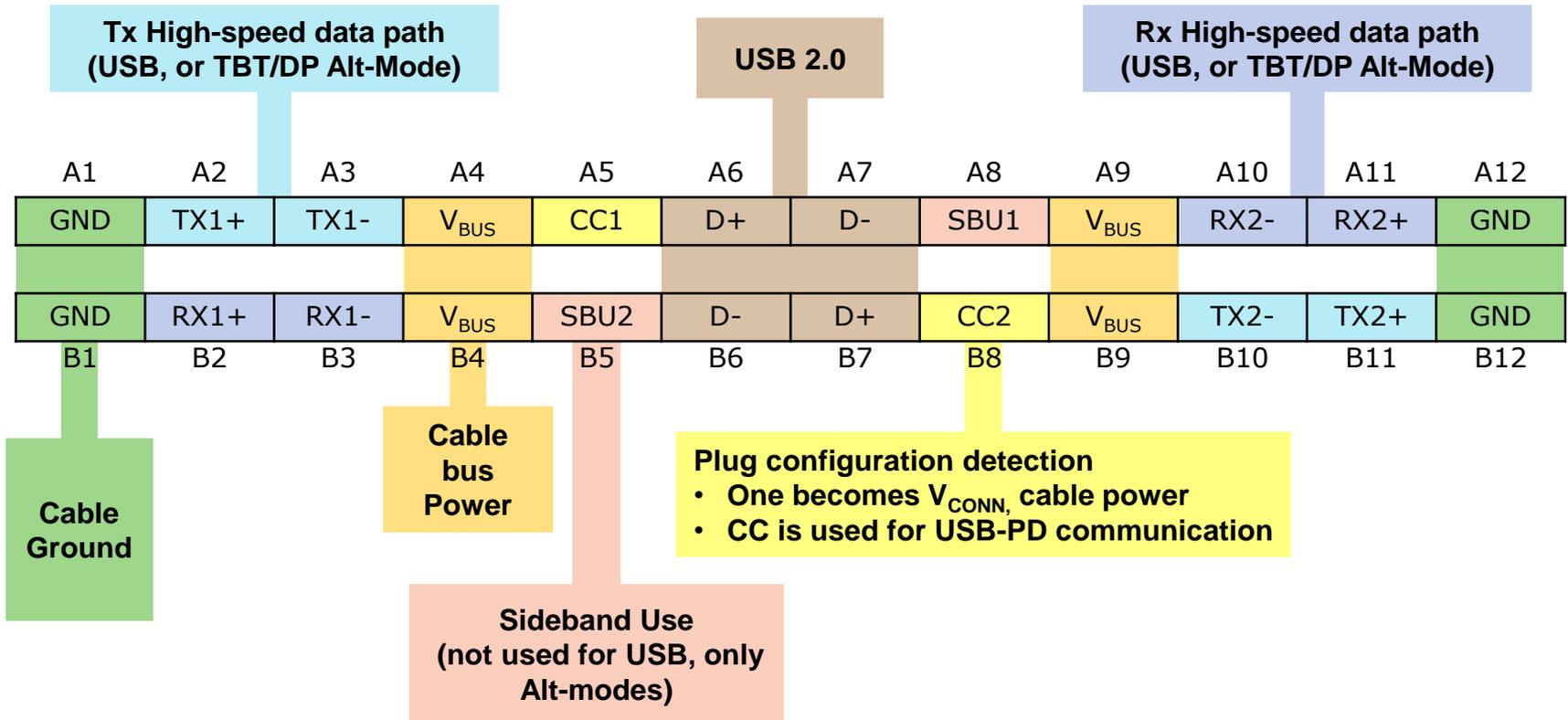
Type-C Plug



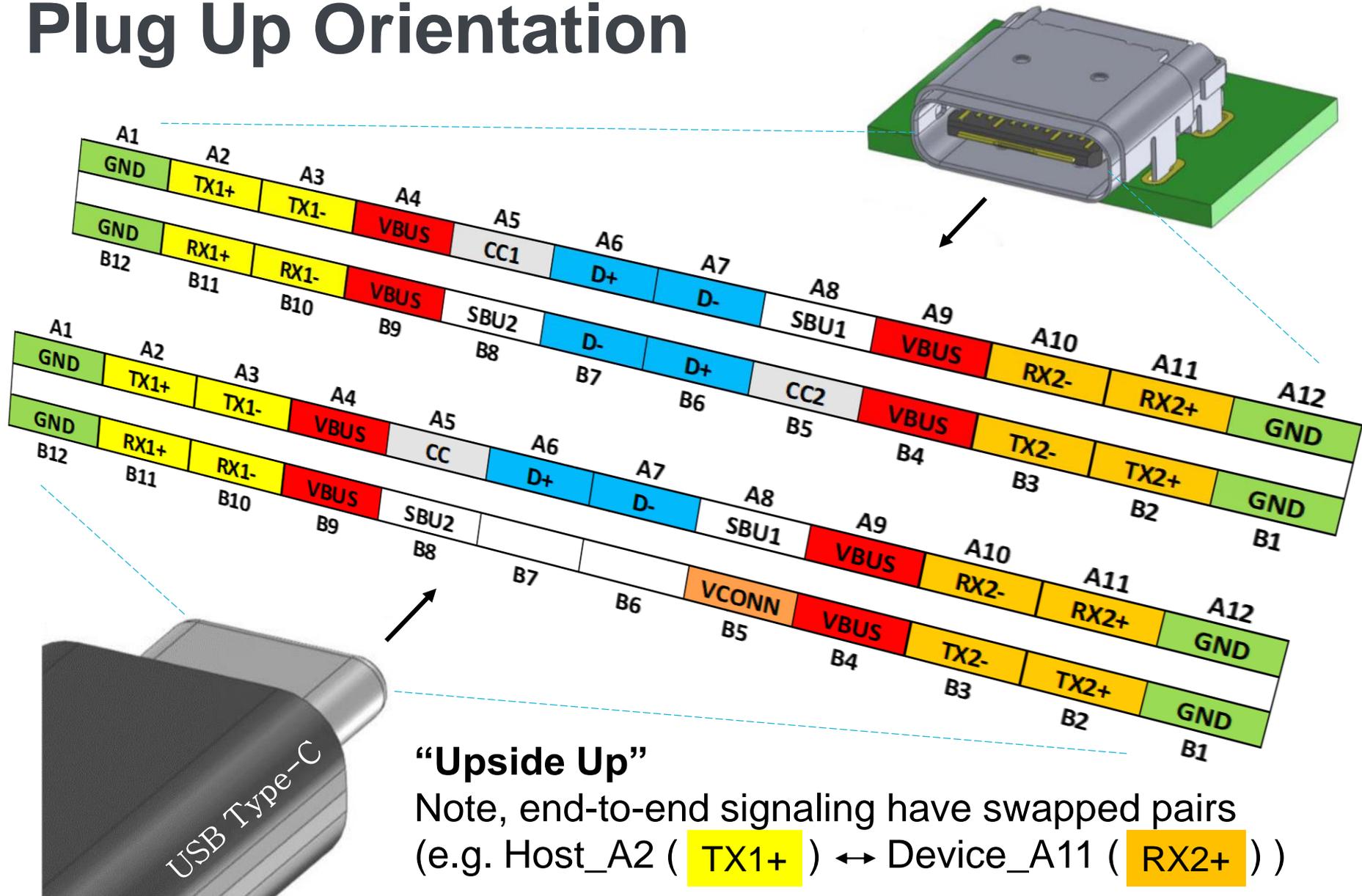
* New signals

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2			VCONN	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

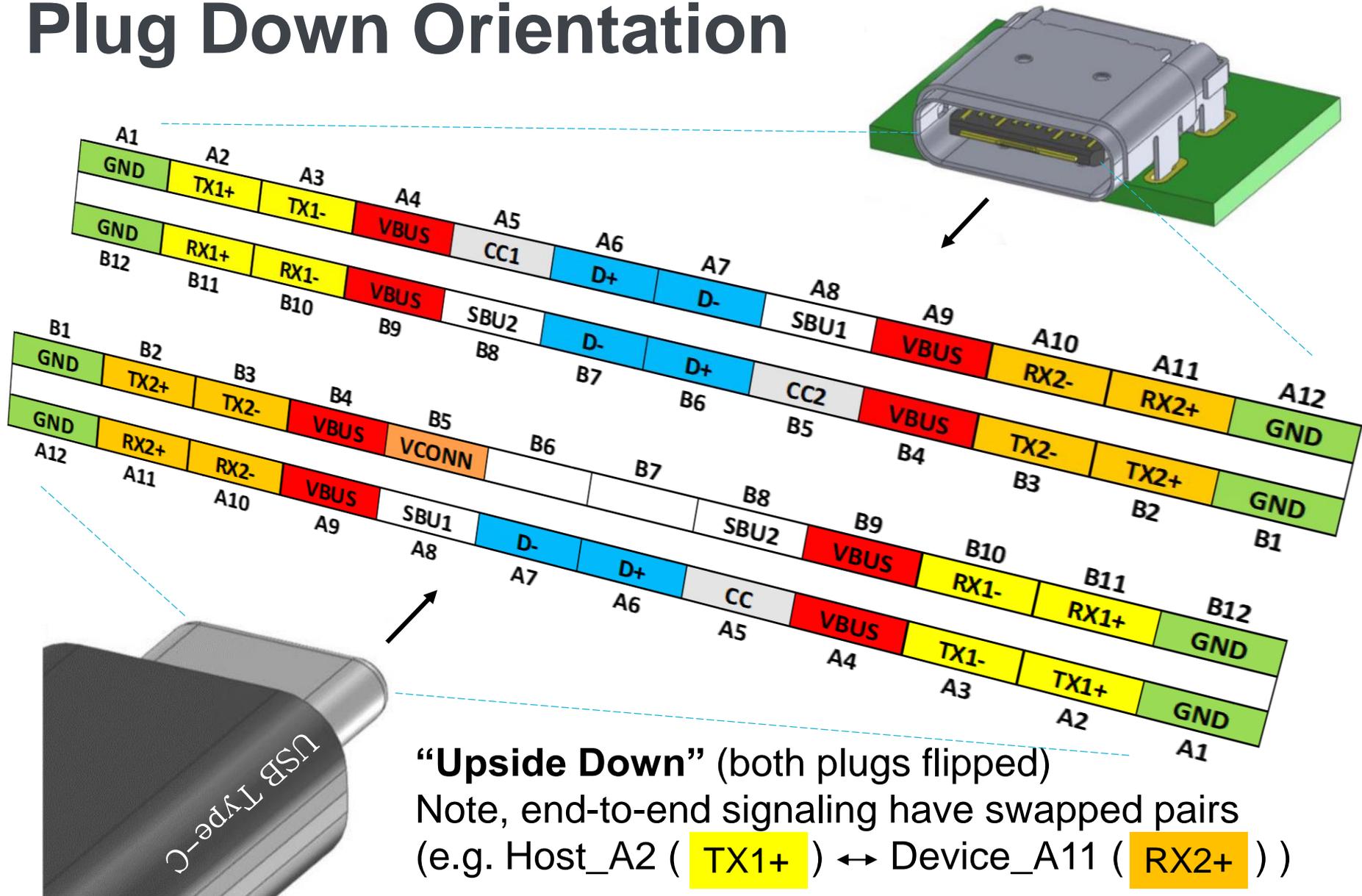
Type-C Pin Definitions



Plug Up Orientation



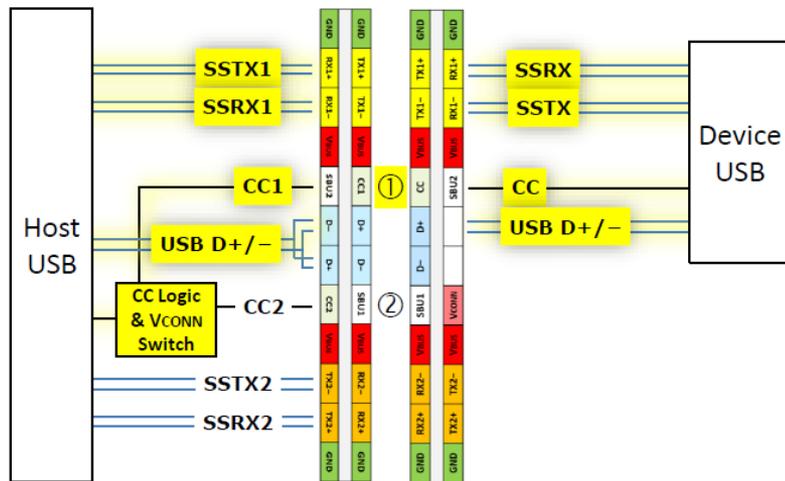
Plug Down Orientation



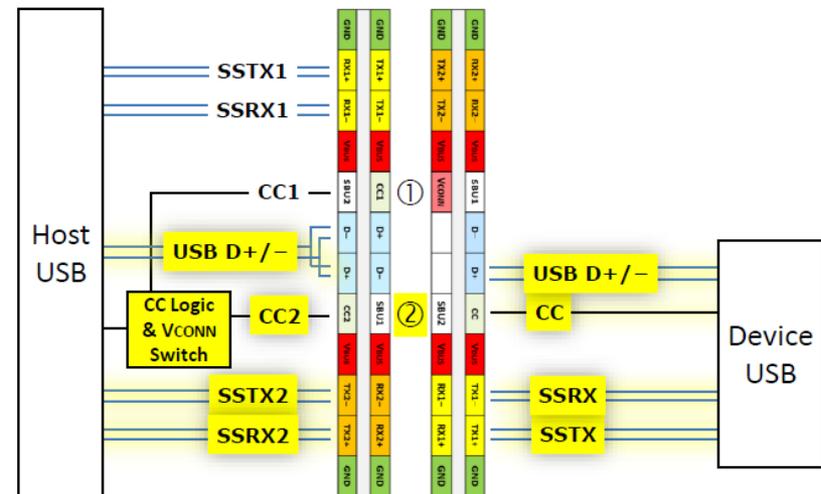
“Upside Down” (both plugs flipped)
 Note, end-to-end signaling have swapped pairs
 (e.g. Host_A2 (TX1+) ↔ Device_A11 (RX2+))

Why is Configuration Channel (CC) signal so important?

- Used to determine downstream and upstream positions (role swapping)
- Discover and configure optional Alternate and Accessory modes
- Resolve cable orientation and twist connections to establish USB data bus routing*



⇒ Un-flipped – Position ①



⇒ Flipped – Position ②

Connector Transition

Legacy Cables

Plug 1	Plug 2	Version	Length
A	C	USB 2.0	≤ 4m
A	C	USB 3.1 Gen2	≤ 1m
C	B	USB 2.0	≤ 4m
C	B	USB 3.1 Gen2	≤ 1m
C	Micro-B	USB 2.0	≤ 2m
C	Micro-B	USB 3.1 Gen2	≤ 1m

Defined Adapters

Plug 1	Plug 2	Version	Length
C	Micro-B	USB 2.0	≤ 0.15 m
C	A	USB 3.1 Gen1	≤ 0.15 m

Host (Type-C)



Cable
(C to Micro-B)



Device
(Micro-B)



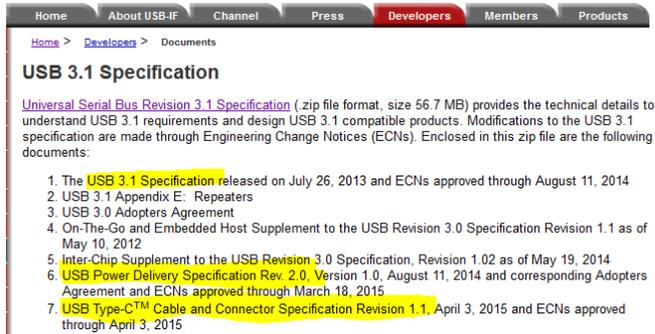
Specifications

The background features several overlapping geometric shapes in various shades of blue and teal. A prominent feature is a large, tilted rectangular area filled with a fine halftone dot pattern. Other elements include solid-colored diagonal stripes and trapezoidal shapes that create a sense of depth and movement.

USB specifications

- Base spec and supplemental specs:

<http://www.usb.org/developers/docs>



- Compliance Test Specification (CTS)

- USB 3.0 CTS 1.0a (March 2015a):

http://www.usb.org/developers/compliance/ssusb_testing

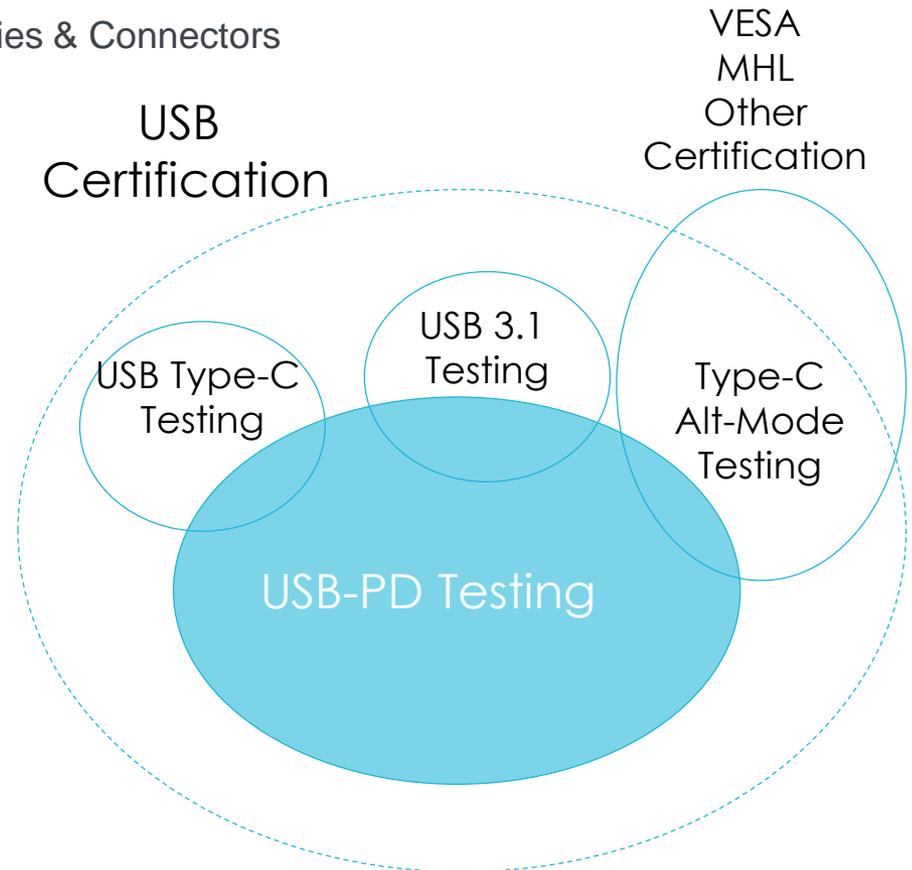
- USB 3.1 CTS (in final editing/revisions)

- Will include both gen1 (5 Gb/s) and gen2 (10 Gb/s) Tx and Rx test procedures
- Standard, MicroAB/B, and Type-C connector channel and connector support

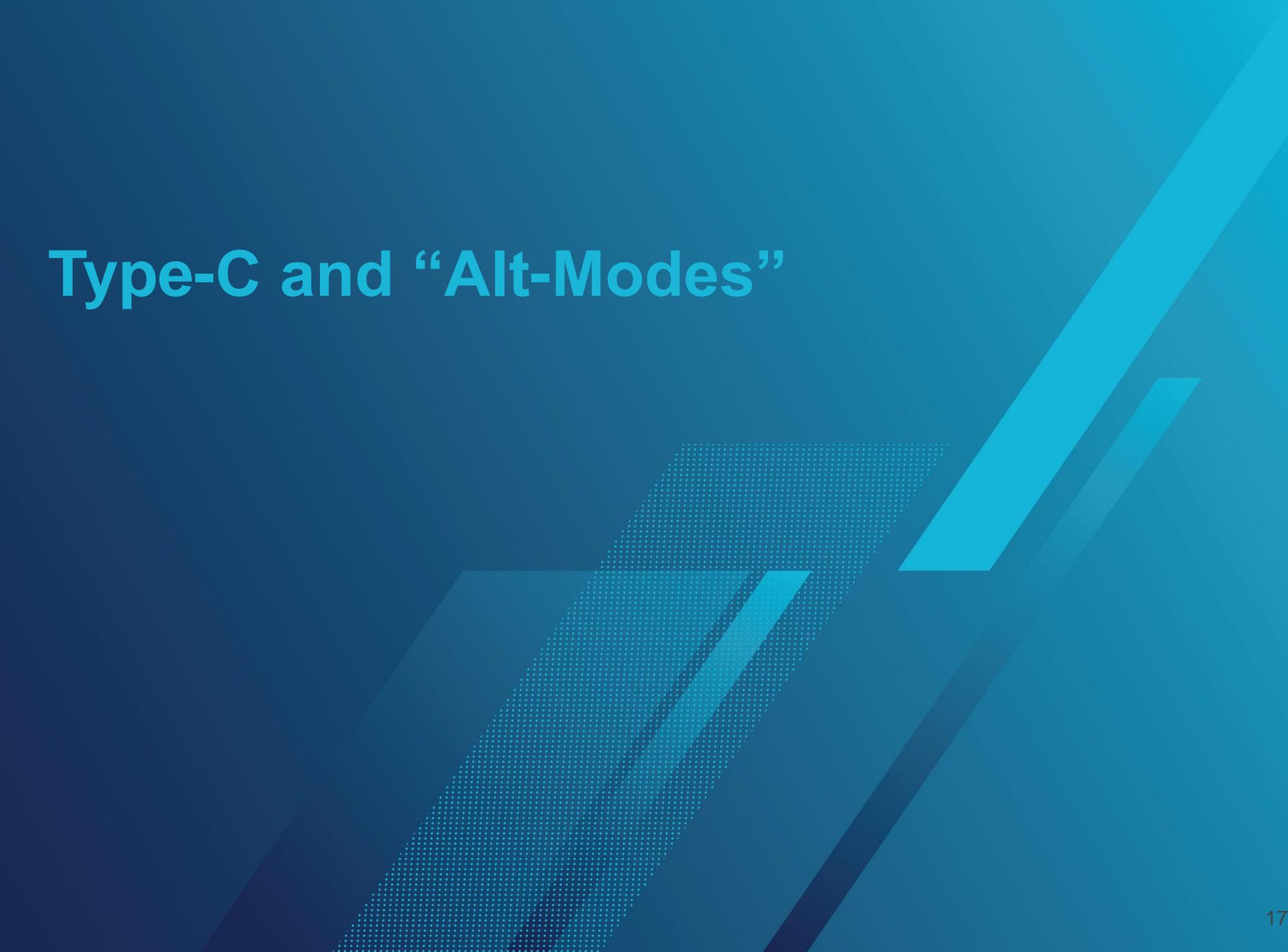


USB-PD & DisplayPort Specification & CTS Overlap

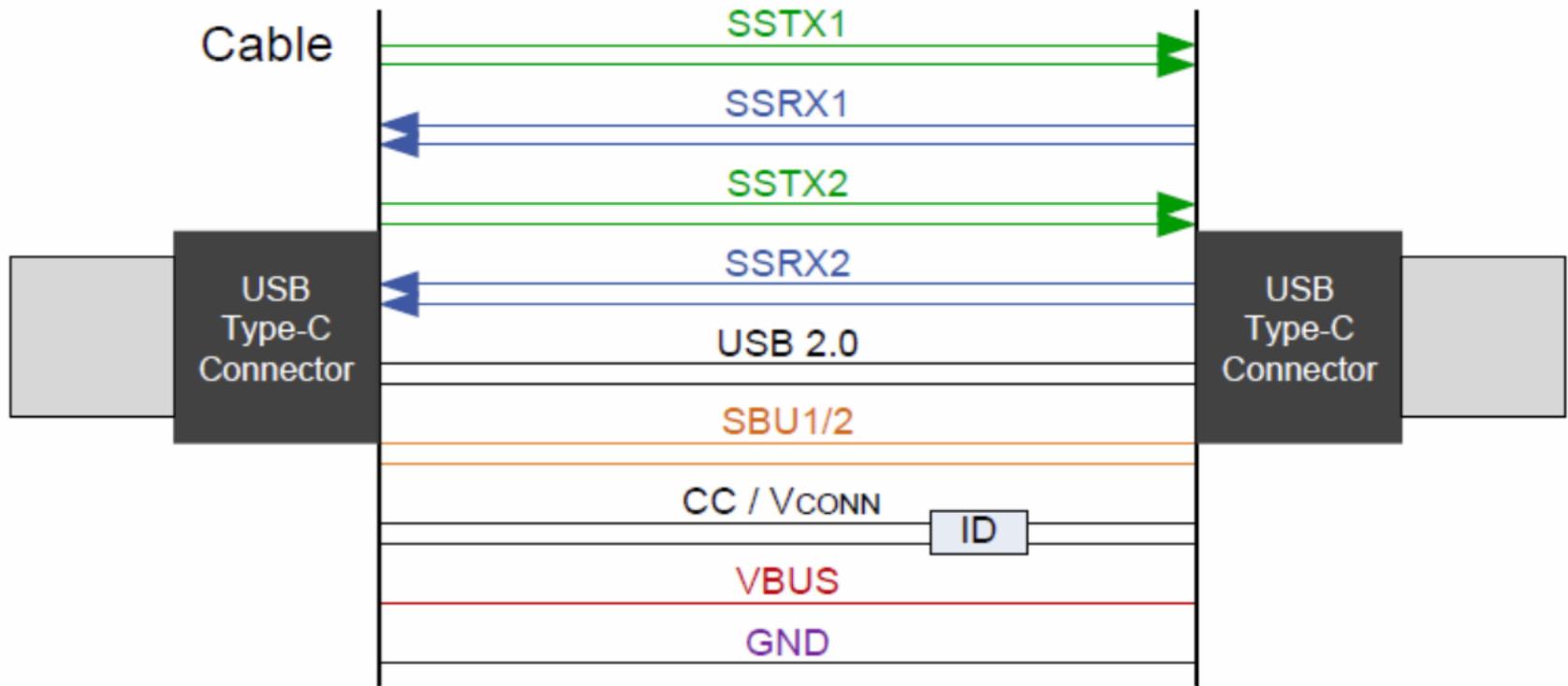
- USB Power Delivery Rev2.0, V2.0
 - Chapter 2 - Overview Section including SOP* Comm and UFP/DFP Communications
 - Chapter 3 Type-A and TypeB Cable Assemblies & Connectors
 - Chapter 4 Electrical Requirements
 - Chapter 5 Physical Layer (BMC & FSK)
 - Chapter 6 Protocol Layer
 - Chapter 7 Power Supply
 - Chapter 8 Device Policy
 - Chapter 9 System Policy
- USB Type-C Cable Specification Rev1.0
 - Chapter 4 – Type-C Functional Testing
- DisplayPort Alt Mode on USB Type-C
 - Chapter 5 – Discovery and USB-PD
- TBT and other 'Alt Modes'



Type-C and “Alt-Modes”



USB 3.1 Data Mode

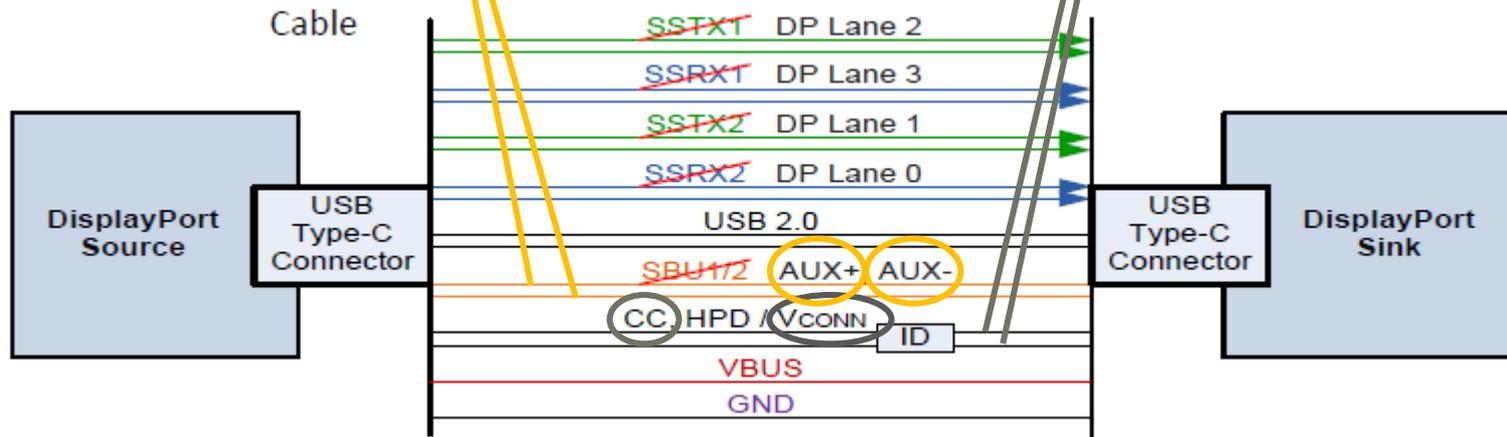


DisplayPort Mode (Alt mode)

Unigraf (AUX Controller)

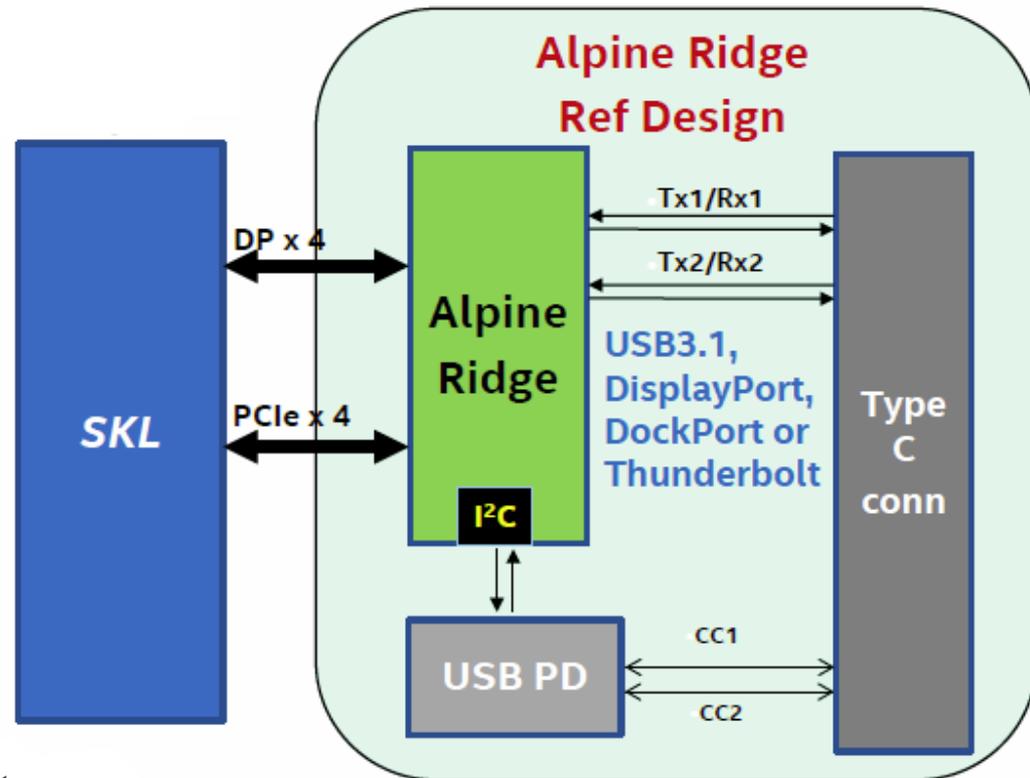


GRL PD/Alt-Mode controller



Thunderbolt Mode

- Integrate Type-C solution (Alpine Ridge)
- Targeted for Intel Skylake platform
- Key features
 - Native USB 3.1 (10 Gb/s)
 - DP over Type-C (4K Video)
 - Thunderbolt (20 Gb/s)
 - DockPort
- Tektronix to provide full Alpine Ridge support in Q3 2016
 - TBT3 controller automation with 4x faster 10G/20G measurement automation
 - Use new TBT 20G Type-C fixture



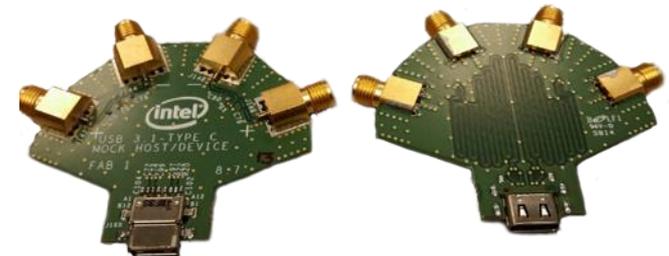
Test Fixtures



Test Fixtures

- USB 3.1 fixtures
 - **USB-IF** (required for certification)
 - Type-C, Standard/Micro A/B
 - Includes USB-specific channels
 - Available **now** on [USBIF website!](#)
 - **Wilder Technologies**
 - DP Type-C fixtures also work for USB
 - **Luxshare-ICT**
- DP over Type-C
 - **Wilder Technologies**
 - **Luxshare-ICT**

**USB-IF
Type-C Fixtures & Channels**



Wilder DP Fixture



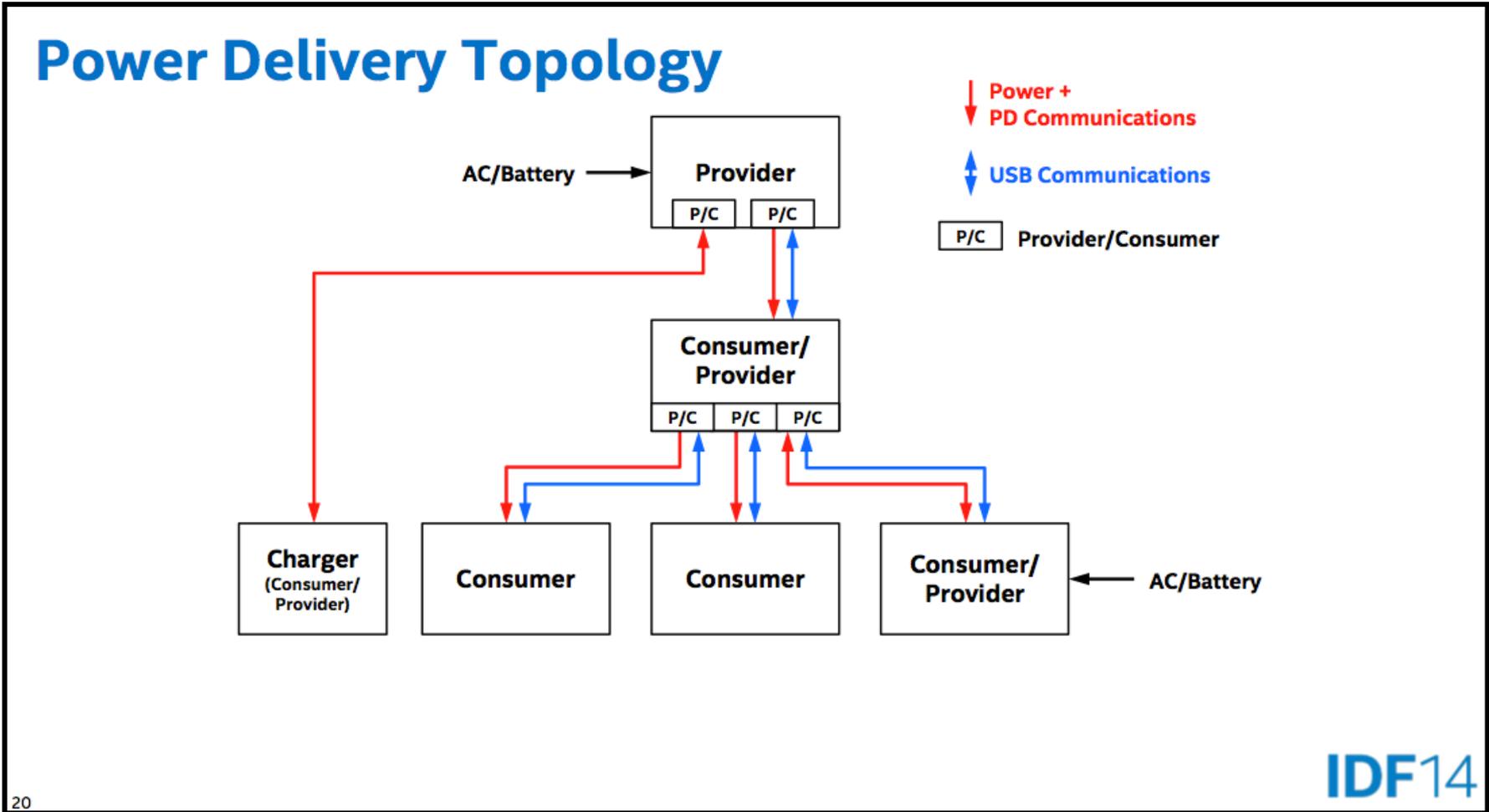
**Luxshare-ICT
High Speed Plug Fixture**



Power Delivery

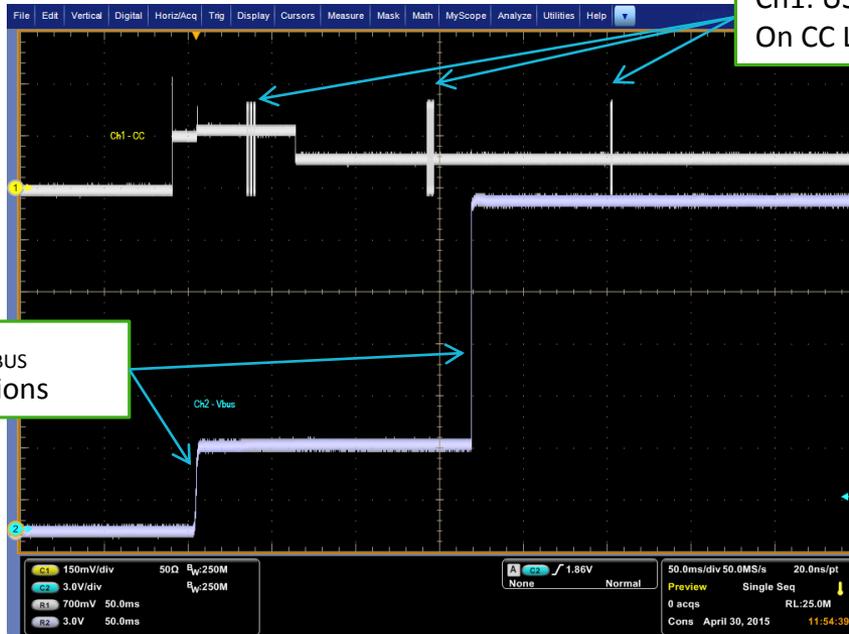
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Power Delivery Topology



Run Tests

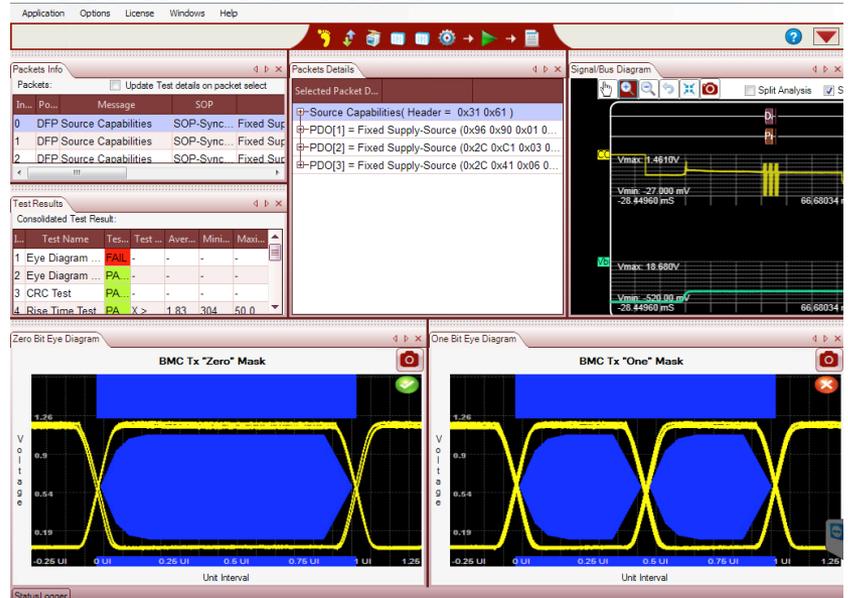
Scope Acquisition



Press Run



Results 'Dashboard'



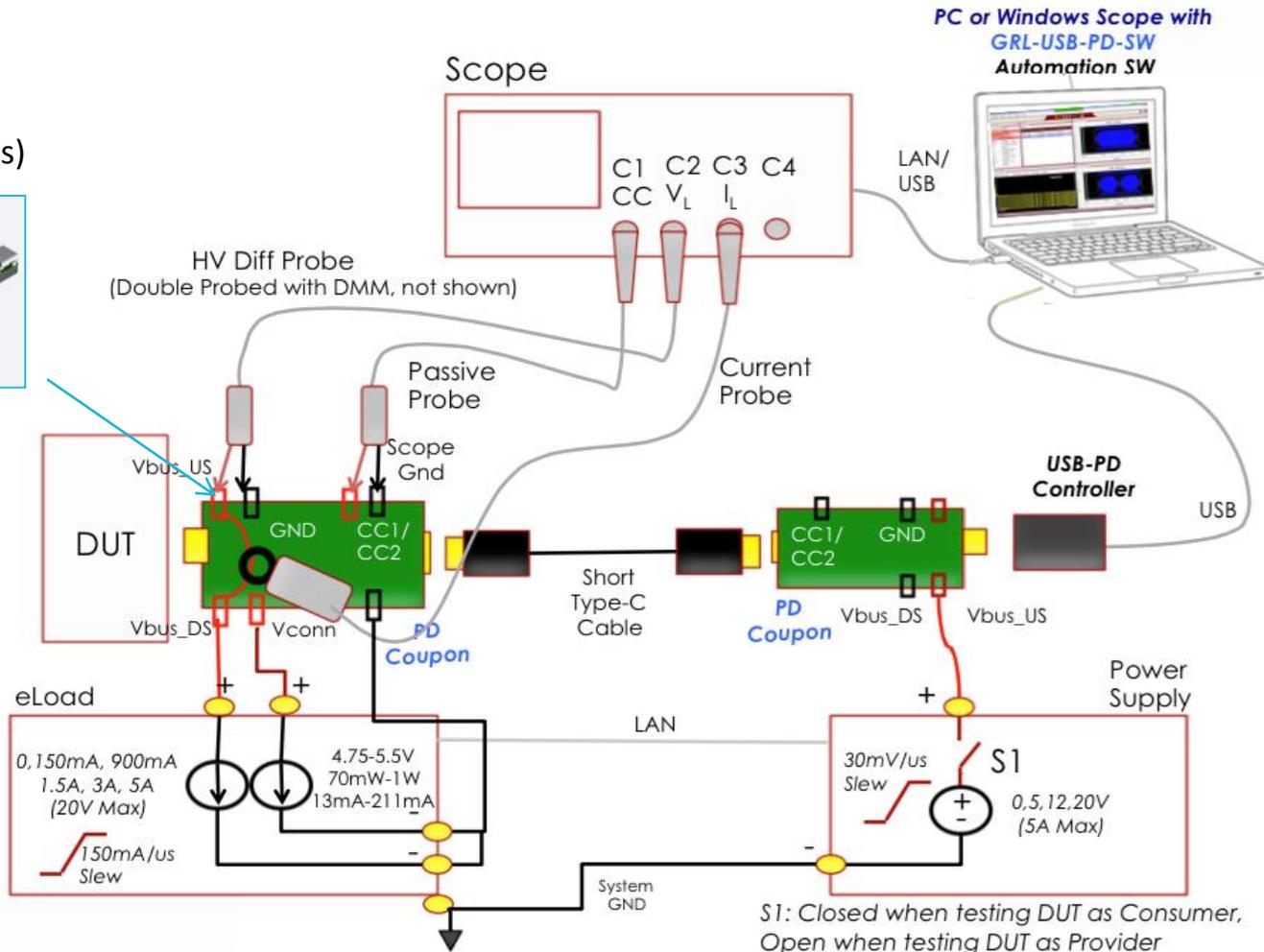
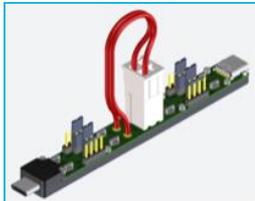
GRL-USB-PD Software

Useful Scope Features

- Lowest Analog BW (100-200MHz)
- High Res Acquisition Mode to filter noise
- Pulse Width Trigger
- Segmented Memory
- Desired: CC Packet Trigger
- HF Reject Trigger Coupling

Confirm Test Setup (Provider/Consumer Example)

USB-PD Coupon(s)



View Power Provider Test Results

'Dashboard' View

Compliance Results

The screenshot displays the USB-PD Protocol Decode Software interface. The main window is titled 'USB-PD Protocol Decode Software (Version: 1.1.0.0)' and contains several panes:

- Test Selection:** A tree view showing compliance test results for various power source load and transient tests, all marked with green checkmarks.
- Packets Info:** A table listing 15 packets with columns for Index, Position, Message, SOP, and PDO. Packet 1 is highlighted as 'DFP Source Capabilities'.
- Packets Details:** A detailed view of the selected packet (PDO[1] = Fixed Supply-Source) showing a table of bit fields and their values.
- Test Results:** A table showing the results of 7 selected packet tests, including Eye Diagram One, Eye Diagram Zero, CRC Test, Rise Time Test, Fall Time Test, Symbol Encoding, and Packet Format Test.
- Signal Bus Timing:** A waveform diagram showing signal transitions with voltage and time measurements.
- Zero Bit Eye Diagram:** A plot showing the eye diagram for a 'Zero' mask.
- One Bit Eye Diagram:** A plot showing the eye diagram for a 'One' mask.

Packet Info

Packet Details

BMC Electrical Meas

BMC Eye

SignalBus Timing



Complete USB-PD Compliance Solution

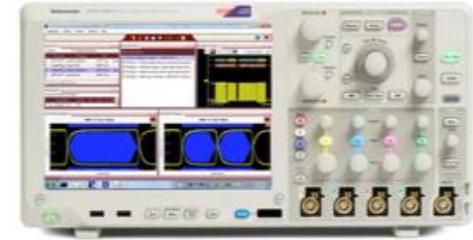
• Required Equipment for PD Testing

- Order Oscilloscope from Tektronix
 - **DPO5000 Series** Scopes and above
 - **GRL-USB-PD** Power Delivery SW
 - **2ea. Passive Probes** for CC and VBUS
 - **1ea. TCP-2020A Current Probe** for Load Current
- Order USB-PD Controller from GRL
 - **1 ea. GRL-USB-PD-C1** Controller
- Keithley eLoad & Power Supplies:
 - **1 ea – Keithley 2380** DC E-Load
 - **Optional Lab PS – Keithley 2280S-32-6 (32V/6A)**
- Download Data Sheet and Demo SW, MOI
 - www.graniteriverlabs.com/usb-pd/



TCP-2020A

TekScope



Keithley 2380



GRL-USB-PD-C1



A screenshot of a product overview document for the GRL-USB-PD-C1 controller. The document includes a title, a brief description of the product, a list of features, and a list of supported power supplies. The features list includes: Runs on any Tektronix Windows based scope; Complies to the latest USB 4.0 USB PD Specification and Test Plans; Performs accurate physical layer (PHY) tests; Chapter 4 of the USB PD Specification; Performs power state (BMC-PHY) tests - Chapter 7 of the USB PD Specification; Fully addresses the PHY and VBUS layer of the USB PD physical layer signal; Tests full range of USB PD sources - Cable, Adapters, Protectors, Consumers, Dual Role Devices (Power Sources); Automatically saves all waveforms for further analysis and debugging; Fully addresses the USB PD Compliance test process from the Physical layer signal; Supports All Market solutions for high speed Physical Layer (PHY) testing; Runs on Windows based Oscilloscopes.

Type-C Testing/Validation Challenges

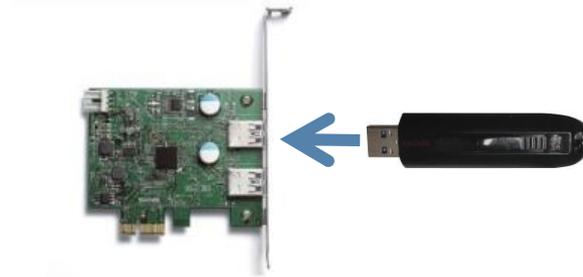


Challenges in validating Type-C designs

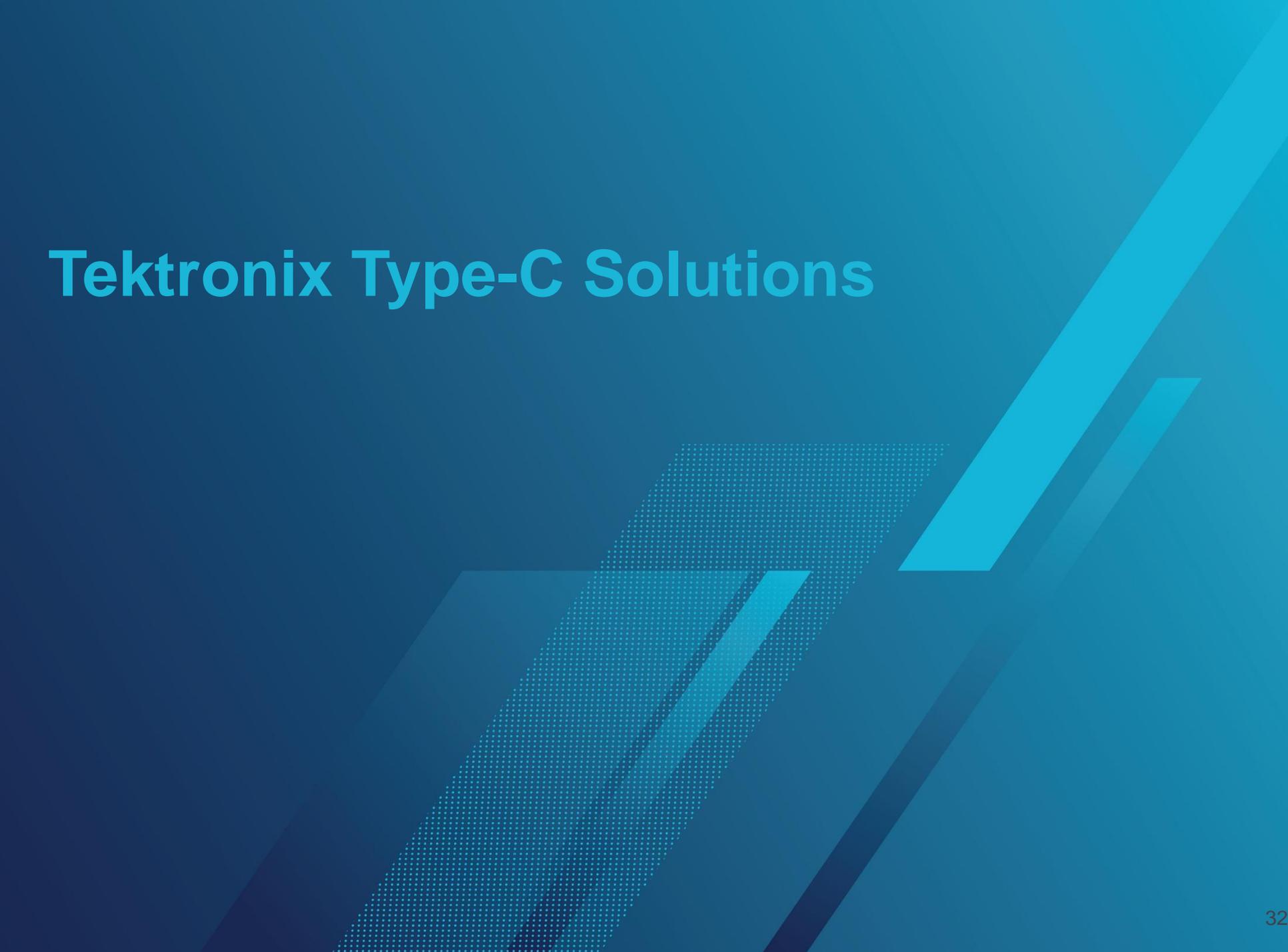
- Channel considerations
 - Need to account for > 20 dB channel loss
 - 10 Gbps requires more complicated (EQ/repeaters) signal conditioning
- New Challenges
 - 4" Long Host Channels @ 10 Gbps
 - Closed Eye at Rx
 - Equalization
 - 3 tap EQ at Tx
 - Continuous Time Linear Equalizer (CTLE) & Decision Feedback equalization (DFE) at Rx

Interoperability Challenge

- **Goal:** Any certified host works with any certified hub or device
- Short Channel
 - 1" host PCB route
 - ¼ " device PCB route
 - Direct plug
- Long channel
 - 4" host PCB route
 - 4" device PCB route
 - 1m cable

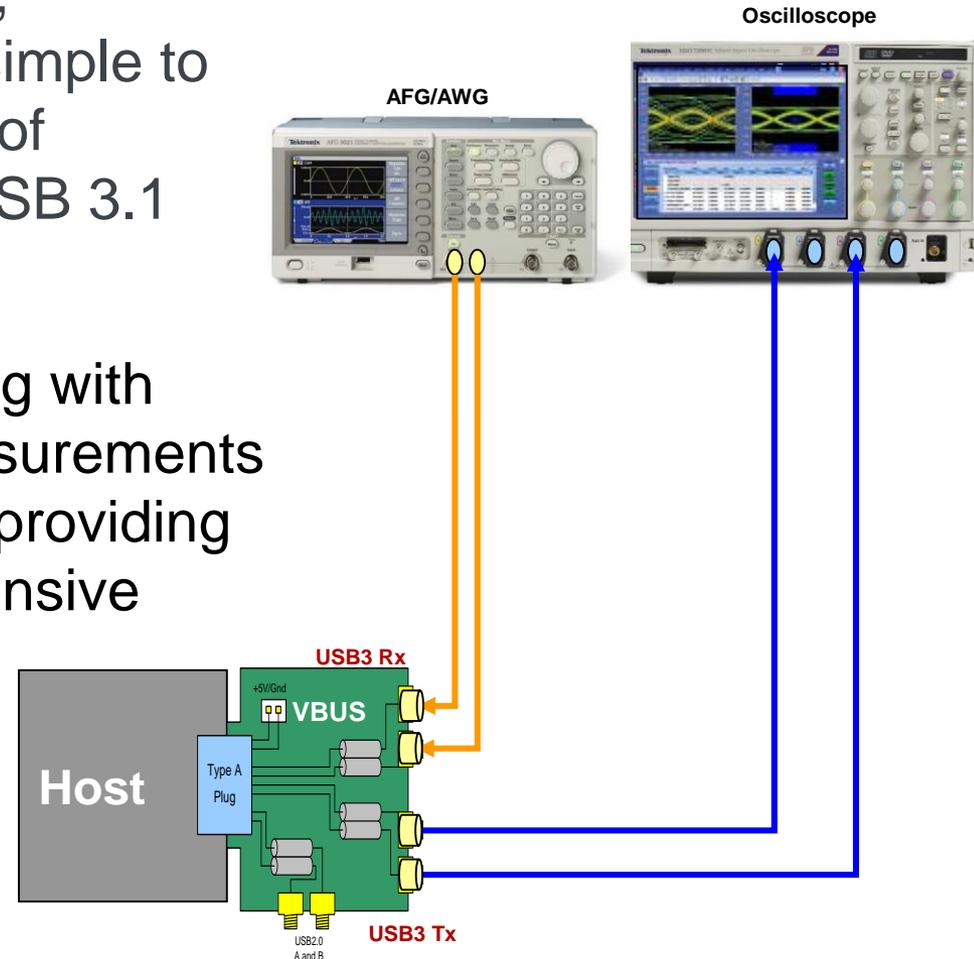


Tektronix Type-C Solutions

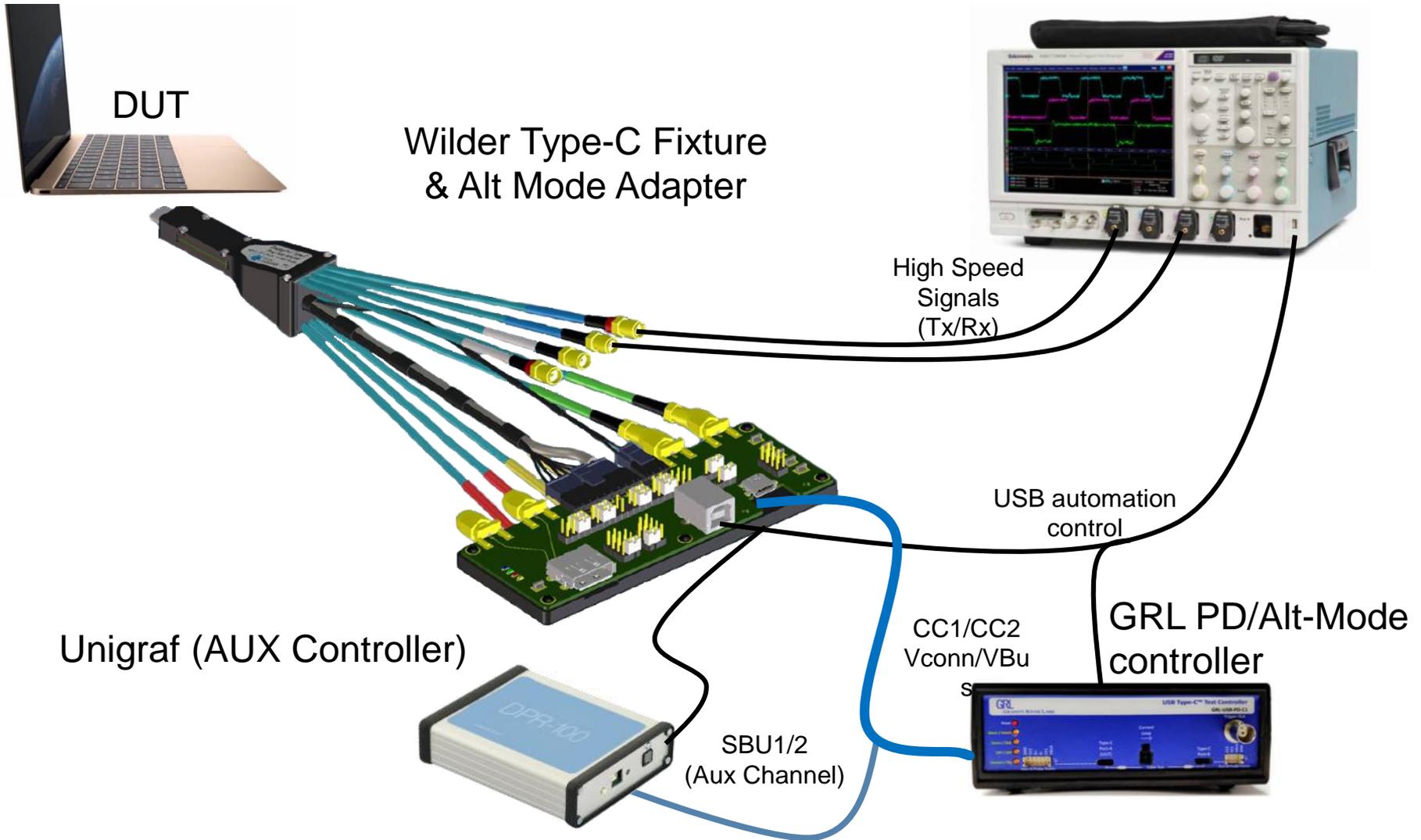
The background features several overlapping geometric shapes in various shades of blue and teal. A prominent feature is a large, tilted rectangular area filled with a fine halftone dot pattern. The overall design is modern and technical.

USB 3.1 Transmitter test

- Tektronix offers test efficiency, automation capability, and a simple to use solution for a wide range of measurements required for USB 3.1 certification.
- In addition to automated testing with TekExpress, all USB 3.1 Measurements are implemented in DPOJET providing the engineer with a comprehensive debug environment



Tek DP Type-C solution



Thunderbolt 3 Transmitter Testing

- 21GHz scope BW required for TX testing
 - 70000DX offers 100Gs/sec on 2-ch
 - 10psec sample interval, 5 samples/UI
 - Available up to 33GHz
 - 70000SX offers 200Gs/sec on 2-ch
 - Available in 33GHz, 50GHz, and 70GHz versions
 - 5psec sample interval, 10 samples/UI
 - 30% noise improvement >20GHz



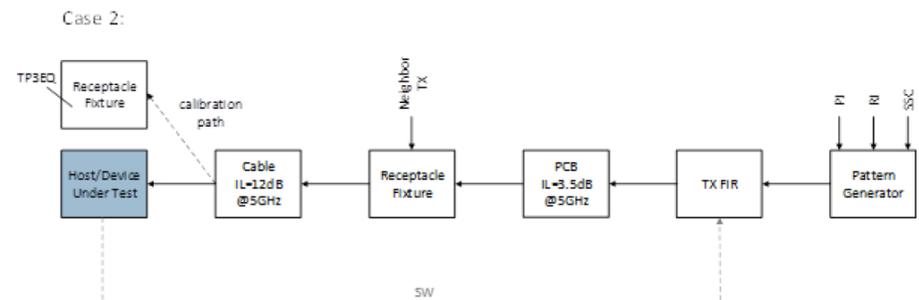
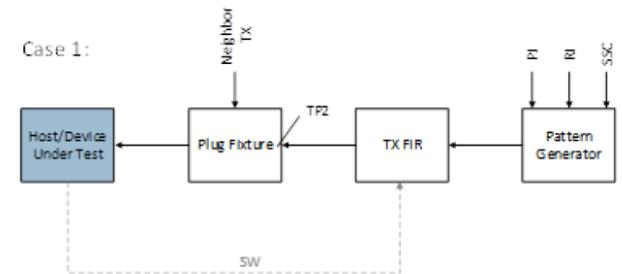
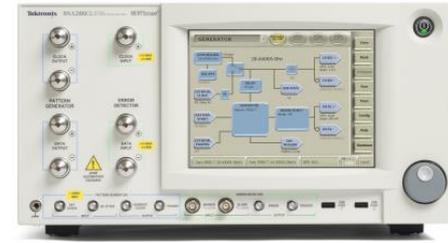
70000DX



70000SX

Thunderbolt 3 Receiver Testing

- Error detection and counting performed by the Thunderbolt device (DUT), no BERT error detector nor loopback used
- 20Gb/s BERT with 3-tap pre-emphasis required for pattern and stress generation
- Tek offers no-mux BERT at 28.6Gb/s
- Recommended configuration
 - (1) 28.6Gb/s BERTScope with stress option
 - (1) 3rd party TX Eq processor (Anritsu 4-tap DPP)
 - (1) ISI board
 - (1) AC CMI noise combiner (Pickoff T-s)
- Calibrate stresses at TP2 & TP3EQ
 - Calibration with PRBS15
 - DPOJET measurements
- Target BER of 1E-12 or lower
- Test with PRBS15 pattern
- Granite River Labs automated RX SW



Summary

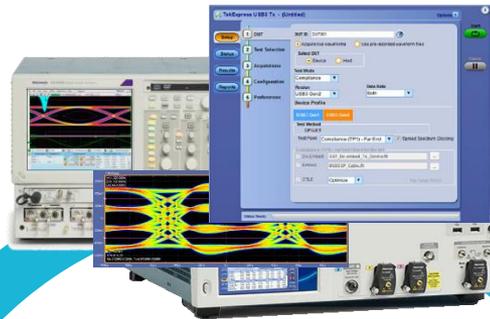
Test Challenge	Tektronix Advantage	Customer Benefits
Long list of required compliance tests	Fully automated TekExpress test solution	Test efficiency, automation capability, and a simple to use solution for a wide range of measurements required for USB 3.1 certification
When compliance test fails, how to do root-cause analysis on the test to determine compliant behavior is really hard and wastes time.	All USB 3.1 Measurements are implemented in DPOJET providing the engineer with a comprehensive debug environment	Customers can go beyond compliance test to characterize their devices by configuring measurement settings to closely model actual silicon
Lack of real-world impairments limits ability to stress their RX design's stability	The BERTScope allow customers to define custom SSC profiles, bit rates, and accurate de-emphasis settings	The engineer stress their RX design beyond compliance to ensure interoperability
Lack of loopback and high frequency SJ errors continues to be the leading cause of Rx test failures	BERTScope-based USB3.1 solution includes flexible loopback controls and user-defined margin analysis	Ensure higher confidence in design performance by going beyond

- Tektronix is the only company that provides an integrated debug solution to enable finding root causes for signal integrity problems

Complete Test solutions for Type-C Technologies

Characterize TX Performance RT Scopes

- Measure Signal Integrity and Jitter Parameters
- TekExpress automated compliance



Characterize RX Performance BERTScope

Interoperability, Validation, Debug RT Scopes and BERTs

- Link Training Debug
- Protocol Debug and Validation

