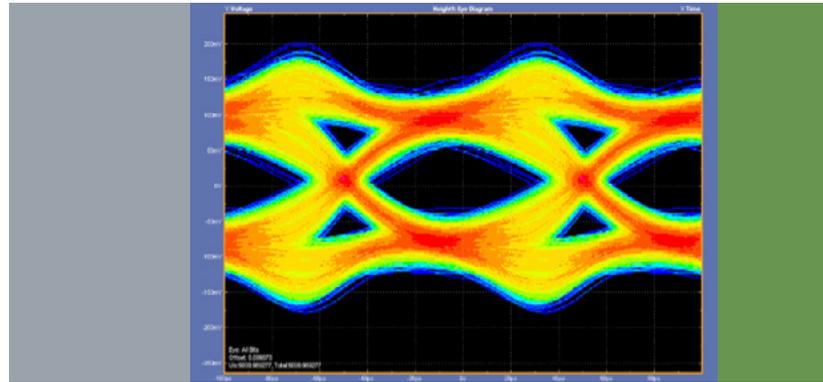


TekExpress USB - [Untitled]

Overall Test Result

Test Name	Pass/Fail	Value	Margin
UI-Unit Interval	Pass	200.423 ps	492.963 fs & 627.037 fs
High Limit	Pass	201.06 ps	
Low Limit	Pass	199.94 ps	
Vto-Diff-PP-Differential I/P Tx voltage swing	Pass	263.475 mV	183.475 mV & 916.525 mV
High Limit	Pass	1.2 V	
Low Limit	Pass	100.0 mV	
TCDR_Slow_Max_Maximum Slew Rate	Pass	3.063 m/s	6.337 m/s
High Limit	Pass	10.0 m/s	
Low Limit	N/A	N/A	
Mask Hits	Pass	0.000	0.000
DJ-Tx deterministic jitter-Dual Dirac	Pass	39.710 ps	46.290 ps
Eye Height Transmitter Eye Mask	Pass	171.099 mV	71.099 mV & 1.029 V
High Limit	Pass	1.2 V	
Low Limit	Pass	100.0 mV	
Width@0dB	Pass	111.861 ps	43.861 ps
High Limit	N/A	N/A	
Low Limit	Pass	68.0 ps	
Rj-Tx random jitter-Dual Dirac	Pass	1.290 ps	2.000 ps



# Simplifying Validation and Debug of USB 3.1 Designs

## Application Note

### Introduction

This application note will explain the evolution of the Universal Serial Bus (USB) standard and testing approaches that have been developed to accommodate the increasing speed and complexity of this popular communications standard.



Figure 1. TekExpress USB2 High speed compliance software.

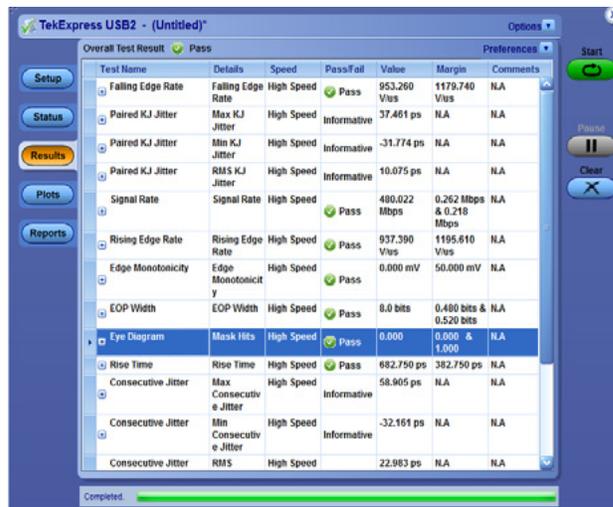


Figure 2. TekExpress USB2 test results.

## History of USB 2.0

Universal Serial Bus has become known as the de facto standard for connecting personal computers and other peripheral devices. USB 2.0 was introduced in 2000 with 40x speed improvement over the legacy USB 1.1 specification. This specification opened the door for a more data-intensive applications and an improved user experience. While the low speed (1.5 Mb/s) and full speed (12 Mb/s) rates were sufficient for devices like keyboards or mice the high speed rate (480 Mb/s) supported developments in the area of multimedia, data storage and transfer, and other high speed i/o applications.

## USB 2.0 Architecture, Test Strategy and Solutions

USB 2.0 is a serial bus that utilizes a 4-wire system — VBUS, D-, D+ and Ground. D and D+ are the prime carriers of the information. There are three main groups of USB implementations: a host, device, and hub. USB 2.0 devices can be either self-powered (having their own power supply) or bus-powered (drawing power through the host).

The USB Implementers Forum (USB-IF) has outlined a set of required compliance tests for product certification which ensures robustness and interoperability. Products that meet the minimum performance levels for the USB-IF Compliance Program are added to the Integrators List. The scope of this application note focuses on performing electrical tests and providing guidance for debugging and resolving test issues.

Figure 1 shows the operation of the option USB2 compliance test package on a DPO7254C oscilloscope. This test package fully automates the signal quality test process, allowing designers to easily test their designs. A user must select the measurements to be performed for a particular signal speed (low, full or high speed). The test package eliminates manual, time consuming oscilloscope set-ups, cursor placements and can automatically compare test results with USB 2.0 specifications. Results are automatically displayed with pass/fail criteria and margin results, as illustrated in Figure 2.

	USB 3.1	USB 2.0
Data Rate	5 (gen1) and 10 (gen2) Gb/s	480 Mb/s
Signaling	8b/10b (gen1) and 128b/132b (gen2), AC coupling, Spread Spectrum Clocking (SSC)	NRZI encoding, DC coupling, No SSC
Bus Power	150mA for un-configured power and 900 mA for configured power. Option Power Delivery class supports up to 100 watts	100 mA for un-configured and suspended devices and up to 500 mA for configured devices
Plug and Play/ Hot Swapping	Asynchronous event handling	Device polling
Power management/ Link Control	Optimized Power Management with idle, sleep and suspend states	Port-level suspend with entry/exit latency
Cable/Interface	2 Differential pairs, Half Duplex, Unshielded twisted pair with Type A/B connectors. 4 Differential pairs, Half Duplex, Unshielded twisted pair iwth Type C connector	3 Differential pairs, Full Duplex, Shielded twisted pair

Figure 3. Physical layer differences between USB 2.0 and 3.1.

## USB 3.1 and Physical Layer Test Challenges

USB 2.0 technology adoption and acceptance highlights its success as a high bandwidth bus. The continued evolution of computing and data storage applications has presented new opportunities and challenges. Industry trends such as increasing memory storage capacities, accelerated video performance such as real-time video streaming and enhanced graphics processing units (GPU), and fast syncing of portable electronic devices with PCs have created a bottleneck with USB 2.0 performance.

USB 3.1 addresses the need for increased bandwidth to support applications that provide a more real-time experience. With billions of USB devices in use USB 3.1, referred to as SuperSpeed USB, also provides the necessary backwards compatibility to support legacy USB 2.0 devices. A list of physical layer differences between USB 2.0 and 3.1 are shown in Figure 3.

Along with new capabilities SuperSpeed USB also brings new design and test challenges. USB 3.1 shares similar characteristics found in existing high speed serial technologies such as PCI Express® 8b/10b (1/2.0) and 128b/130b (3.0) encoding, significant channel attenuation, and spread spectrum clocking. Those familiar with test methods for PCIe may be more prepared to handle the test challenges associated with USB 3.1. We'll review methods for compliance and how to get the most accurate, repeatable measurements possible for transmitters, receivers, cables and interconnects. Additional techniques for thorough characterization and debug will be presented to provide a complete test strategy.

Compliance Pattern	Value	Bit Sequence Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences.
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist frequency/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1's and 0's	With de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP8	50-250 1's and 0's	Without de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP9		Pseudo-random data pattern (see section 6.4.4.1)
CP10	AAh	Nyquist pattern at 10Gb/s. This is not 128b132b encoded.
CP11	CCh	Nyquist/2 at 10Gb/s. This is not 128b132b encoded.
CP12	LFSR15	Uncoded LFSR15 for PHY level testing and fault isolation. This is not 128b132b encoded. The polynomial is $x^{15}+x^{14}+1$
CP13	64 1's and 0's	With pre-shoot defined in section 6.7.5.2 (no de-emphasis). Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP14	64 1's and 0's	With de-emphasis defined in section 6.7.5.2 (no pre-shoot). Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP15	64 1's and 0's	With pre-shoot and de-emphasis defined in section 6.7.5.2. Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP16	64 1's and 0's	No de-emphasis or pre-shoot. Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.

Figure 4. USB 3.1 Gen1 and Gen2 Compliance Patterns (from table 6-13 of standard).

Signal Characteristic	5GT/s			10GT/s			Unit	Note
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum		
Eye Height	100		1200	70		1200	mV	2,4
Dj			0.43			0.530	UI	1,2,3
Rj			0.23			0.184	UI	1,2,3,5
Tj			0.66			0.714	UI	1,2,3

Notes:

1. Measured over  $10^5$  consecutive UI and extrapolated to  $10^{-12}$  BER.
2. Measured after receiver equalization function.
3. Measured at end of reference channel and cables at TP1 in Figure 6-19.
4. The eye height is to be measured at the minimum opening over the range from the center of the eye  $\pm 0.05$  UI.
5. The Rj specification is calculated as 14.069 times the RMS random jitter for  $10^{-12}$  BER.

Figure 5. USB 3.1 Transmitter Eye height and jitter requirements.

## Transmitter Testing

### Compliance Measurements

Transmitter testing is facilitated through the use of various test patterns, which are listed in Figure 4. Each pattern was selected for characteristics relating to the test under which the pattern is evaluated. CP0, a D0.0 scrambled sequence running at 5 Gb/s, is used to measure deterministic (Dj) jitter such as data-dependent jitter (DDJ) while CP1, an unscrambled D10.2 full rate 5 Gb/s clock pattern, doesn't produce DDJ and is therefore better suited for evaluating random jitter (Rj). The equivalent gen2 compliance patterns for Dj and Rj are CP9 (scrambled 00h) and CP10 (10 Gb/s clock) respectively

Jitter and eye height are measured with 1 million consecutive unit intervals after applying an equalizer function and appropriate clock recovery settings (2nd order PLL, closed loop bandwidth of 10 MHz (gen1)/ 15 MHz (gen2) and damping factor of 0.707). Jitter results are calculated by projecting beyond the measured data population to quickly extract jitter performance at  $1 \times 10^{-12}$  BER levels. For example, with jitter extrapolation the target Rj is calculated by multiplying measured Rj (rms) by 14.069.

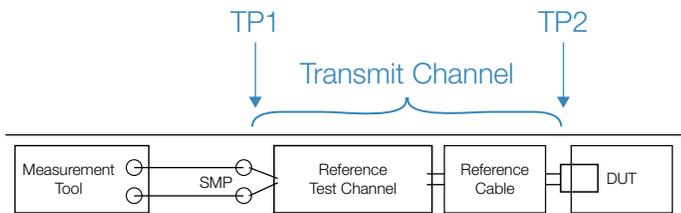


Figure 6. Transmitter test points.

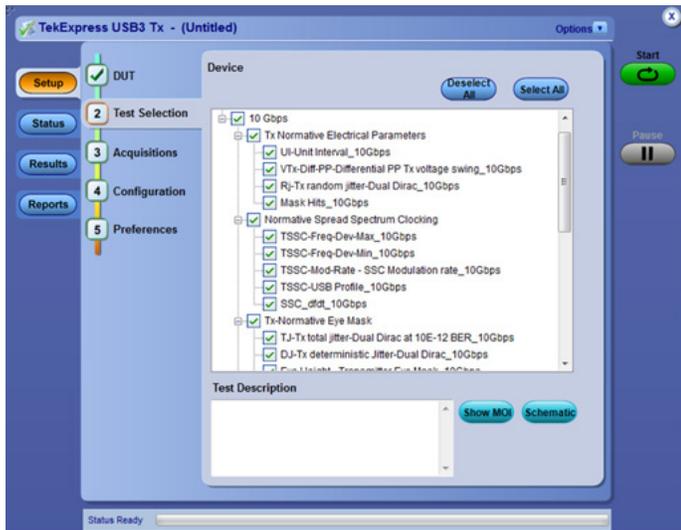


Figure 7. DPO/DSA70000 Series Option USB-TX for USB 3.0 Normative and Informative measurements.

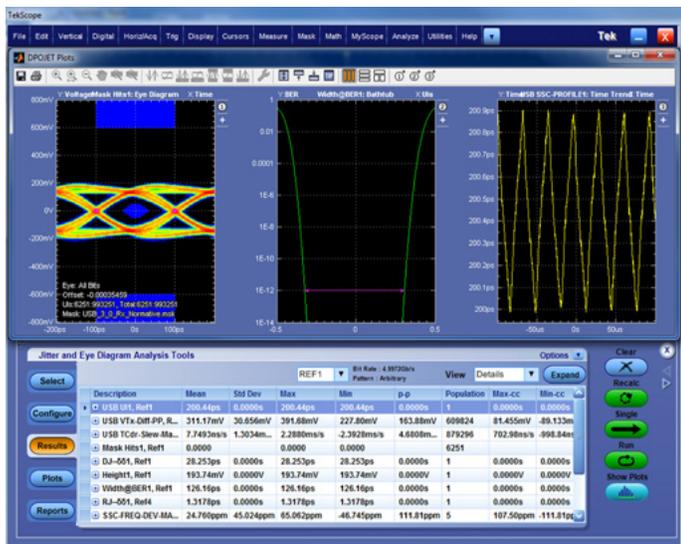


Figure 8. USB 3.0 debug with DPOJET including custom control settings.

Figure 6 shows the normative transmitter compliance setup including the reference test channel and cable. Test point 2 (TP2) is located closest to the device under test (DUT) while test point 1 (TP1) is the far end measurement point. Note all Tx normative measurements are performed on signals at TP1.

After the signal is acquired at TP1 the data is processed using a software tool called SigTest, similar to official PCI Express compliance testing. For applications that require pre-compliance, characterization or debug other tools are available that provide additional insight into design behavior over varied conditions or parameters. The Tektronix MSO/DPO/70000 Series Oscilloscopes with option USBSSP-TX enables execution of the USB 3.1 PHY layer transmitter tests as shown in Figure 7. Single-button automation software tools like USBSSP-TX save time by ensuring the test equipment is configured properly. This enables the testing to be accurately run by lab technicians instead of a senior engineer who has deep domain expertise in the USB specification. After the tests complete a detailed pass/fail test report highlights where design issues may occur. If there are discrepancies between different test locations (e.g. company lab, test house, etc.) the tests can be run again using the saved data from previous test run.

The TekExpress test automation software with Option USBSSP-TX leverages the characterization and debug environment built upon the general purpose analysis capabilities of DPOJET. A flexible jitter and eye analysis software package provides more user-defined control of analysis parameters which helps speed in troubleshooting and makes design characterization much easier. For example, multiple eye diagrams can be displayed at one time allowing the user to analyze the effects of different clock recovery techniques or software channel models. Also different filters can be applied to analyze the effects of SSC for resolving system interoperability issues.

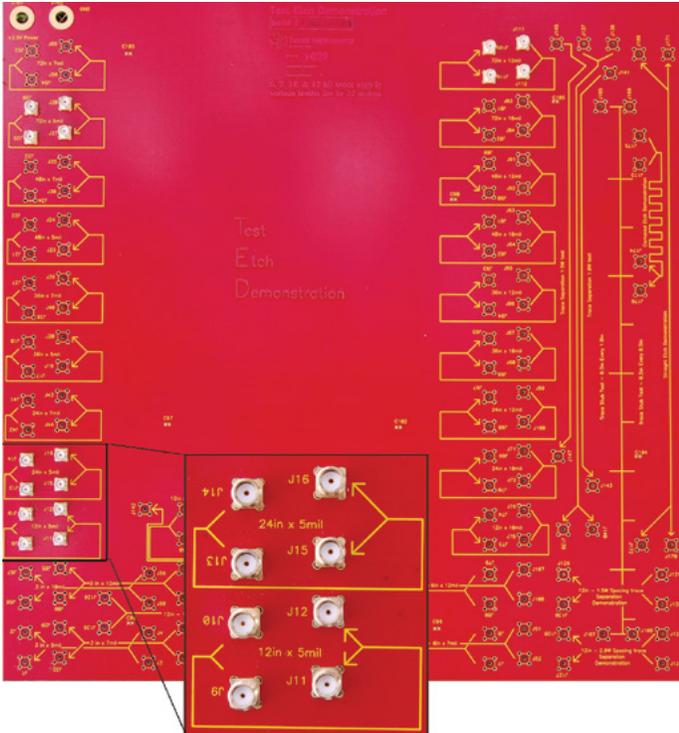


Figure 9. ISI board with 12 and 24 inch traces.

## Reference Test Channels

There are two methods for capturing ‘far end’ signals at TP1. The first method is to use hardware-based cables and fixtures from USB-IF and acquire the data at TP1. The second method is to simulate the hardware channel effects in software using extracted models from TDR, VNA, or a simulator. The generally accepted channel model is an S-Parameter file, which includes magnitude and phase response effects. The signal is first acquired at TP2 or closest to the transmitter. The acquired data is then convolved with the S-Parameter file, which has been converted to a Finite Impulse Response (FIR) filter (for more information about applications for filters on Tektronix oscilloscopes see the white paper “Arbitrary FIR Filter Theory, Design, and Application” on [www.tektronix.com](http://www.tektronix.com)).

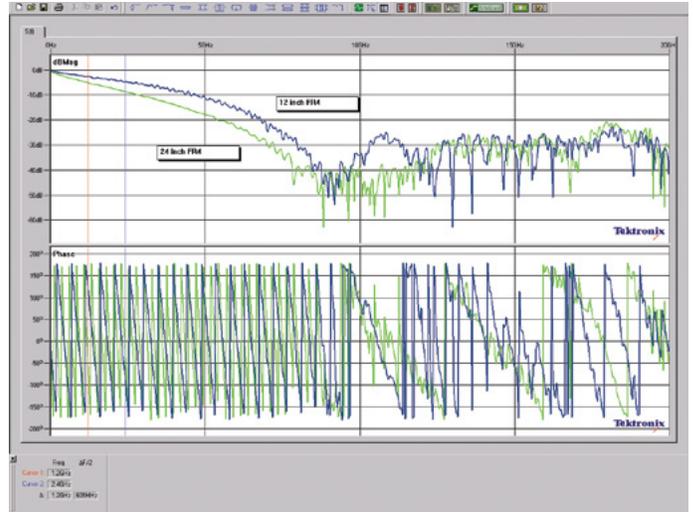


Figure 10. Magnitude and Phase response of 12 and 24 inch PCB traces.

This method allows the engineer to measure the device under test with specific channel requirements that are variable but also repeatable. For example, let’s compare measurements of a 5 Gb/s signal across varying PCB trace lengths. Figure 9 shows an ISI test board with connections to 12 and 24 inch traces and Figure 10 provides the corresponding Sdd21 channel response.

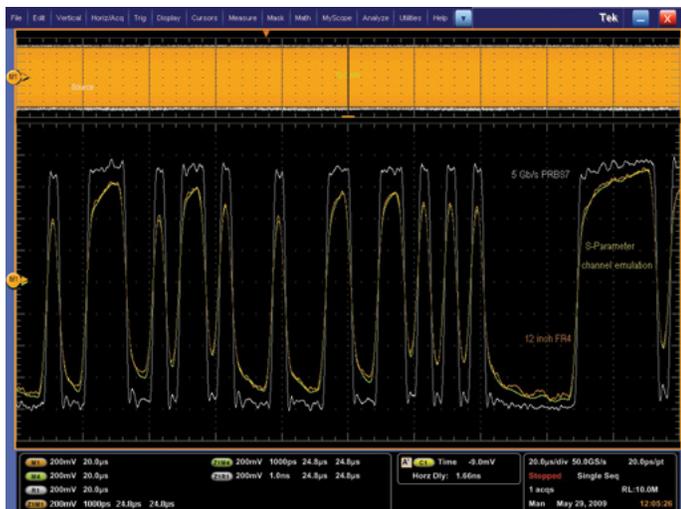


Figure 11. Hardware channel vs. Software emulation of 12 inch trace.



Figure 12. Hardware channel vs. Software emulation of 24 inch trace.

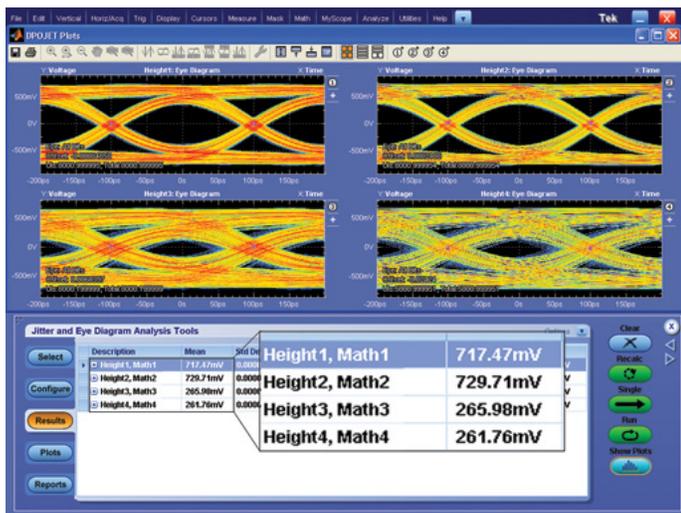


Figure 13. 5 Gb/s eye diagrams after 12, 24 inch traces with hardware (left) and software (right) channels.

The test signal is acquired both with and without the hardware channel included. Figures 11 and 12 show the original signal (white), far end hardware response (orange), and the original signal convolved with the S-Parameter data for each trace length. Figure 13 includes the eye diagrams from the hardware and software based test data.

## Equalization

With significant channel attenuation SuperSpeed USB requires some form of compensation to open the eye at the receiver. To accomplish this, equalization, in the form of de-emphasis, is used at the transmitter. The nominal de-emphasis ratio specified is 3.5 dB or 1.5x in linear scale. As an example, with a transition bit level of 150 mV pk-pk the non-transition bit level would be 100 mV pk-pk. A 3-tap equalizer model is defined for USB 3.1 gen2. This model uses de-emphasis as well as pre-shoot. The normative settings for de-emphasis and pre-shoot are -3.1 dB and 2.2 dB respectively. De-emphasis is a negative value as the ratio of the non-transition bit is smaller than the transition bit. The opposite is true for pre-shoot, hence this is why the ratio is a positive value.

The gen1 compliance equalization model is a Continuous Time Linear Equalizer (CTLE). CTLE implementations include on-die, active receiver equalization or passive high frequency filters such as those found on cable equalizers. This model is well suited for compliance testing because of its simplicity in describing the transfer function. A CTLE is implemented with a set of poles and zeros in the frequency domain resulting in peaks at desired frequencies. As mentioned above, the TekExpress software with option USBSSP-TX includes the reference compliance channels as well as the required CTLE filter, all combined into a single file. T

The gen2 compliance equalizer is also a CTLE model but uses an Aac gain parameter along with a two-pole system. The Aac parameter is set to 3 dB which provides an overall high gain profile, which is needed for the high loss expected for gen2. In addition to the CTLE, USB 3.1 gen2 also uses a 1-tap Decision Feedback Equalizer (DFE) model. This is an adaptive non-linear equalizer that has a maximum tap value defined at 50mV.

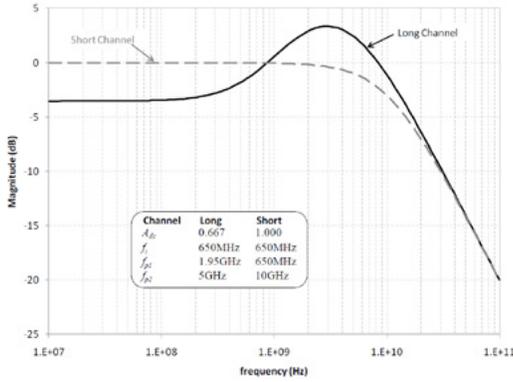


Figure 14b. USB 3.0 USB 3.1 gen1 CTLE transfer function and magnitude response.

$$H(s) = \frac{A_{dc} \omega_{p1} \omega_{p2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

$$A_{dc} = 0.667$$

$$\omega_z = 2\pi(650 \times 10^6)$$

$$\omega_{p1} = 2\pi(1.95 \times 10^9)$$

$$\omega_{p2} = 2\pi(5 \times 10^9)$$

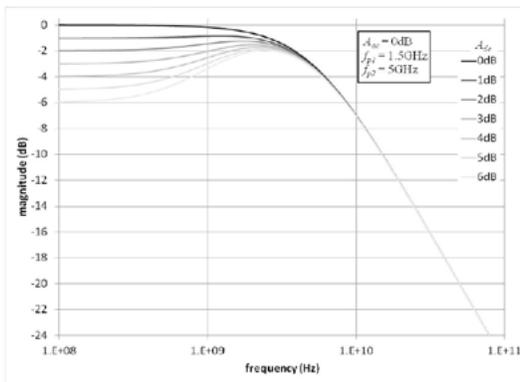


Figure 14b. USB 3.0 USB 3.1 gen1 CTLE transfer function and magnitude response.

$$H(s) = A_{ac} \omega_{p2} \frac{s + \frac{A_{dc}}{A_{ac}} \omega_{p1}}{(s + \omega_{p1})(s + \omega_{p2})}$$

where  $A_{ac}$  is the high frequency peak gain

$A_{dc}$  is the DC gain

$\omega_{p1} = 2\pi f_{p1}$  is the first pole frequency

$\omega_{p2} = 2\pi f_{p2}$  is the second pole frequency

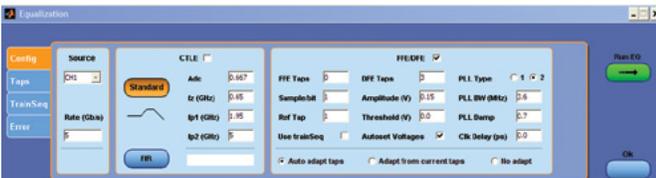


Figure 15. SDLA equalization configuration for CTLE, FFE, and DFE.



Figure 16. 5 Gb/s signal (yellow) after de-emphasis (blue), long channel (white), CTLE (red) and 31 tap DFE (grey).

In addition to using compliance filters provided in the TekExpress automation software, designers can use the Tektronix Serial Data Link Analysis (SDLA) software to validate different CTLE parameters and how they impact link performance. Advantages of CTLE implementations are that they are simpler to design and they consume less power than alternative techniques. However in some instances they may not be adequate due to limitations in adaptation, precision, and noise amplification. Alternative techniques include Feed-Forward (FFE) and Decision-Feedback (DFE) equalization, which uses data samples weighted with scale factors to compensate for channel loss. CTLE and FFE are linear equalizers and as such both suffer from signal to noise degradation through boosting of high frequency noise. DFE, however, uses a non-linear component in a feedback loop thereby minimizing noise amplification and compensating for ISI. Figure 16 shows a 5 Gb/s signal after significant channel attenuation along with the equalized signals using de-emphasis, CTLE, and DFE techniques.

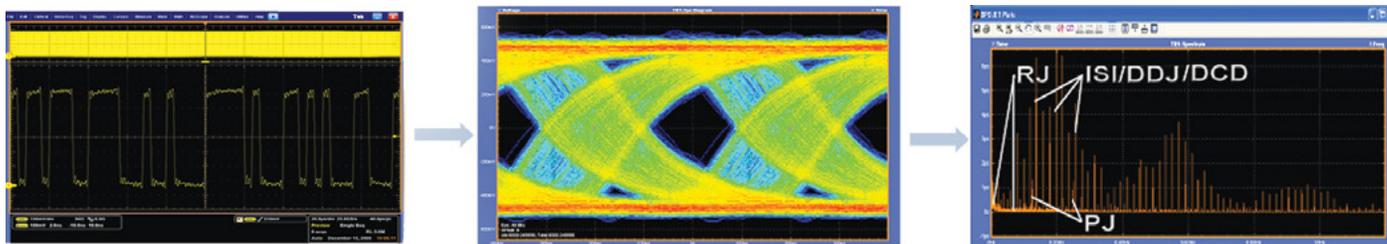


Figure 17. DPOJET software for advanced serial data characterization and debug.

## Characterization and Debug

Throughout the process of design characterization and compliance testing invariably debug tools will be needed to resolve signal integrity or jitter issues. With added complexity of reduced margin for circuit and link problems silicon designers and system integrators need tools that incorporate intelligent statistical analysis capabilities along with visualization tools such as histogram, jitter spectrum, and BER “bathtub” plots. DPOJET analysis plots, like Spectrum and Trend, provide insight beyond simple measurements and results display. Trend analysis shows how timing parameters change over time, like frequency drift, PLL startup transients, or a circuit’s response to power supply changes. Jitter spectrum analysis can show the precise frequency and amplitude of jitter and modulation sources such as adjacent oscillators and clocks, power-supply noise, or signal crosstalk.

After a failure occurs it’s important to be able to switch from “compliance-mode” using automated test software to a “user-defined” jitter and eye analysis toolset. The DPOJET software provides users with control over parameters such as clock recovery, filters, reference levels, Rj/Dj separation techniques, or measurement limits and gating. It also includes many timing, amplitude, and eye measurements in addition to the standard normative and informative USB 3.1 measurements.

An example procedure for debugging and analyzing jitter is shown in Figure 17. First the data is acquired with a relatively large data population for jitter analysis including the effects of SSC. One 33 kHz SSC cycle requires a 30 us time window. Once the data is acquired eye diagram analysis provides a quick visual indication of voltage and timing performance. This eye shows excessive periodic jitter and data-dependent jitter. Finally jitter decomposition is performed to isolate signal integrity problems. The jitter spectrum plot highlights jitter components and their corresponding relative amplitude and frequencies.

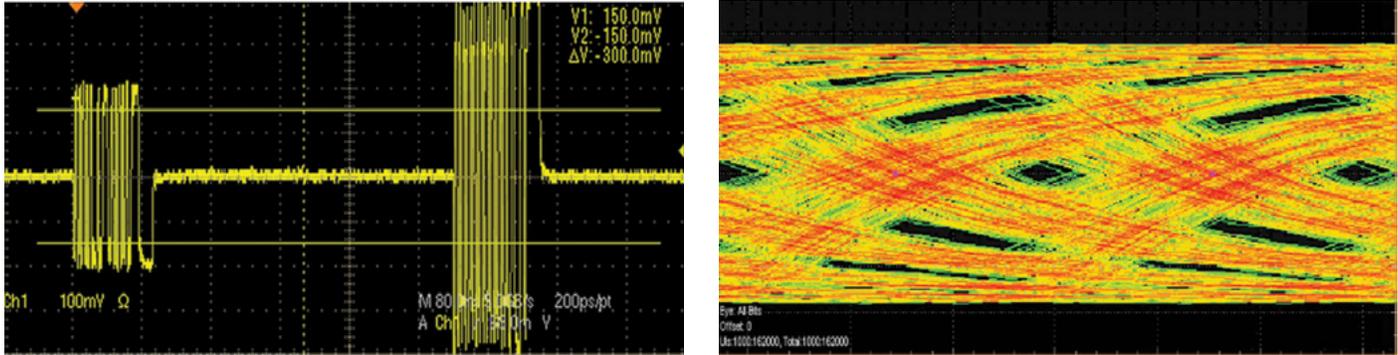


Figure 18. USB 2.0 and 3.0 receiver testing examples.

## Receiver Testing

### Compliance Testing

The purpose of USB receiver testing is to confirm a receiver's ability to correctly detect transmitted data at or below a target Bit Error Rate (BER) of  $1 \times 10^{-12}$ . While the focus of transmitter testing is on amplitude, jitter and other parametric measurements a receiver test strategy usually involves a single test: jitter tolerance. Jitter tolerance ensures a receiver system will interoperate with a high degree of confidence with other products. The conditions of interoperability may vary widely with factors such as different cable lengths, low signal amplitudes, asynchronous reference clocks, and power management and link states. A good stressed eye calibration approach will ensure that jitter tolerance is reaching as many potential conditions as possible.

USB 3.1 compliance testing has changed significantly to accommodate the new challenges associated with a higher speed interface. Validation of a USB 2.0 receiver involves performing a receiver sensitivity test. A High Speed device must respond to a test packet at or above 150 mV and ignore

(squelch) signals below 100 mV. SuperSpeed USB receivers must function with many more signal impairments and therefore the test requirements are more demanding than USB 2.0. While the USB 3.1 specification defines a target BER of  $1 \times 10^{-12}$  the receiver compliance test strategy allows for shorter test times by increasing the deterministic jitter which creates an effective BER of  $1 \times 10^{-10}$ . With increased Dj and a lower effective Rj, based on a lower BER, this results in an equivalent Tj(BER) for both target BER levels.

For characterization testing, which is often done for first article silicon, instruments such as a BERTScope may be a good choice. A BERTScope Bit Error Rate Analyzer combines the capabilities of an enhanced high performance Bit Error Rate Tester (BERT), with the eye pattern display of an oscilloscope. For test scenarios where it is important to dynamically change parameters such as data rate, jitter profile or data patterns; a BERTScope provides versatile pattern generation and BER-based troubleshooting tools that supports the complete suite of measurements required for USB 3.1 Rx testing.

## Receiver Characterization and Debug Testing

The primary basis of evaluating a receiver is determining the effective bit error rate. A known pattern is transmitted to the receiver and the data is verified after the receiver's comparator. Data is checked externally through a loopback mechanism inside the receiver. One of the challenges of receiver testing is generating the required test patterns and initiating test modes within the device under test.

Receiver testing for USB 3.1 is similar to other high speed serial bus receiver compliance testing, and is generally split up into two phases.

- Stressed eye calibration is the industry name for the procedure to create a worst case signal condition to test receivers. This worst case signal is usually impaired both horizontally by added jitter, and vertically, by setting the amplitude to the lowest a receiver would see when deployed. Stressed eye calibration must be performed when any of the test fixtures, cabling, or instrumentation have been changed.
  - Jitter tolerance tests the receiver by using the calibrated stressed eye as input, and then applies additional sinusoidal jitter (SJ) of increasing frequency. This applied SJ exercises the clock recovery circuitry inside the receiver, so not only is the receiver being tested using worst case signal conditions, but its clock recovery is also explicitly tested. The magnitude and frequency of the applied SJ follows a template as prescribed by the standard. This jitter tolerance template covers the bandwidth of the clock recovery PLL; high amounts of applied SJ should be tolerated within the loop bandwidth since the clock recovery will track out this sinusoidal jitter, but only small amounts can be withstood beyond the loop bandwidth, since this jitter is not tracked out, and will affect the downstream receiver circuit.
- This characterization process can be automated, ensuring accurate results and proper stressed pattern generation capability. Here is a review of the automated characterization functionality:
- Loopback initiation provides users who may otherwise be unable to perform receiver testing. Loopback initiation is a specific handshake between the BERTScope and device under test (DUT) that prepares the DUT for receiver testing. This is a key step that is a challenge for many customers, regardless of test instrumentation.
  - Automated stressed eye calibration simplifies a procedure that can otherwise be tedious and time consuming.
  - Jitter Tolerance testing is performed with a single click, and results are stored in a database for straightforward management of test results. The automated Jitter Tolerance test can also search for the limits of the device, termed "search for margin."

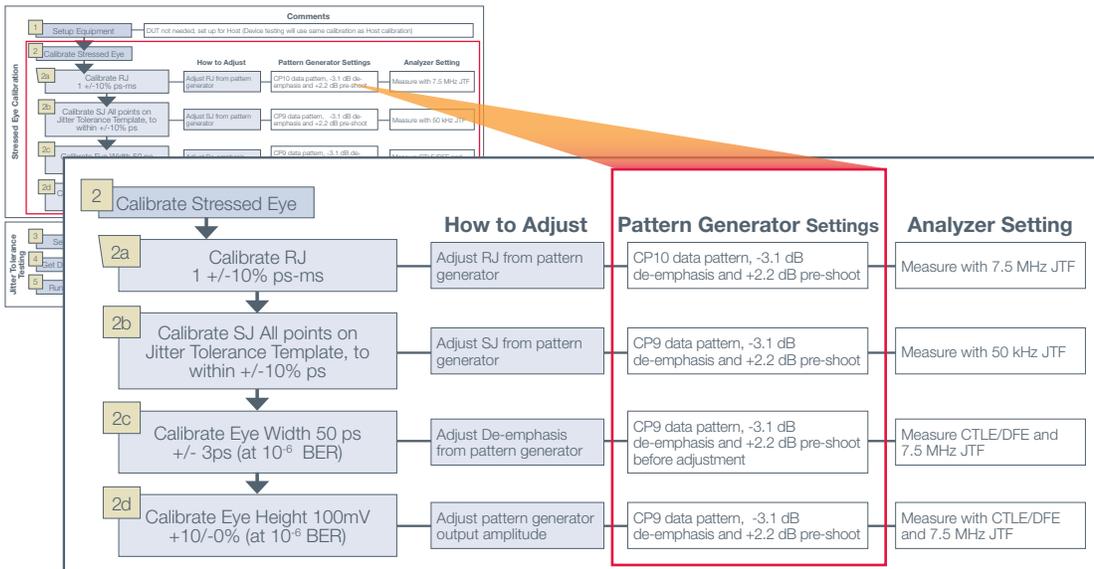


Figure 19. Pattern Generator Settings used for Stressed Eye Calibration, including specifications for data pattern, de-emphasis level, and spread spectrum clocking (SSC).

## Stressed Eye Calibration

Stressed eye calibration involves first setting up the test equipment with compliant fixtures, cables, and channels, and then iteratively measuring and adjusting various types of applied stresses such as jitter. The calibration step is performed without the DUT, with compliant test fixtures and channels, and with specific data patterns generated by the test equipment.

### Sinusoidal Jitter (SJ)

- Definition:** SJ is bounded jitter that is periodic in nature, but usually not correlated to the data pattern (unless the SJ frequency just happens to be a multiple of the pattern repetition frequency), so like RJ, its measurement is the same regardless of data pattern. Unlike RJ, it does not grow with measurement depth due to its bounded nature.
- How to adjust:** Like RJ, the pattern generator must be able to adjust the amount of injected SJ to achieve the desired amount. The injected SJ must be of a particular frequency, with adjustable amplitude. All SJ frequencies and amplitudes in the USB 3.1 Jitter Tolerance Mask (above right) need to be calibrated.
- How to measure:** The USB 3.1 compliance test procedures specify that the amount of SJ should be measured by taking the difference in Total Jitter (TJ) between a signal with 0 amplitude of injected SJ, and the desired amount of injected SJ. TJ measurements can be found on most oscilloscopes.

### Eye Height

- Definition:** Eye height is the opening of the eye in the center of the unit interval and is accompanied by a measurement depth, in this case,  $10^6$  waveforms. The eye height is data pattern dependent because it is impacted by the amount of Data Dependent Jitter (DDJ) in the signal.
- How to adjust:** The eye height is adjusted via the output amplitude of the pattern generator.
- How to measure:** Eye height can be measured on oscilloscopes, and should meet the  $10^6$  waveforms requirement.

### Eye Width

- Definition:** Eye width is the horizontal opening of the eye and is accompanied by a measurement depth, in this case,  $10^6$  waveforms. The eye height is data pattern dependent because it is impacted by the amount of Data Dependent Jitter (DDJ) in the signal. The eye height specification is 50 ps +/-3 ps.
- How to adjust:** The eye width is adjusted via de-emphasis of the pattern generator.
- How to measure:** Eye width can be measured on oscilloscopes, and should meet the  $10^6$  waveforms requirement.

### Pattern Generator Settings

Now that we have covered “what” needs to be calibrated, we will discuss the additional requirements of the pattern generator for each step of the calibration, including:

- The data pattern to be used.
- The amount of de-emphasis and pre-shoot.
- Whether or not spread spectrum clocking (SSC) should be enabled.

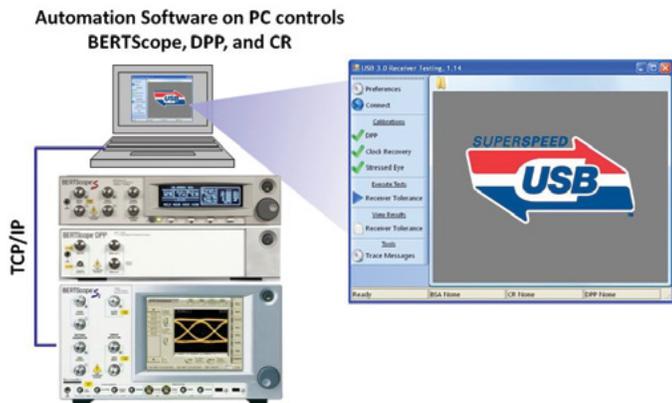


Figure 20. Setup for USB 3.0 Receiver Test.

The setup of equipment for receiver testing is similar to that of stressed eye calibration, with the DUT inserted into the test loop. Instead of the signal being routed straight back to the analyzer, the test signal from the pattern generator passes through the DUT's receiver, is "looped back" through its transmitter (hence, the term "loopback"), back through the adapter, and to the error detector. The connection to the error detector should be as high quality as possible. (See Figure 20)

For Jitter Tolerance testing, the test instrumentation must be able to perform error detection and keep track of the BER. Instruments such as BERTs and some protocol analyzers and oscilloscopes are capable of this function.

Loopback is one of the USB 3.1 link states in which the device sends the bits it receives back through its transmitter. If the receiver makes a mistake, the bit in error will be sent back through the transmitter and to the downstream analyzer for detection. To initiate loopback, a series of handshakes must be performed between the pattern generator and DUT.

USB 3.1 uses 128b/132b encoding, and as is common in 8b/10b encoded systems, the receiver and transmitter may be on slightly different clock frequencies – the recovered clock of the received data stream may not be exactly equal to the clock frequency of the transmitter. When in loopback mode for

receiver testing, this mismatch in frequencies poses a problem for the DUT; bits may be coming in faster than they can be sent back out, or vice versa. To compensate for the frequency mismatch, clock compensation symbols are used and either deleted or inserted into the data stream as it is passed from the receiver back through the transmitter. For example, symbols are added if the recovered clock frequency is less than (slower than) the transmitter clock frequency and vice versa. USB 3.1 uses SKP symbols for clock compensation.

The BERTScope BSA Series can be setup to handle this non-deterministic number of clock compensation symbols in the incoming data stream, commonly termed asynchronous BER testing. This may be difficult for some BERTs, as BER is typically measured by comparing the incoming data stream to a known data pattern. Protocol analyzers may be able to handle this mode of testing by maintaining the frame error count.

Once the stressed eye has been calibrated, the DUT and equipment have been set up for testing, and the DUT has been put into loopback mode, the DUT's receiver is ready to be tested.

Jitter tolerance testing applies varying levels of SJ amplitude at specific SJ frequencies to test the receiver. The lower SJ frequencies tend to have higher SJ amplitude, as these frequencies are well within the loop bandwidth of the CR of the receiver and will thus get tracked out. As the SJ frequency approaches the loop bandwidth and surpasses it, the SJ amplitude levels out at an amplitude less than 1 UI. Jitter above the loop bandwidth of the receiver will not get tracked out, and will be passed down to the receiver's decision circuit.

The USB 3.1 CTS specifies that each SJ point on the tolerance curve be tested using 3x10<sup>10</sup> bits. The DUT fails if more than one error is detected at any SJ test point.

For proper USB 3.1 receiver testing, the test regimen is wholly based on Jitter Tolerance using a calibrated stressed eye input. For receiver characterization and debug; the BERTScope BSA Series combines the calibrated stressed eye setup and automation capability to ensure a successful receiver test troubleshooting environment.

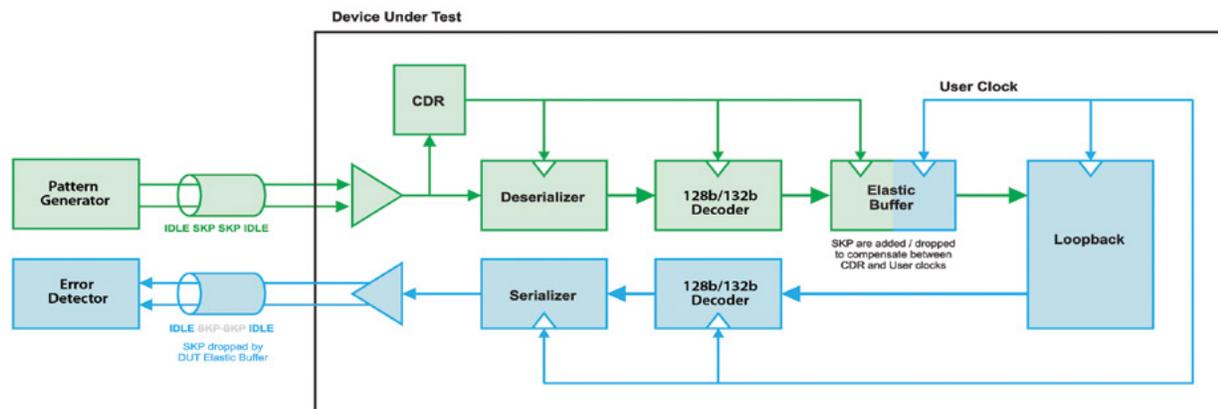


Figure 21. Frame Error Detection with AWG and Oscilloscope.

## Channel Emulation and Automation

With 5 Gb/s signaling and long channels and cables this results in a closed eye at the receiver requiring equalization. Test specification developers define the requirements of a channel that will enable testing to worst case conditions, but practical enough for engineers to design and manufacture products in a cost-effective and efficient manner. After the channel model and budget are created they are validated to ensure actual physical layer performance matches expected results. Software simulation tools provide many degrees of freedom and allow for quick modeling and corner case testing. However at some point the model has to be produced into a physical channel for verification. Usually a reference design is fabricated on a PCB that provides similar electrical characteristics to the specification.

An alternative method to creating a channel model in hardware is to convert the model into a differential S-Parameter file and convolve the channel, including magnitude and phase effects, with the signal generator's test pattern. This method allows the engineer to drive the device under test with specific channel requirements that are variable but also repeatable. There are software tools available, such as Tektronix BERTScope BSAUSB3, which can automate complex signal generation for USB 3.1 receiver testing by integrating all impairments into one signal. Complex jitter components such as  $R_j$ ,  $S_j$ , ISI, custom SSC modulation profiles and pre-emphasis can be added simultaneously to create complex channel models that are often seen in real world environments. Figure 22 show the USB3 Receiver Test Automation Tools for consistent pattern generation and device control.

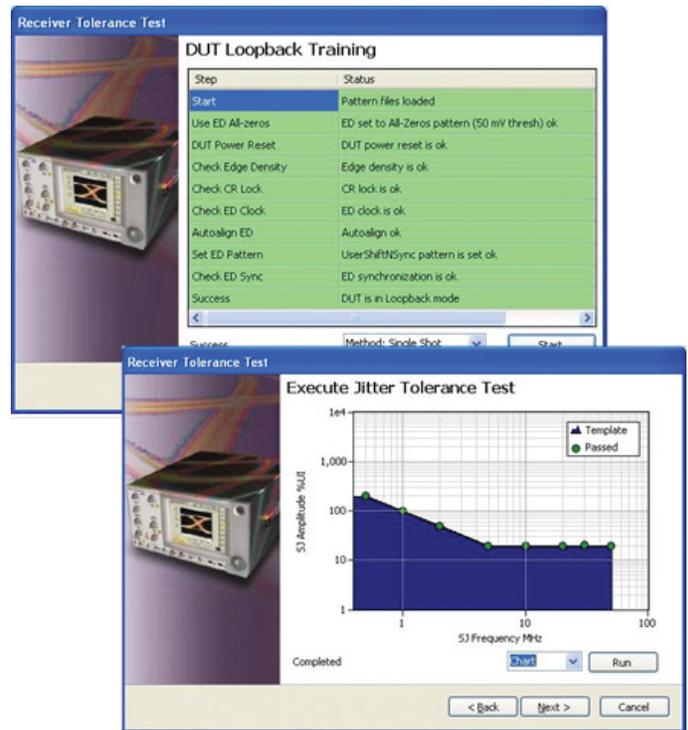


Figure 22. BSAUSB3 Automation Software setup screens.

## Channel Measurements

### Compliance

At 10 Gb/s data rate, anything that affects a signal's rise time, pulse width, timing, jitter or noise content can impact reliability at the system level. To ensure signal integrity, it is necessary to understand and control impedance and losses in the transmission environment through which the signals travel. Mismatches and variations can cause reflections that decrease signal quality as a whole. USB 3.1 channel compliance helps minimize potential sources of performance degradation. The list below includes the required USB 3.1 channel measurements. The DSA300 sampling oscilloscope, 80E04 TDR module with IConnect measurement software and A/B/C receptacle test fixtures provide complete channel compliance testing.

1. Impedance
2. Intra-Pair Skew
3. Differential Insertion Loss
4. Differential Return Loss
5. Differential Near-End Crosstalk
6. Differential Crosstalk between USB3.1 and USB2.0 Pairs
7. Differential to CM Conversion



**Figure 23.** DSA300 Sampling oscilloscope with IConnect TDR/S-Parameter measurement software.

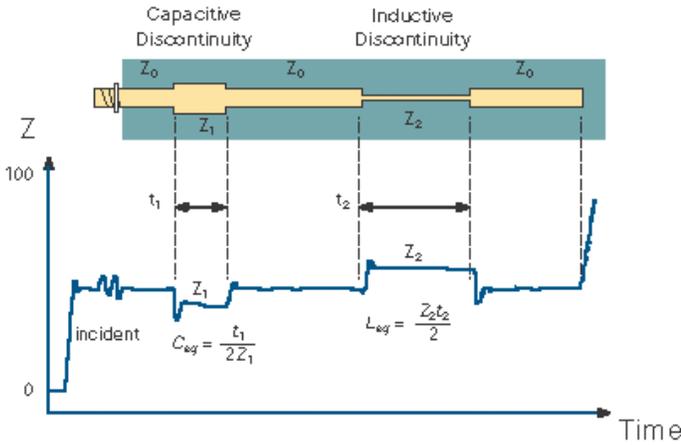


Figure 24. TDR uncovers impedance discontinuities.

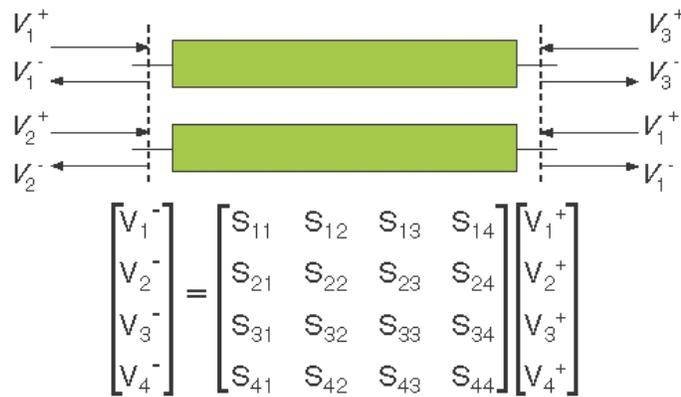
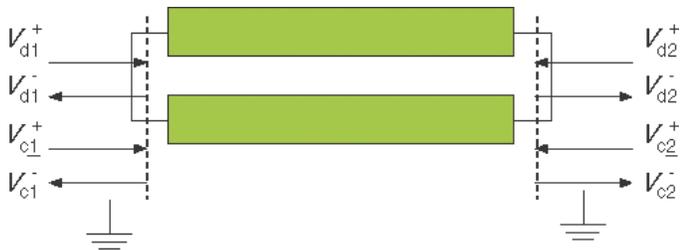


Figure 25. 4x4 matrix describes system of equations for computing 4 port S-Parameters.



		Differential	Common
Response	Differential	S <sub>dd</sub>	S <sub>dc</sub>
	Common	S <sub>cd</sub>	S <sub>cc</sub>

Figure 26. Differential and Common-mode stimulus and response.

## Characterization and Debug

Impedance measurements are relative; they are made by comparing reflected amplitudes to incident amplitudes. Modern TDR instruments perform all of the calculations to compare the incident and reflected amplitudes with reported values in rho (reflection coefficient) or ohms. Figure 24 shows impedance variations from the characteristic impedance  $Z_0$  as the incident TDR step moves along from the connector to the end of the trace into an open circuit. Note the accuracy of this process is highly dependent upon the reference impedance of the TDR source, in this case  $Z_0$ .

S-Parameters (scattering parameters) have become more common-place in describing frequency domain network performance. They are defined in terms of incident and reflected waves at each port and describe power or voltages present as a function of frequency. Figure 25 shows the single-ended incident and return voltages relative to each port. A more popular measurement configuration is found in Figure 26 where measurements are performed in differential mode. S-Parameter measurements in mixed mode, including differential and common-mode measurements, offer advantages of insight into potential signal integrity issues. Differential measurements directly relate to signal attenuation as most of the signal's energy propagates in this mode. Common mode relates to skew and ground bounce. Mode conversion results in electromagnetic interference (Diff-CM) and electromagnetic susceptibility (CM-Diff). Finally cross-coupling between adjacent lines can produce crosstalk. Both impedance and S-Parameter measurements are invaluable to the designer as tools to identify potential signal integrity issues. In the time-domain TDR can isolate impedance discontinuities and even correlate simulation models to physical measurements. In the frequency-domain S-Parameters provide essentially a transfer function representation or behavioral model in relative terms.

USB 3.0 measurements that can be made with TDR include differential impedance, frequency domain crosstalk, and S-Parameters including S<sub>dd21</sub> insertion loss and differential-to-common-mode conversion. These measurements are performed using a reference impedance of 45 ohms or 90 ohms differential. Since most TDR systems use a 50 ohm reference impedance the measured data will need to be normalized in software to the target 90 ohm differential reference impedance.

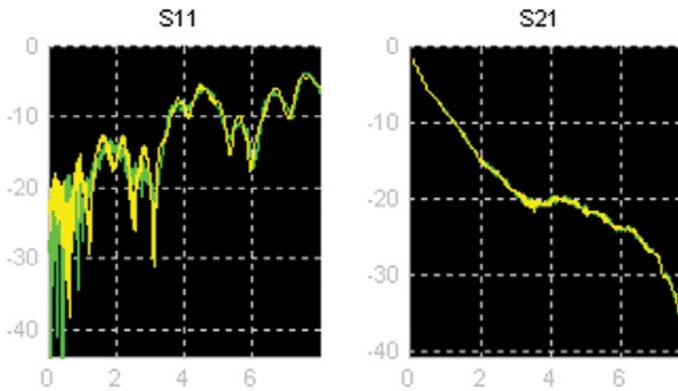


Figure 27. S-Parameters before (green) and after (yellow) 90 ohm normalization.

## Summary

In this application note we've explored many of the new challenges associated with USB 3.1 and have introduced tools needed for validation and debug of SuperSpeed designs. Since the advent of USB in the late 1990s Tektronix equipment has been used to certify millions of USB devices through industry plugfests and at independent test labs. USB-IF members can leverage the Platform Integration Lab (PIL) to test and correlate early designs. The PIL is available for USB developers to test host and device interoperability and ensure that devices perform correct USB 3.1 electrical and link level signaling

For more details about USB compliance testing visit the USB Implementers Forum page at [www.usb.org](http://www.usb.org). Here you will find detailed test procedures, white papers, and other support materials. Additional information about USB testing can be found at [www.tektronix.com/usb](http://www.tektronix.com/usb). This site includes extensive materials like application notes, webinars and recommended test equipment.

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