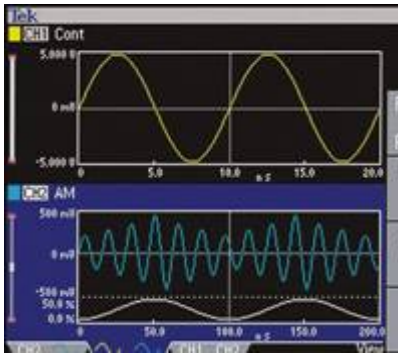
Simplifying Validation and Debug of USB 3.0 Designs

- Tektronix USB Testing Solutions Introduction



name

title

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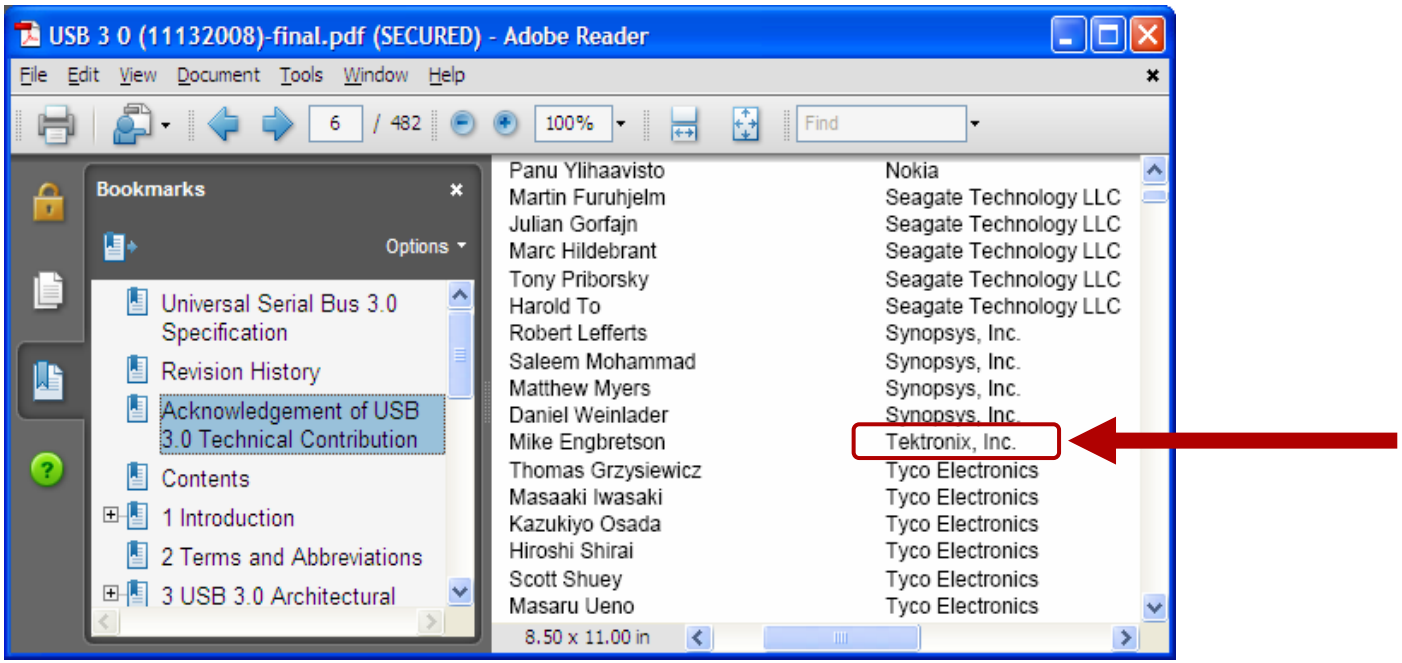
Agenda

- Introduction
- USB 3.0 SuperSpeed
  - Why USB 3.0?
  - Timeline
  - Cable
  - Transmitter
  - Receiver
  - Protocol analysis
- USB 2.0
  - Introduction
  - Compliance Testing
- Wireless USB
  - Overview
  - Compliance and Debug

Disclaimer: The material and content that describes specific details of the USB 3.0 specification (and SuperSpeed logo) belong to the USB 3.0 Promoters. Tektronix is not speaking or presenting on behalf of the USB 3.0 Promoters.

USB Industry Leadership

- Tektronix 1st to market for USB 2.0
- Only approved Method of Implementation (MOI) for WiMedia PHY Leadership in USB
- Millions of certified products shipped, enabled by Tektronix USB solutions
- Tektronix is only T&M Technical Contributor in the USB 3.0 specification!



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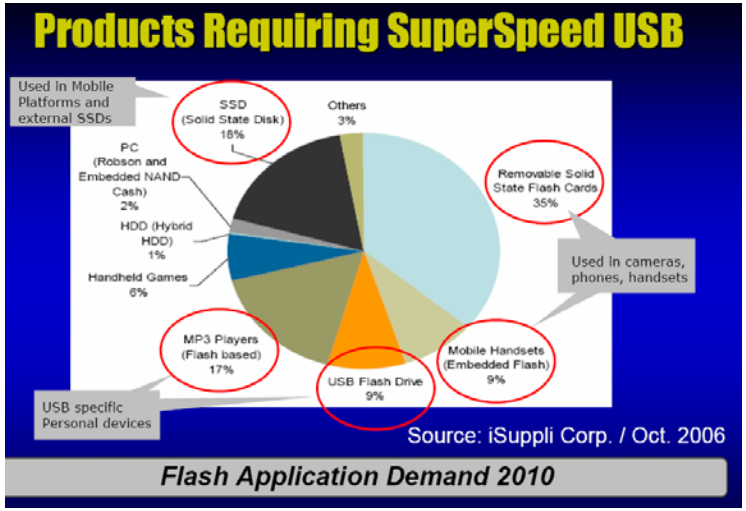
Why SuperSpeed USB?

- USB 2.0 is adequate for many products…
- Emerging applications will benefit from higher performance.
- Something faster is needed for large digital multi-media files

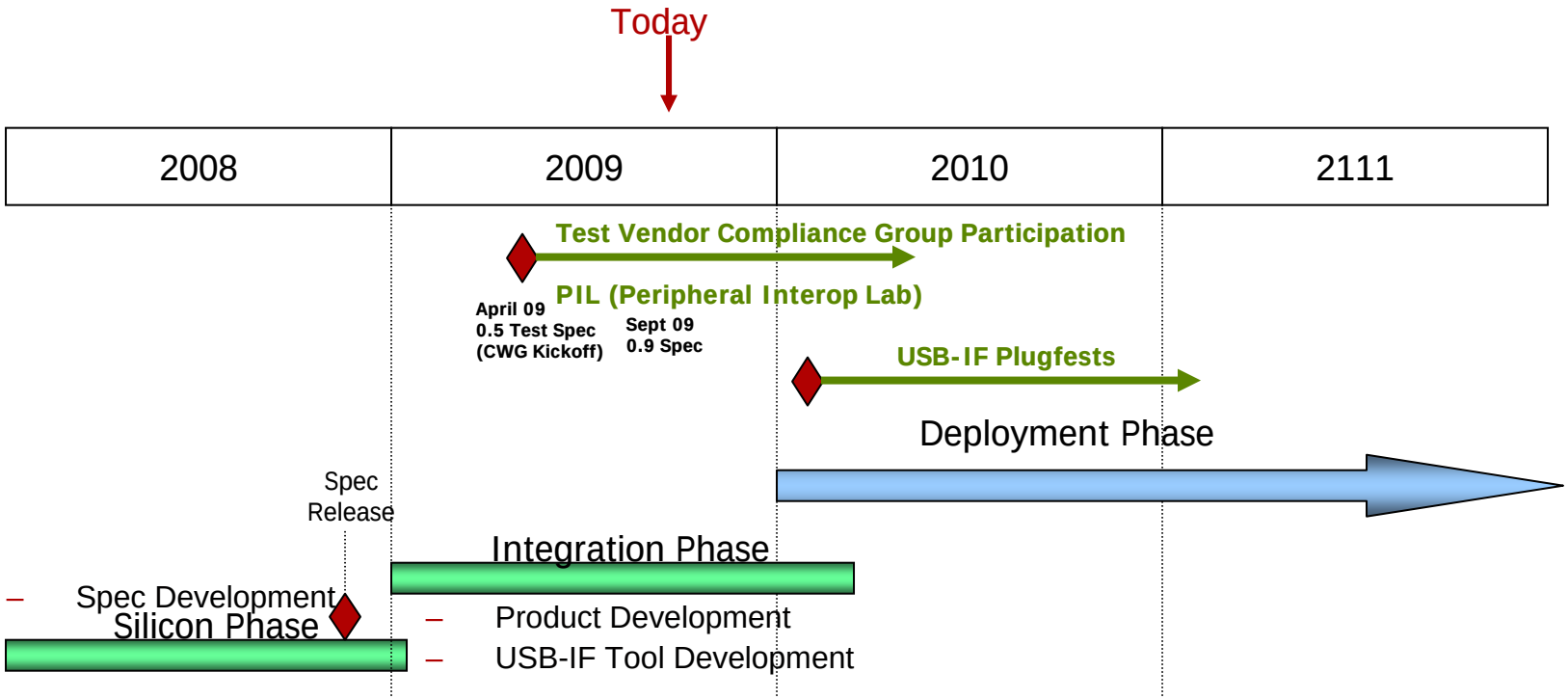


Source: USB-IF

- **User wait time requirement is 1½ minutes to synchronize**

	Song /Pic	256 Flash	USB Flash	SD-Movie	USB Flash	HD-Movie
	4 MB	256 MB	1 GB	6 GB	16 GB	25 GB
USB 1.0	5.3 sec	5.7 min	22 min	2.2 hr	5.9 hr	9.3 hr
USB 2.0	0.1 sec	8.5 sec	33 sec	3.3 min	8.9 min	13.9 min
USB 3.0	0.01 sec	0.8 sec	3.3 sec	20 sec	53.3 sec	70 sec

USB 3.0 Technology Timeline & Tektronix Involvement



Tektronix Test Solution Updates

- Chapter 5 - Cable
- Chapter 6 - Transmitter, Receiver, Channel
- Chapter 7 - Protocol (Partner Solution)

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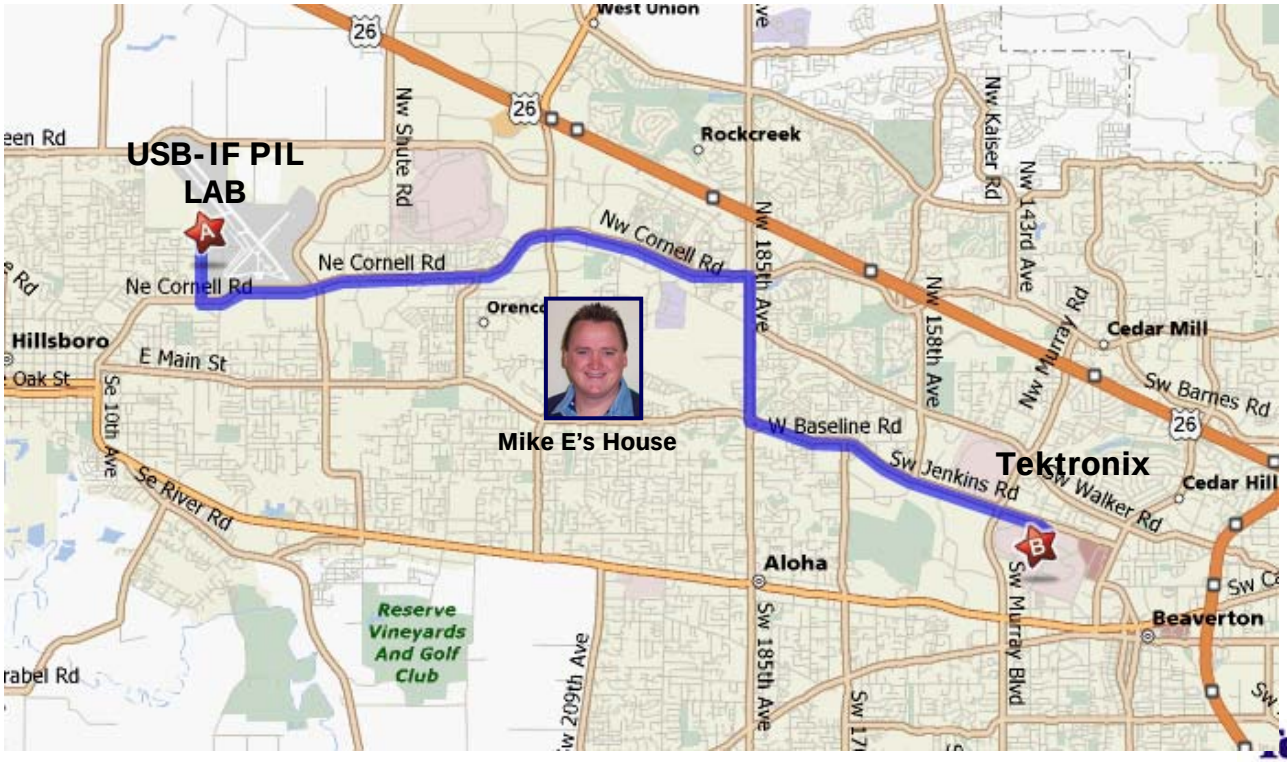
USB-IF Platform Interoperability Lab (PIL) Collaboration

- The PIL is available for USB developers to test host and device interoperability and ensure that devices perform correct USB 3.0 electrical and link level signaling
- Tektronix is located less than 10 miles from the PIL
- Tektronix will work with you at the PIL or local Tektronix Technology Centers
  - Contact your local Tektronix representative to schedule an appointment



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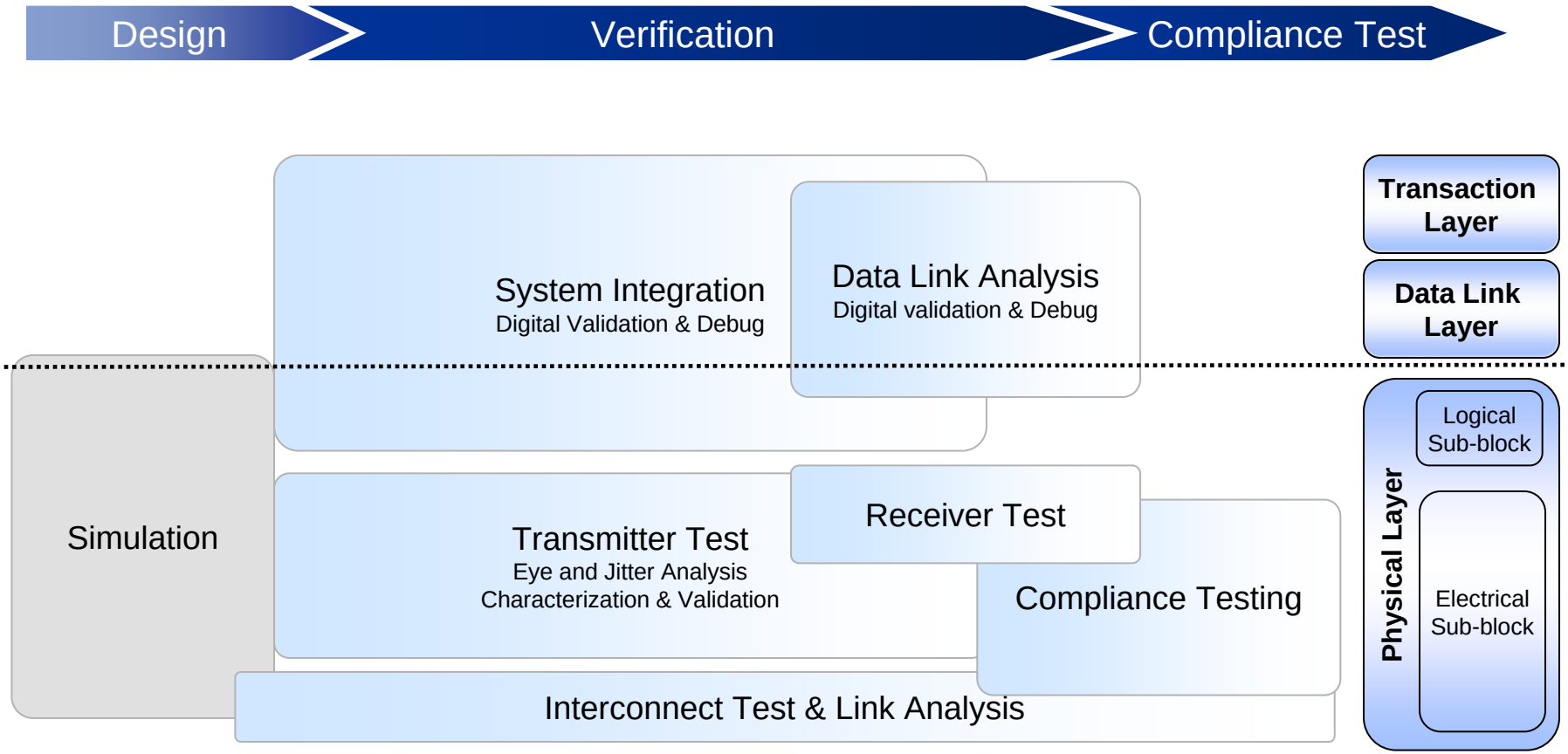
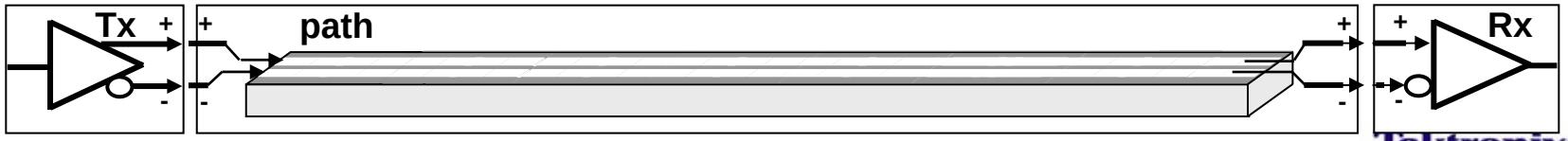
High Speed Serial Test Challenges





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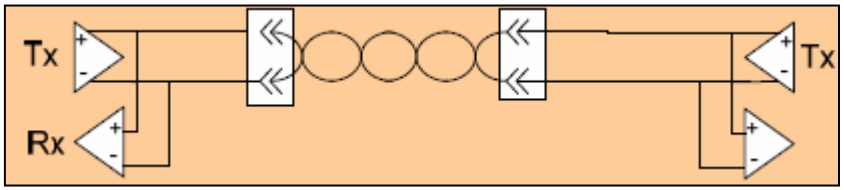
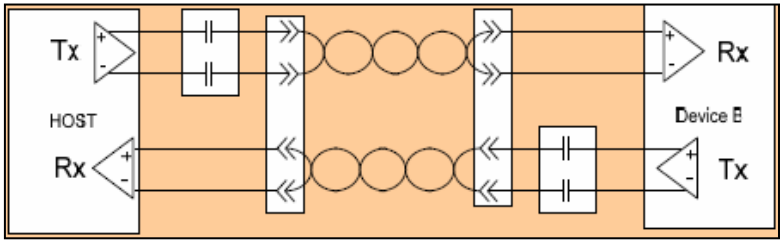
Differences from High-Speed Electricals

- High-Speed
  - 480MT/s
  - No-SSC
  - 2 wires for signaling
    - Tx and Rx use the same wire
    - 1 bi-directional link
  - DC coupled bus
  - NRZ encoding



- SuperSpeed
  - 5.0GT/s (10X speed increase)
  - SSC is required
  - 4 wires for signaling
    - 2 for Tx and 2 for Rx
    - Each Uni-directional
  - AC Coupled bus
  - 8b/10b Encoded (Scrambing)



USB 3.0 Key Considerations

- Receiver testing now required
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues
- Channel considerations
  - Need to consider transmission line effects
  - Software channel emulation for early designs
- New Challenges
  - 12” Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx
- Test strategy
  - Cost-effective tools
  - Flexible solutions

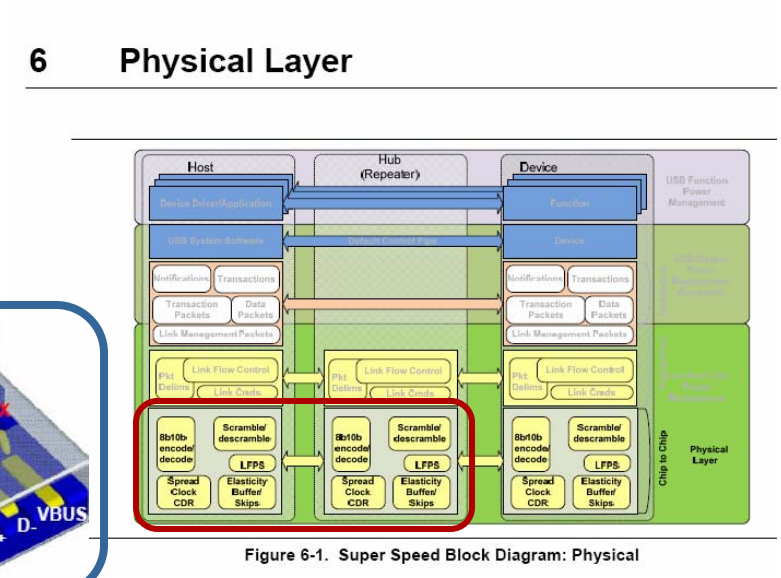


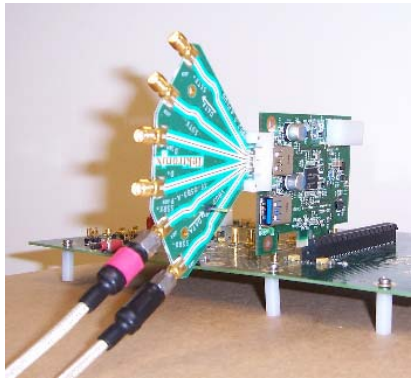
Figure 6-1. Super Speed Block Diagram: Physical

Source: USB 3.0 Rev 1.0 Specification

Connecting to the Device Under Test

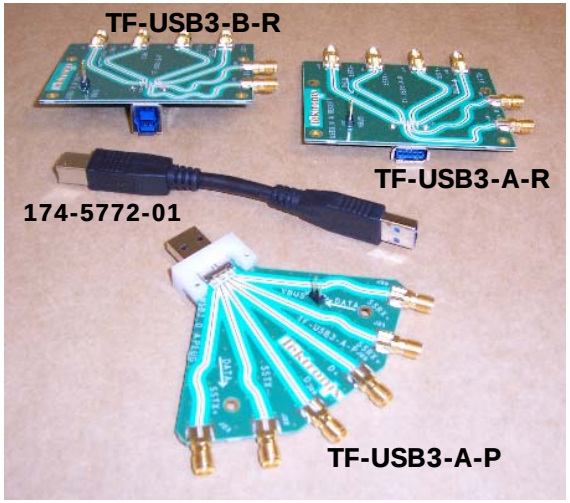
- For Host Tx/Rx Testing
  - A Plug
  - B Receptacle + Short USB3 Cable
- For Device Tx/Rx Testing
  - A Receptacle + Short USB3 Cable
- For Cable Testing
  - A Receptacle
  - B Receptacle
  - USB 2.0 for X-Talk
- For De-Embed
  - A Receptacle mated with A Plug

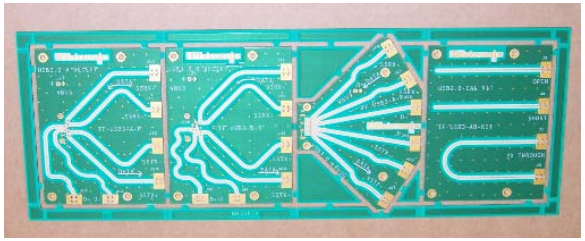
TF-USB3-A-P



World's Only Plug Style Fixture!

TF-USB3-AB-KIT





Manufactured on single flat

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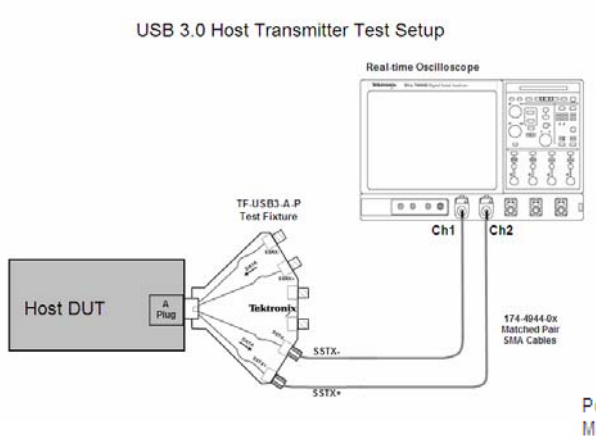
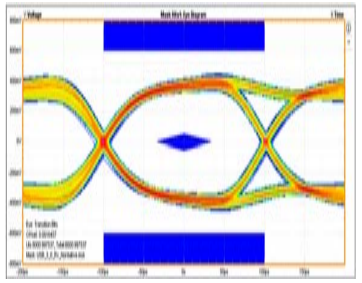
Fixture Considerations

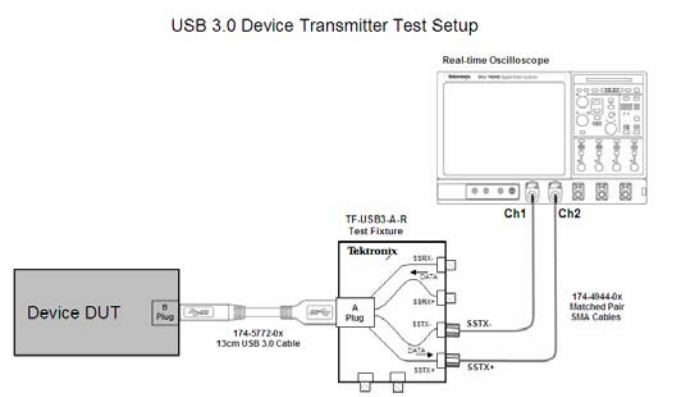
- Acquire signal as close to the Silicon/Connector
- Host Testing
  - A Plug
  - B Receptacle + Short USB3 Cable
- Device Testing
  - A Receptacle + Short USB3 Cable
- 13cm Cable Adds Error!
  - 7% Amplitude Loss
  - 500fs Rj
  - 2.5ps Dj

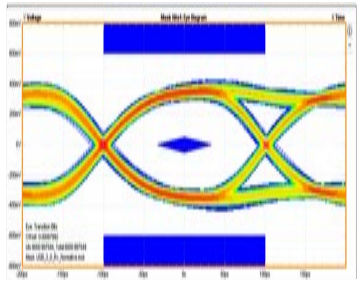




Golden Result used for comparisons
(Meas. Channel: Fixture and Matched SMA Cables)

	Tek A Plug RevB Fixture No CTLE			
	Rj	Dj	Tj	Height
Port-420	1.3	10.1	28.8	525
Margin	1.9	75.9	103.2	425
Compliance Limit	3.27	86.0	132.0	100





	13cm Hosiden Cable w/ Tek B-Receptable Fixture No CTLE			
	Rj	Dj	Tj	Height
Port-420	1.8	12.5	37.3	487
Margin	1.5	73.5	94.67	387
Compliance Limit	3.27	86.0	132.0	100

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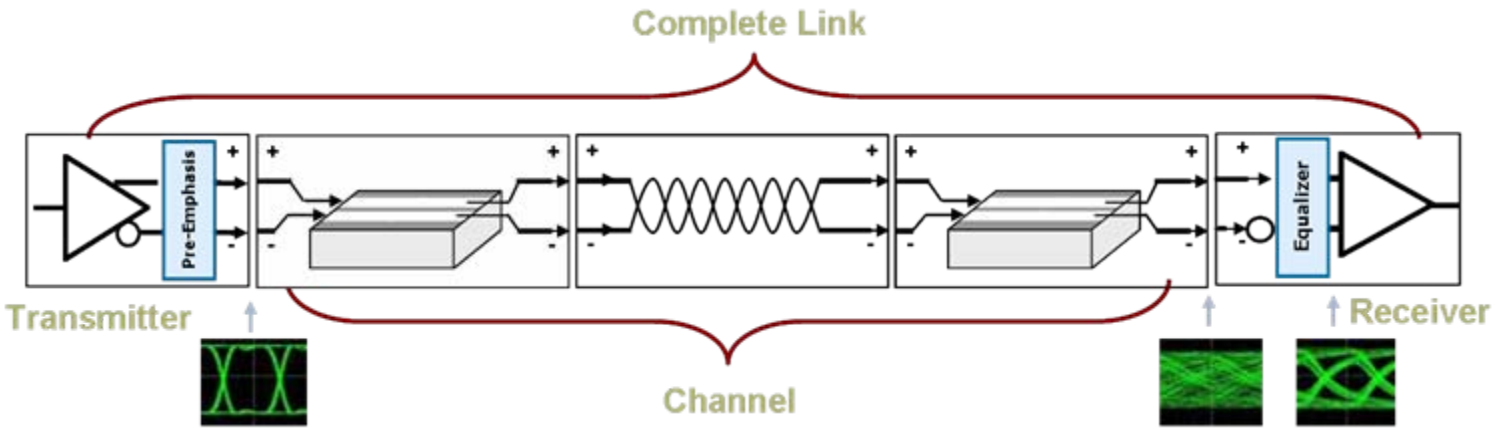
USB Characterization and Debug

Beyond Compliance

- USB 3.0 specification has informative measurements
  - Measurements at silicon pads
  - AC/DC parametric, common-mode measurements
- Complete link analysis with custom equalization functions
- De-embed fixture for accurate results
- Model channel and cable beyond required compliance reference channels
  - Worst case channel analysis
  - Cascading of S-Parameters for various interconnect topologies
- Equipment considerations



Informative Transmitter Measurements

At Transmitter Pads

- Measurement at Transmitter Pads Requires Tx Channel DeEmbed

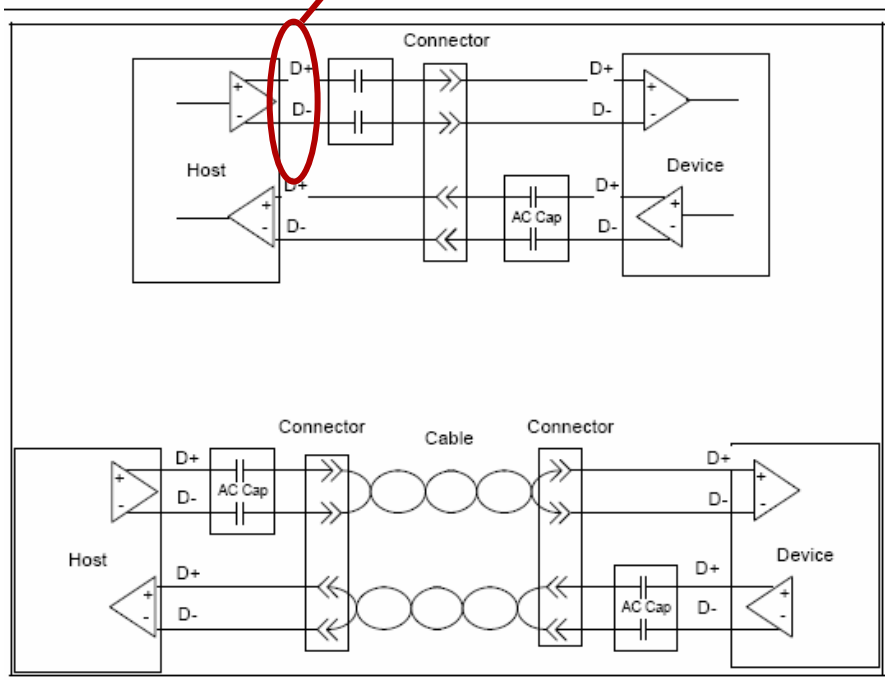


Figure 6-4. Channel Models without Cable (Top) and with Cable (Bottom)

Table 6-10. Transmitter Normative Electrical Parameters

Symbol	Parameter	5.0 GT/s	Units	Comments
UI	Unit Interval	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each device. Period does not account for SSC induced variations.
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX-DE-RATIO}$	Tx de-emphasis	3.0 (min) 4.0 (max)	dB	Nominal is 3.5 dB
$R_{TX-DIFF-DC}$	DC differential impedance	72 (min) 120 (max)	Ω	
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	0.6 (max)	V	Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an "off" receiver's input goes below ground. See Section 1.2.5.6 and Note 9 for details
$C_{AC-COUPLING}$	AC Coupling Capacitor	75 (min) 200 (max)	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
$T_{CDR\_SLEW\_MAX}$	Max slew rate	10	ms/sec	See the jitter white paper for details on this measurement.

Table 6-11. Transmitter Informative Electrical Parameters at Silicon Pads

Symbol	Parameter	5.0 GT/s	Units	Normative	Comments
$T_{MIN-PULSE-DJ}$	Deterministic min pulse	0.96	UI		Tx pulse width variation that is deterministic.
$T_{MIN-PULSE-TJ}$	Tx min pulse	0.90	UI		Min Tx pulse at 10^{-12} including Dj and Rj.
T_{TX-EYE}	Transmitter Eye	0.625 (min)	UI		Includes all jitter sources
$T_{TX—DJ-DD}$	Tx deterministic jitter	0.19 (max)	UI		Deterministic jitter only assuming the Dual Dirac distribution
$C_{TX-PARASITIC}$	Tx input capacitance for return loss	1.25 (max)	pf		Parasitic capacitance to ground

Symbol	Parameter	5.0 GT/s	Units	Normative	Comments
R_{TX-DC}	Transmitter DC common mode impedance	18 (min) 30 (max)	Ω		DC impedance limits to guarantee Receiver detect behavior. Measured with respect to AC ground over a voltage of 0-500mV.
$I_{TX-SHORT}$	Transmitter short-circuit current limit	60 (max)	mA		The total current Transmitter can supply when shorted to ground.
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	0 (min) 2.2 (max)	V		The instantaneous allowed DC common-mode voltages at the connector side of the AC coupling capacitors.
$V_{TX-CM-AC-PP\_ACTIVE}$	Tx AC common mode voltage active	100 mv	mVPP		Max mismatch from D+ D- for both time and amplitude. While signaling.
$V_{TX-CMDC-ACTIVE-IDLE-DELTA}$	Absolute Common Mode Voltage between U1 and U0	200 (max)	mV		peak
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Peak – Peak Output Voltage	0 (min) 10 (max)	mV		
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	0 (min) 10 (max)	mV		Voltage must be low pass filtered to remove any AC component. This limits the common mode error when resuming U1 to U0

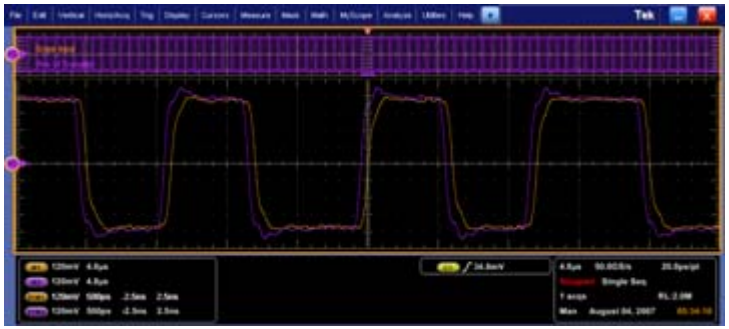
Source: USB 3.0 Rev 1.0 Specification

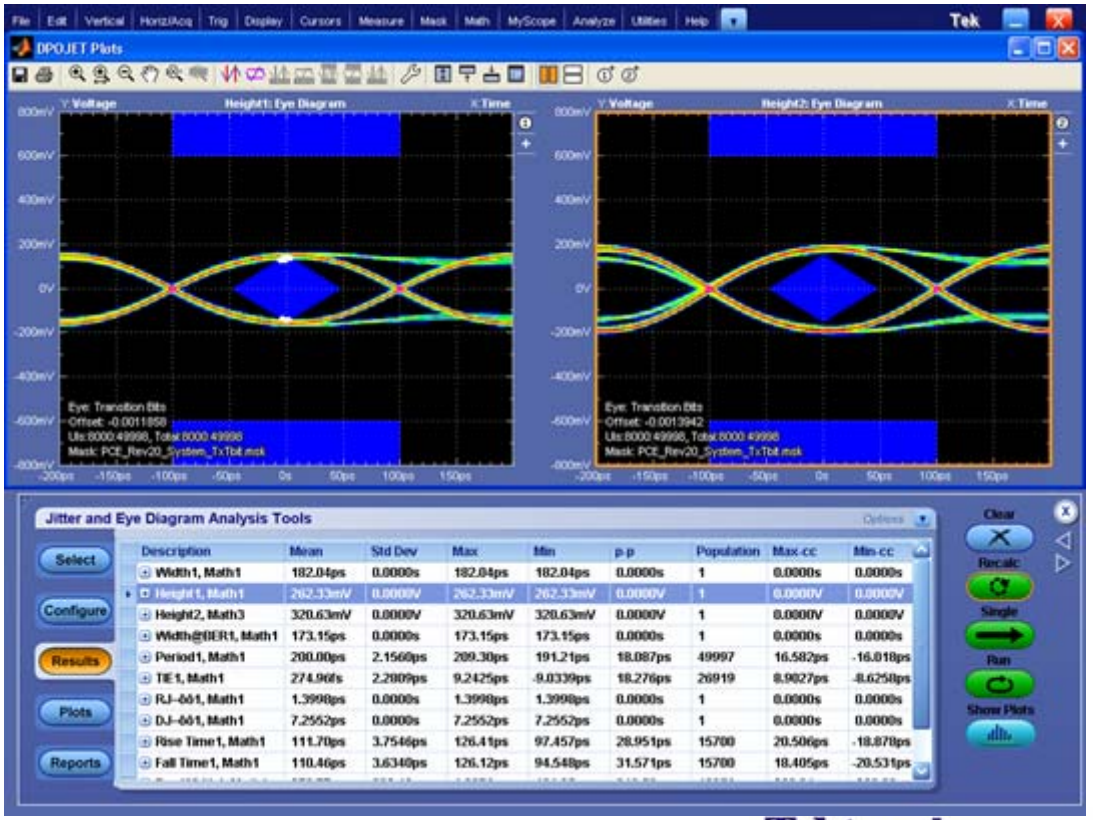
Accurate Transmitter Characterization

Channel De-Embedding

- Measure true representation of signal at the Tx output
  - Characterize channel with TDR or Simulator
  - Import S-Parameter file
  - Create fixture de-embed filter with SDLA software
- Identify root cause failures
  - Removes fixture effects
  - Improved margin

Before → **After**





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USB Channel Modeling

- Understand transmitter margin given worst case channels
- Model channel and cable combinations beyond compliance requirements
- Easily create interconnect models with SDLA software to analyze channel effects

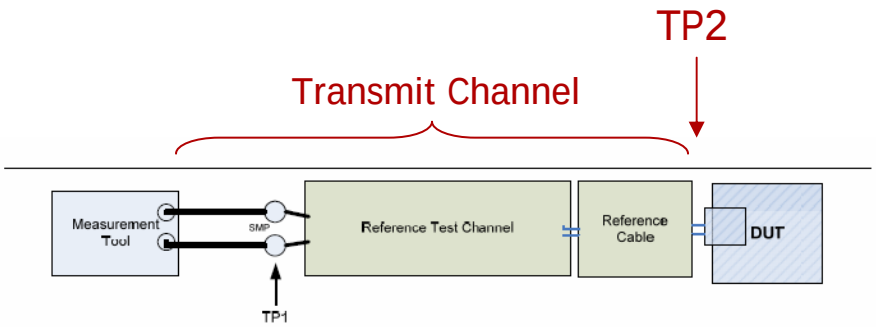
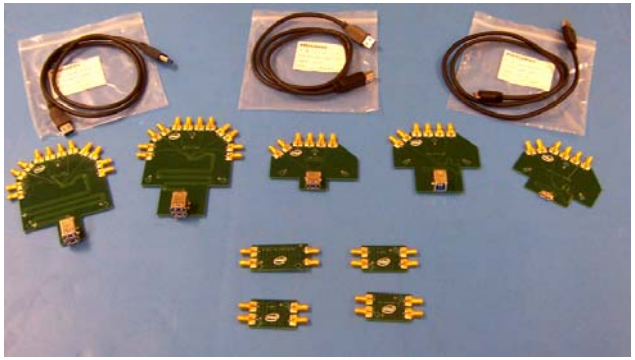


Figure 6-14. Tx Normative Setup with Reference Channel



USB-IF HW Channel Prototypes

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Custom Equalization Analysis

- Equalizer models
  - Pole, Zero, and Frequencies for Continuous Time Linear Equalizer (CTLE)
  - Feed-Forward (FFE) and Decision-Feedback (DFE) Equalizers

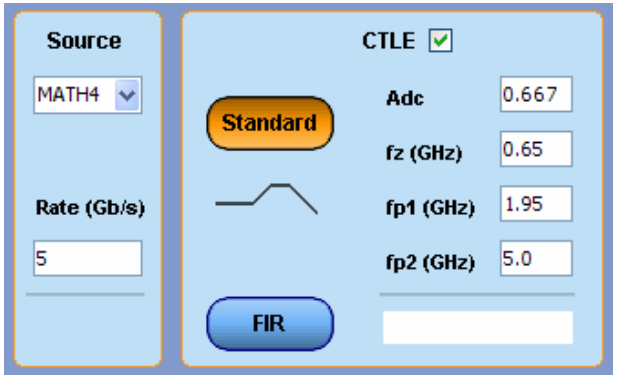
$$H(s) = \frac{A_{dc}\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})}$$

$$A_{dc} = 0.667$$

$$\omega_z = 2\pi(650x10^6)$$

$$\omega_{p1} = 2\pi(1.95x10^9)$$

$$\omega_{p2} = 2\pi(5x10^9)$$



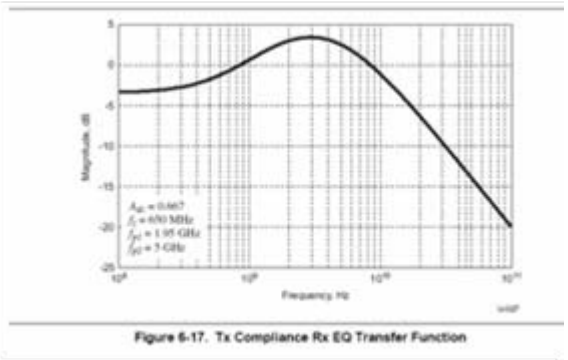
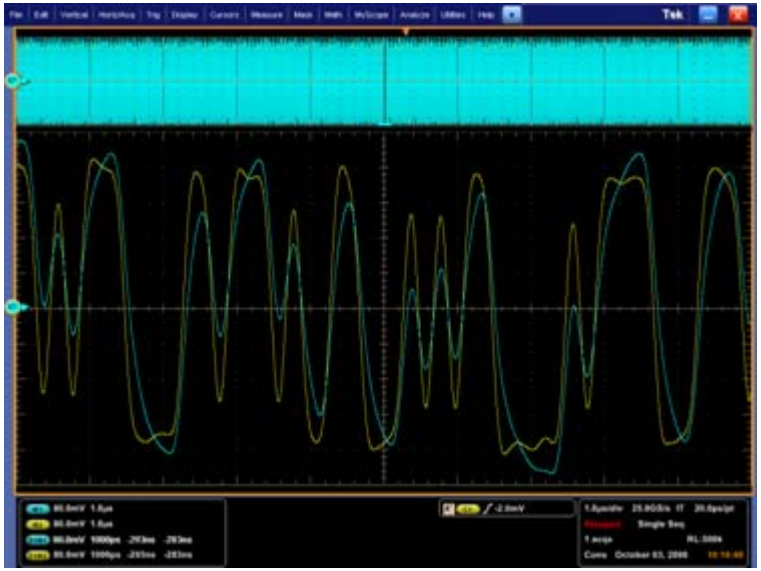
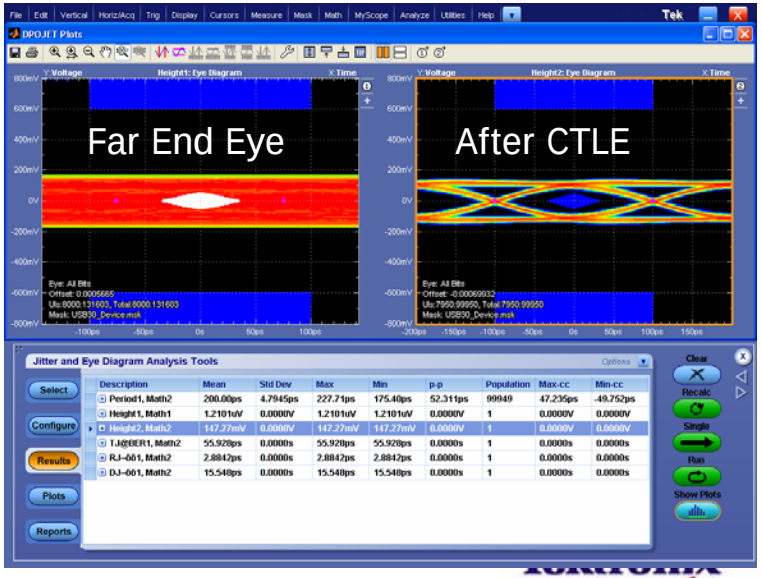


Figure 6-17. Tx Compliance Rx EQ Transfer Function





Transmitter Compliance Testing (Normative Testing)

Channel Embedding

- Measurements at TP1
- HW Channel Probed at TP1
  - CTLE applied in SW
- SW Channel Probed at TP2
  - CTLE combined with Channel

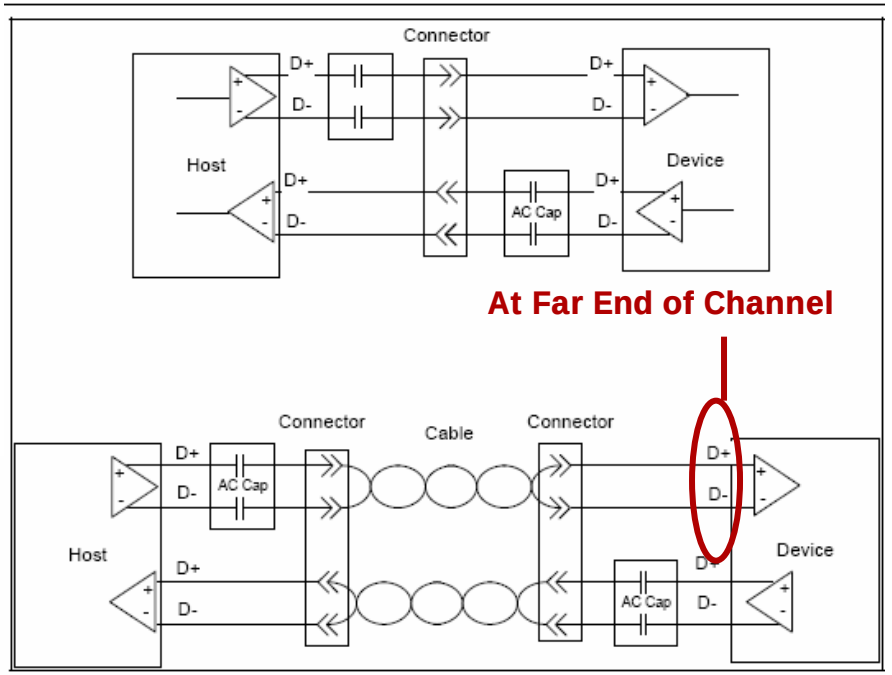


Figure 6-4. Channel Models without Cable (Top) and with Cable (Bottom)

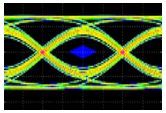
6.7.2 Transmitter Eye

The eye mask is measured using the compliance data pattern CD1 described in Section 6.4.4. Eye Height is measured from 10^{6} UI. Jitter is extrapolated from 10^{6} UI to 10^{-12}.

Table 6-12. Normative Transmitter Eye Mask

Signal Characteristic	Minimal	Nominal	Maximum	Units	Note
Eye Height	100		1200	mV	2
Dj			93	ps	1,2,3
Rj			60	ps	1,2,3
Tj			132	ps	1,2,3

Notes:
1. Measured over 10^{6} UI and extrapolated to 10^{-12} BER
2. Measured after receiver equalization function
3. Measured at end of reference channel and cables at TP1 figure 6-14



CTLE

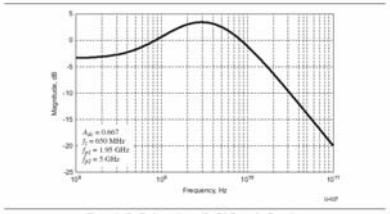


Figure 6-17. Tx Compliance Rx EQ Transfer Function

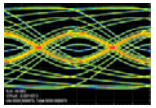


Figure 6-14. Tx Normative Setup with Reference Channel

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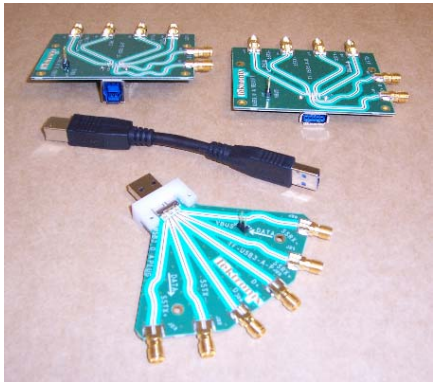
Complete USB 3.0 Transmitter Solution

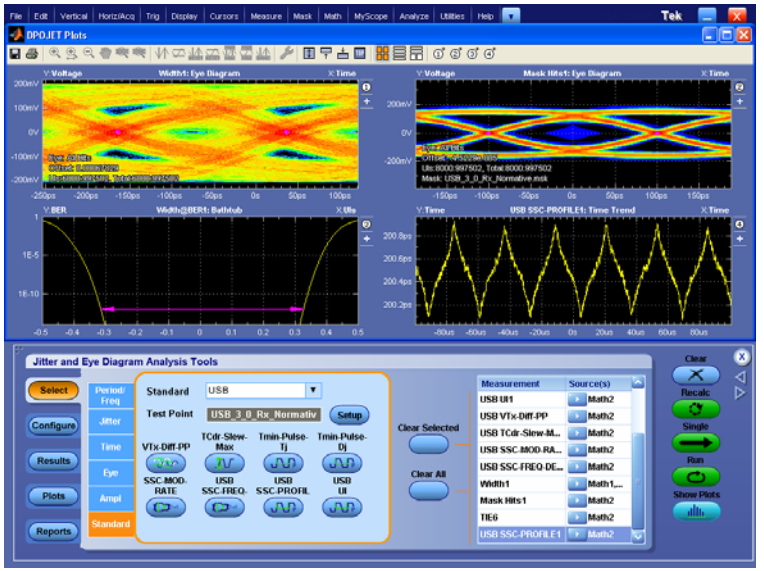
DPO/DSA70000B Series Oscilloscopes

- Tektronix Super Speed USB Fixtures
- 12.5 GHz Real-Time Scope
  - 5th Harmonic Performance
  - 50GS/s Sample Rate
  - P7313SMA Differential Probe (Optional)
- Analysis software for validation and debug
  - Serial Data Link Analysis SW (Optional)
  - DPOJET with option USB3
- Automation software for characterization and compliance
  - TekExpress with option USB-TX

TF-USB3-AB-KIT



Opt. USB3



Opt. USB-TX

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Normative Receiver Tolerance Test

- SSC Clocking is enabled
- BER Test is performed at 10^{-10}
- De-Emphasis Level is set to -3dB
- Voltage Level is set to 0.75V
- Each SJ term in the table below is tested one at a time after the device is in loopback mode

Frequency	SJ	RJ
500kHz	400ps	2.42ps
1MHz	200ps	2.42ps
2MHz	100ps	2.42ps
4.9MHz	40ps	2.42ps
50MHz	40ps	2.42ps

Normative Receiver Testing

- Receiver processes the BERT Ordered Sets using ‘built-in BERT’ feature
- Impairment at TP1
- HW Channel Attached at TP1
- SW Channel Attached at TP2

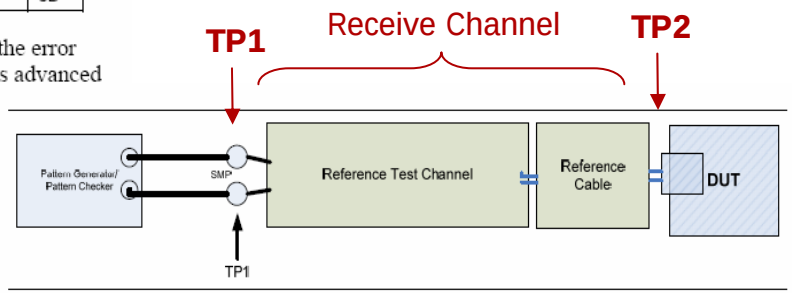
6.7.4.1 Loopback BERT

During loopback the receiver processes the BERT ordered sets BRST, BDAT, and BERC. These ordered sets are given in Table 6-14 through Table 6-17. BRST and BDAT are looped back as received. BERC ordered sets are not looped back but are replaced with BCNT ordered sets. Anytime a BRST is received the error count register EC is set to 0 and the scrambling LFSR is set to 0FFFF h. Any number of consecutive BRST ordered sets may be received.

BRST followed by BDAT starts the bit error rate test. BDAT sequence is the output of the scrambler and is equivalent to the logical idle sequence. It consists of scrambled 0 as described in Appendix B. As listed in Appendix B, the first 16 characters of the sequence are reprinted here:

FF	17	C0	14	B2	E7	02	82	72	6E	28	A6	BE	6D	BF	8D

The receiver must compare the received data to the BDAT sequence. Errors increment the error count register (EC) by 1. EC may not rollover but must be held at FFFF h. The LFSR is advanced once for every character except SKPs. The LFSR rolls over after 2^16 symbols. SKPs inserted or deleted as necessary for clock tolerance compensation.

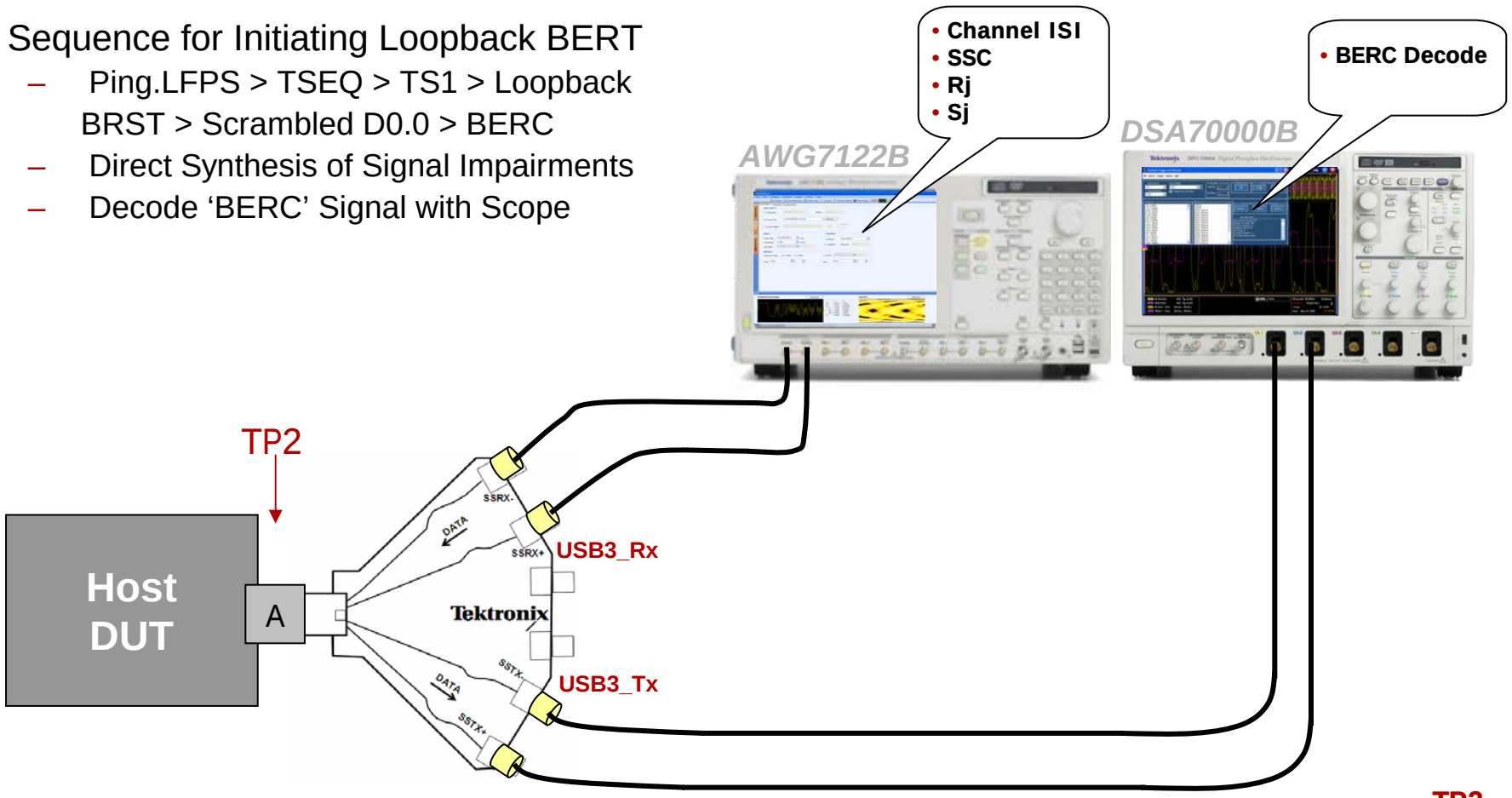


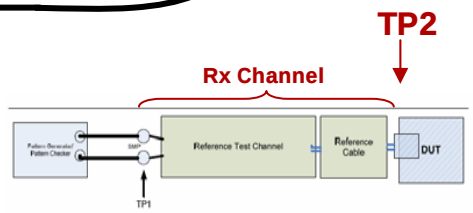
Source: USB 3.0 Specification Figure 6-18. Rx Tolerance Setup

Receiver Testing MOI (with SW Channel Emulation)

If DUT supports 'Loopback BERT'

- Sequence for Initiating Loopback BERT
  - Ping.LFPS > TSEQ > TS1 > Loopback BRST > Scrambled D0.0 > BERC
  - Direct Synthesis of Signal Impairments
  - Decode 'BERC' Signal with Scope





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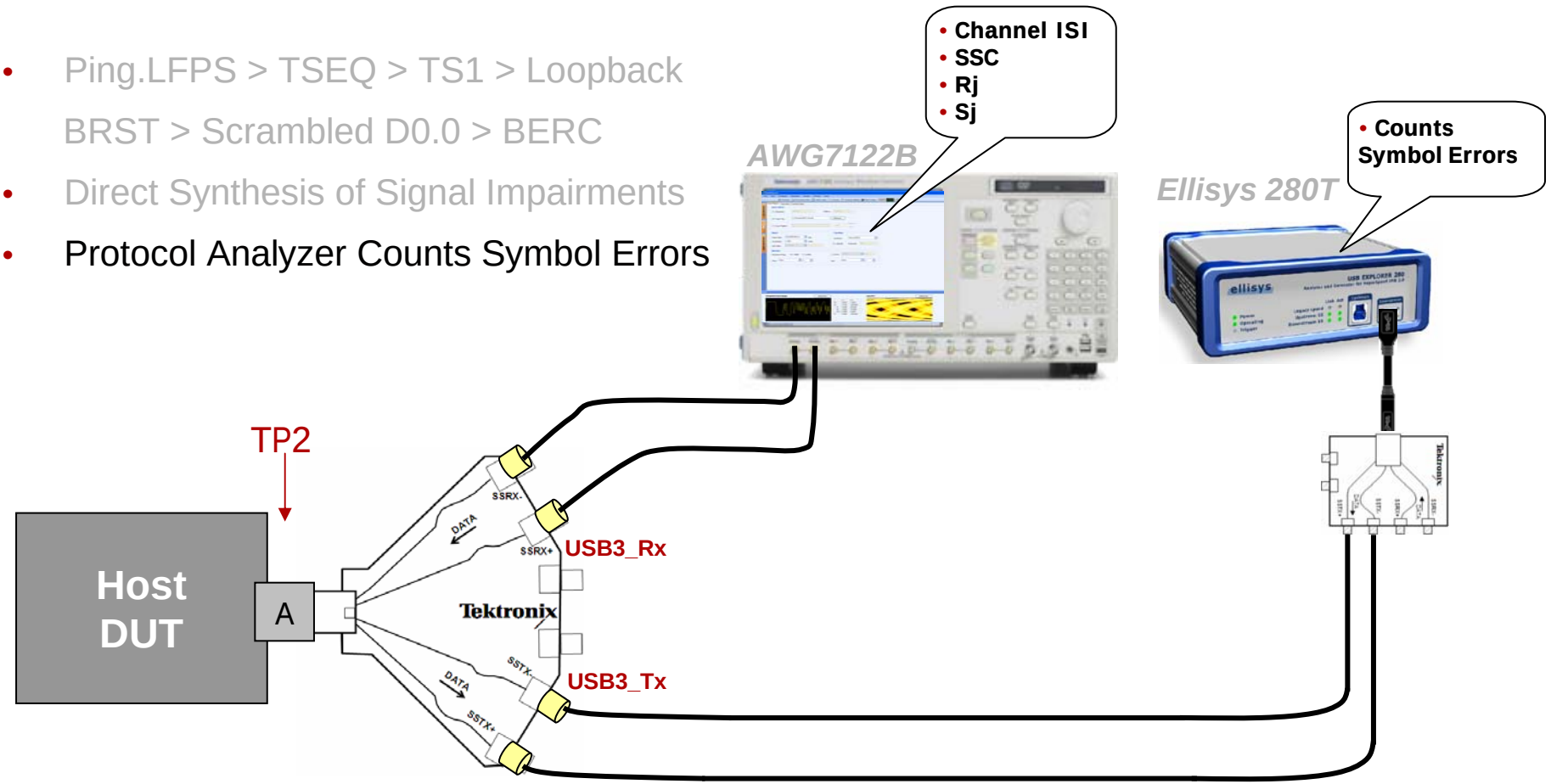
Receiver Test MOI (with SW Channel Emulation)

If DUT does not support 'Loopback BERT'

- Ping.LFPS > TSEQ > TS1 > Loopback
  BRST > Scrambled D0.0 > BERC
- Direct Synthesis of Signal Impairments
- Protocol Analyzer Counts Symbol Errors



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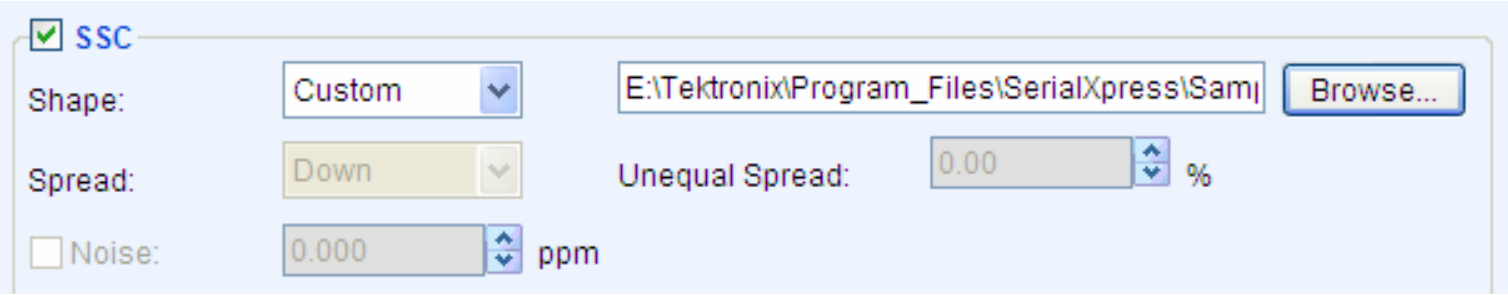
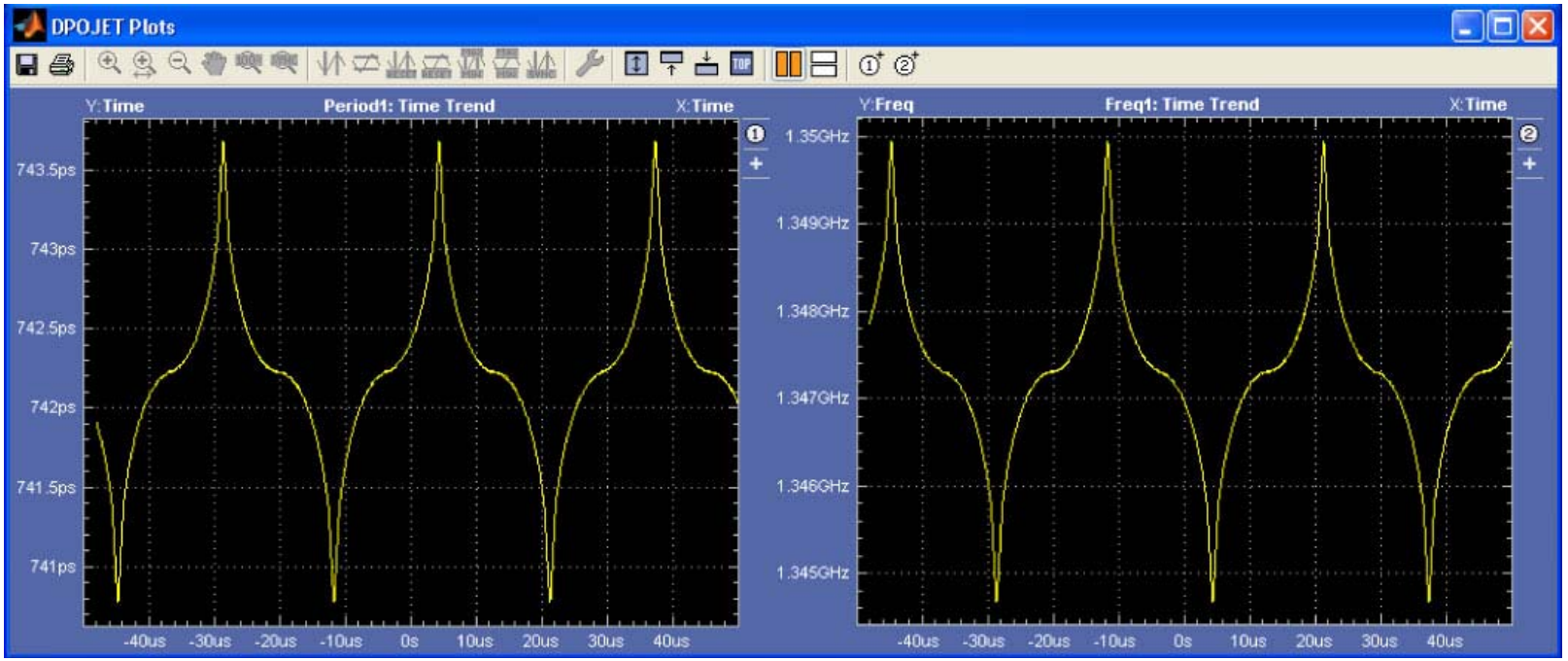
Custom SSC

SerialXpress SW





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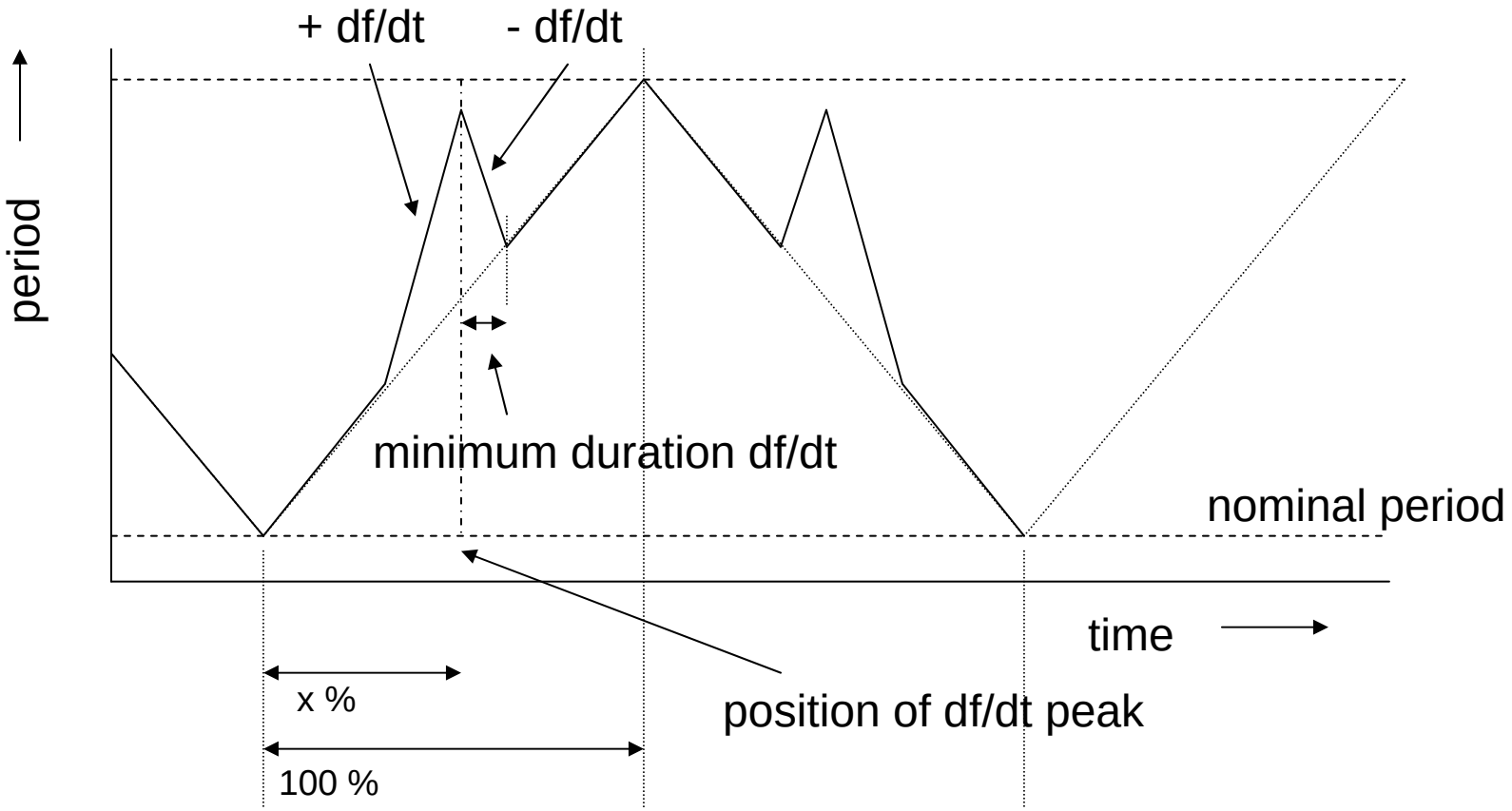
SSC Slew Rate



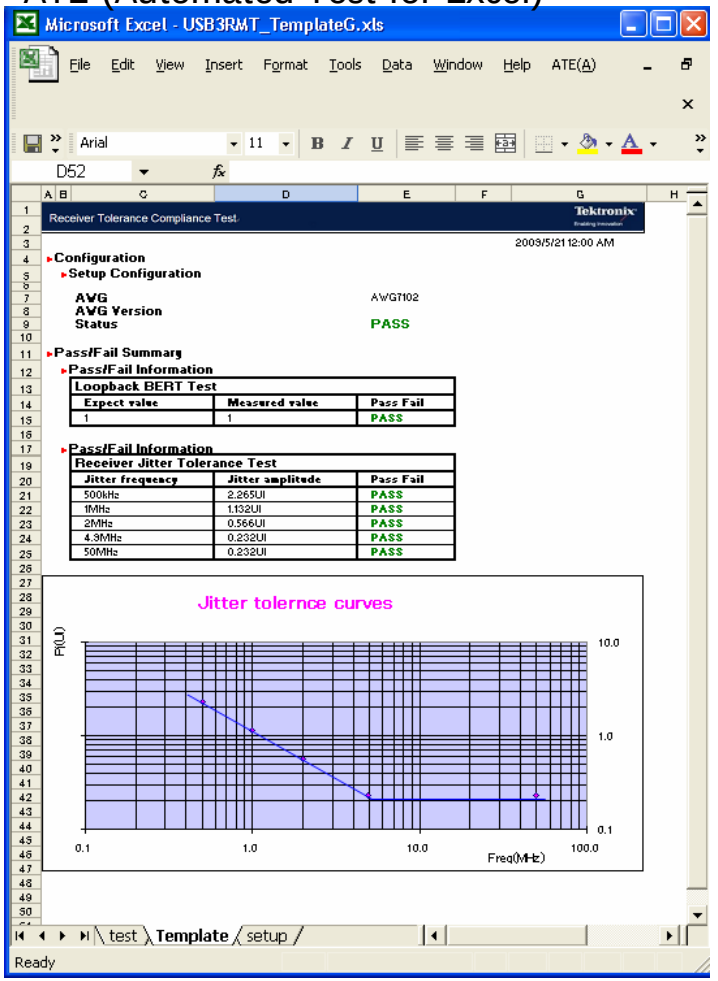
Receiver Compliance & Margin Testing

- Early Market Automated Test Solution

Table 6-19. Input Jitter Requirements for Rx Tolerance Testing

Symbol	Parameter	Value	Units
f1	Tolerance corner	4.9	MHz
J_{RJ}	Random Jitter	0.0121	UI rms
$J_{RJ\_p\text{-}p}$	Random Jitter peak- peak at 10^{-12}	0.17	UI p-p
J_{PJ_500kHZ}	Sinusoidal Jitter	2	UI p-p
J_{PJ_1Mhz}	Sinusoidal Jitter	1	UI p-p
J_{PJ_2MHz}	Sinusoidal Jitter	0.5	UI p-p
J_{PJ_f1}	Sinusoidal Jitter	0.2	UI p-p
J_{PJ_50MHz}	Sinusoidal Jitter	0.2	UI p-p
V_full_swing	Transition bit differential voltage swing	0.75	V p-p
V_EQ_level	Non transition bit voltage (equalization)	-3	dB

ATE (Automated Test for Excel)



USB-IF DevCon Demo – Tokyo, Japan
May 20th, 2009 - NEC Electronics Booth

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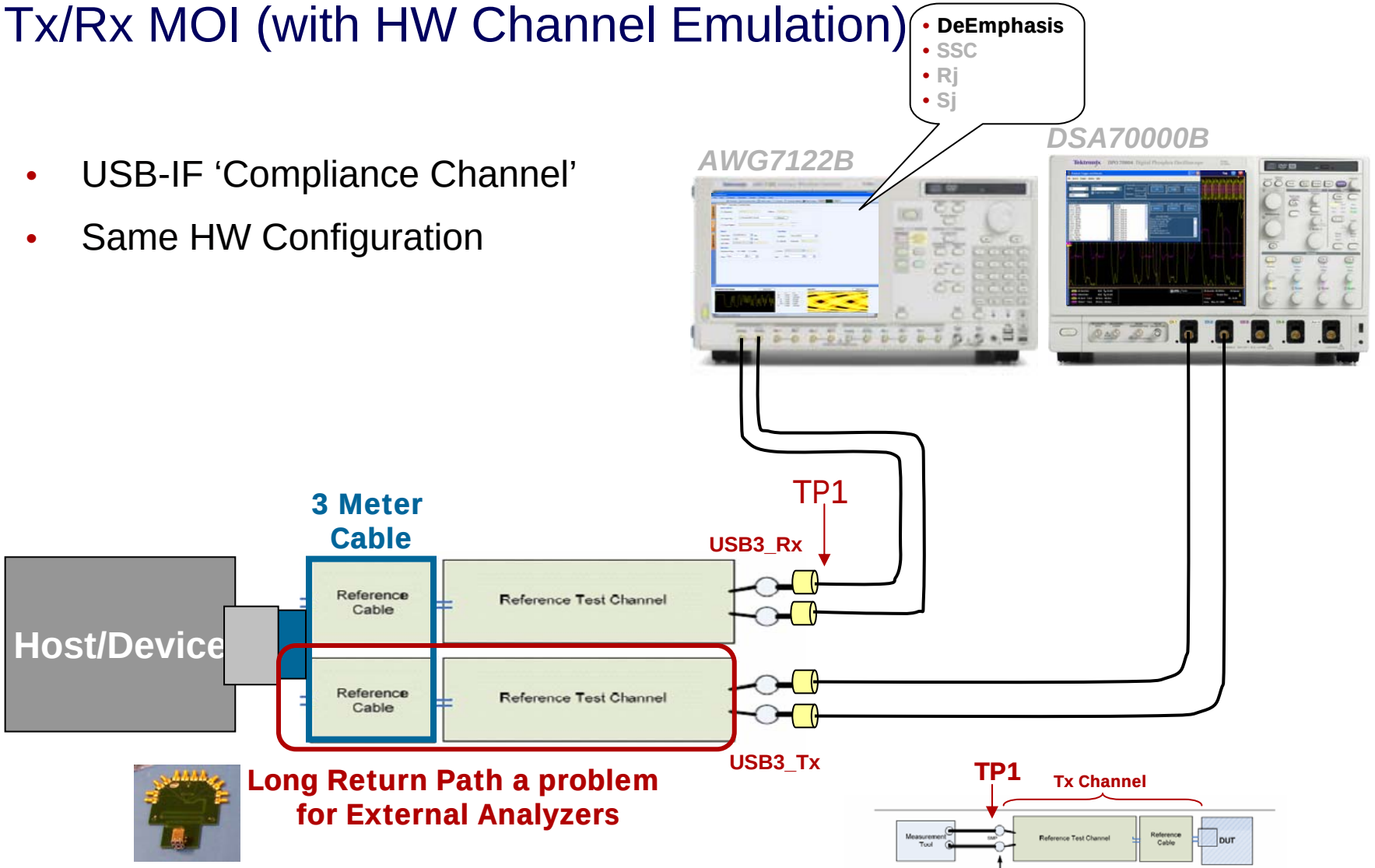
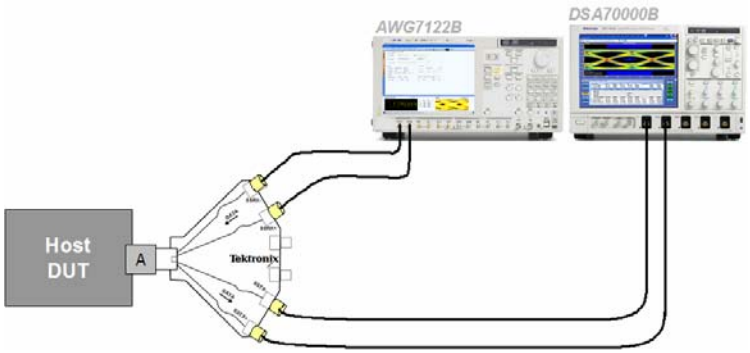
Tx/Rx MOI (with HW Channel Emulation)

- USB-IF ‘Compliance Channel’
- Same HW Configuration



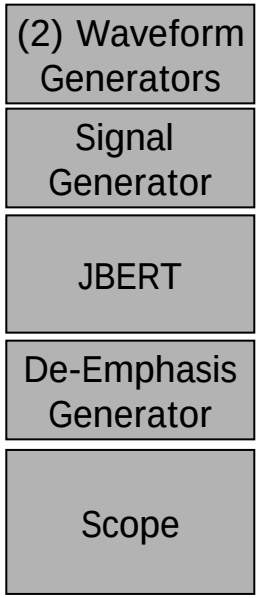
USB 3.0 Tx/Rx Test Equipment Considerations

AWG & RT Scope



- **Simplified Setup**
  - 2 Instruments, add Protocol Analyzer for system level test
  - 1 Fixture, 4 Cables, 4 Connectors
  - AWG7122B (Opt. 06, 08)
- **RX Tolerance Testing**
  - Supports Silicon, Host/Device per the USB 3.0 Specification
- **Flexible Signal Impairment Generation**
  - All required impairments are generated with the AWG using Direct Synthesis
  - Precise ISI generation for channel emulation

BERT & RT Scope



- **Complex Setup**
  - 6 Instruments, add Protocol Analyzer for system level test
  - 1 Fixture, 35 Cables/Connectors
  - BERT HW + External impairment sources
- **RX Tolerance Testing**
  - Synchronous Clock Required, BERT method not suitable for system/device test
- **Impairment Capabilities Limited by Hardware**
  - SSC and Sj require external equipment
  - ISI generation limited by Hardware Channels

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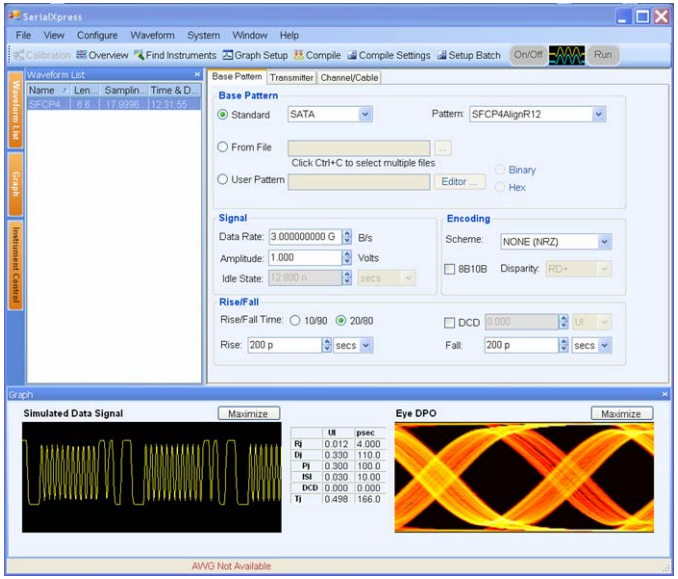
Key Advantages of the AWG for USB Receiver Testing

AWG7000B Arbitrary Waveform Generators with SerialXpress®

- Flexibility to support all signal impairments required for jitter tolerance testing
- Model real-world complexities of SSC profiles to avoid system interoperability issues
- No tradeoffs between any signal impairments - No limitations in generating SSC and SJ at the same time
- Multiple SJ tones can be generated at one time
- Flexible ISI generation enables customers to test ISI models that exceed the test specification
  - No need to wait for USB hardware compliance channels
- Minimize time needed for re-cabling
- Improved repeatability and portability of Receiver test configurations with setup files



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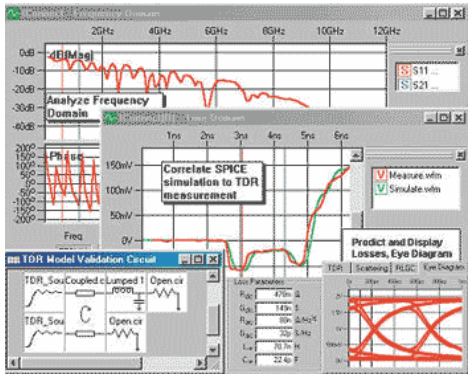
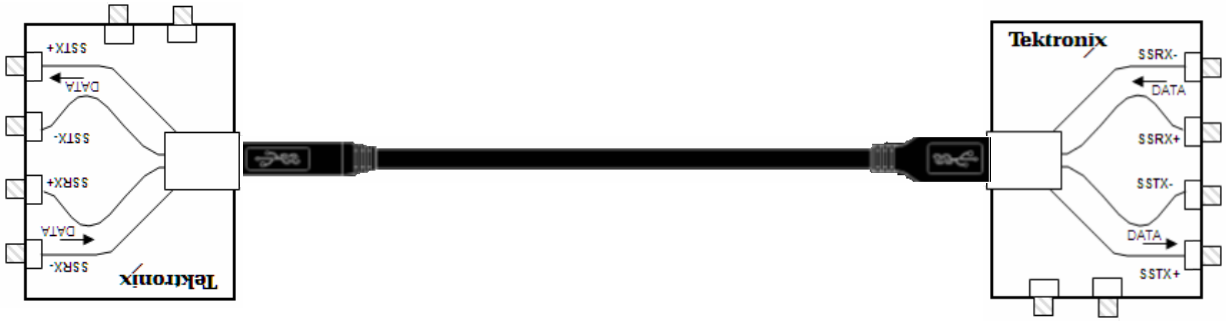
Cable Testing

DSA8200 Sampling Oscilloscope with IConnect®

- Test Fixtures
  - A Receptacle
  - B Receptacle
  - USB2/USB3 Connectors Available for Crosstalk measurements
- Using Sampling Oscilloscope & S-Parameter SW
- Measurements:
  - Impedance
  - Intra-Pair Skew
  - Differential Insertion Loss
  - Differential Return Loss
  - Differential Near-End Crosstalk
  - Differential Crosstalk between USB3.0 and USB2.0 Pairs
  - Differential to CM Conversion





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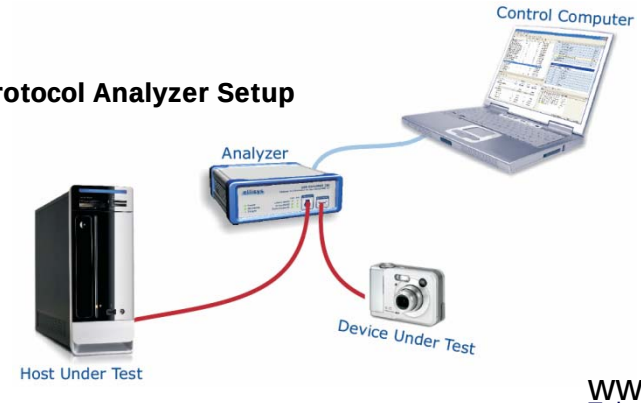
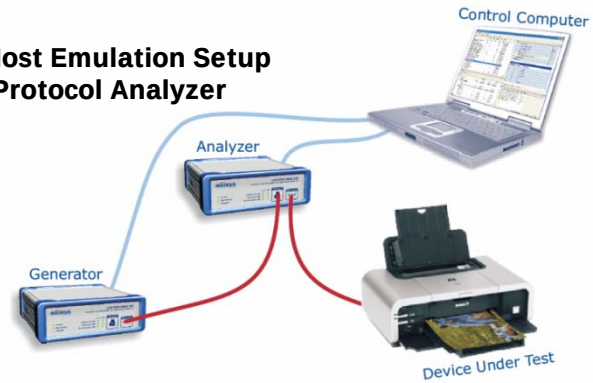
Ellisys EX280 Explorer- USB 3.0 Analyzer/Exerciser

- Analyzer Applications
  - USB host & device monitoring
  - Performance analysis
  - Debug of drivers & software stacks
  - Link state analysis
  - Protocol errors checks
- Generator Applications
  - USB host & device emulation
  - Testing error recovery mechanisms
  - Performance stress testing
  - Compliance verification
  - Link state analysis

Typical Protocol Analyzer Setup



Typical Host Emulation Setup with Protocol Analyzer



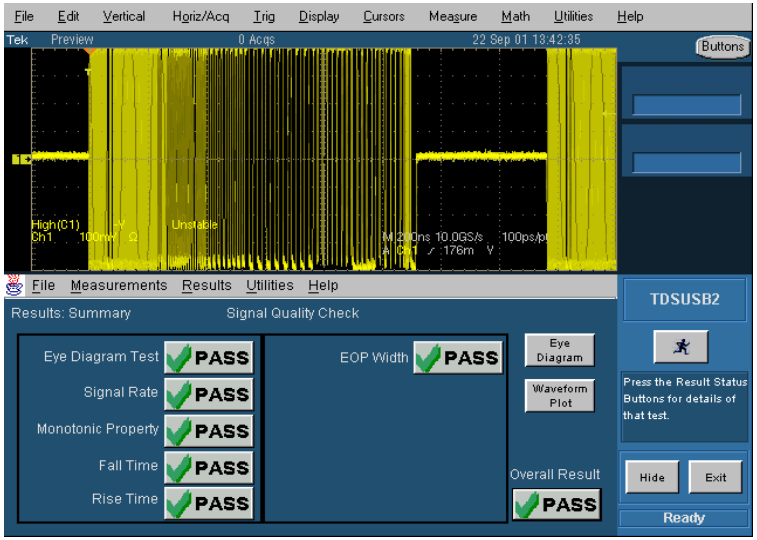
USB 2.0 Compliance

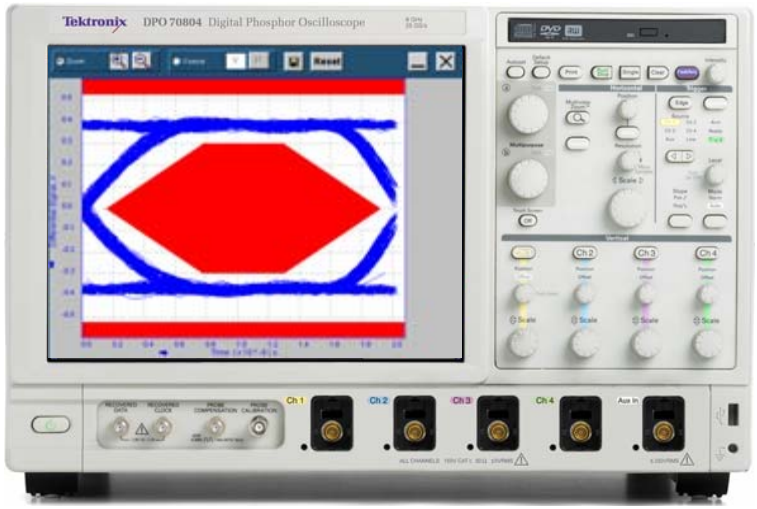
Signal Quality

- Eye-Diagram testing
- Signal Rate
- End of Packet Width
- Cross-over voltage range (for LS and FS)
- JK jitter
- KJ jitter
- Consecutive jitter
- Monotonicity test (for HS)
- Rise and Fall times

Timing Measurements

- Packet Parameters
- Suspend
- Resume
- Reset from High-Speed
- Reset from Suspend





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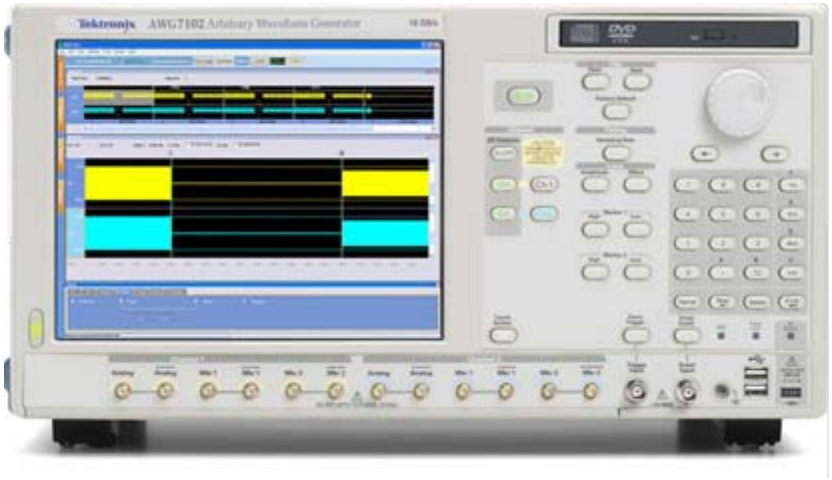
Tektronix Wireless USB Validation Solution

- Easy to setup: Automatically detect Time Frequency Codes (TFCs) and data rates from the RF waveform header
- Demodulate, Analyze and Record measurements of each packet independently
- Perform Measurements Outlined in the Wireless USB EVM Test Specification
- Industry's only MOI (Method of Implementation) for WiMedia test!
  - WUSB EVM test is a subset of WiMedia PHY certification



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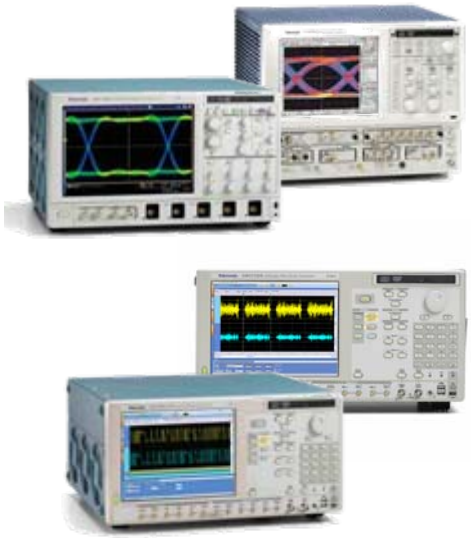
Tektronix USB Solution

Complete solution: from PHY layer to Protocol for USB 2.0, 3.0 and Wireless USB (Only approved Method of Implementation (MOI) for WiMedia PHY Leadership in USB)



Cost Effective: Automation with a single box solution

Connectivity: Measure closest to Tx output for true performance of USB 3.0 device/host

Flexibility: Compliance, debug, characterization with software channel emulation

USB leadership:

1. Tektronix 1st to market for USB 2.0
2. Tektronix is active in USB-IF Compliance Group and USB 3.0 PIL and contributes to USB 3.0 specification (only T&M Technical Contributor in the USB 3.0 specification)

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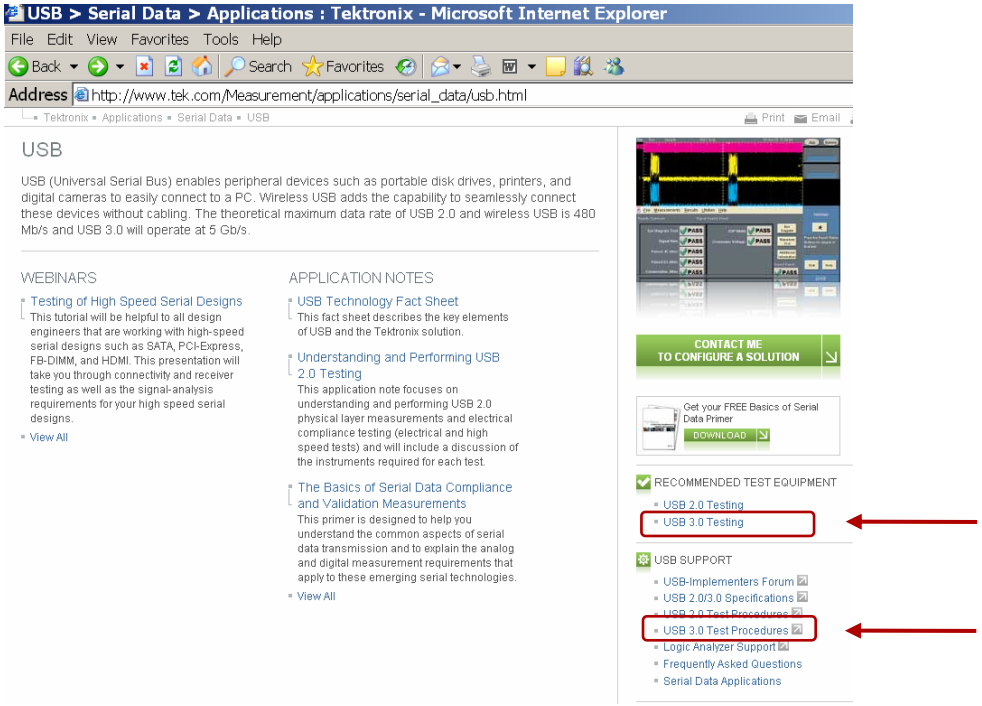
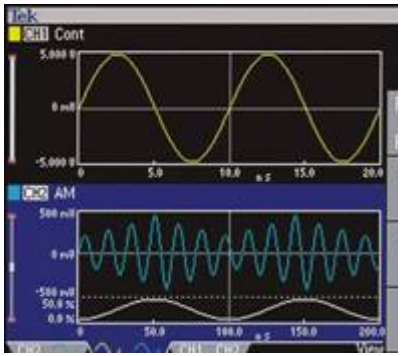
Resources

- Access to Specifications
  - Rev 1.0, http://www.usb.org/developers/docs/
- Tektronix USB Electrical PHY Tools
  - www.tektronix.com/usb
  - www.tektronix.com/software
- Ellisys Protocol Tools
  - www.ellisys.com



Enabling Innovation in the Digital Age



Accelerating Performance

Enabled by High-speed Serial Technologies

Tektronix®
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