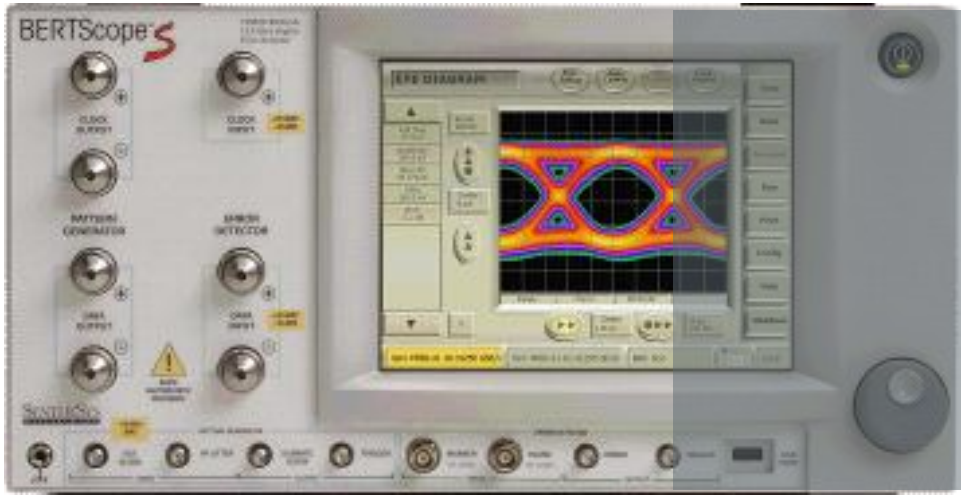
高速串行系统接收端测试解决方案
BERTScope



The Vision of Oscilloscope, the Confidence of BERT

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日程

下一代高速串行系统测试解决方案-BERTScope

- 高速串行技术发展趋势和潜在挑战
- BERTScope系列产品介绍
- BERTScope "BASIC"
  - 基本功能(BER Measure)
  - 信号分析(Analysis)
  - 压力测试(Stressed Eye)
  - 系统集成(Integrated Solution)
  - 总结(Conclusion)

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高速串行技术趋势和影响

PCI EXPRESS

SERIAL ATA

HDMI

ddr3 A JEDEC STANDARD

DisplayPort

SUPERSPEED CERTIFIED USB

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IEEE GbE

行业/技术/市场趋势

- 接口从低速并行技术转向高速串行技术
- 数据速率继续提高：
  3 ⇒ 6 ⇒ 10 ⇒ 12 Gb/s
- 行业标准化，实现即插即用互连
- 消费电子成为更大的推动因素

对测试测量的影响

- 千兆位数据速率需要性能更高的产品
- 行业标准提出了严格的测量和分析要求
- 测试整个系统，包括发射机、接收机和传输路径或电缆
- 要求广泛的产品系列及提高一致性测试的自动化程度
- 测试测量在标准机构中发挥着关键作用

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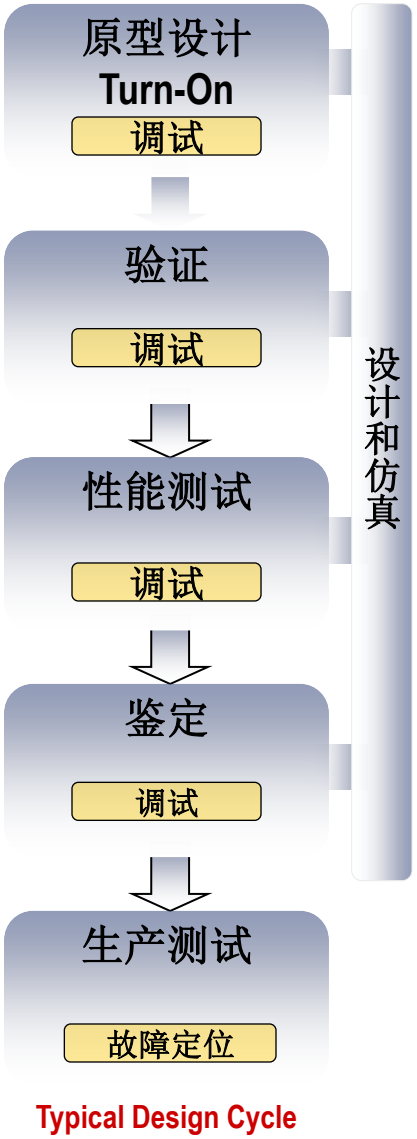
客户挑战

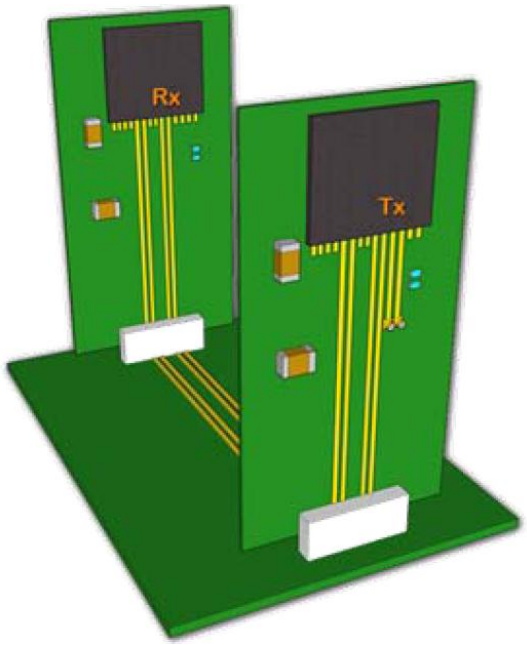
- Time to Market
  - 最小化每一个环节的设计周期
- 更大系统复杂性
  - 更复杂的信号特性
  - Tx、Rx和链路之间的交互性越来越强
  - 信号完整性越来越复杂
- 越高的速率= 越少的裕量
  - 越少的裕量意味着要求更精确的测试工具
  - 越少的裕量意味着要求更精准的信号完整性

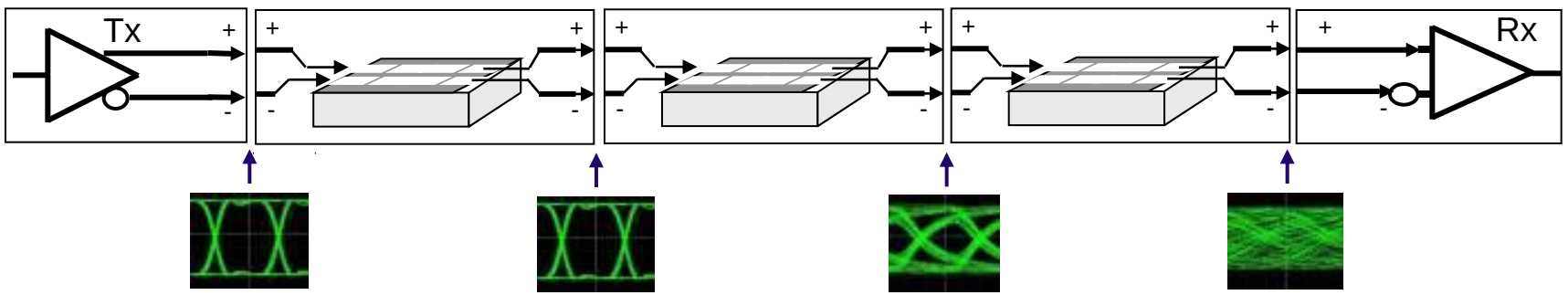


Typical Design Cycle

Why Test the Receiver?

- Serial Data communications standards have always specified both the **transmitter** and **receiver** physical layer characteristics
- Historically receivers have not been tested in compliance workshops except in communication standards
- *Why?*
  - Receiver testing was perceived as “difficult”
    - In reality – not familiar
    - Testing requires different instruments
    - Test set up requires “calibration” before use.
  - There was enough margin to assure system testing covered through transmitter test and interoperability





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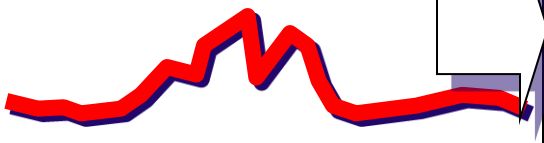
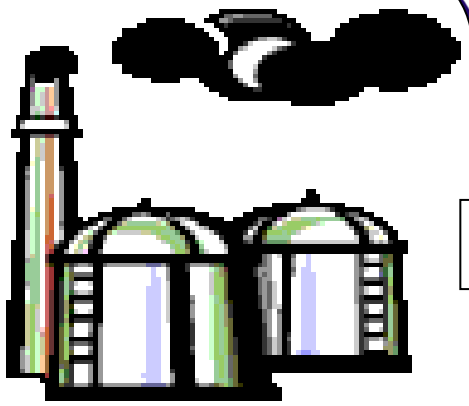
Why Receiver Testing is Different

Receivers

Poor quality bits in….

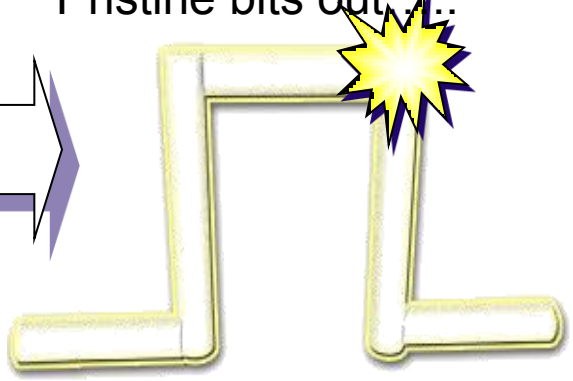


"Receiver", "Re-Timer"
"Decision Circuit", "SERDES"



Receiver

Pristine bits out…..



- Transmitters are tested with eye diagram analysis but a Receiver Changes *Everything*
- Can no longer rely on how good the eye looks as a measure of performance….
  ….the eye shape only tells how nice the output stage is.

Bright… Shiny…
New…

Wrong?

Receivers are Tested with BER

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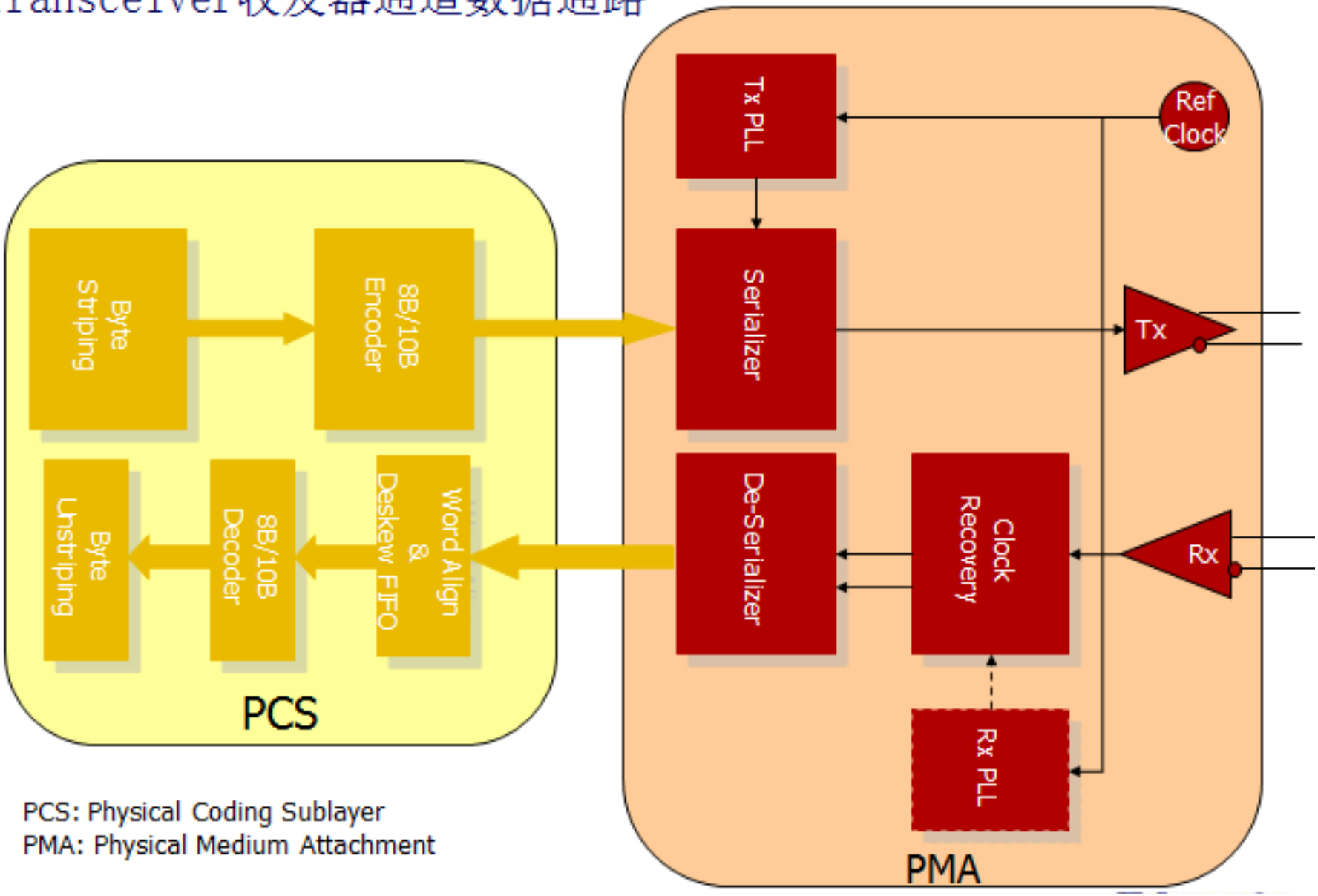
Transceiver收发器通道数据通路



PCS: Physical Coding Sublayer
PMA: Physical Medium Attachment

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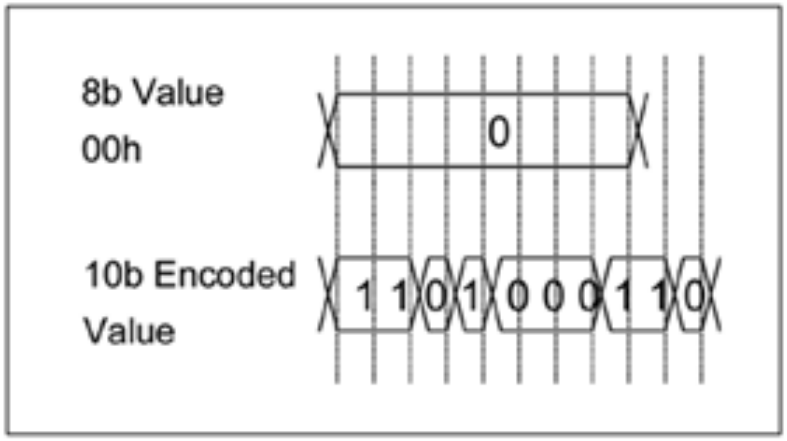
8B/10B 编码

- 提供足够的跳变，加快时钟重建
  - CDR要求数据有足够的pattern Density，否则会锁定错误时钟频率
- 控制码型
  - 输入256个码型
  - 输出1024个码型
  - 有意义的输出码型512个（positive/negtive各256个）
  - 控制码型24个（Positive/Negtive各12个）
- 提供平衡的直流偏置，减少漂移
  - 高速串行信号大多是NRZ基带编码
  - 通过8B10B编码，能够避免过多的0和1出现，平衡信号直流成分
  - 大多数SerDes都用共模电压的要求
- 错误检测
- 带宽开销25%

Bad



Patent: Widmer & Franaszek IBM, September 1983

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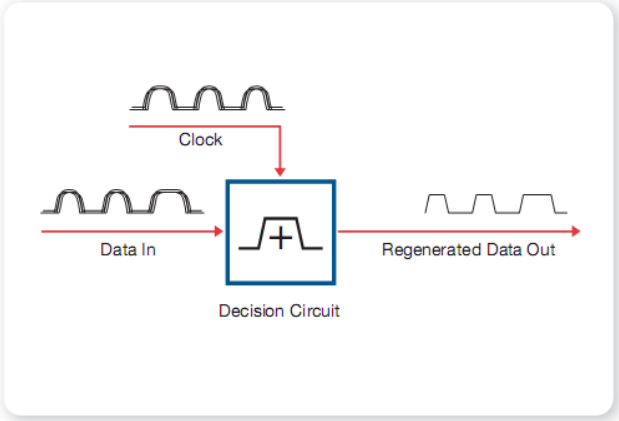
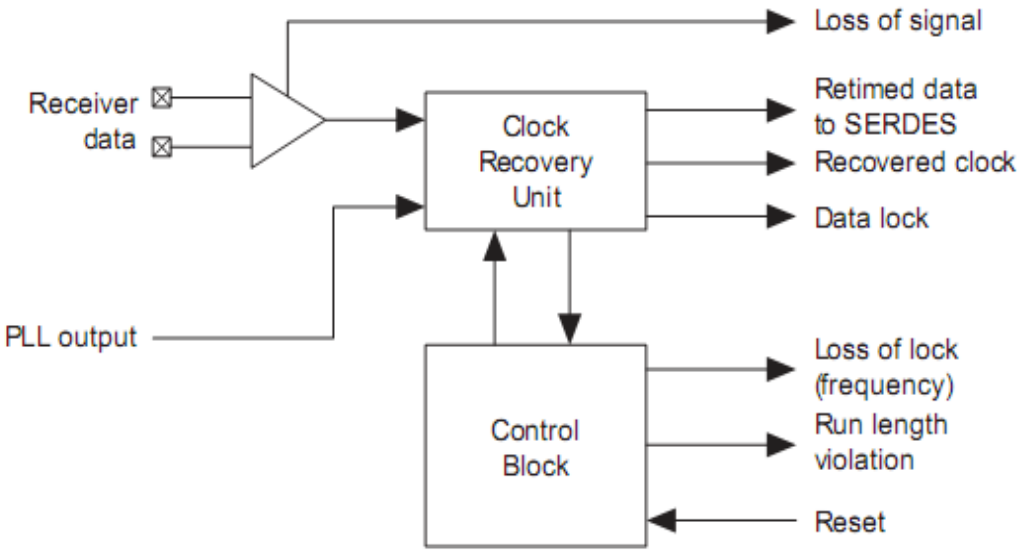
Clock Data Recovery

- 由于串行高速信号没有单独的始终传输，因此需要从数据中得到时钟信息，进而进行数据采样
- CDR内部核心是PLL。因为PLL传输响应为LPF，因此CDR能够“跟踪”一定频率下的抖动
- De-serializer依靠CDR恢复出的时钟进行采样。
- 数据Pattern Density必须足够多
- “跟踪”上的抖动“不算”抖动

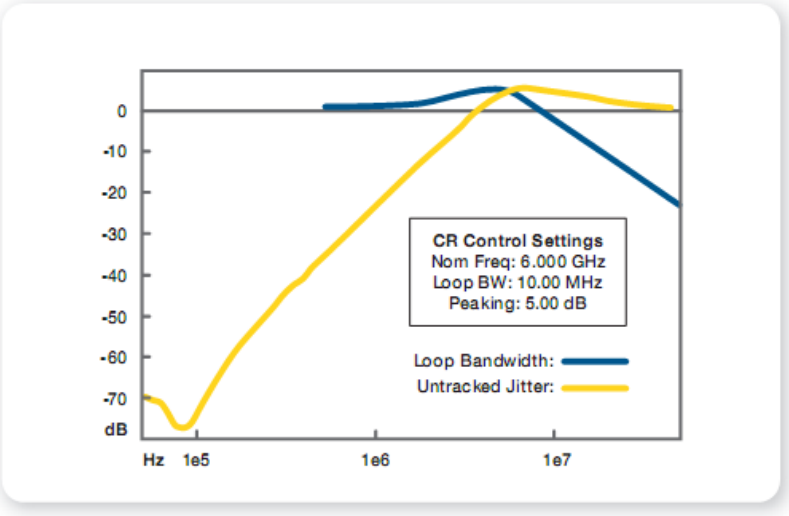




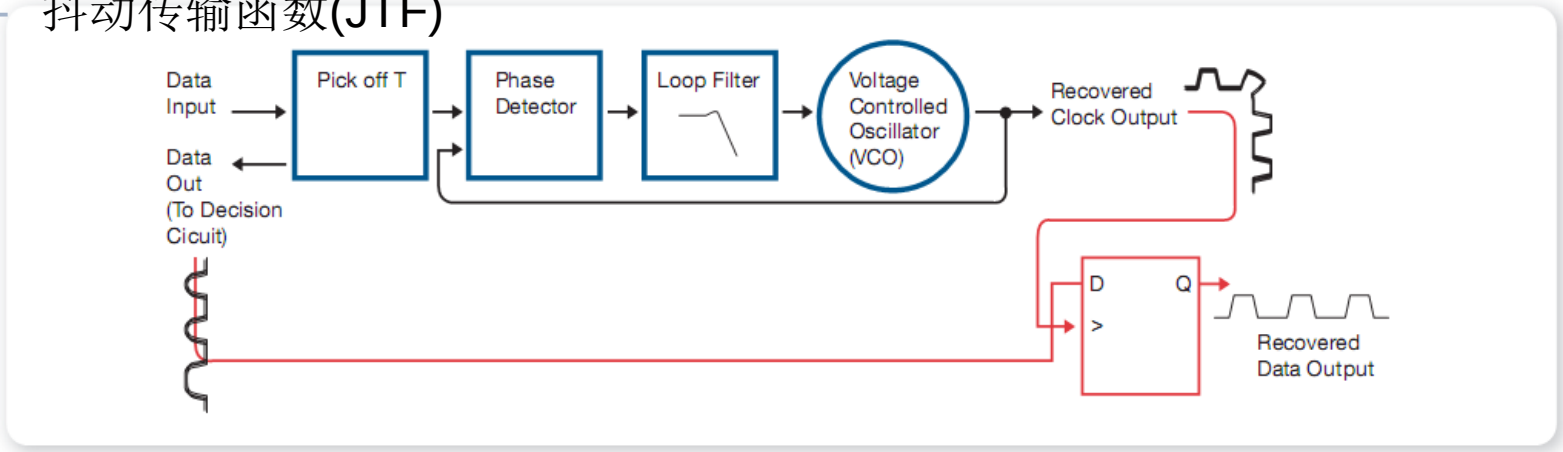
CDR功能框图

CDR基本结构

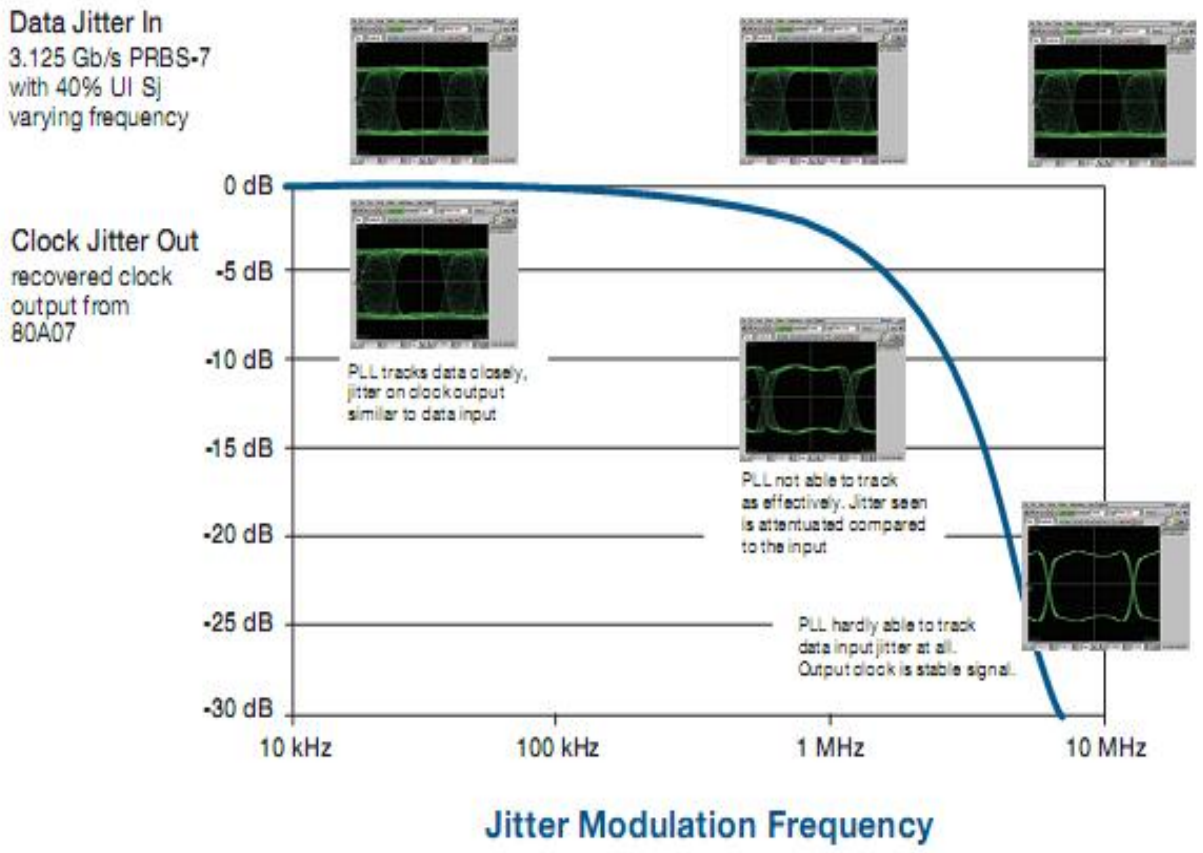
- PLL
  - Phase Detector
  - Loop Filter
  - VCO
- Loop Filter决定了CDR跟踪抖动的带宽
  - Type I / Type II
  - 一阶 / 二阶
- 描述方式
  - PLL传输函数
  - 抖动传输函数(JTF)



PLL传输函数和JTF



CDR对系统抖动的影响



注意：示波器是以Receiver的角度考察信号。在上例中，信号以及从信号恢复出的时钟同时输入到示波器中

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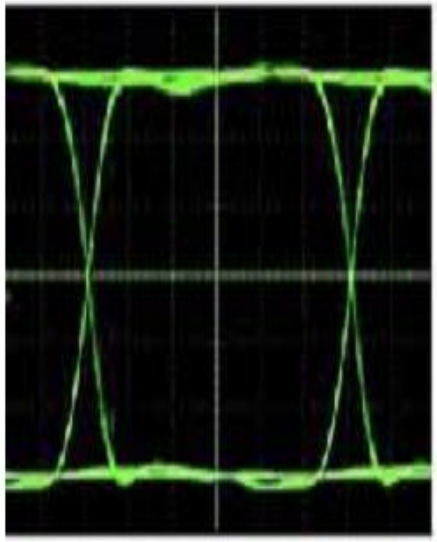
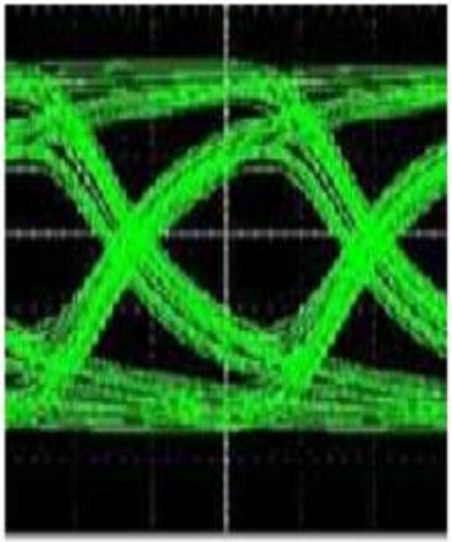
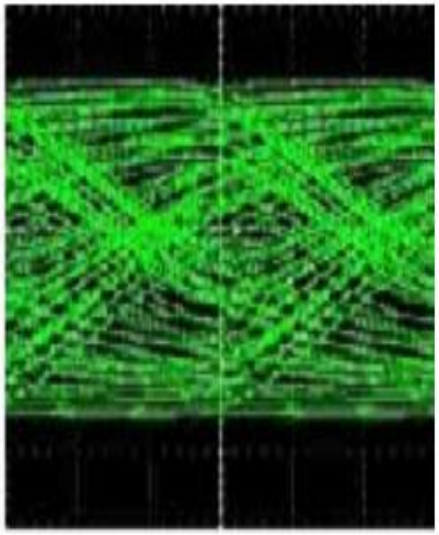
Lossy Line的原因及后果

- Conductor Loss
  - DC resistance
  - Skin Effect
- Dielectric Loss
  - Material Property
  - Variant of Dielectric constant
- ISI产生的根源

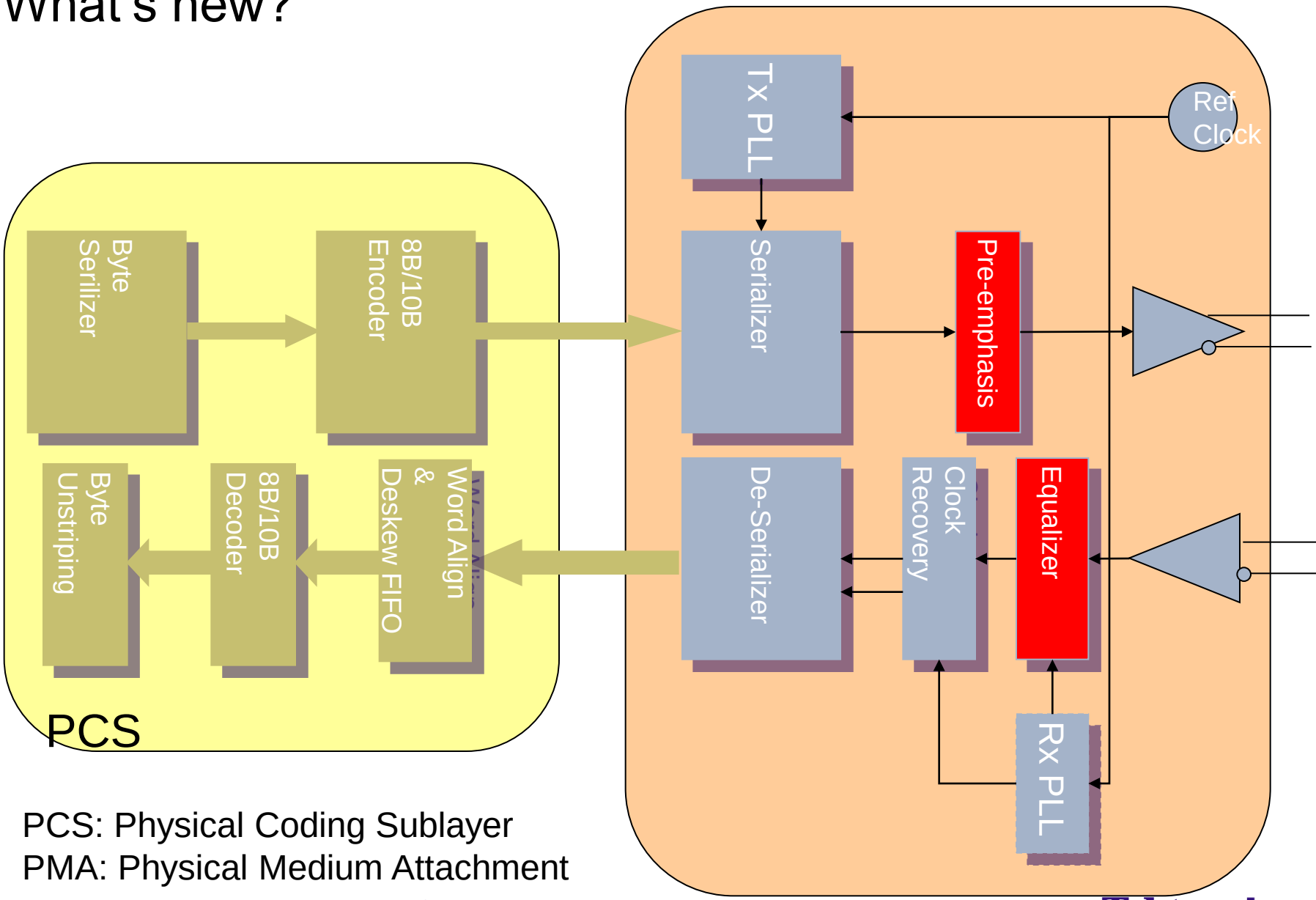
- 从频域角度的理解
  - Channel带宽低，将信号的高频能量衰减，导致上升时间缓慢







Transceiver收发器通道数据通路
What's new?



PCS: Physical Coding Sublayer
PMA: Physical Medium Attachment

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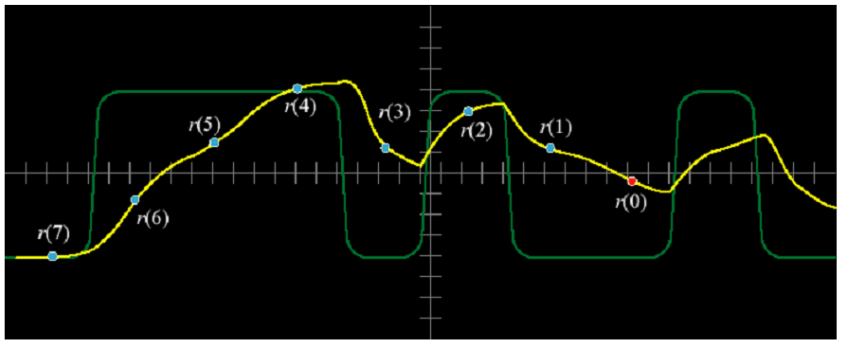
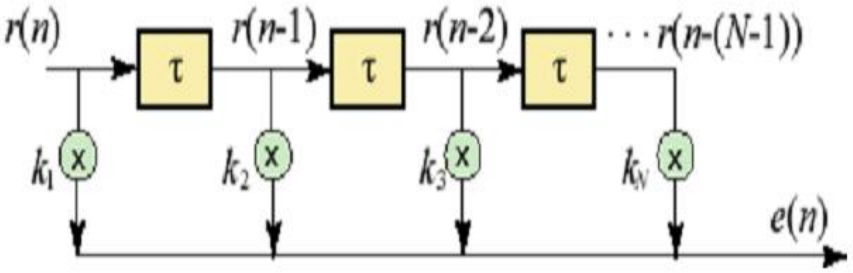
Equalization

- 为了弥补Channel对信号的损伤，可以采用Equalization均衡技术，主动或者被动的对信号进行补偿
- Tx端的Equalizer称为Emphasis
  - Pre-emphasis
  - De-emphasis
  - Tx端对信号主动的调节
- Rx端的Equalizer
  - FFE
  - DFE
  - CTLE（连续时间线性均衡）
- Emphasis在Tx运用的非常多，几乎所有的芯片都提供了Emphasis的能力
- Equalization在高速的芯片Rx端才会使用
  - SATAIII，PCIE Gen2，USB3，etc.（BitRate>5.0Gbps必须使用）

最基本的Equalizer：FFE

- FFE：Linear Feed Forward Equalization
- 又称为LFE、FFE
- 思路：当前bit位r(n)受到前边r(n-1) 、r(n-2) 、r(n-3)…的影响，因此，根据r(n-1) 、r(n-2) 、r(n-3)的情况来修正r(n),即构建：
- $e(n)=r(n)*k_1+r(n-1)*k_2+\cdots+r(n-(N-1))*k_N$
- FFE天生就是FIR



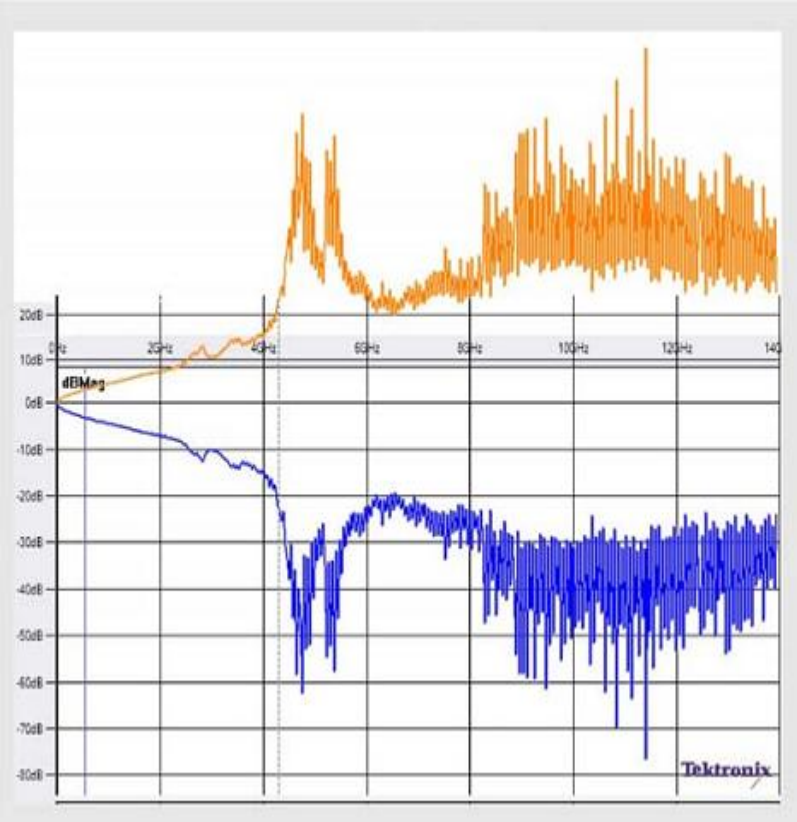


如何构建FFE

- 使用TDR或VNA对Channel进行S参数测试，得到Channel的频响
- FFE的频响应该是Channel频响以Gain=0dB为轴的对称，使FFE和Channel的频响乘积为0dB
- 结构简单、成本低廉
- 在放大了信号的同时放大了噪声
- N取值有限，即只能考虑到有限个bi的t影响
- Emphasis就是有2个tap的FFE
- 例如3dB的Pre-emphasis：

$$e(n) = a * r(n) + b * r(n-1)$$

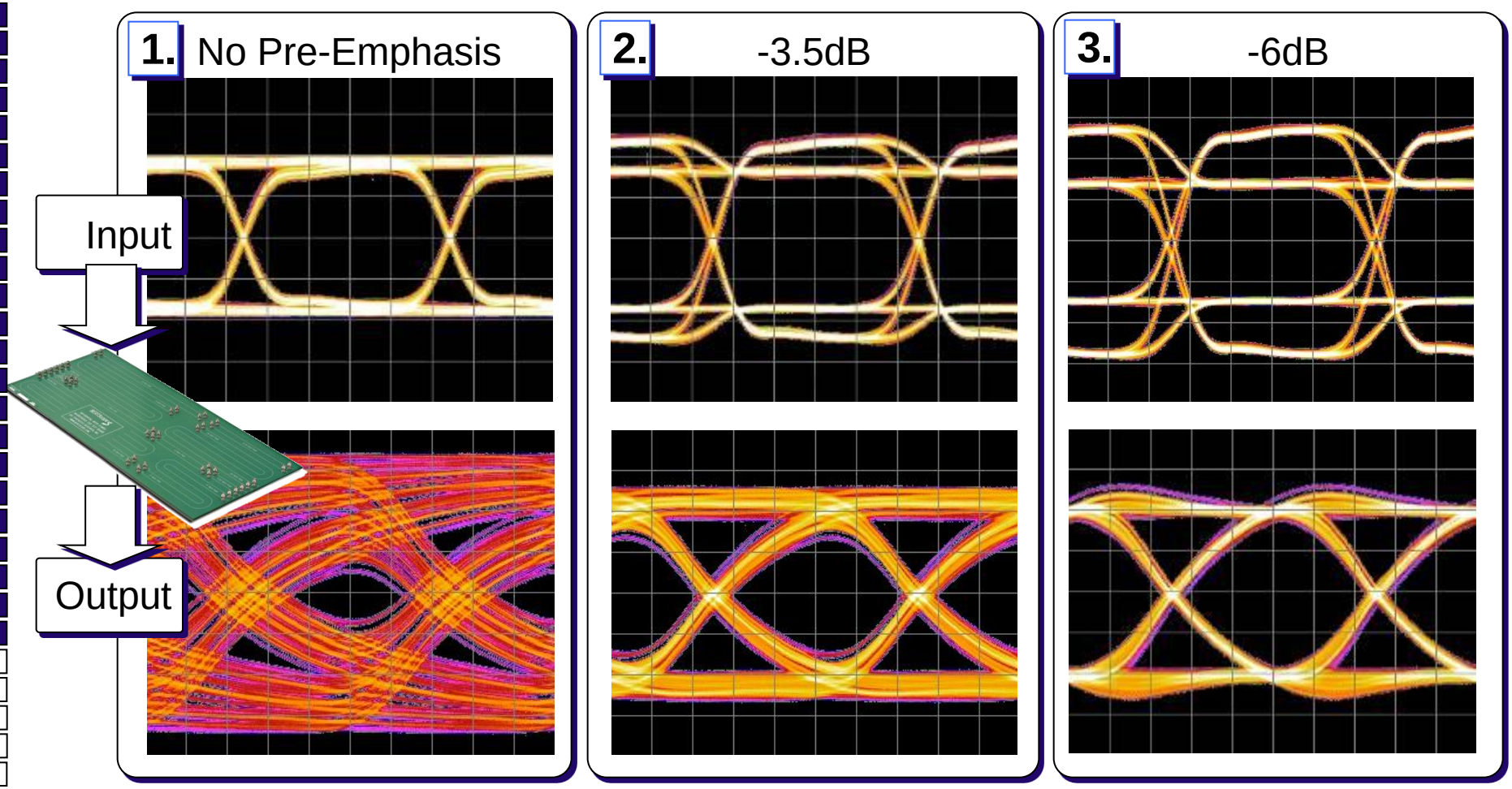
e(n)	r(n)	r(n-1)
1	1	1
1.4	1	-1
-1.4	-1	1
-1	-1	-1



Channel S参数
设计FFE的频响

按照pre-emphasis要求可以列出上表，解出该二元一次方程即可得到tap系数
Solution: a=1.2，b=-0.2
[r(n)归一化为±1]

Pre-Emphasis
Impact on Eye Diagrams



Measurement of Eye Diagrams on BERTScope

40” PCI Compliance ISI Board, 5Gbps PRBS-7 Data

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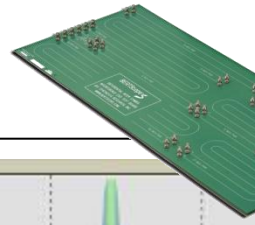
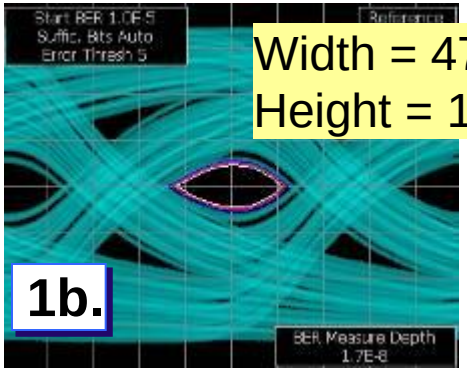
Pre-Emphasis
Impact on BER and Eye Margin



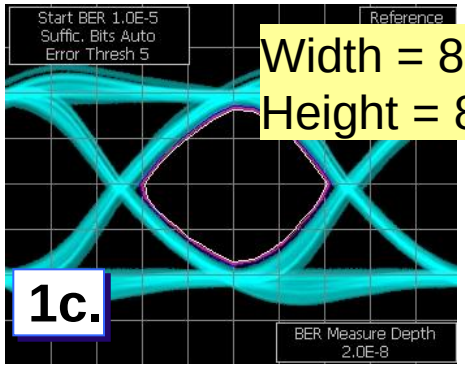
Eye Opening 1.
(BER Contour Measurement)

Measurements on BERTScope



Width = 47%UI
Height = 18%UA

1b.



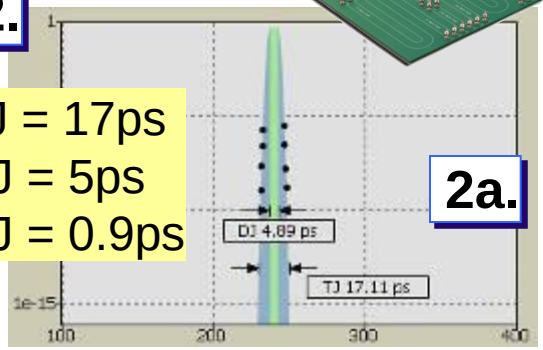
Width = 81%UI
Height = 82%UA

1c.

Jitter Peak 2.
(Bathtub)

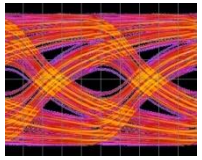
No Channel a.

TJ = 17ps
DJ = 5ps
RJ = 0.9ps



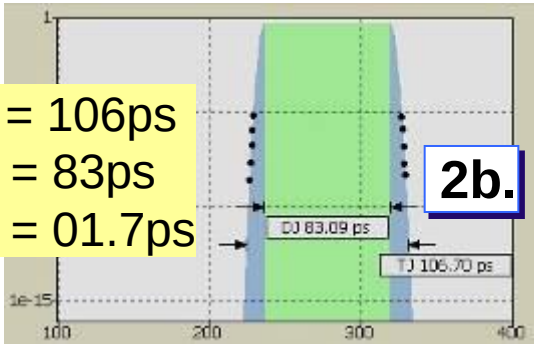
2a.

40" Trace, no Pre-Emphasis



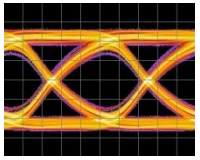
b.

TJ = 106ps
DJ = 83ps
RJ = 01.7ps



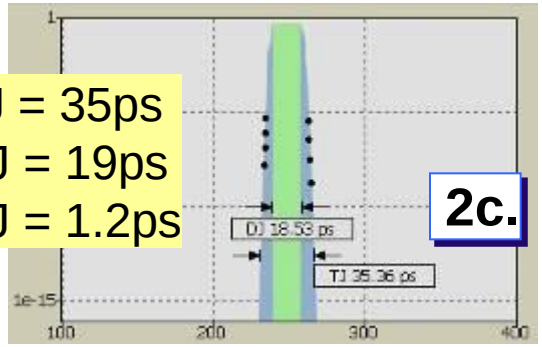
2b.

40" Trace, 6dB Pre-Emphasis



c.

TJ = 35ps
DJ = 19ps
RJ = 1.2ps



2c.

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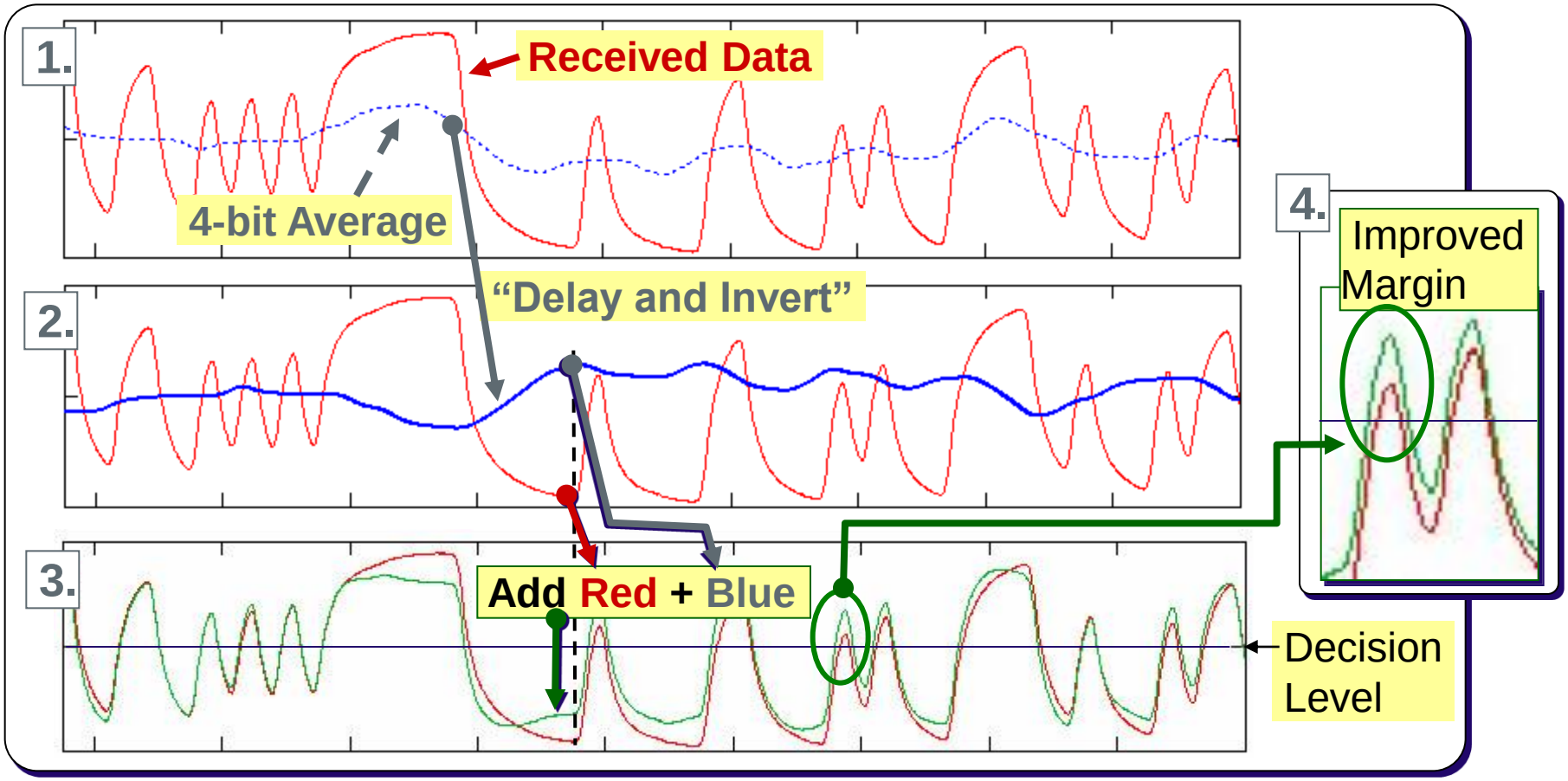
Decision Feedback Equalization

Effectively further open the eye

Correct baseline wander of received data stream by subtracting-off a portion of recent history



40" PCI Compliance ISI Board, 5Gbps PRBS-7 Data

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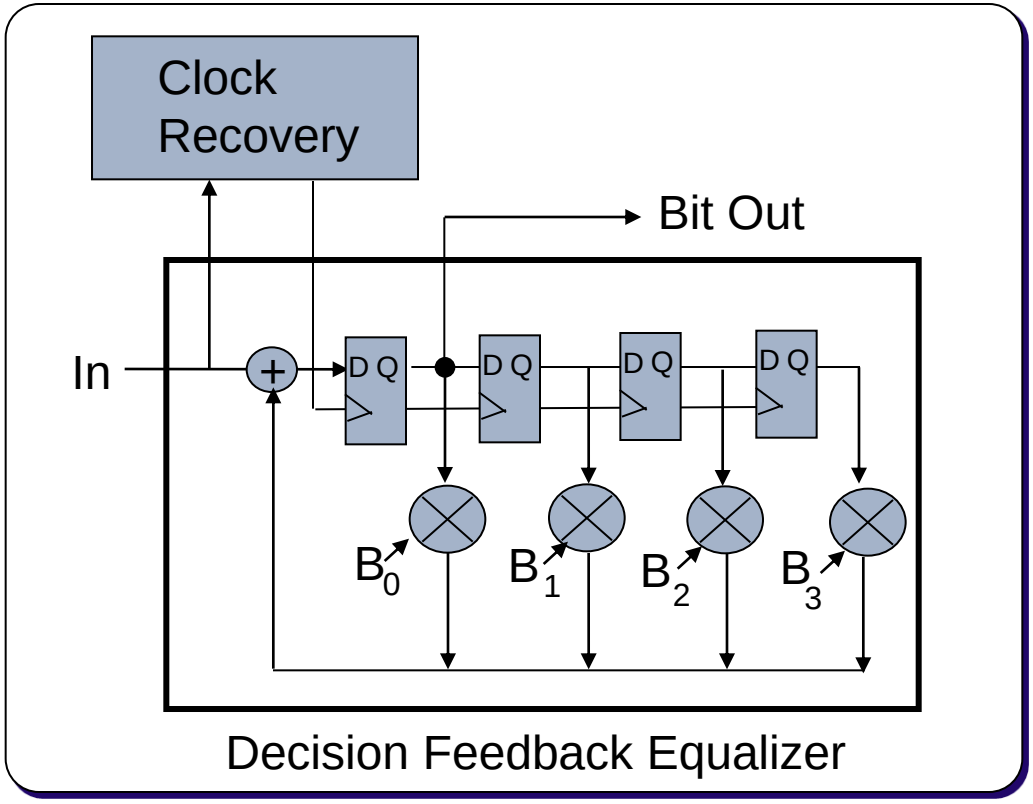
Decision Feedback Equalization
Block Diagram



- Clock recovery is required for the DFE to operate
- More or Less flip-flops can be used
  - This varies the amount of equalization

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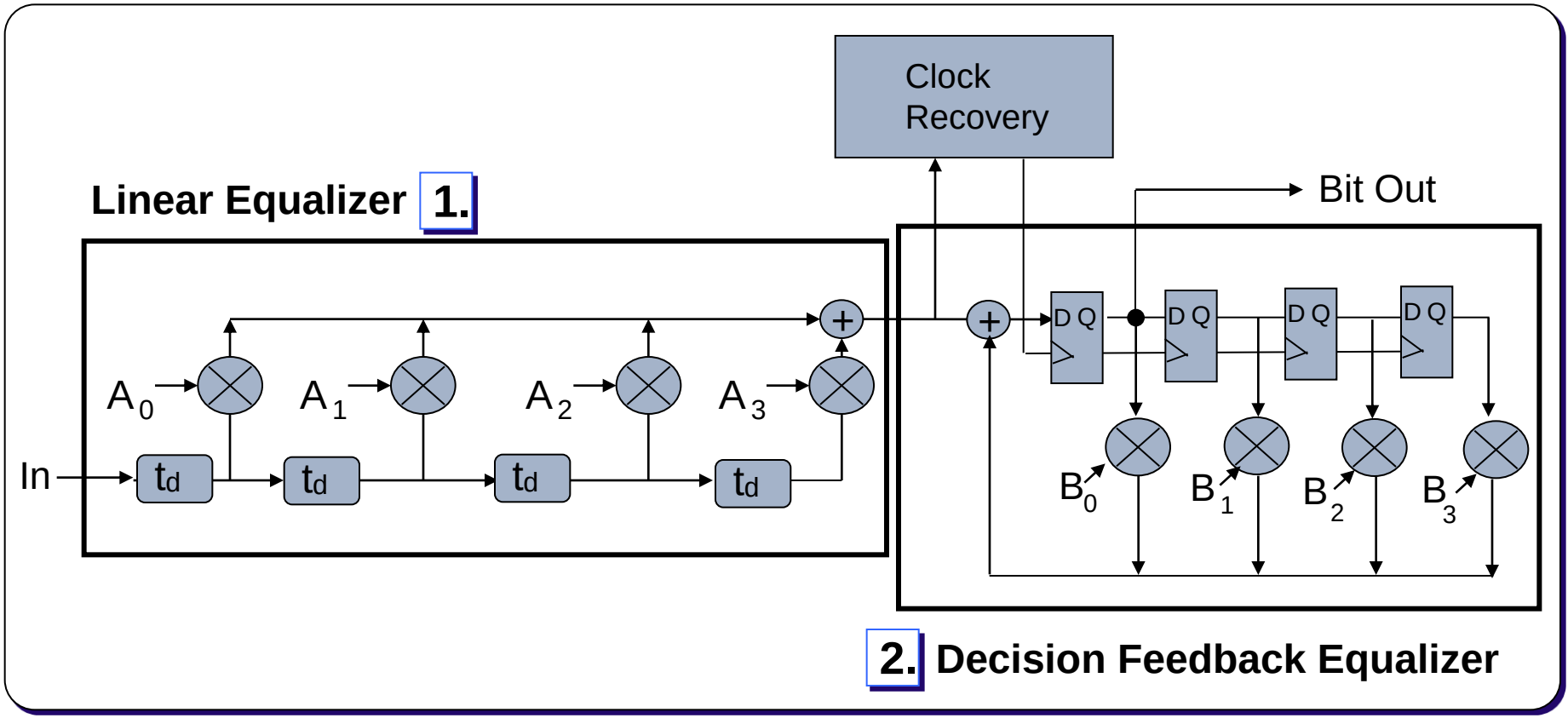
High-End Receiver-Side Equalization
Block Diagram



- Implements a 4 tap linear equalizer with a 4 tap DFE

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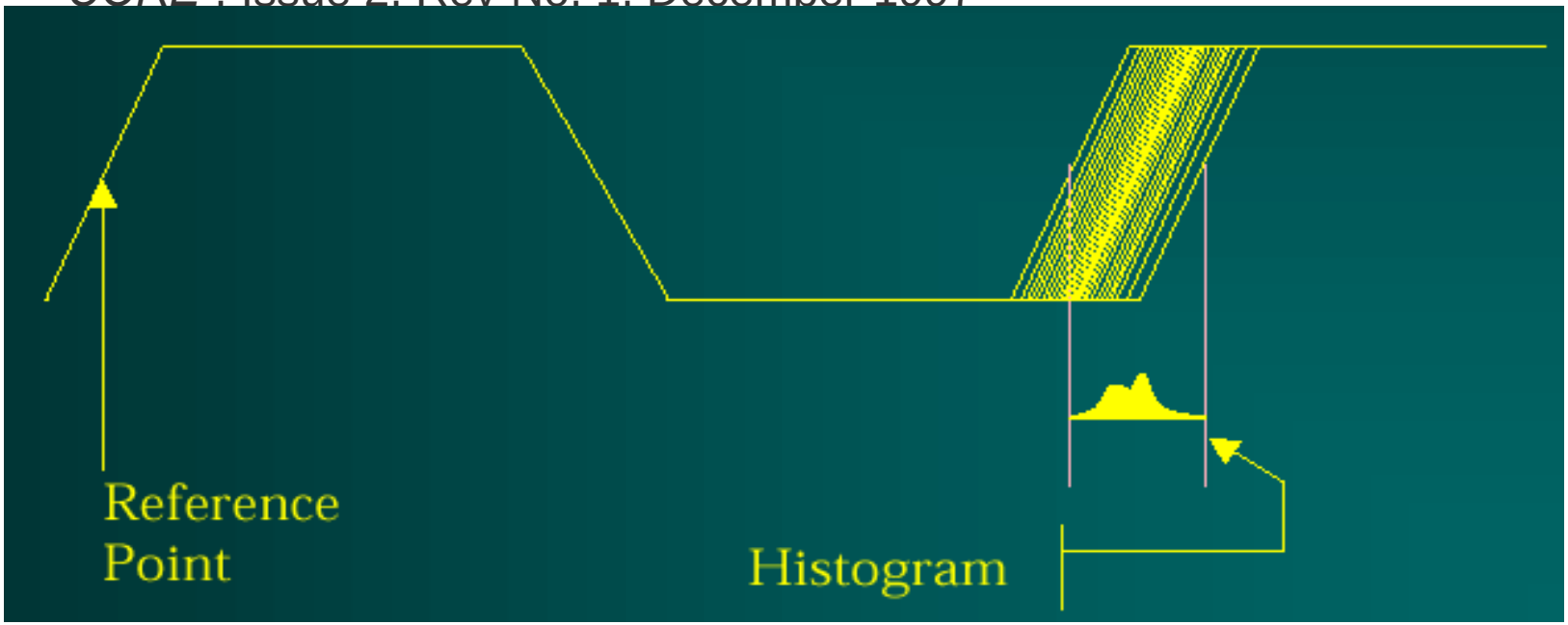
抖动ABC-什么是抖动

- **定义：“信号的某特定时刻从其理想时间位置上的短期偏离为抖动”**
  - 参考: Bell Communications Research, Inc (Bellcore), *“Synchrouous Optical Network (SONET) Transport Systems: Common Generic Criteria, TR-253-CORE”*, Issue 2, Rev No. 1, December 1997



抖动会带来什么问题？

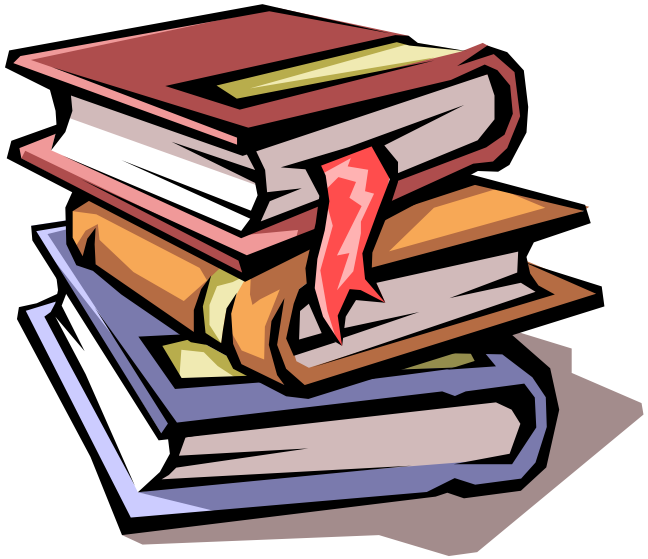
- 传统的并行式数据通信，即多通道数据与时钟分别传送，往往因为PCB阻抗不匹配，传输路径不一致而产生建立与保持时间违反。当速度增加的时候，准确控制传输时延显得异常的困难，今天新颖的数据通信都已经是串行了，不单只使用一对差分线来传送数据，以减低信号EMI的干扰，更往往将时钟嵌入在数据中， 而接收端则使用CDR从数据中恢复时钟出来。 所以，若数据的抖动过大，频率过高，接收端的CDR将无法恢复时钟而导致误码。 所以需要控制系统的时钟与输出的数据抖动。

- 抖动直接减小了逻辑数字系统的建立保持时间的余量， 严重的影响逻辑运作。

- 有些情况，尤其以计算机行业应用为多（因不能有足够的空间进行EMI控制），使用一低频信号调制其高速时钟，在频谱上的效果是使其能量被扩散， 从而减小EMI干扰。在时域上效果是时钟的周期性抖动，其抖动波形正是调制信号。

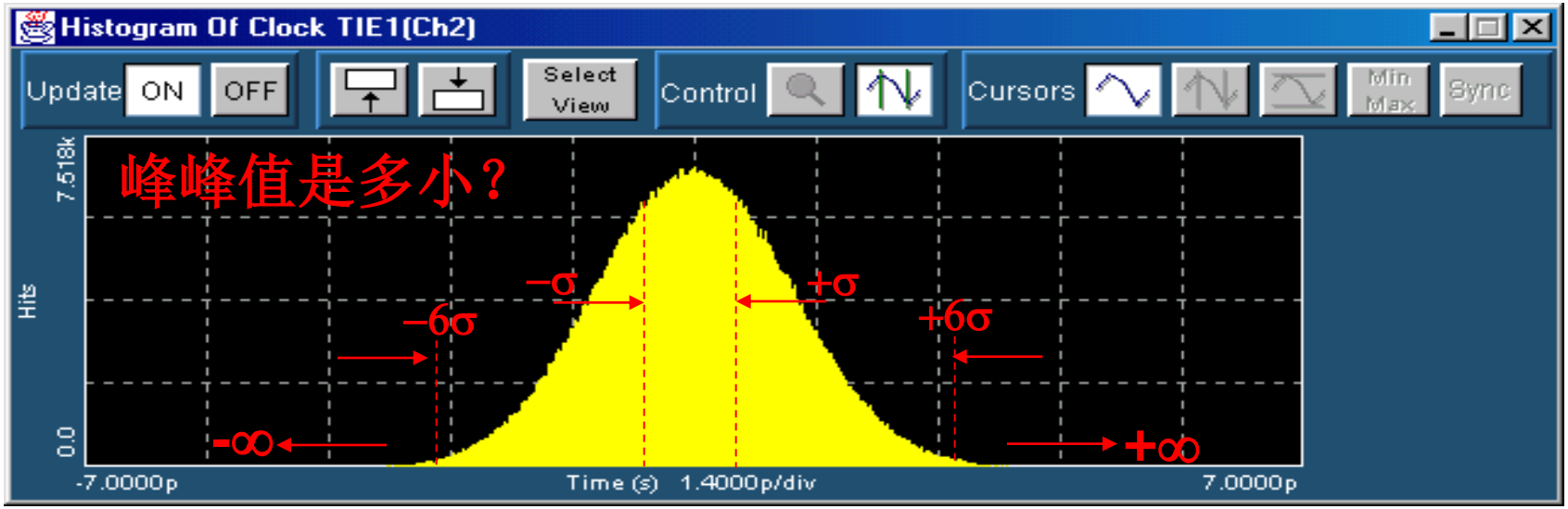
抖动深入剖析—抖动的成因及分类

- Total Jitter (Tj)
- Random Jitter (Rj)
- Deterministic Jitter (Dj)
  - Periodic Jitter (Pj)
  - Duty Cycle Distortion (DCD)
  - Inter-Symbol Interference (ISI or DDJ)



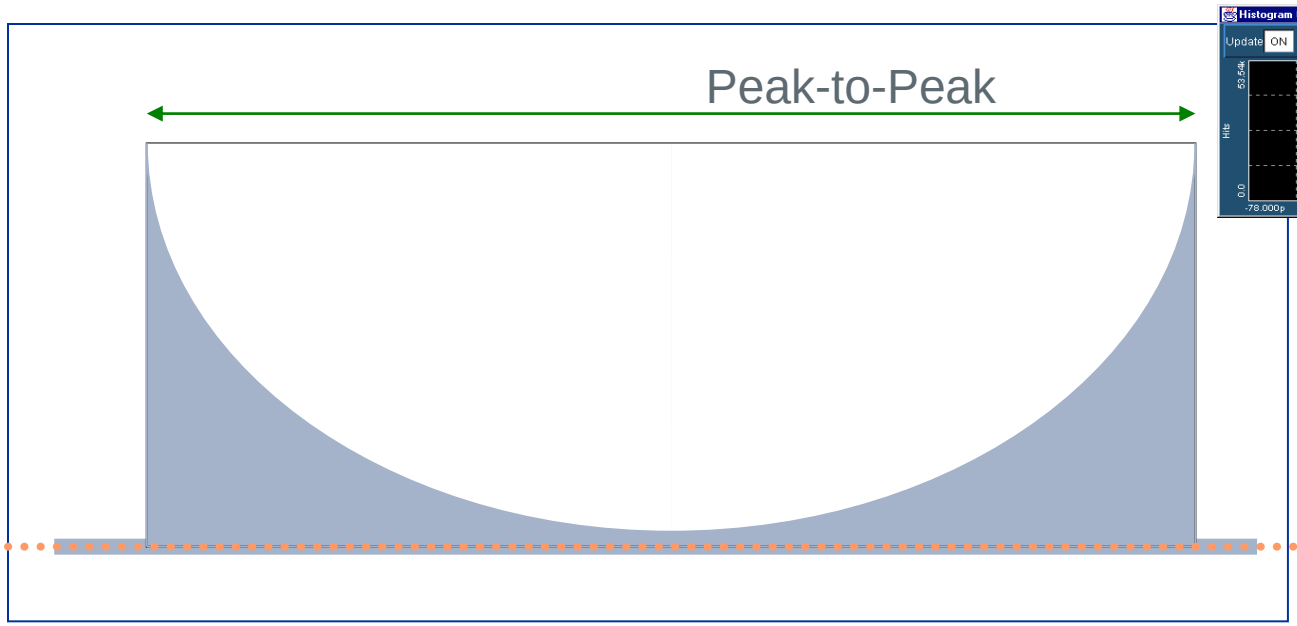
Random Jitter

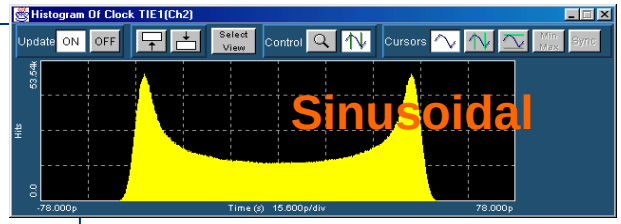
- 随机抖动的统计分布是正态高斯分布
- 直方图 (有限的采样数) ↔ 概率密度函数呈现高丝分布(数学的模型)
- 因为随机抖动是高斯分布，所以是无边际的。按理论，随机抖动的峰峰值随测量时间变长而增加。



Periodic jitter

- TIE vs. time 时间间距误差随时间的变化是一重复的，周期性波形
- 效果等同于频率调制FM
- 可能的抖动源– 电源的EMI干扰与扩频时钟SSC的调制信号

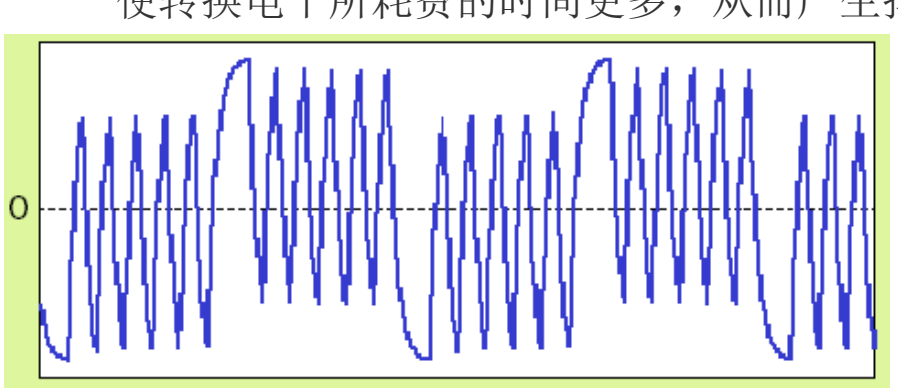


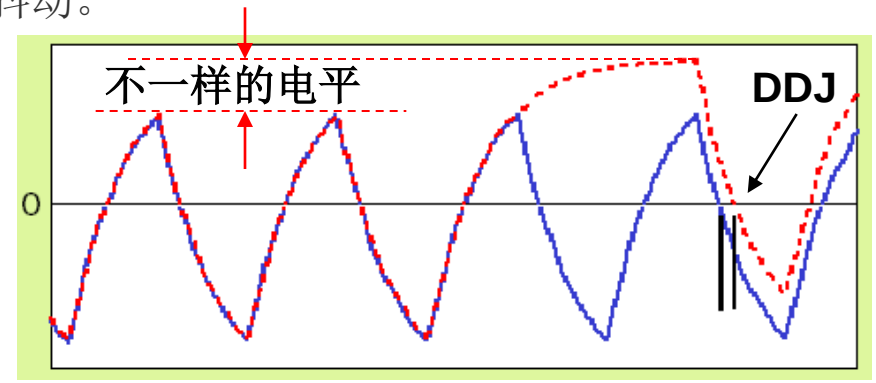


ISI Jitter

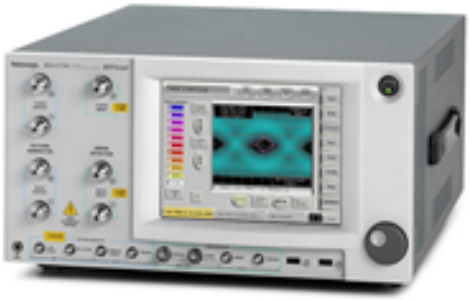
- ISI又称为DDj数据相关抖动或PDj码型相关抖动
- 因为有限的带宽限制
  - 驱动器 Driver
  - 对比器Comparator
  - PCB线路与电缆的衰减与损耗

  对经常切换的“1,0,1,0,…”的高频信号，衰减比连续的“1,1,1,1,0,0,0,0,…”的低频信号要来得厉害。所以长的连续不变码到达更高的电平，在跳变时需要更多的时间才能到达门限电平，导致信号抖动。因为这个抖动的幅度与码型相关，所以又称码型相关抖动。
- 因为阻抗不匹配导致信号发射。被发射的信号叠加在原由的信号导致幅度增加而最终使转换电平所耗费的时间更多，从而产生抖动。





BERTScope系列产品概览



BERTScope

- 主要产品BSA系列
- BERT和示波器的结合，基于BER的分析、测试平台
- 主要应用于高速串行和通信的芯片、系统测试

New Product Launch

- ☐ 28.6G
- ☑ 26G
- ☑ 17.5G
- ☑ 12.5G
- ☑ 8.5G

Clock Recovery

- 配合BERT和示波器使用
- 抖动测量

- ☑ 28.6G
- ☑ 17.5G
- ☑ 12.5G

Pre-Emphasis

- 配合BERTScope码型发生器使用
- 提高输出加重以克服通道损耗

- ☑ 12.5G

Bitanalyzer

- 基本的误码仪和示波器
- 最低码速率100K，适合于卫通应用

- ☑ 1.5G/1.6G

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什么是BERTScope?

针对计算机系统和通信串行数据的应用而设计，同时集成误码仪和示波器的仪器。

1 Pattern Generator产生特定的比特码流，例如. PRBS 码型；信号可以被施加压力

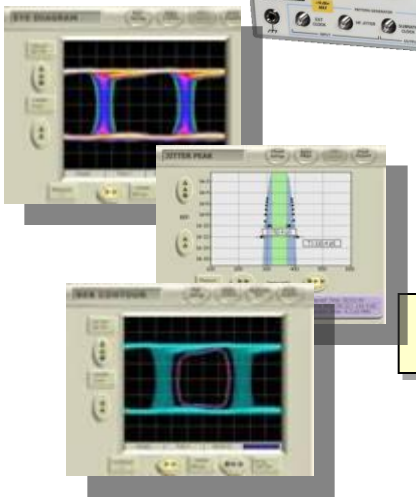
从带压力的Pattern Generator输出

loopback

到 Error Detector

被测芯片/被测系统
有源/无源

2 比特码流从DUT输出到Error Detector比较以进行BER测量



3 进行BER测试，也能像示波器一样进行分析

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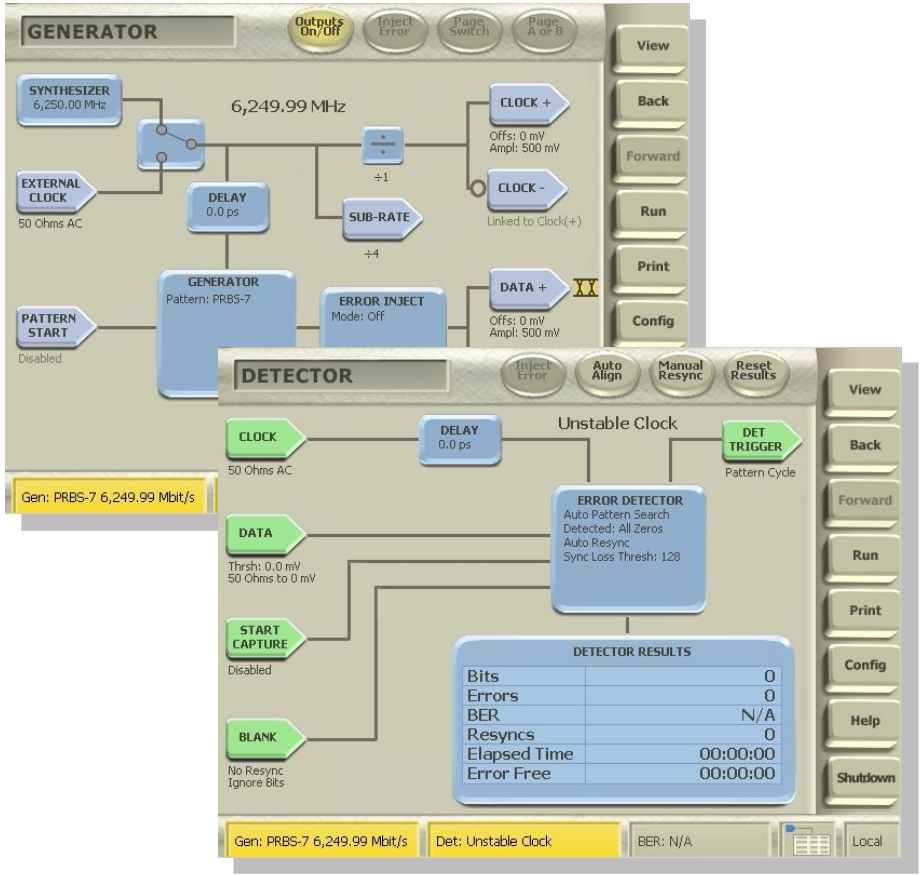
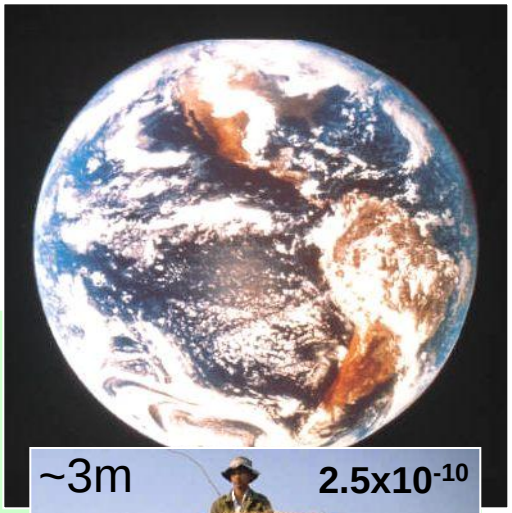
BERT基本功能

- 码型发生器(PG)
  - 业内最高速可加压码型发生器：26Gbps
  - 业内最深的延迟线，产生幅度更大的抖动
- 误码检测器(ED)
  - 精确高达100fs的延迟线，业内唯一BERT可支援PRBS31抖动分离的黄金参考 (option J-MAP)
  - 专利的Dual ED构架，快速准确完成眼图、抖动测量
  - 快速比特同步
- 时钟恢复器(CR)
  - 业内最高速的仪器级CR: 28.6Gbps
  - 业内参数设置最全的CR: 连续调谐 Loop BW/Peaking
  - 外置模块、配置灵活



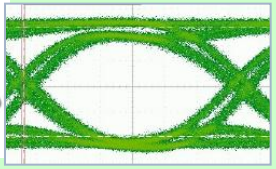
Beyond the BERT...

误码仪和示波器之间的信息鸿沟



示波器：非常直观，能够进行故障定位和调试

Oscilloscopes



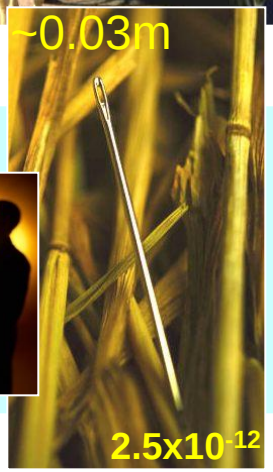
"I think I may have seen a glimpse of it, but it's hard to tell…. It sure looks pretty from up here though!"

Information Gap

Bits	56,718,374,656
Errors	14,134

BERTs

"I can see it - I can't show you it, but you've missed it!"
"You've missed it again!"
"You've missed it again!"



误码仪：精确的测量每一个比特，但是对故障调试没有帮助

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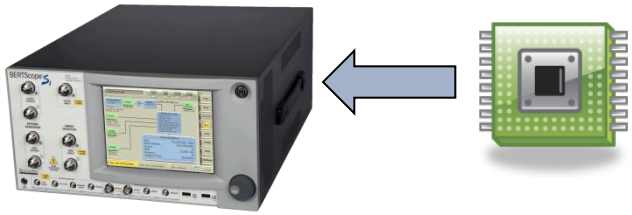
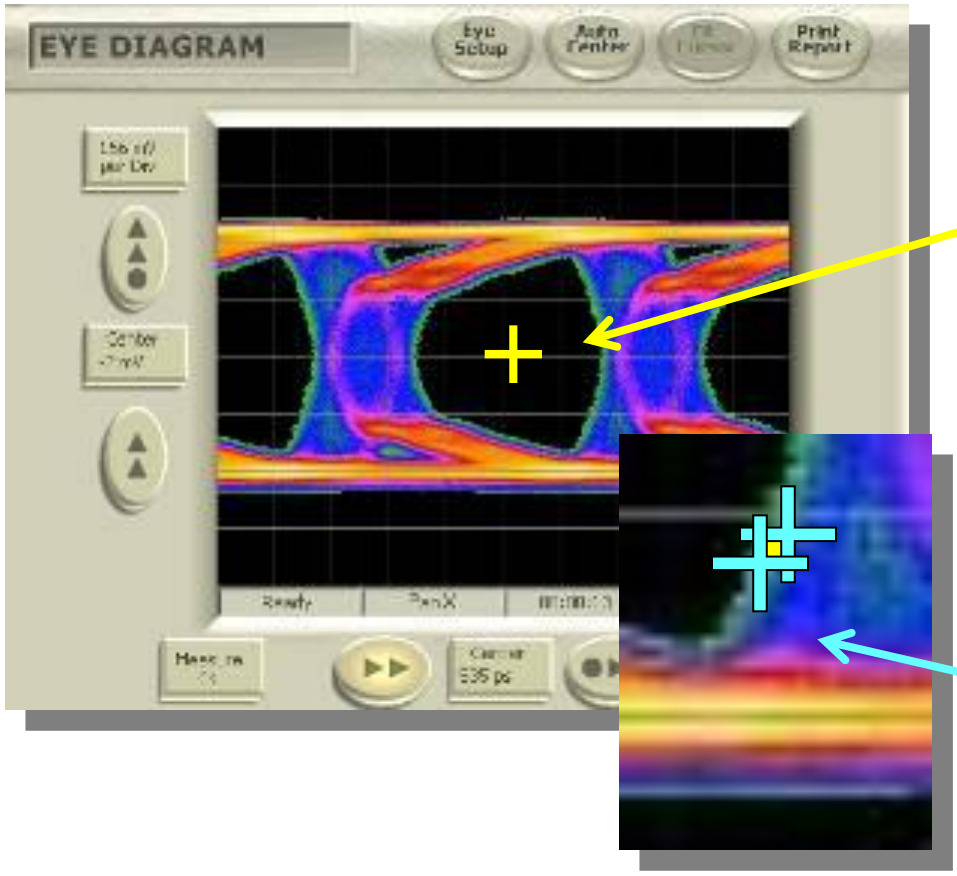
使用BERTScope深入分析误码率事件

The BERTScope Eye Diagram





1

用一个比较器，可以比较输入的bit和参考bit之间的差异-> BER 测量

2

用两个比较器，可以测量出有多少bit落在两个比较器之间–> 眼图！

可以区分不同误码率事件，找到外部信号和误码之间的关联

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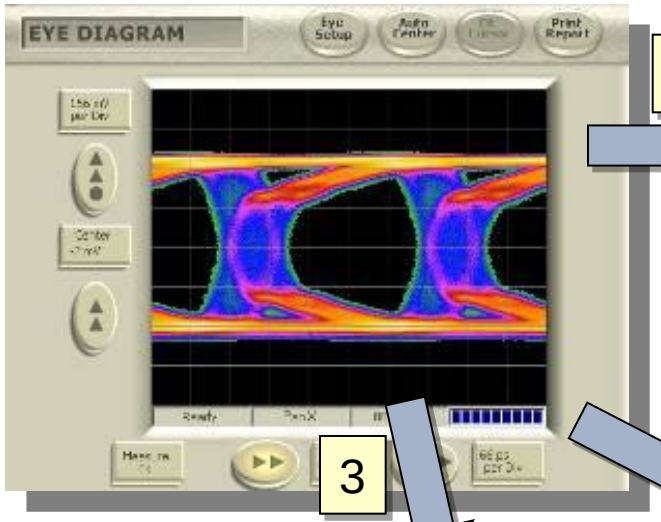
Beyond the BERT...

使用BERTScope深入分析误码率事件

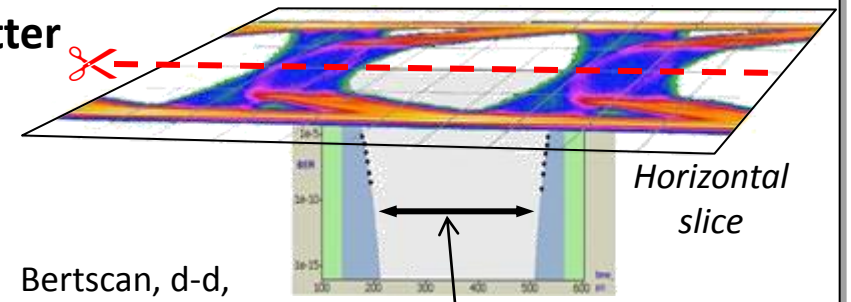


1

2

3

Jitter

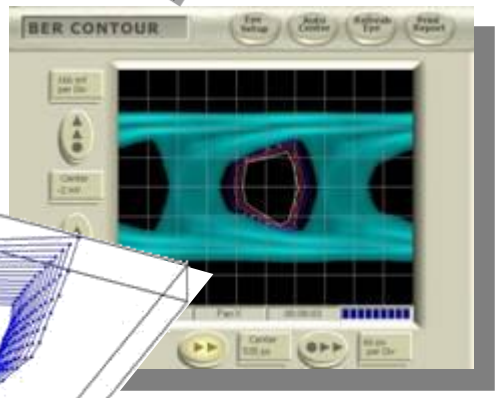


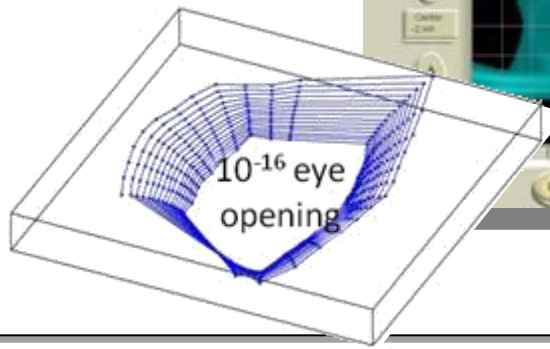
Horizontal slice

Bertscan, d-d, ber bathtub

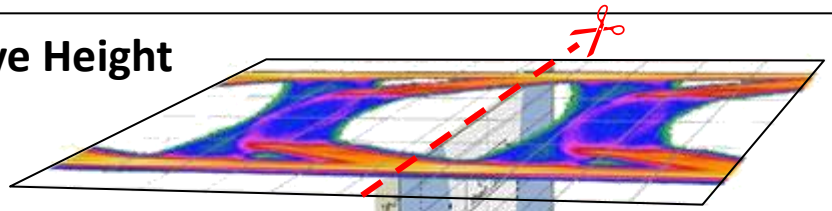
Eye width at 10^{-12} BER level

BER Contour

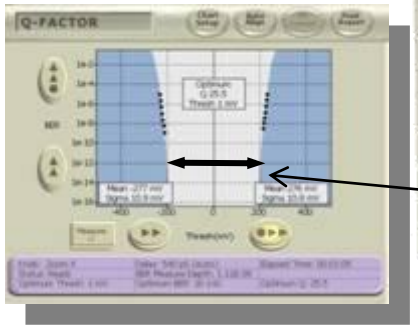




Eye Height



Vertical slice



Eye height at 10^{-12} BER level

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Beyond the BERT...

多种工具联合使用深入信号特征

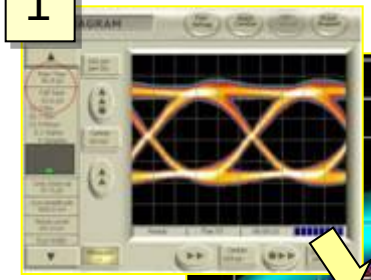
眼图

眼图的趋势

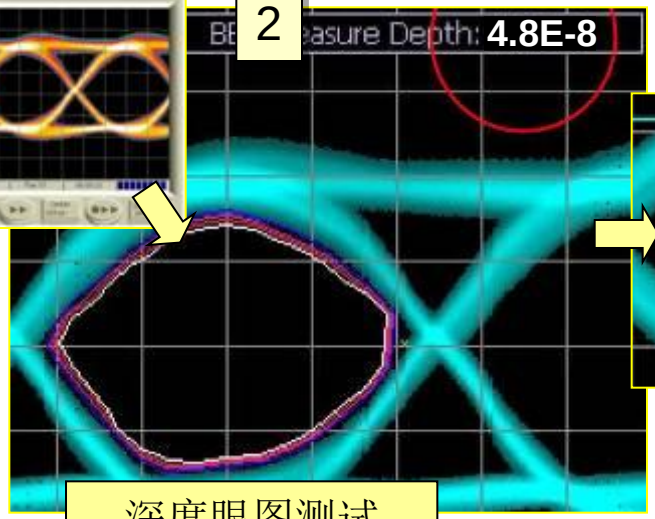
模板测试

寻找Fail点的线索

1

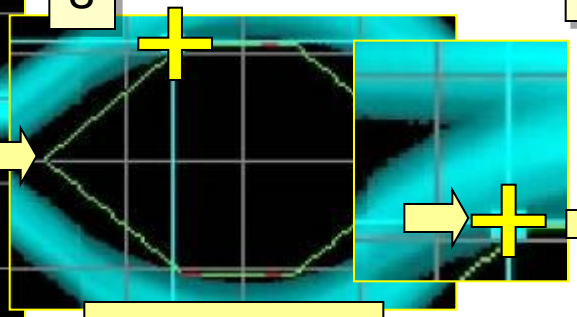


2



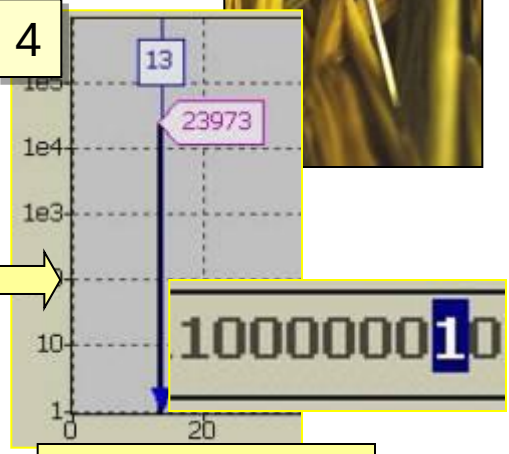
深度眼图测试

3



从BER域捕获眼图违规

4



发现线索

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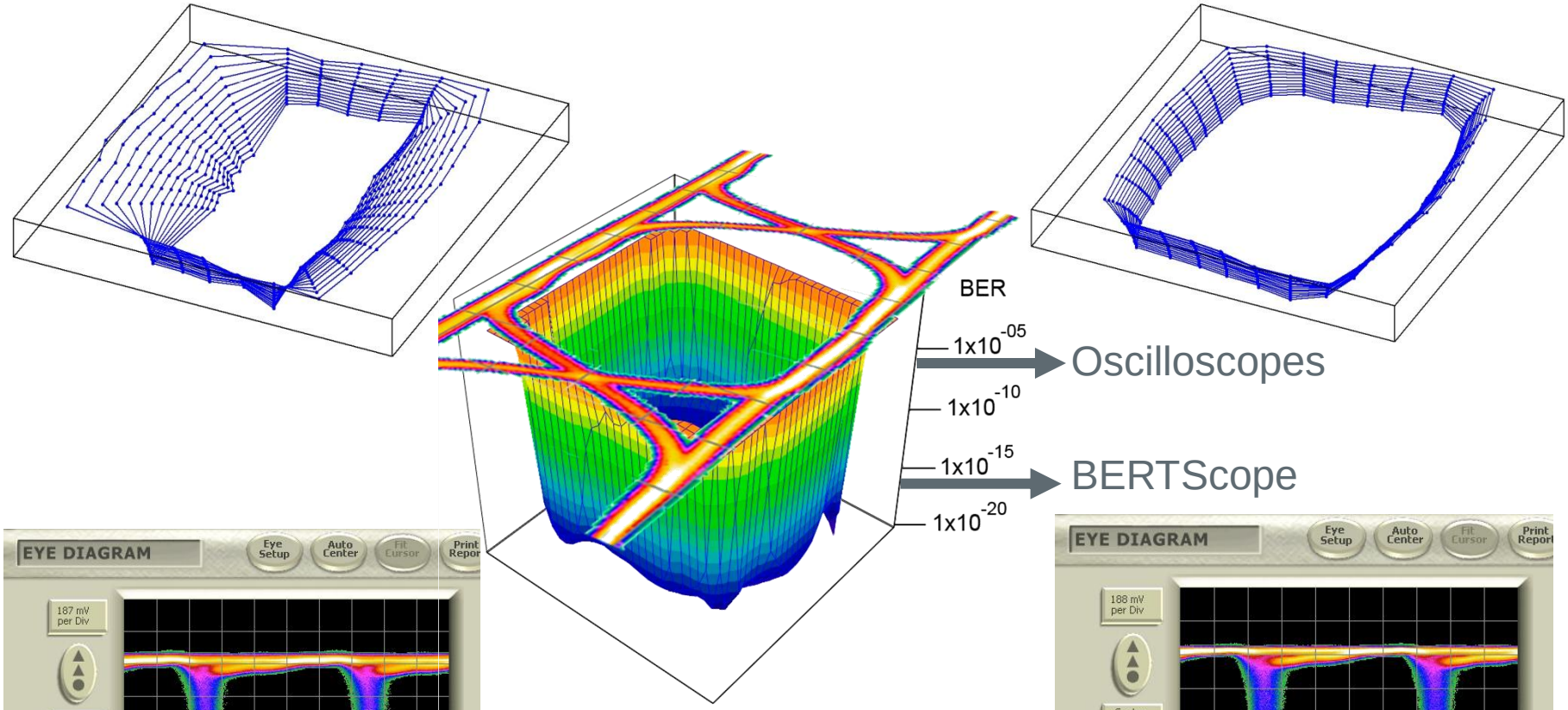
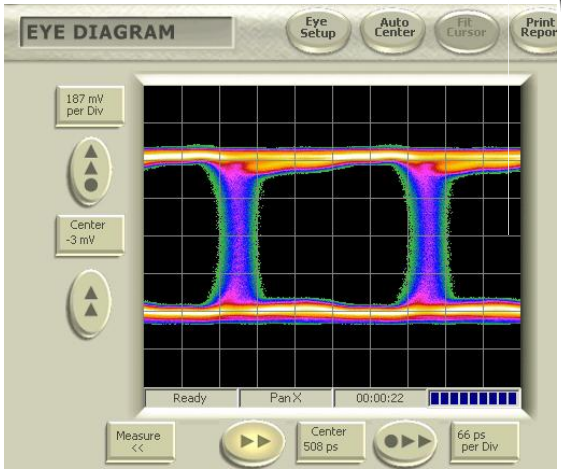
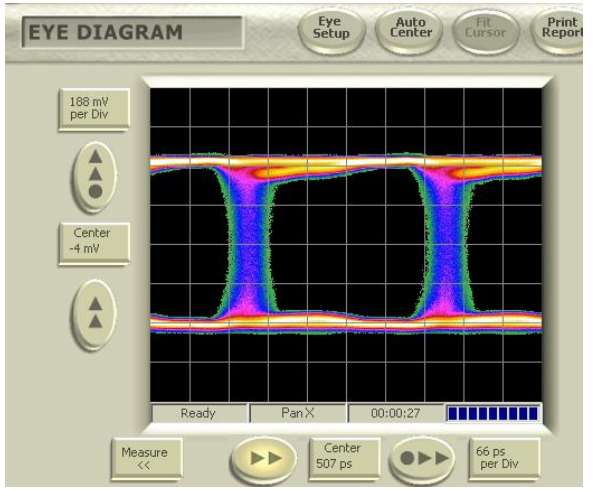
案例：System BER Trend





在示波器中看到系统的眼图是一样的



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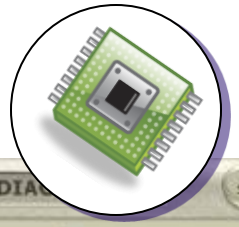
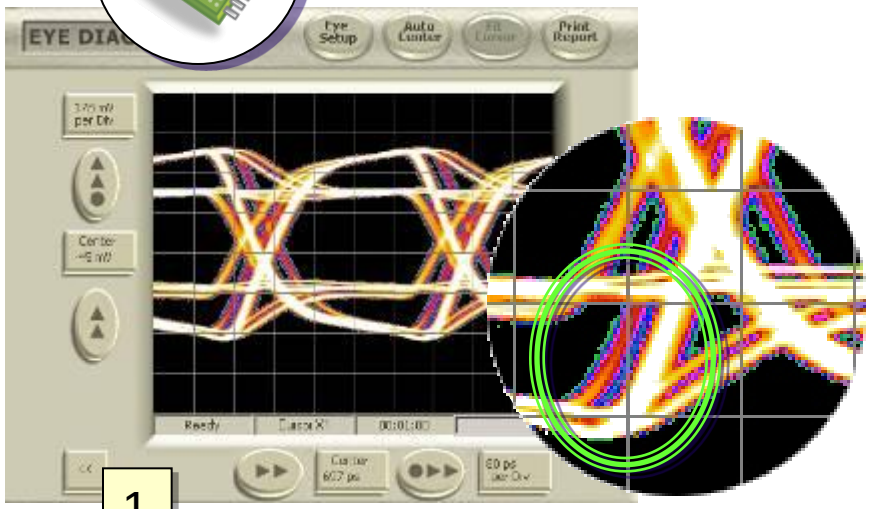
案例：参考时钟渗透

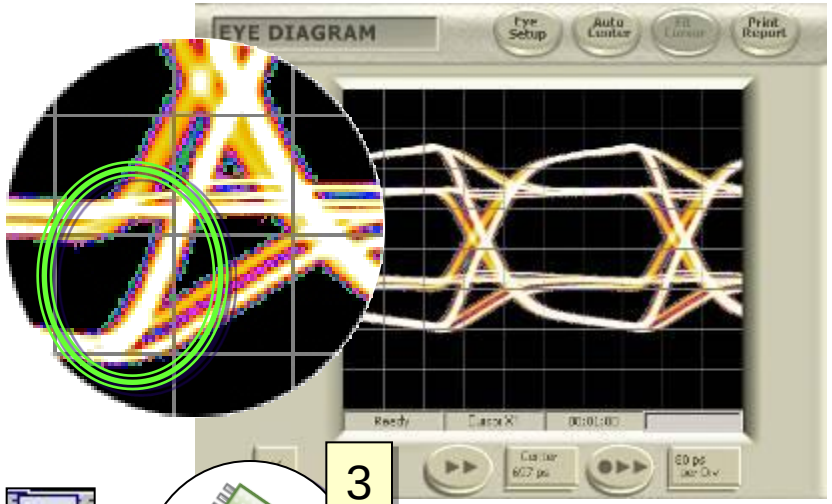


内存芯片设计



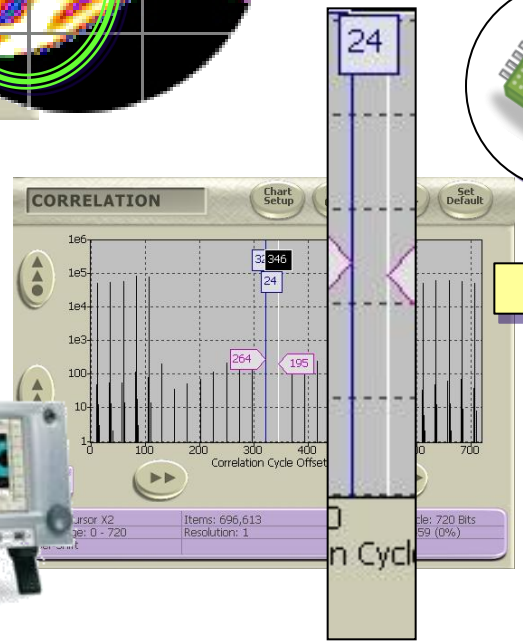
1

多余的波形：出现的频度不高



3

芯片重新设计：增加了对时钟路径的隔离，解决的问题



2

Error analysis 发现和第24码型相关– 和系统时钟的数据率相关

Clue

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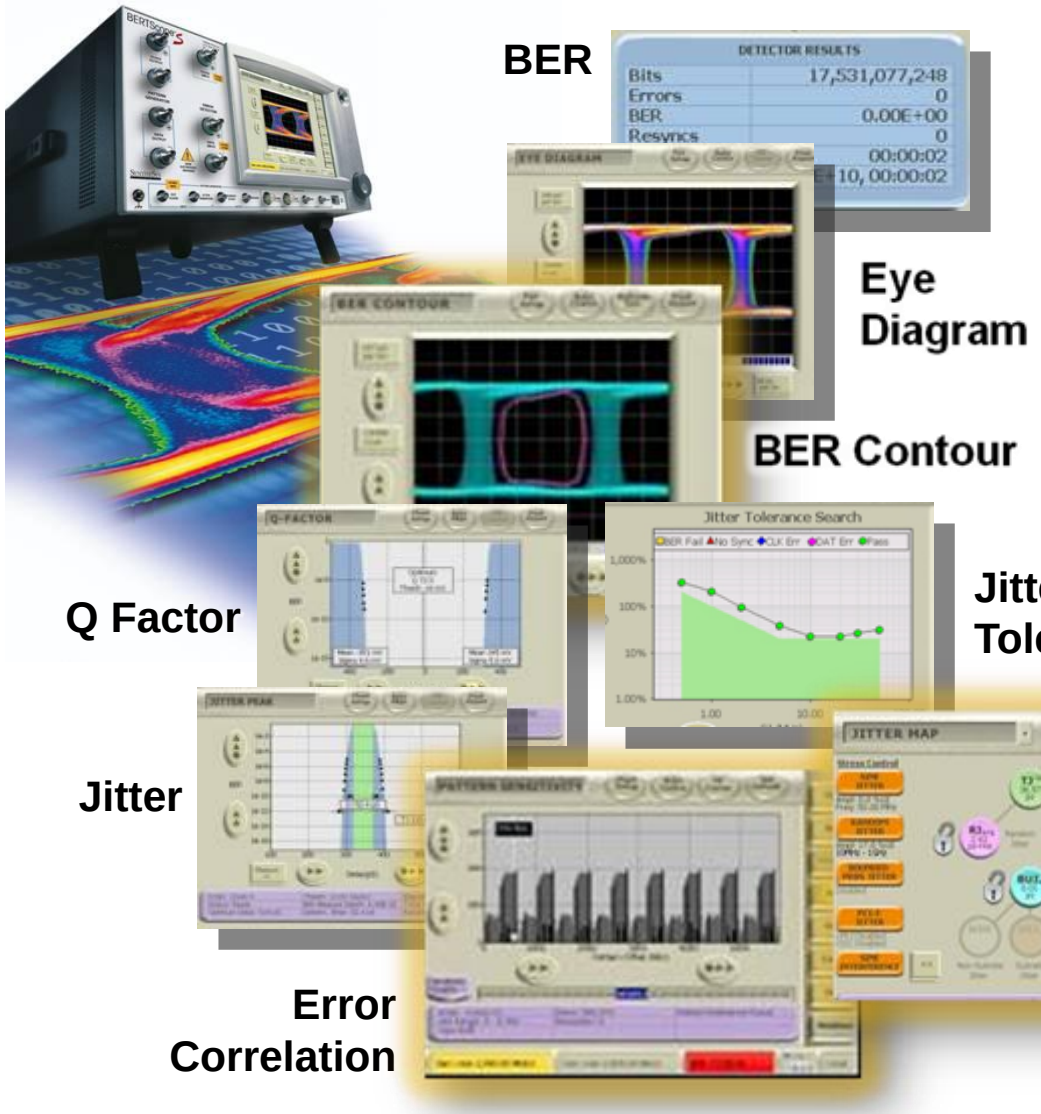
Beyond the BERT...

BERTScope工具集



BERTScope 将眼图、抖动、信号发生和信号损伤集成在一起，简单易用，而且有和误码仪一样的测深度和精度

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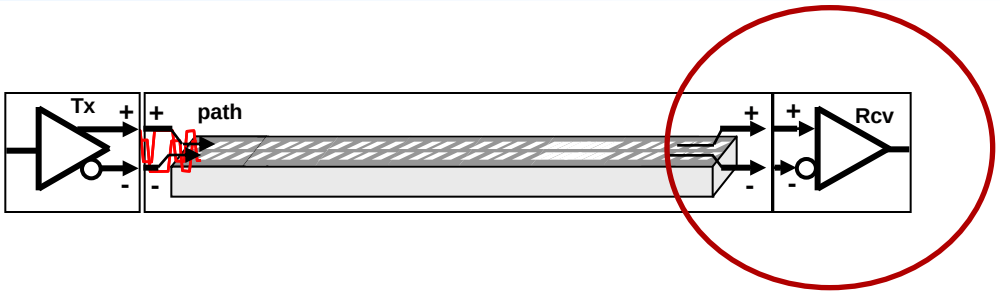
Stressed Eye

高速串行系统Rx端容限测试

- 单纯考察Tx端是不足以保证BER
- Rx端复杂的结构：Equalizer、CDR
- 没有Tx和传输链路时对Rx的压力测试
- 对Rx端施加各种各样的压力和一致性测试信号

- 信号产生
  - 高速串行信号不断增加的数据率
  - 不断增加的信号带宽
- 复现现实世界中的信号
  - 复现传输线效应
  - 产生各种干扰信号：抖动、噪声和其他干扰，并精确的知道干扰量的大小



各种高速串行总线对Rx接收端测试的要求

无论是针对设计还是生产制造，规范都定义了明确的Rx端测试需求

所有标准都要求进行Jitter Tolerance一致性测试

被测设备类型:

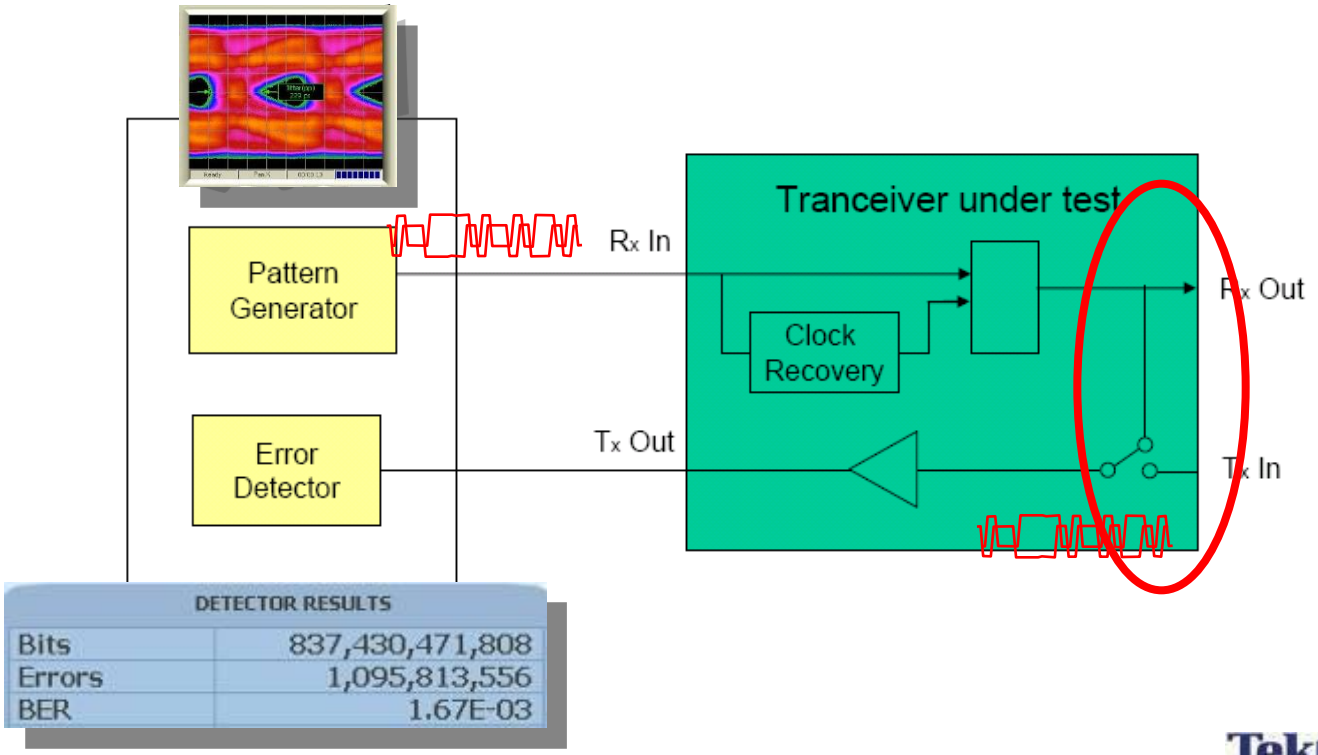
- SerDes
- Transceivers
- Multi Media Sink devices
- Rx devices

Standard	Data Rate	Jitter Tolerance	Timing Skew	Amplitude Sensitivity	Emphasis
SATA Gen 3	6 Gb/s		-		-
PCI Express 2.0	5 Gb/s				
PCI Express 3.0	8 Gb/s				
HDMI 1.3	0.75 Gb/s to 3.4 Gb/s				-
FC 4, 8 G	4.25 Gb/s to 8.5 Gb/s				
DisplayPort	2.7 Gb/s 5.4Gb/s				
USB 3.0	5 Gb/s		-		

Stressed Eye

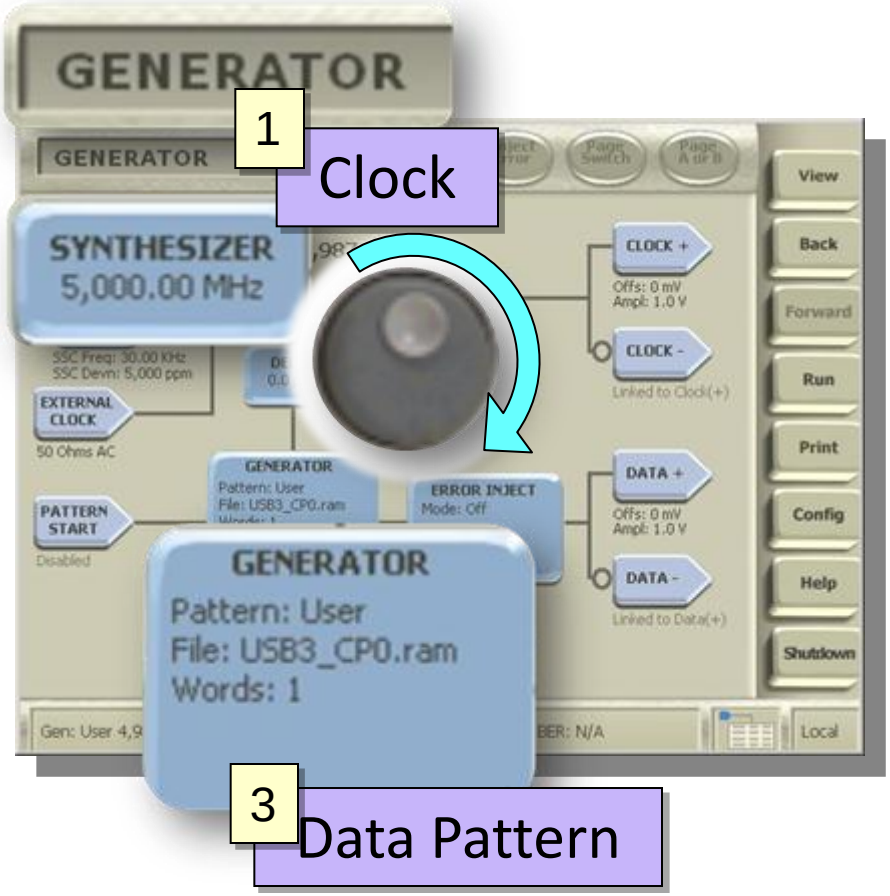
Rx接收端测试的流程

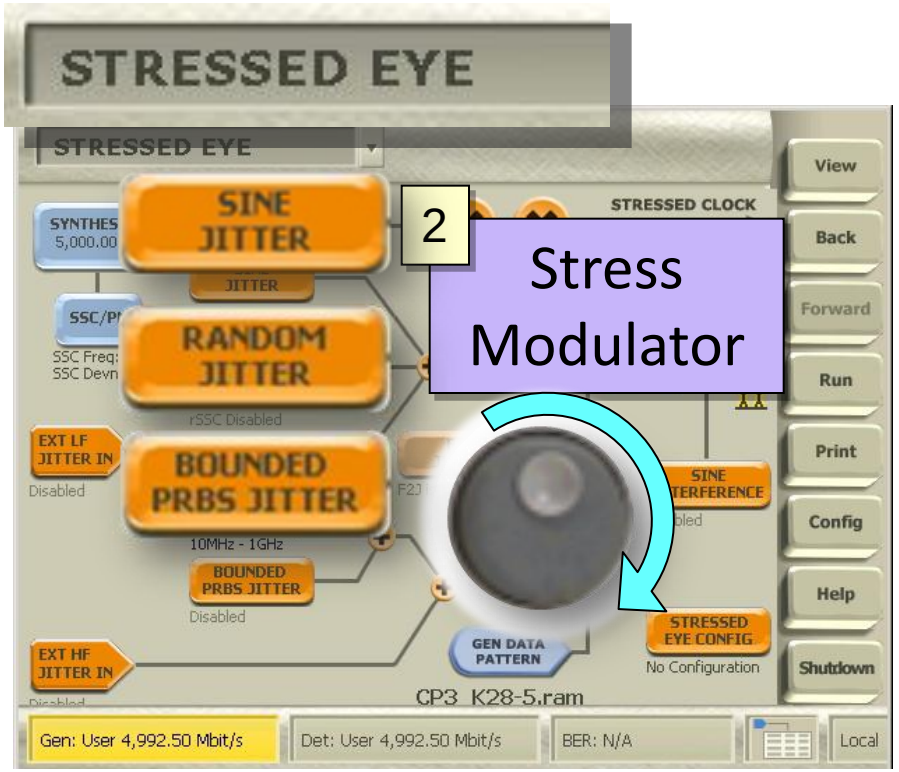
1. 设置DUT进入Loopback模式
2. 产生规范要求的抖动分量，在不同的频点上分别产生相应的抖动量
3. 将stressed信号注入DUT Rx
4. 统计DUT Tx端发出的信号的误码率是否达到要求



动态改变数据率、压力损伤和码型

- ✓Sine jitter
- ✓Random jitter
- ✓Bounded PRBS jitter
- ✓Sine Interference
- ✓ISI





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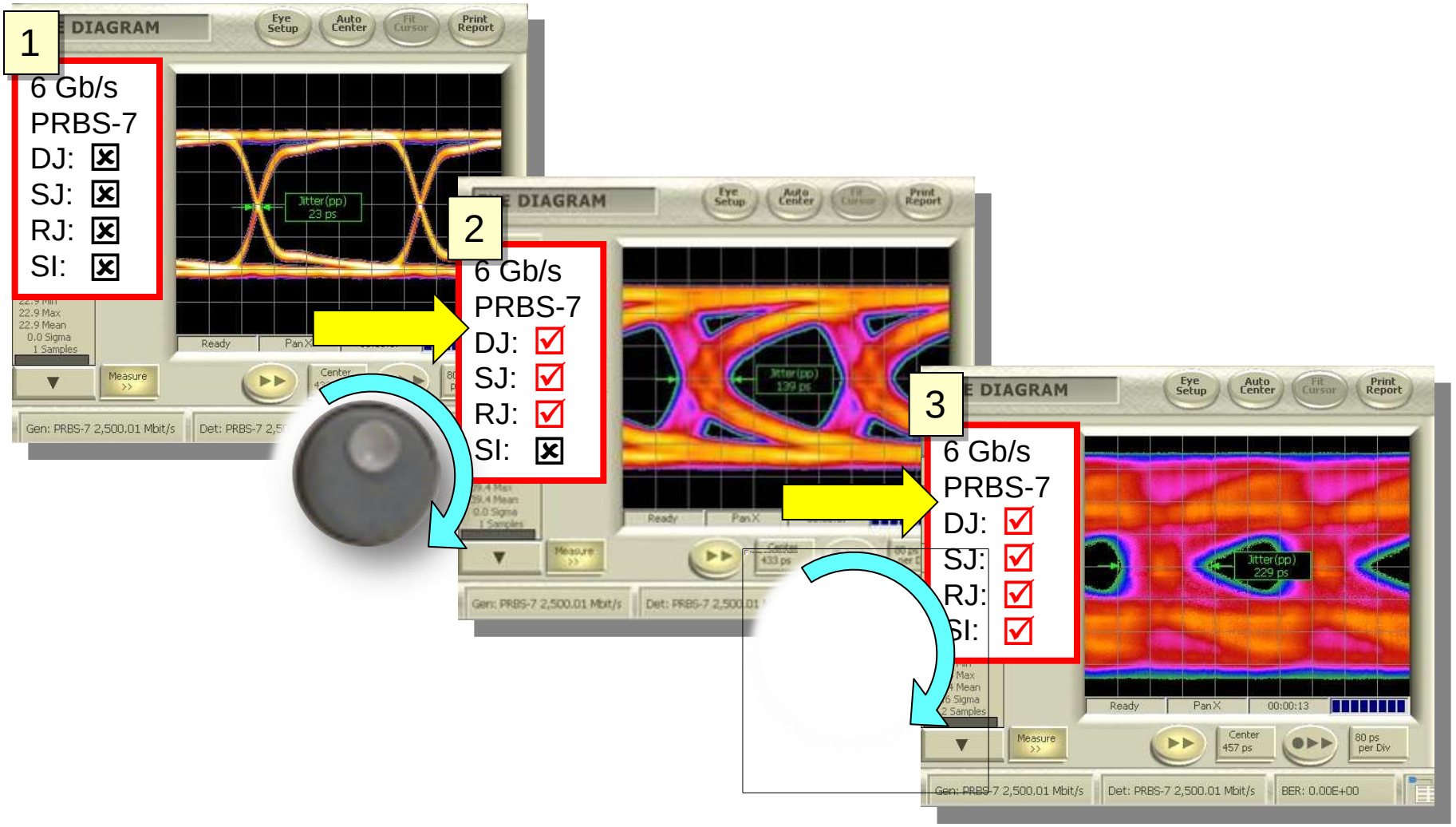
Stressed Eye

案例：SATA3 6Gbps压力信号



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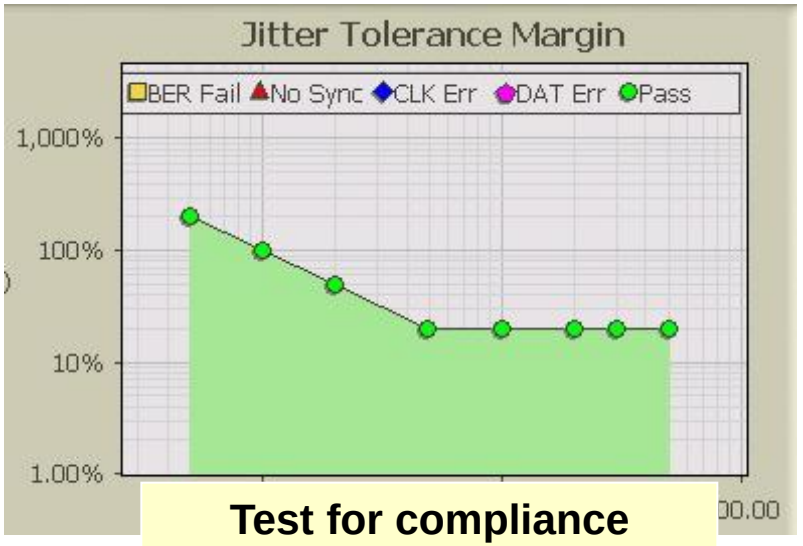
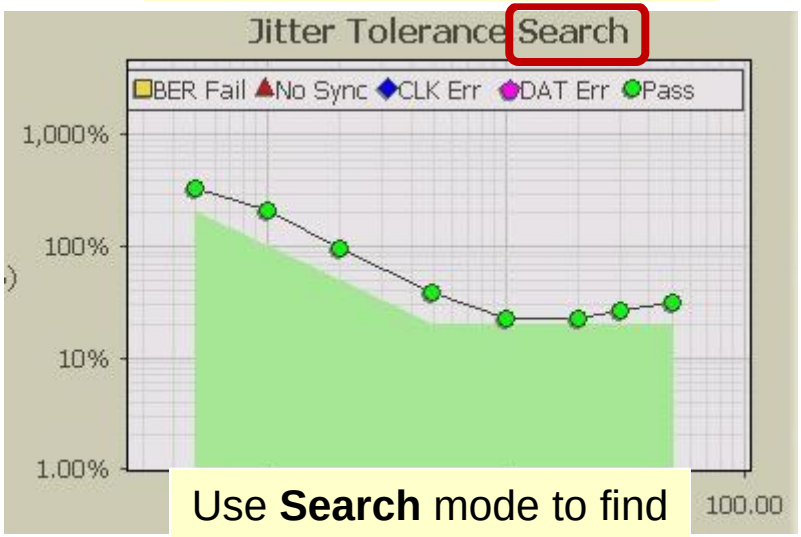
自动化Jitter Tolerance一致性测试方案

- ✓PCIE
- ✓SATA
- ✓USB3
- ✓Display Port
- ✓XFP/XFI
- ✓10GBase-KR
- ✓Optical
- ✓Serial Bus...



Test for compliance



Use **Search** mode to find device limits

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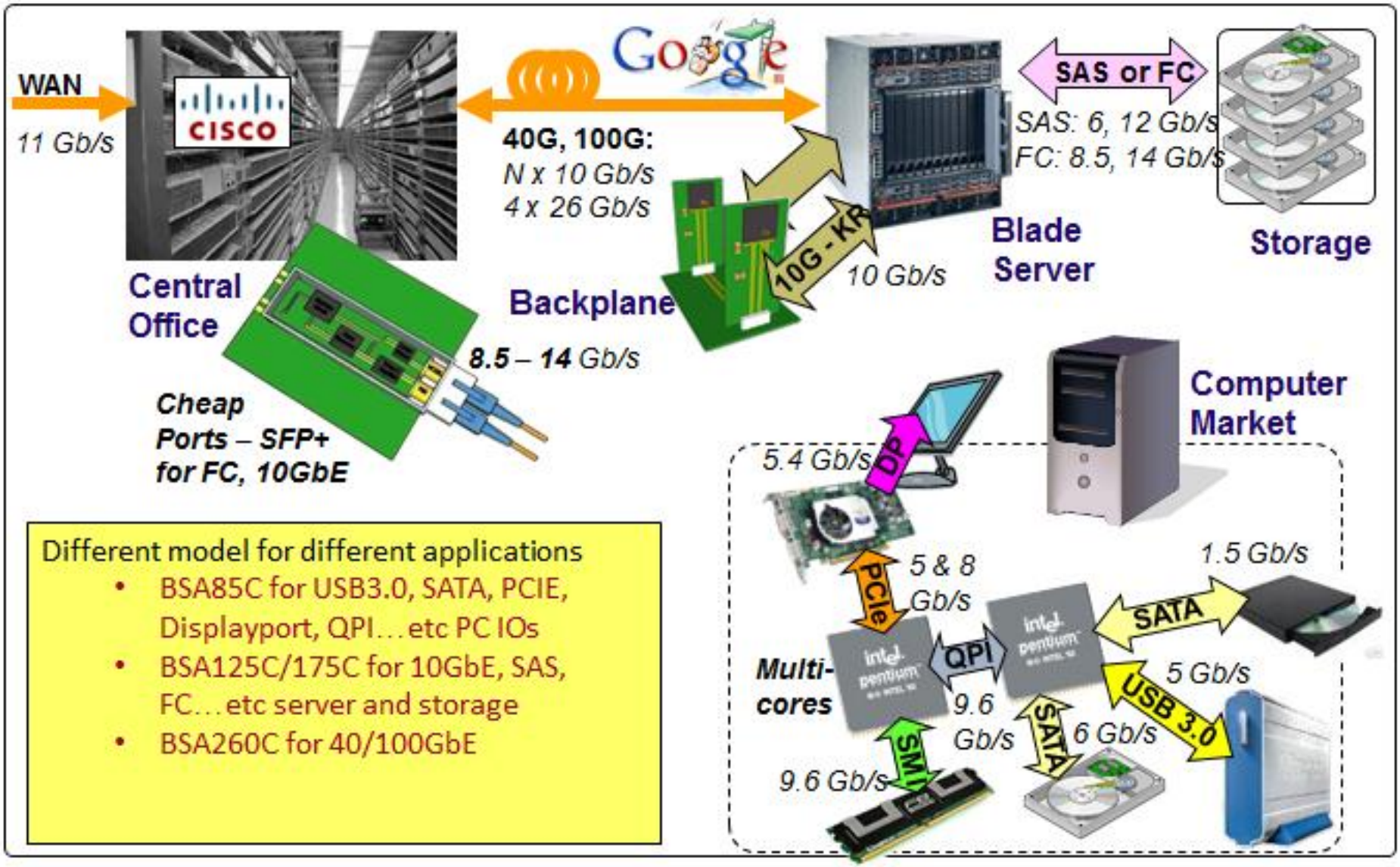
BERTScope高速串行应用解决方案



Different model for different applications

- BSA85C for USB3.0, SATA, PCIE, Displayport, QPI…etc PC IOs
- BSA125C/175C for 10GbE, SAS, FC…etc server and storage
- BSA260C for 40/100GbE

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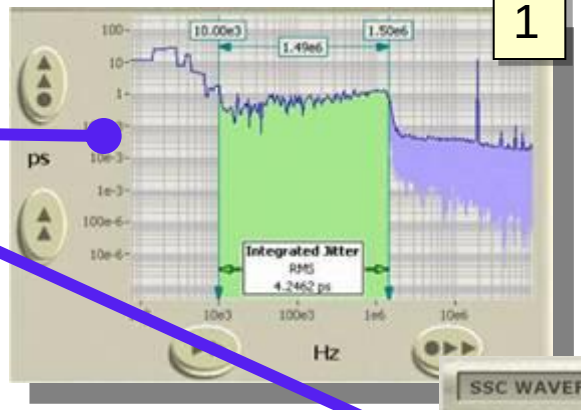
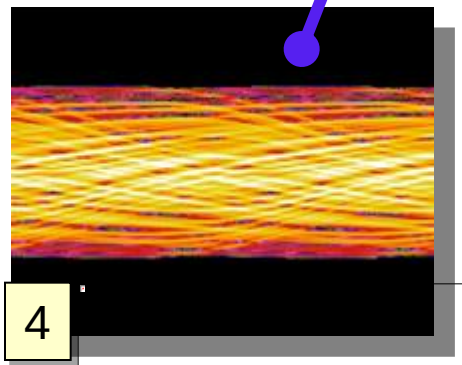
BERTScope时钟恢复仪



1

Jitter Spectrum

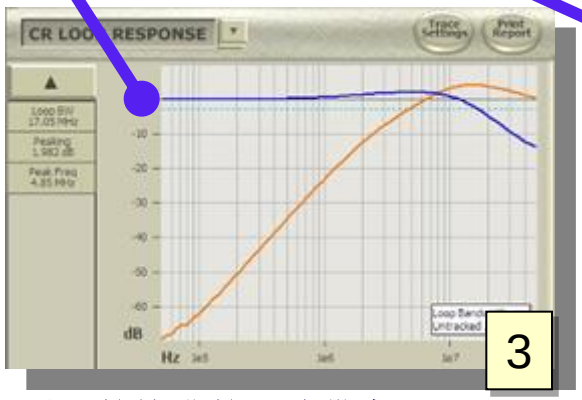
- 集成抖动测量
- 数据率150Mbps 到28.6 Gb/s
- PLL带宽100KHZ到12MHZ可调
- 抖动频谱范围200Hz 到90 MHz



4

从闭合的眼图中恢复时钟

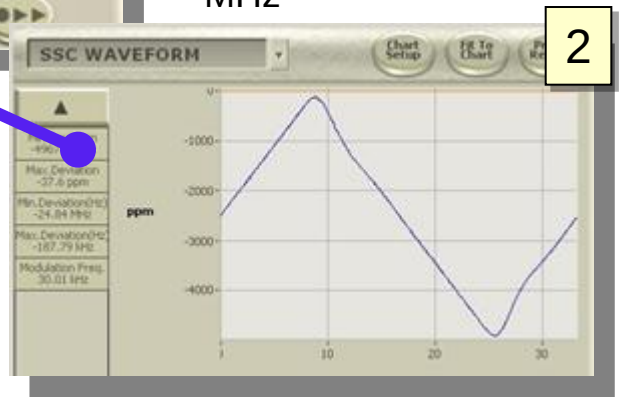
- 在时钟路径上集成了均衡
- 无分接的高灵敏度模块



3

灵活的校准的环路带宽和peaking

- 针对USB3.0抖动传输函数提供高带宽的loop bandwidth



2

扩频时钟(SSC)

- 可靠和锁定带SSC的信号
- 测量SSC波形

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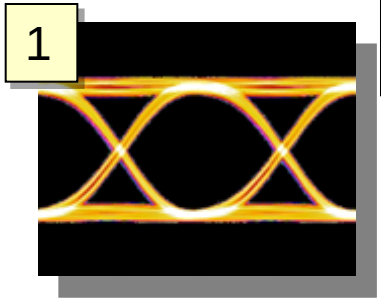
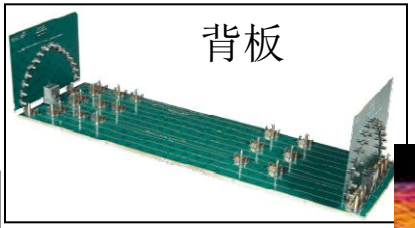
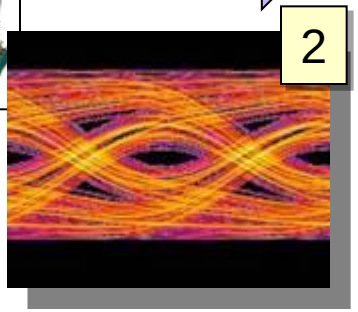
BERTScope DPP预加重处理器

没有预加重





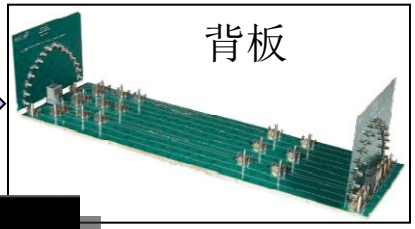
Rx



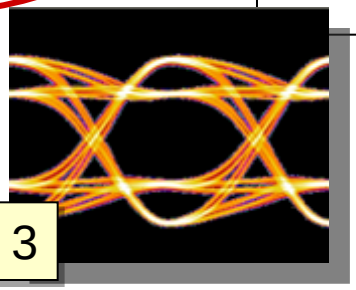
眼图基本闭合

带预加重

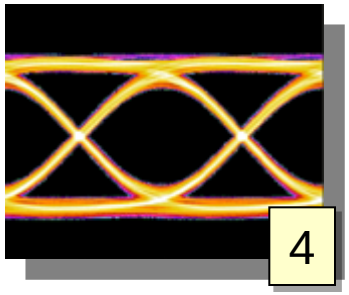
BERTScope DPP
3 & 4 Tap
Pre-Emphasis
To 12.5 Gb/s



Rx



眼图睁开



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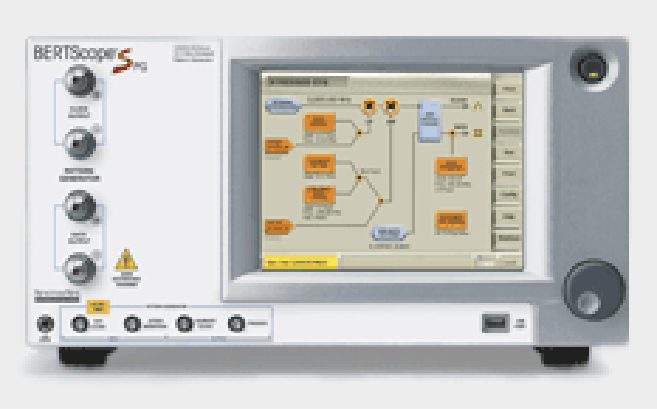
与Tektronix现有系统的集成

- 40G/100GE
  - DSA8300+80C10C+82A04
  - BSA260C/BSA286C
  - CR286A
- 无源背板、cable眼图测试
  - DSA8300+80E04
  - BSA125CPG
  - DPP125B



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BERTScope误码分析仪产品

- BERTScope 系列产品为设计和测试工程师提供结合了示波器的直观观察、误码仪的精度性能于一体的、快速的发现、定位被测系统问题的解决方案。

不仅仅是误码率测试...

- ✓ 深度样本的信号完整性测量
- ✓ 测试验证和调试的快速切换
- ✓ 快速准确的抖动容限测量
- ✓ 极佳的可用性
- ✓ 丰富灵活的配套产品

Thank You

更多资料请访问：

www.Tek.com

www.Bertscope.com

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