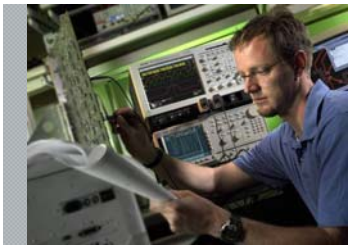
工业应用标准及高速接口测试解决方案

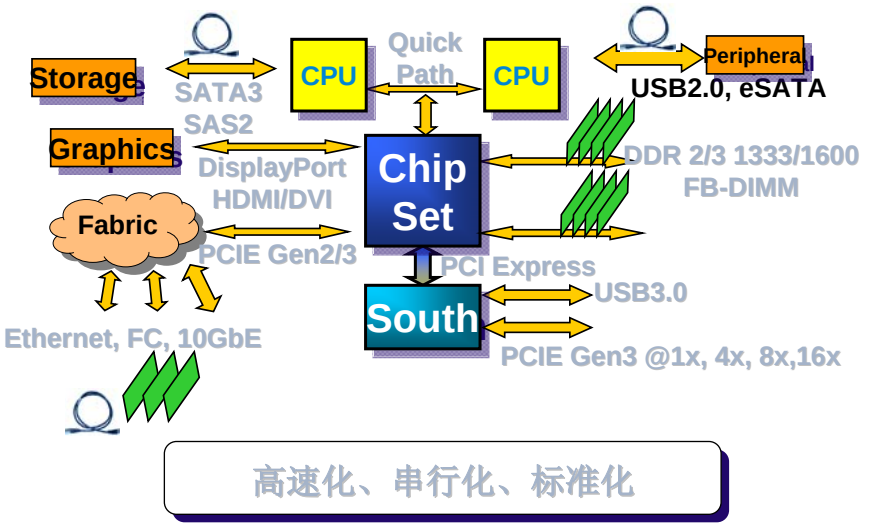
PCIE/SATA/USB/DDR



张文超　Raymond.zhang@tektronix.com

Tektronix

计算机技术发展趋势分析-高速串行



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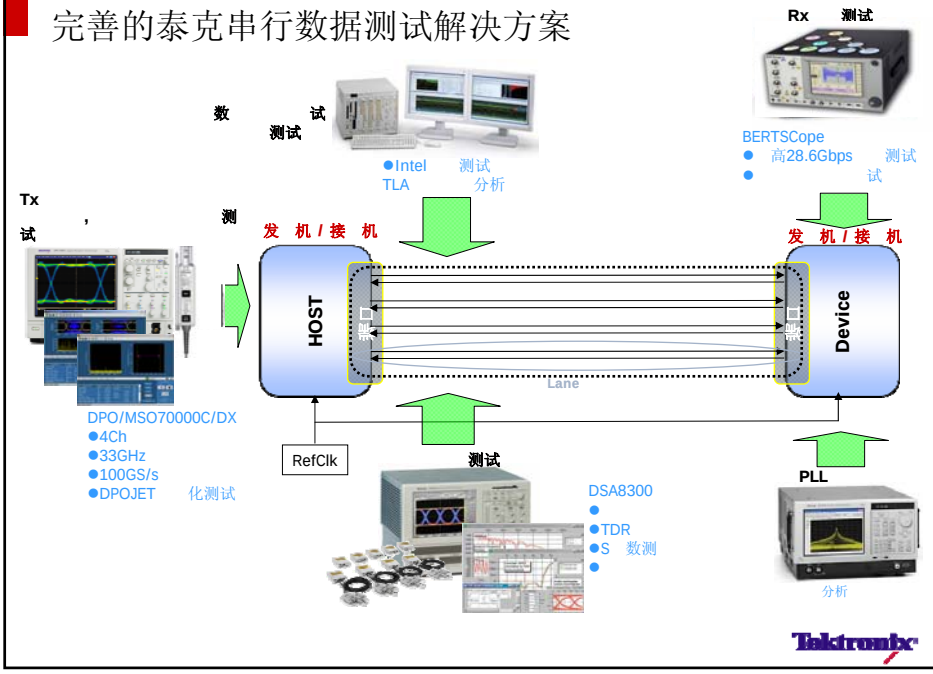
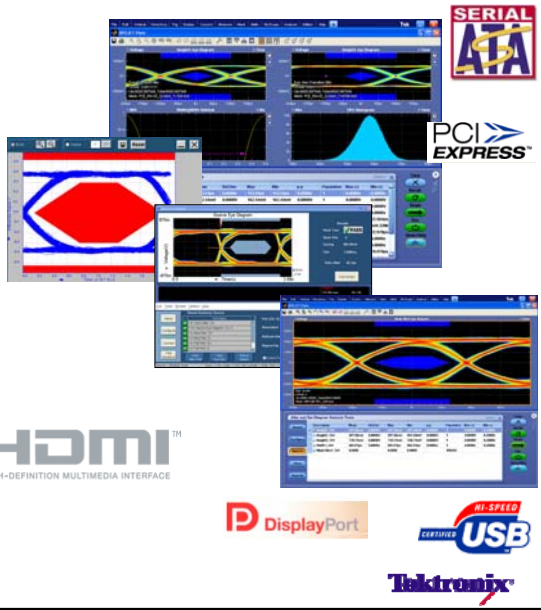
完善的泰克串行数据测试解决方案



Tektronix 计算机、 行业 测试标准

- PCIExpress Gen 2/Gen 3
- DisplayPort
- HDMI
- SATAII/III
- DDR2/3/4
- Ethernet
- USB
- WiMedia
- Inifiband
- FiberChannel
- XAUI



PCIe Tx Solutions

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PCIe Gen4 Update

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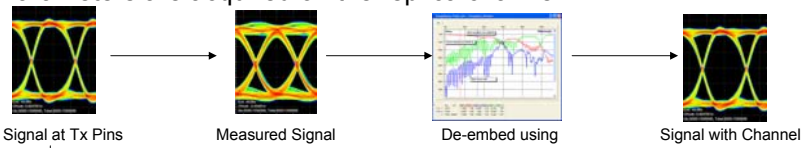
Gen4 Update

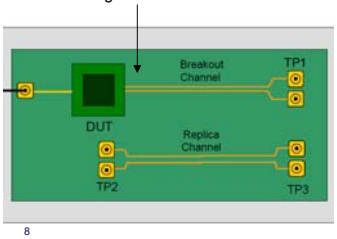
- Key attributes/requirements of PCIe 4.0
  - 16 GT/s, using scrambling, same as 8 GT/s, no encoding change
  - Maintains compatibility w/ PCIe installed base
  - Connector enhanced electrically (no mechanical changes)
  - Limited channel: ~12”, 1 connector; repeater for longer reach
- Uniform measurement methodology applied across all data rates
- New ‘SRIS’ independent RefClk modes
  - SRIS – Separate RefClk Independent SSC Architecture
- Rev 0.3 Base spec just introduced in PCI-SIG (June 2013)
  - Rev 0.9 no earlier than 1H/2015
  - Rev 1.0 no earlier than 2H/2015

System (Base Spec) Tx Testing

- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not possible
- De-embedding is required to see what the signal looks like at the pins of the TX, without the added effects of the channel
- S-Parameters are acquired on the replica channel

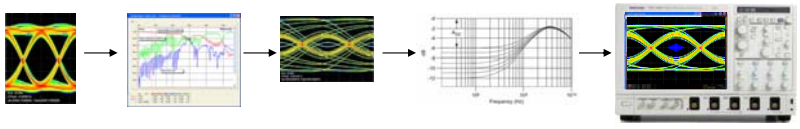


Signal at Tx Pins | Measured Signal at TP1 | De-embed using S-Parameters | Signal with Channel Effects Removed



Add-In Card (CEM Spec) Tx Testing

- CEM Specification Measurements are defined at the slice of a receiver
- Signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements

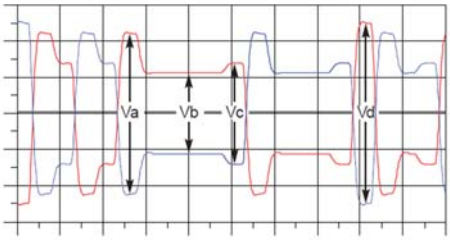


Signal Acquired from Compliance Board | Embed Compliance Channel and Package | Closed Eye due to the Channel | Apply CTLE + DFE | Open Eye for Measurements

Compliance Patterns

- Once in compliance mode, bursts of 100MHz clock can used to cycle through various settings of compliance patterns to perform, Jitter, voltage, timing measurements.

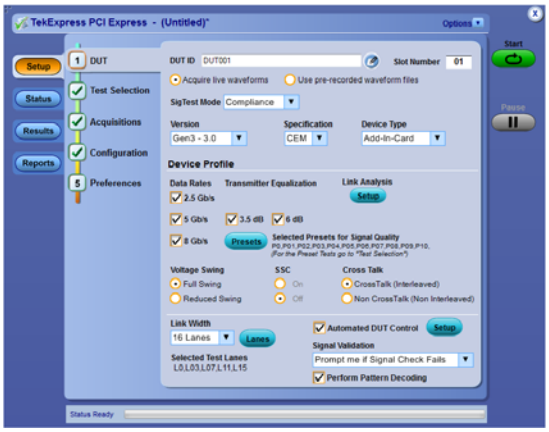
Data Rate	Preshoot	De-emphasis
2.5 GT/s,		-3.5 dB
5.0 GT/s,		-3.5 dB
5.0 GT/s,		-6.0 dB
8.0 GT/s,	P0 = 0.0	-6.0 1.5dB
8.0 GT/s,	P1 = 0.0	-3.5 1.5dB
8.0 GT/s,	P2 = 0.0	-4.4 1.5dB
8.0 GT/s,	P3 = 0.0	-2.5 1dB
8.0 GT/s,	P4 = 0.0	0.0dB
8.0 GT/s,	P5 = 1.9 1dB	0.0dB
8.0 GT/s,	P6 = 1.9 1dB	0.0dB
8.0 GT/s,	P7 = 1.9 1dB	-6.0 1.5dB
8.0 GT/s,	P8 = 1.9 1dB	-3.5 1dB
8.0 GT/s,	P9 = 1.9 1dB	0.0dB
8.0 GT/s,	P10 = 1.9 1dB	Test Max Boost Limit



De-emphasis = $20\log_{10}$ Vb/Va
Preshoot = $20\log_{10}$ Vc/Vb
Boost = $20\log_{10}$ Vd/Vb

Introducing the PCE3

- TekExpress Automation for Tx Compliance with unique features including:
  - √ Sets up the Scope and DUT for testing
  - √ Toggles thru and verifies the different Presets and Bit Rates
  - √ Tests multiple slots and lanes
  - √ Acquires the data
  - √ Processed with PCI-SIG SigTest
  - √ Provides custom reporting



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Automation Simplifies Tx Testing

- While convenient single capture capability is essential, automation makes the testing practical
- Iterate over multiple presets and lanes
- Gather results in a single report
- Provide means for quick switch to debugging and additional measurements
- Remove test fixture effects by using de-embedding

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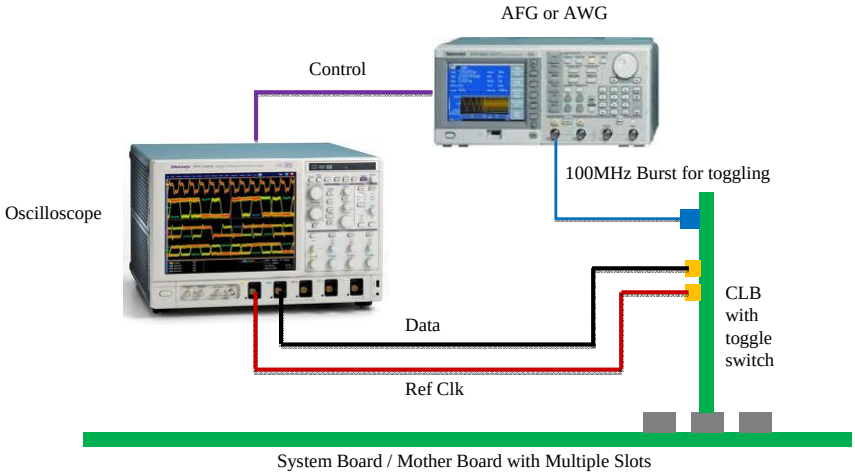
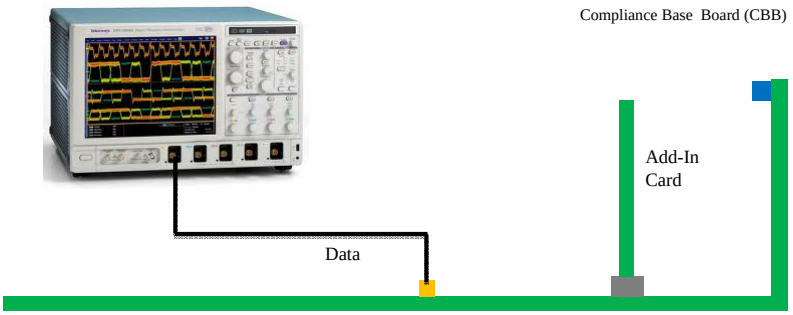
Automated DUT Control



Add-In Card Test Fixture

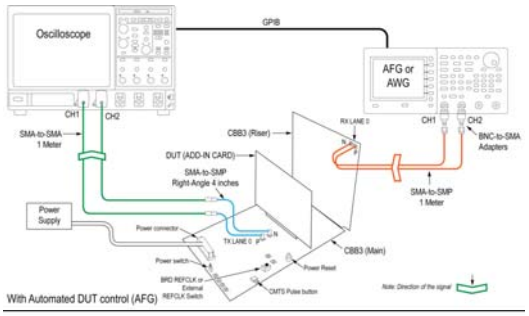
- Compliance Base Board (CBB)
  - Used for Testing Add-In cards
  - All Tx / Rx Lanes are routed to SMP
  - Compliance Mode Toggle Switch
  - Low Jitter Clean Reference Clock
  - Separate CBB for Gen 1/2/3

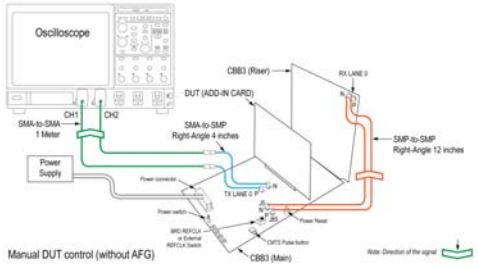
Compliance Base Board (CBB)



CBB with Multiple Slots of different widths and toggle switch

CBB3 Config for Automatic & Manual DUT Control



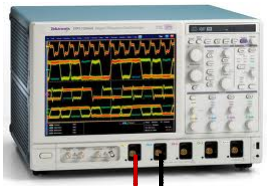


Refer to "PCIe 3.0 Compliance Base Board (CBB3.0) Test Fixture User's Document", www.pcisig.com

System Test Fixtures

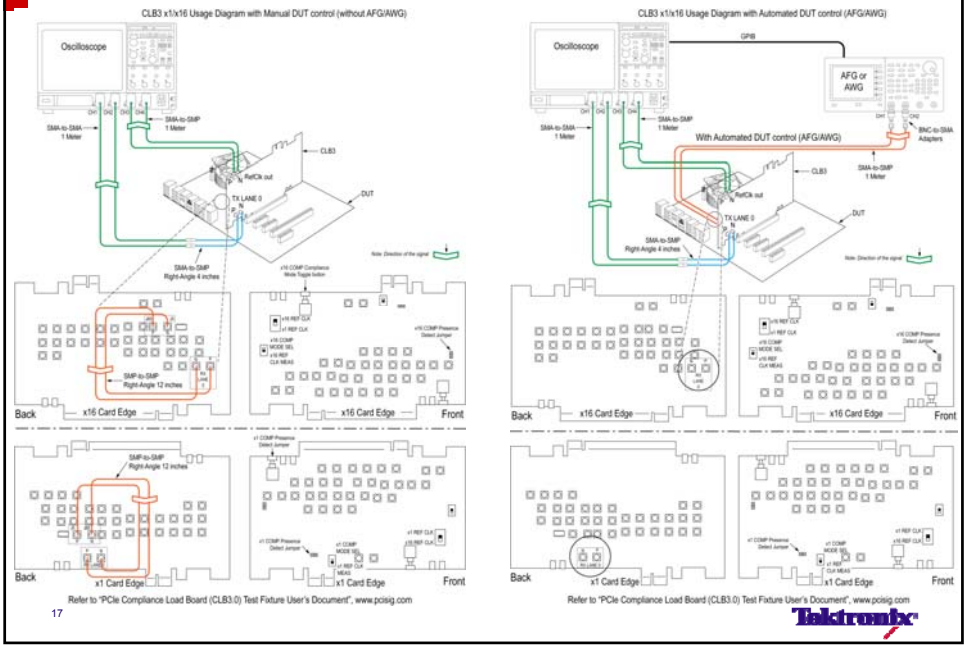
- Compliance Load Board (CLB)
  - Used for testing System Boards
  - All Tx / Rx Lanes and Ref Clk routed to SMP
  - Compliance Mode Toggle Switch
  - Various types of Edge Connectors to support different types of Slots on System Boards
  - Separate CLB's for Gen1/2/3

Compliance Load Board (CLB)

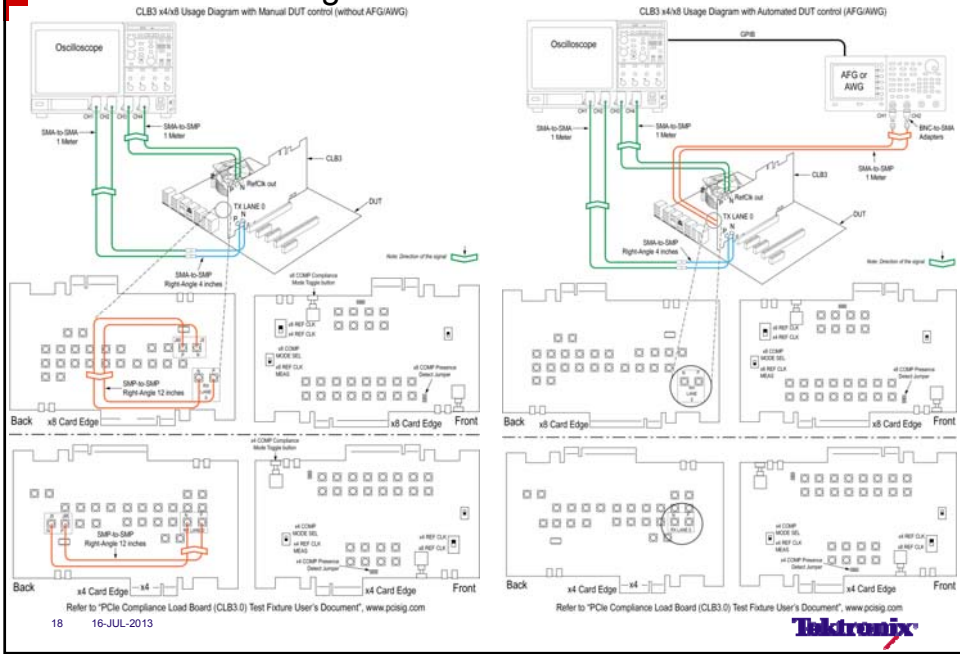


System Board / Mother Board with Multiple Slots

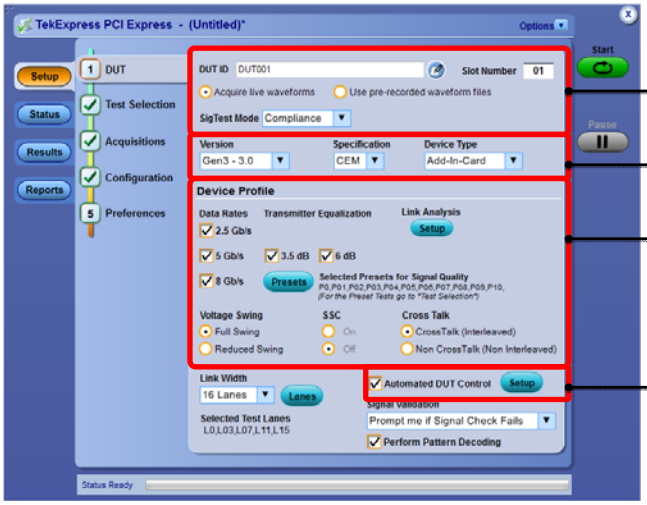
x1/x16 CLB3 Config for Automatic & Manual DUT Control



x4/x8 CLB3 Config for Automatic & Manual DUT Control



TekExpress Automation for Tx Compliance - Setup



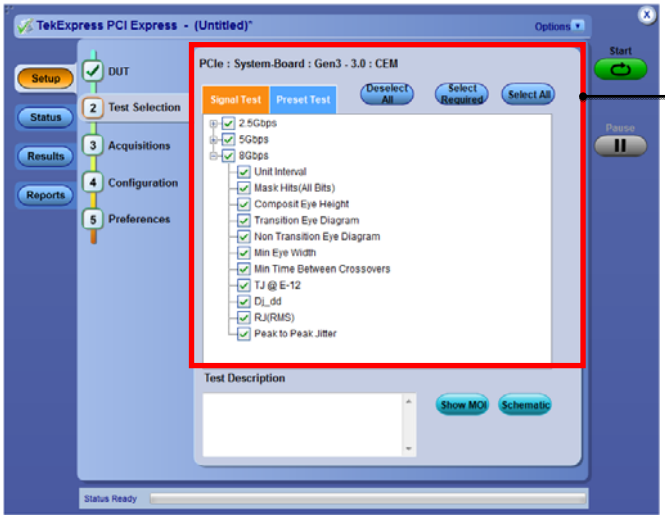
Run Analysis on Live or Pre-Recorded Data

Type of test / device selection

Test selection

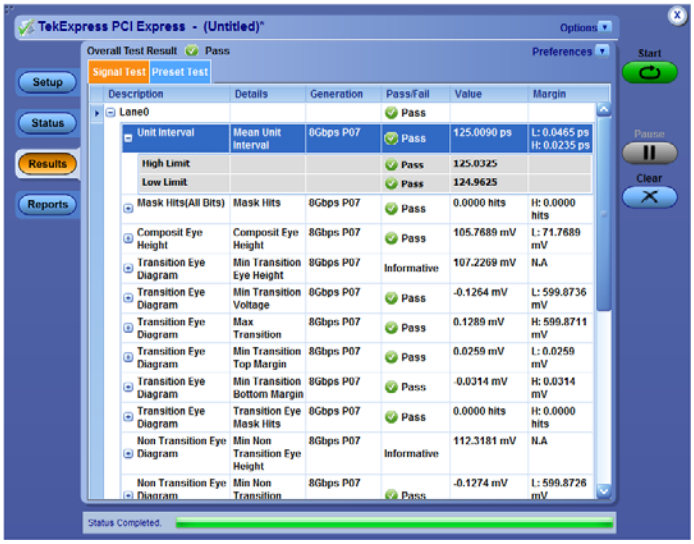
Automate DUT control

TekExpress Automation for Tx Compliance – Test



Test Selection

TekExpress Automation for Tx Compliance – Reports



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TekExpress Automation for Tx Compliance – Reports

Tektronix Enabling Innovation

TekExpress PCI Express

Add-In-Card Test Report

Setup Information	
	DPOJET Version : 6.0.1 Build 8
	Scope Model : DPO73304D
	Scope Serial Number : B241123
DUT ID : DUT001	SPC, FactoryCalibration : PASS,PASS
Date/Time : 2013-06-10 17:28:45	Scope F/W Version : 6.7.4 Build 3
Device Type : PCIe	Probe1 Model : TCA292D
TekExpress Version : PCI Express 2.0.0.66 (Beta_Build) Framework:3.0.0.16_RevD	Probe1 Serial Number : N/A
Spec Version : Gen3 - 3.0	Probe2 Model : TCA292D
SigTest Version : 3_2_0	Probe2 Serial Number : N/A
Slot Number : 01	Probe3 Model : TCA292D
Overall Execution Time : 0:03:21	Probe3 Serial Number : N/A
Overall Test Result : Pass	Probe4 Model : TCA292D
	Probe4 Serial Number : N/A
	Signal Source Model : AFG3252
	Signal Source Serial Number : C010899
DUT Comment :DUT001	

Test Name Summary Table	
Unit Interval	Pass
Mask Hits(All Bits)	Pass
Composit Eye Height	Pass
Transition Eye Diagram	Pass
Non Transition Eye Diagram	Pass
Min Eye Width	Informative
Min Time Between Crossovers	Informative
mhtml:file:///X:/PCI Express/Reports/DUT001.mht#TJ @ E-12	Pass
DJ_dd	Informative
RJ(RMS)	Pass
Peak to Peak Jitter	Informative

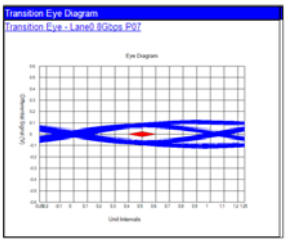
Unit Interval

Measurement Details	Lane Name	DataRate	Equalization	Measured Value	Test Result	Margin	Low Limit	High Limit	Comments
Mean Unit Interval	Lane0	8Gbps	P07	125.0090 ps	Pass	L: 0.0465 ps H: 0.0235 ps	124.9625	125.0325	

Back To Summary Table

Transition Eye Diagram

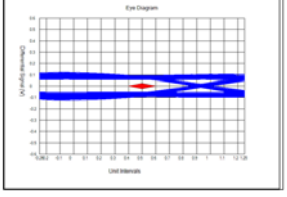
Transition Eye - Lane0 8Gbps P07



Back To Summary Table

Non Transition Eye Diagram

Non Transition Eye - Lane0 8Gbps P07



Back To Summary Table

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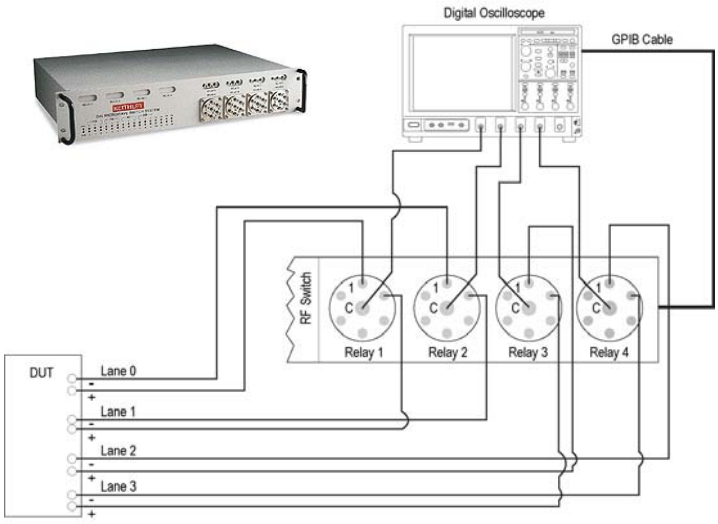
RF Switch and Auto Toggling

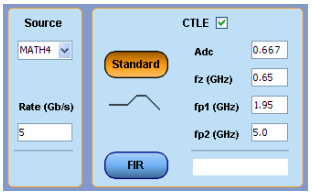
- Use RF switch to handle multiple lanes without reconnections
  - √ Must provide termination to maintain compliance mode
  - √ Use programmatic interface to control from automation software
  - √ While switches typically have good signal quality at 4GHz, extra cables must be accounted for by de-embedding
  - √ Design you device so that automatic toggling works for all presets

PCI Express Tx Test with RF Switch



Testing Beyond Compliance

- What happens if a measurement fails Compliance?
- Could it be the channel?
  - Measurements can be taken before the channel to evaluate results
  - Different channel models can be created using SDLA Visualizer
- How does the optimized RX setting compare to other settings?
  - Easily compare the results of multiple Equalization settings
- Does deeper analysis of the waveform need to be done?
  - PCIe specific measurements can be taken in Tektronix' measurement system DPOJET
  - Determine if data dependent, uncorrelated or pulse width jitter is in spec
  - Measurements filters and settings can be adjusted to get to root cause, but remember you must pass SigTest to be certified for compliance
- Is the TX compliant?
  - NEW PCIe 3.0 base spec measurements are available to verify Tx compliance



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USB 3.0 Tx Physical Layer Testing

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Tektronix Solutions for USB 3.0 Transmitter Testing

- Comprehensive Solution Goes Beyond Compliance
  - All measurements accessible in DPOJET for debug
  - Support for multiple test points (i.e. at the silicon pins or compliance test point)
- Complete Toolset for Characterizing USB 3.0 Designs
  - Create custom CTLE and Channel Emulation or De-Embed Filters with SDLA (Serial Data Link Analysis)
- Automated
  - No need to be a USB 3.0 Expert
  - Automatically acquire all necessary waveforms for processing (CP0, CP1, LFPS) with AWG7K or AFG
- SigTest Integration
  - SigTest is completely integrated into TekExpress
  - No need to manually configure the scope and setup SigTest for processing
  - User flexibility to process the waveforms using Tektronix algorithms and SigTest to compare the results
- Comprehensive Reporting
  - Complete Test Report in .mht format with pass / fail and margin results
  - Plots include for quick visual inspection

Transmitter Solutions

- TekExpress Fully Automated Compliance Environment
- DPOJET Debug and Analysis

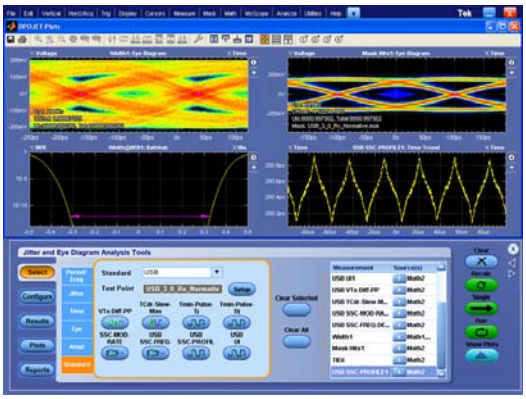
USB 3.0 Test Fixtures

- Two options for USB 3.0 Test Fixtures
  - Tektronix supplied fixtures
    - Enables SW channel emulation for TX and RX testing
    - Published electrical specifications
    - Supports TX, RX, and Cable testing
    - Available from Tektronix
  - USB-IF supplied fixtures and cables (shown below)
    - Used for compliance testing
    - Enables SW channel emulation for TX only
    - Supports TX and RX testing
    - Available from the USB-IF



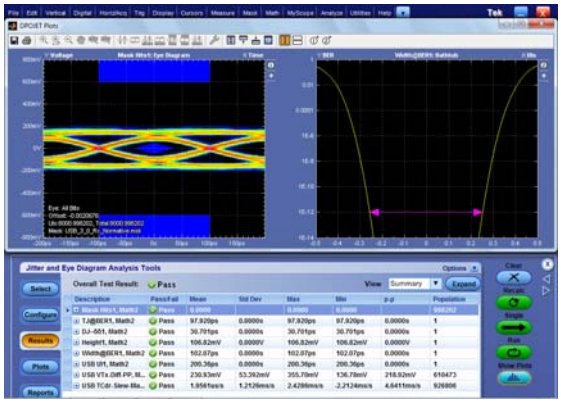

USB 3.0 Transmitter Measurement Overview

- Voltage and Timing
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate
- Low Frequency Periodic Signaling (LFPS)
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod
- SSC
  - Modulation Rate
  - Deviation



Voltage and Timing

- Voltage, Eye Height, Jitter



LFPS TX Measurements

- LFPS signaling is critical for establishing link communication
- LFPS TX test verify common mode, voltage, tPeriod, tBurst, tRepeat
- Channel is not embedded for LFPS tests

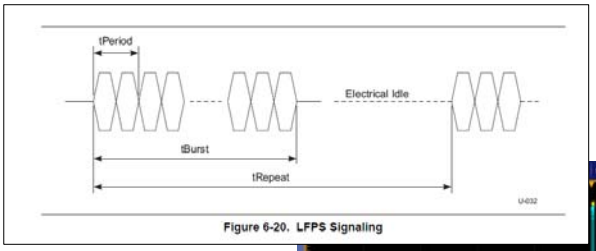
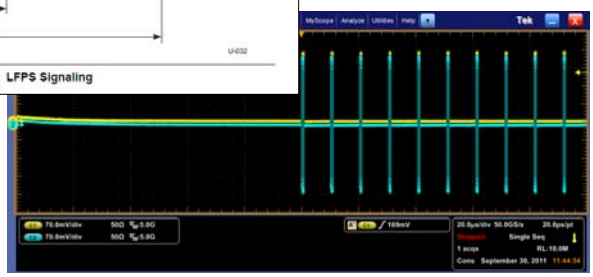
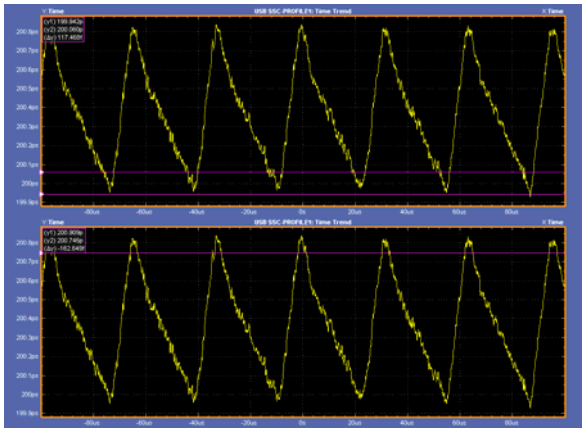


Figure 6-20. LFPS Signaling



SSC Measurements

- Both Maximum and Minimum Frequency Deviation must be considered
  - Assume nominal UI of 200ps
  - Limits are +0/-4000ppm and +0/-5000ppm, plus +/- 300ppm for ref clock accuracy
- Compliance Channel is not embedded for SSC measurements

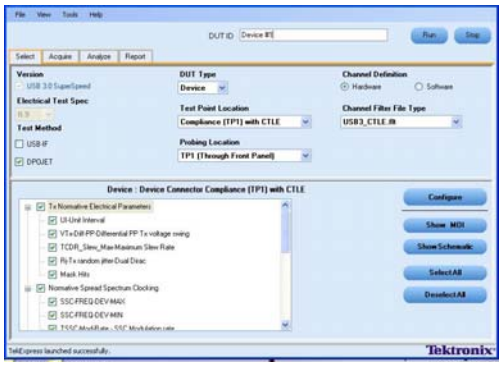


USB 3.0 Compliance and Automation

- Complete Automation of USB 3.0 Measurements with TekExpress
- No need to learn technology specific software applications- TekExpress is a Common Framework from Serial Applications including SATA, USB, DisplayPort, HDMI, and Ethernet
- TekExpress utilizes DPOJET USB 3.0 Specific algorithms making it easy to move from compliance to DPOJET for debug

TekExpress USB 3.0 Automated Solution

- Supports testing for USB 3.0 Hosts and Devices
- Automatically selects the correct channel emulation filter when software is selected
- Easily select measurements of interest for test execution
- Supports all compliance and LFPS TX measurements
- Automates DUT toggling to acquire CP0, CP1, and LFPS Patterns



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SATA/SAS Tx Physical Layer Testing

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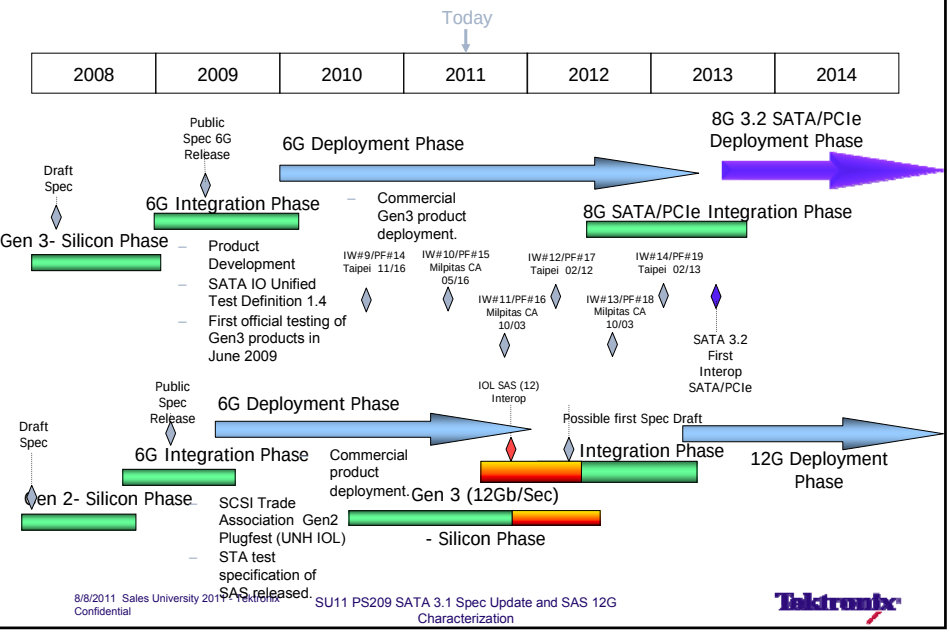
Storage Timelines and Solutions Development



SATA UTD 1.4.2 Test Requirements

Phy Transmit Signal Requirements
TSG-01 : Differential Output Voltage
TSG-02 : Rise/Fall Time
TSG-03 : Differential Skew
TSG-04 : AC Common Mode Voltage
TSG-05 : Rise/Fall Imbalance
TSG-06 : Amplitude Imbalance
TSG-07 : Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, fBAUD/10
TSG-08: Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, fBAUD/10
TSG-09 : Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, fBAUD/500
TSG-10 : Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, fBAUD/500
TSG-11 : Gen2 (3Gb/s) TJ at Connector, Clock to Data, fBAUD/500
TSG-12 : Gen2 (3Gb/s) DJ at Connector, Clock to Data, fBAUD/500
TSG-13: Gen3 (6Gb/s) Transmit Jitter w/wo CIC
TSG-14 : Gen3 (6Gb/s)TX Maximum Differential Voltage Amplitude
TSG-15 : Gen3 (6Gb/s) TX Minimum Differential Voltage Amplitude
TSG-16 : Gen3 (6Gb/s) Tx AC Common Mode Voltage

Phy Receive Signal Requirement
RSG-01 : Gen1 (1.5Gb/s) Receiver Jitter Tolerance Test (Normative)
RSG-02 : Gen2 (3Gb/s) Receiver Jitter Tolerance Test (Normative)
RSG-03 : Gen3 (6Gb/s) Receiver Jitter Tolerance Test
RSG-05 : Gen1 Asynchronous Receiver Stress Test at +350ppm
RSG-06 : Gen1 Asynchronous Receiver Stress Test With SSC

SI General Requirements
SI-1:8 : Cable Characterization
SI-09 : Inter-Symbol Interference

Phy General Requirements
PHY-01 : Unit Interval
PHY-02 : Frequency Long Term Stability
PHY-03 : Spread-Spectrum Modulation Frequency
PHY-04 : Spread-Spectrum Modulation Deviation

Phy OOB Requirements
OOB-01 : OOB Signal Detection Threshold
OOB-02 : UI During OOB Signaling
OOB-03 : COMINIT/RESET and COMWAKE Transmit Burst Length
OOB-04 : COMINIT/RESET Transmit Gap Length
OOB-05 : COMWAKE Transmit Gap Length

Phy Receiver/Transmitter Channel Reqs
RX/TX-01 : Pair Differential Impedance
RX/TX-02 : Single-Ended Impedance (Obsolete)
RX/TX-03 : Gen2 (3Gb/s) Differential Mode Return Loss
RX/TX-04 : Gen2 (3Gb/s) Common Mode Return Loss
RX/TX-05 : Gen2 (3Gb/s) Impedance Balance
RX/TX-06 : Gen1 (1.5Gb/s) Differential Mode Return Loss
RX/TX-07 : Gen3 (6Gb/s) Differential Mode Return Loss
RX/TX-08 : Gen3 (6Gb/s) Impedance Balance

obsolete

ECN-50 Revised

ECN-51 Revised

SATA Measurement Legends:
No change from previous UTD 1.3 spec version
Revised methodology from UTD1.3 to UTD 1.4
New test definitions in UTD 1.4
Obsolete

Summary: TSG05/06 have been classified as EMI related and moved to an obsolete status. TSG15 will use an eye height methodology and will have different limits depending on the DUT being a Host or Device

SATA ECN 50 Asymmetric Amplitude and Measurement Methodology

- Host and Device Transmitter signal amplitude asymmetry has now been instituted in the SATA 3.1 specification.

Parameters	Units	Limit	Electrical Specification					Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	Gen2i	Gen2m	Gen3		
SSC_{mod} Spread-Spectrum Modulation Rate	ppm/usec	Max	1250		1250		1250	7.2.2.1.6 7.3.3	7.4.16

Parameter	Units	Limit	Electrical Specification					Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	Gen2i	Gen2m	Gen3		
V_{CMTX} TX Differential Device Output Voltage	mVppd	Min	400		400		-	7.2.2.3	7.4.6
		Min	-		-		240		7.4.4 7.4.4.3
		Nom	500		-		-		7.4.6
		Max	600		700		-		
		Max	-		-		900		7.4.4
V_{CMTX} TX Differential Host Output Voltage	mVppd	Min	400		400		-	7.2.2.3	7.4.6
		Min	-		-		200240		7.4.4 7.4.4.3
		Nom	500		-		-		7.4.6
		Max	600		700		-		
		Max	-		-		900		7.4.4
UI_{nom} TX Minimum Voltage Measurement Interval	UI		0.45-0.55		0.45-0.55		-	7.2.2.3.2	7.4.6
			-		-		0.60 0.45-0.55		7.4.6.2

- Hosts may signal as low as 200mV (40mV lower than previously allowed)
- Devices must retain the original 240mV levels.
- Measurement methodology has been revised from a vertical BER contour to a simple Eye Height measurement.

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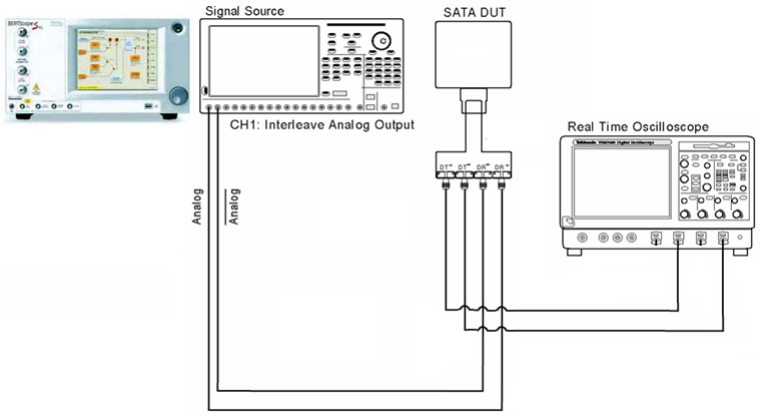
SATA发 端测试



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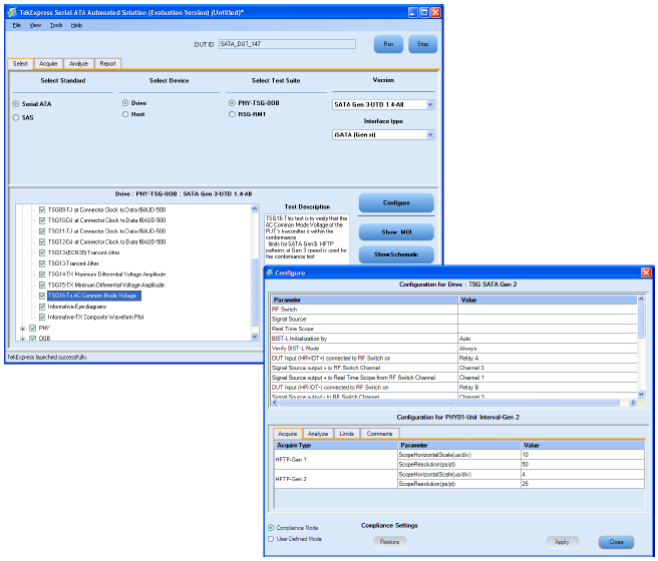
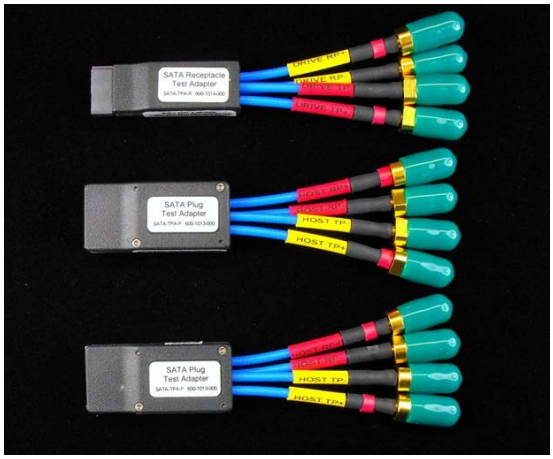
TekExpress SATA-TSG



测试　　SATA-TPA-P、SATA-TPA-R



Interconnect

New fixtures Summary

TF-DP-CIC-C1	DisplayPort Bulk Cable Compliance Interconnect Channel Board	$9,559
TF-MINI-DP-TPA-PT	miniDisplayPort Plug	$3,977
TF-MINI-DP-TPA-R	miniDisplayPort Receptacle	$3,173
TF-MINI-DP-TPA-PR2XT	miniDisPlayPort Plug, Receptacle, Dual 2X Calibration, with 18 inch Aux Box Pigtail Cable	$8,384
TF-MINI-DP-TPA-PRT	miniDisplayPort Plug, Receptacle, with18 inch Aux Box Pigtail Cable	$6,554
TF-DP-TPA-2XC	DisplayPort with Dual 2X Calibration	$2,089
TF-DP-TPA-PT	DisplayPort Plug with 18 inch Aux Box Pigtail Cable	$3,613
TF-DP-TPA-PR2XCT	DisplayPort Plug, Receptacle, with Dual 2X Calibration with 18 inch Aux Box Pigtail Cable	$7,479
TF-TB-TPA-P	Thunderbolt Plug	$3,629
TF-TB-TPA-R	Thunderbolt Receptacle	$3,566
TF-TB-TPA-2XC	Thunderbolt Dual 2X Calibration	$3,297
TF-TB-TPA-PR2XC	Thunderbolt Plug, Receptacle, Dual 2X Calibration	$10,401
TF-MSATA-TPA-P	miniSATA Gen 3 Plug	$1,553
TF-MSATA-TPA-R	miniSATA Gen 3 Receptacle	$1,237
TF-MSATA-TPA-PR2XC	miniSATA Gen 3 Plug, Receptacle, Dual 2X Calibration	$4,281
TF-MSATA-TPA-PR	miniSATA Gen 3 Plug, Receptacle	$2,667
TF-MSATA-TPA-2XC	miniSATA Gen 3 Dual 2X Calibration	$1,799
TF-SATA22-TPA-P	SATA Gen 3, 22 position Plug	$1,446
TF-SATA22-TPA-R	SATA Gen 3, 22 position Receptacle	$1,284
TF-SATA22-TPA-PR2XC	SATA Gen 3, 22 position Plug, Receptacle, Dual 2X Calibration	$3,999
TF-SATA22-TPA-PR	SATA Gen 3, 22 position Plug, Receptacle	$2,430
TF-SATA22-TPA-2XC	SATA Gen 3, 22 position Plug, Receptacle, Dual 2X Calibration	$1,696
TF-TPA-SATA25-P	SATA Gen 2.5, 7 position Plug	$973
TF-TPA-SATA25-R	SATA Gen 2.5, 7 position Plug	$969
TF-TPA-SATA25-PR2C	SATA Gen 2.5, 7 position Plug, Receptacle, Dual 2X Calibration includes (2) 1X, (2) 2X THRU Cables	$2,981
TF-TPA-SATA3-PR2C	SATA Gen 3, 7 position Plug, Receptacle, Dual 2X Calibration includes (2) 1X, (2) 2X THRU Cables	$3,536
TF-SASHD-TPAR-P	miniSASHD 12G SAS (Right Side) Plug	$4,414
TF-SASHD-TPAL-P	miniSASHD 12G SAS (Left Side) Plug	$4,414
TF-SASHD-TPA-R	miniSASHD 12G SAS Receptacle	$4,221
TF-SASHD-TPA-PR2XC	miniSASHD 12G SAS (Right Side) Plug, Receptacle, Dual 2X Calibration	$10,841
TF-SASHD-TPA-2XC	miniSASHD 12G SAS Dual 2X Calibration	$3,331
TF-SASHD-TPAR-PR	miniSASHD 12G SAS (Right Side) Plug, Receptacle	$7,696

- Comprehensive SATA, mSATA, miniSASHD, displayPort, Thunderbolt fixtures are now on PAL.
  - Kit configurations are in the TPA-PR2XC (Plug-Receptacle-2X Cal Structure) nomenclature.
  - Replacement parts can be obtained standalone with the remaining nomenclature.
  - Lower performing SATA fixtures are now available for the Gen1 and Gen2 applications.
  - 12G SASHD and Thunderbolt fixtures are also available,

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Fundamentals of 12G SAS characterization

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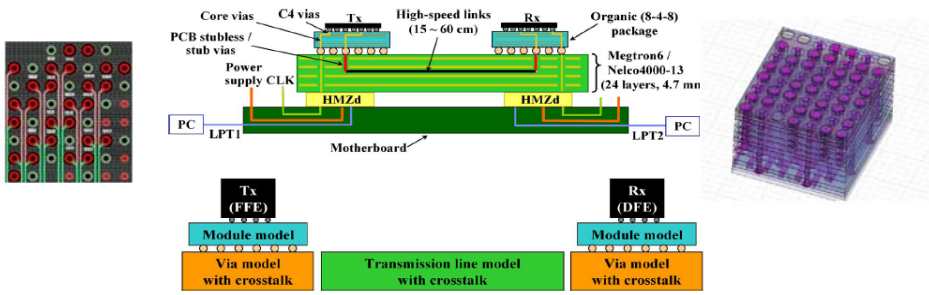
12+G Design Problem:
1000mV, FFE, Crosstalk, Crosstalk, Crosstalk, DFE, 50mV

- Significant advances in high tap count Decision Feedback Equalization are key to operating at 12+G.
- Mitigating the complex Channel Crosstalk and Signal loss problems which 12+G designs present, is the largest design challenge today.
- Typical Escape Structure bandwidth is 18GHz.
- Crosstalk is often beyond the capability of current equalization architectures to combat, and needs to be quantified if accurate performance projections are to be made based on experimental measurements. For short channels, NEXT may be less of an issue since the insertion loss is not as severe; however, in longer links and at higher data rates it has the potential to become a dominant design consideration. Ref:[1]

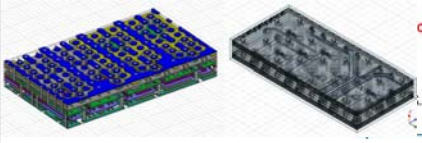
KAM *et al.*: IS 25 Gb/s ON-BOARD SIGNALING VIABLE? 329

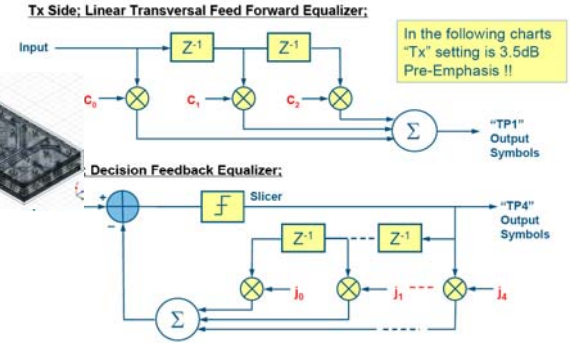


12G Design Problem:
FFE, DFE

- A non-recursive DFE can only compensate a fixed time span of ISI. In very low-bandwidth channels, significant post-cursor ISI may fall outside the time span covered by the DFE taps.
- FFE can compensate ISI over a very wide time span since the FFE filter response is convolved with the impulse response of the channel.
- The utility of FFE alone drops off rapidly over complex channels which have spectral nulls (Via stubs, connectors, etc) which require many FFE taps to cancel reflections.
- Optimal solutions exist around 4-tap FFE with 20+ (20*60mW) tap DFE designs. More emphasis is required in the Receiver section of the topology as more aggressive FFE makes crosstalk worse.

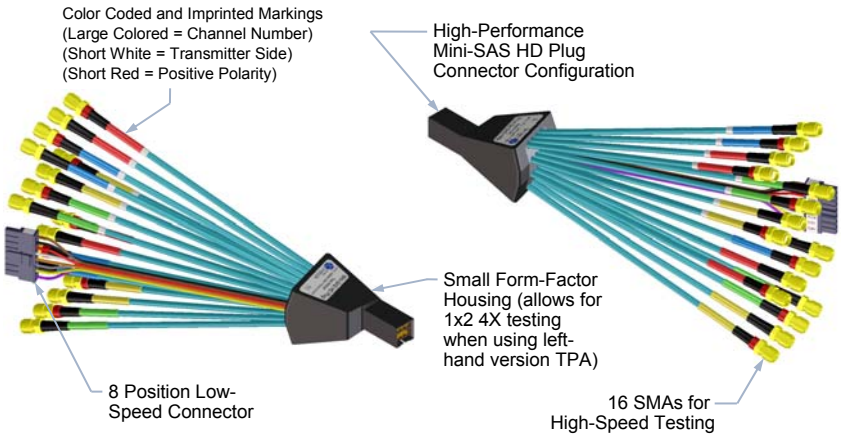
Ref:[1], [2]



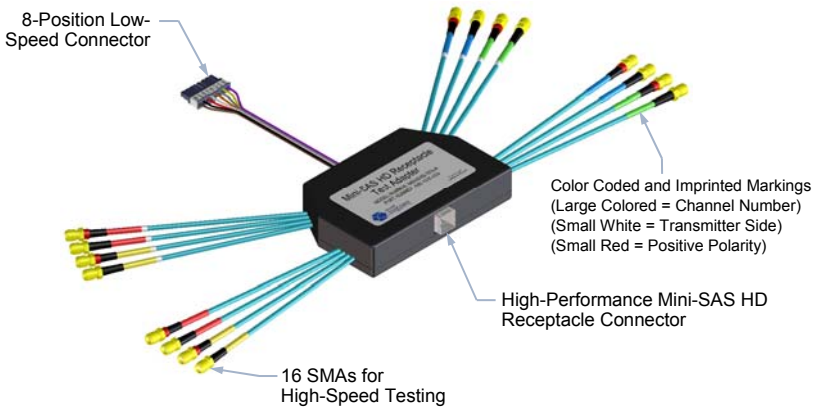


Ref:[2]: Tyco Electronics

Mini-SAS HD Plug Test Adapter (right-hand) Top Views



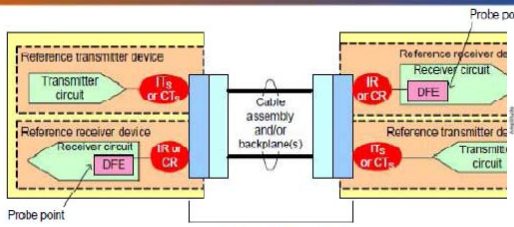
Mini-SAS HD Receptacle Test Adapter Top View

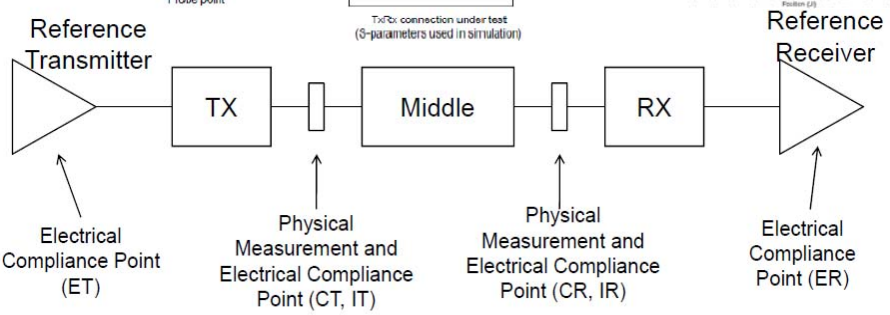


SAS3_EYEOPENING Usage Review
Compliance Points

PMC-SIERRA
Enabling connectivity. Empowering people.

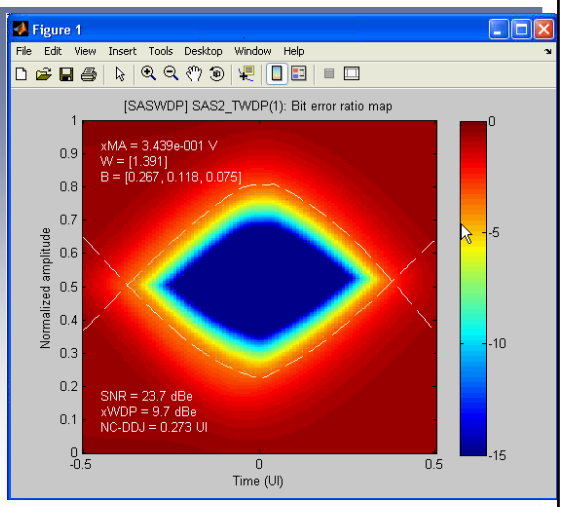
Note from Harvey: In SAS2, "Probe point" did not include any channel model, only the DFE model.





Waveform Distortion Penalty

- Waveform Distortion Penalty (WDP): Is a measurement method deployed in the SAS-2 spec. It uses acquired data against a simulated reference channel and DFE model, to evaluate the ratio of Non Compensatable Data Dependant Jitter to it's Compensatable counterpart.
- Tektronix has spent 20 months negotiating the terms of licensed re-distribution of WDP and is **currently the only T&M provider licensed to redistribute WDP and TWDP with test tools**.



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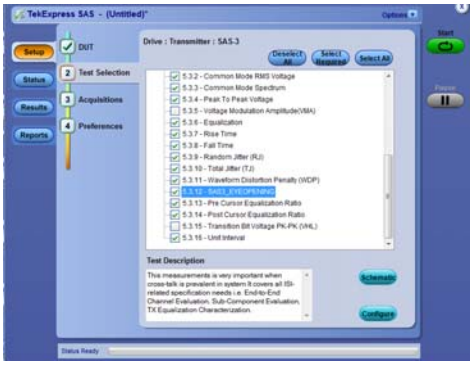
SAS test solution



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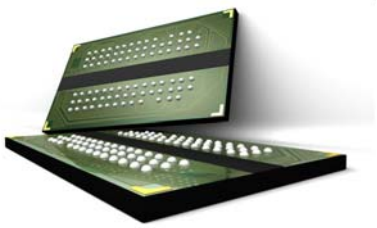
Analog Verification & Debug of DDR Memory



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Memory Technology – Quick Overview

- DRAM - dominant memory technology
  - Computer system memory
    - Server, desktop, laptop
    - Dynamic, volatile memory, plug-in DIMMs
  - Embedded systems
    - Cell phones, printers, cars
    - Fixed memory configuration
  - DRAM driven by faster processors, faster data rates
    - DDR3 now available at 2400 (2.4Gb/s) data rates
    - DDR4 3200(3.2Gb/s) data rates
- DRAM variants
  - LPDDR – Low Power DDR
    - Power savings for portable computing
  - GDDR – Graphic DDR
    - Optimized for Speed - faster access

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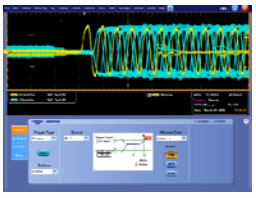
Analog Verification Challenges

- Signal Access & Probing
  - Easy-to-use / reliable connections
  - Bandwidth & Signal Integrity
  - Affordable
- Isolation of Read/Write bursts
- Specialized Measurements
  - JEDEC Conformance tests
    - Clock Jitter, Timing, Electrical Tests
  - Custom Settings
- Debug tools



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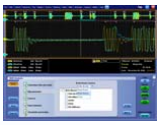
DDR Analog Verification & Debug – Tektronix Solutions

Signal Access - Probing

- Requires easy but reliable physical connectivity
  - access to various measurement points on DRAM or Memory
- Requires maximum signal integrity
  - sufficient performance for signal speeds

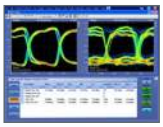
Signal Acquisition

- Automatically trigger and capture DDR signals
  - Identify and trigger directly on DQ, DQS in real-time to isolate Reads/Writes
  - Automatically set voltage levels and data rates
- Capture long time duration at high resolution
  - Direct connection to DPOJET for signal analysis



Signal Analysis

- DDRA – Automated setup, read/write burst detection, JEDEC pass/fail meas.
- DPOJET – The most powerful Jitter, Eye and Timing analysis tool
  - Time, Amplitude, Histogram, measurements
  - Advanced Jitter, Eye diagram measurements and Pass/Fail testing
  - Many display and plotting options
  - Report generator



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Analog Verification & Debug

Signal Access - Probing

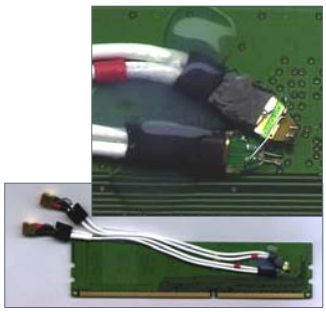
Performance

- Sufficient performance for increasing signal speeds
- Patented TriMode™ providing superior signal fidelity, fast risetime and low circuit loading.
- Trace models available for Instrumented DIMM to remove the effect of the probing from the captured signals

Connectivity

Solder down probing

- Easy probe attachment
- Need access near BGA (Board Grid Array) connections on DRAM
- Verify signals at receiving end of Read channel (at Memory controller) DDR3 DIMM



P7500 TriMode Differential Probe, solder tip connected to DDR3-1033 DIMM

BGA Chip Interposer

- Socket or Solder-In versions available
- Excellent signal fidelity with Tektronix probes

Nexus DDR3 Chip Interposer on DIMM

Instrumented DIMM

- Dual Rank, x8 memory chips, 72 bit
- Designed to JEDEC standards
- Easy connections to oscilloscope - no soldering needed
- Both sides of DDR3 differential signals available for probing

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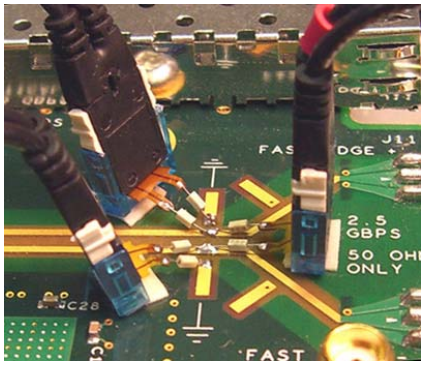
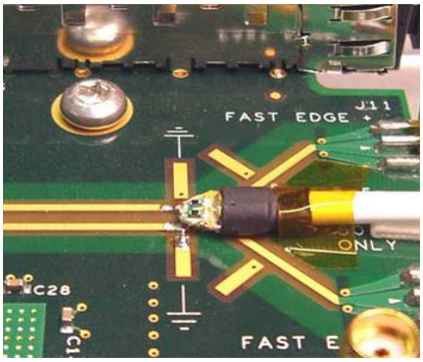
Before and After



Before TriMode Probing
1 Probe for Differential
2 Probes for SE and Common Mode
or
1 Probe Soldered and Re-soldered 3 times
2 Probes for Common Mode



After TriMode Probing
1 Probe and 1 setup for
Differential, SE and Common Mode

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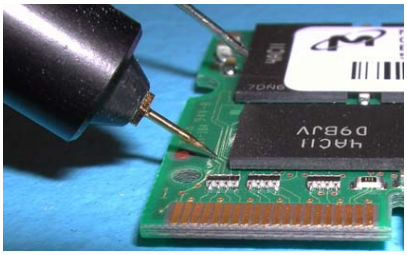
DDR Probing

- Computer Systems use standardized DIMM's for which several probing solutions are available
- Memory in Embedded Designs is usually directly mounted on the PCB.
- All DDR2 & DDR3 Components use BGA Packages
  - Reduces the parasitics, enabling performance at higher speeds
  - Mandate from JEDEC
- Probing a BGA package is Difficult
  - Unable to probe at the Balls of the Device
  - Probing at a connector, trace, or a via is not the same as probing at the device
  - Not a true representation of the signal



*Courtesy Micron Technologies

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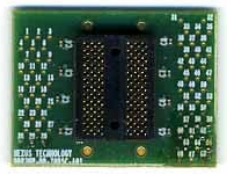
Introducing
Nexus DDR3 BGA Chip Interposers
For Oscilloscopes



BGA Chip Interposer

Retention Socket

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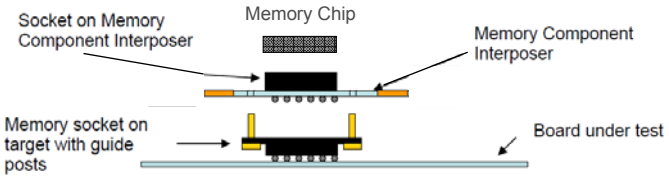
Installation Process



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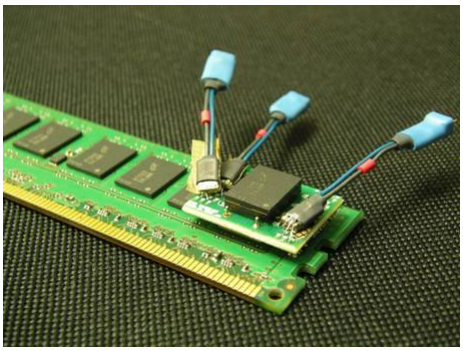
BGA Chip Interposer for Oscilloscopes



- Available in socket and solder-in versions
  - Socket design allows for multiple chip exchanges
  - Solder-in best for single use
- Recommended probes: P7500 Series
  - P7504, P7506, P7508, P7513A
  - 020-3022-00 TriMode solder tips for Nexus Interposer

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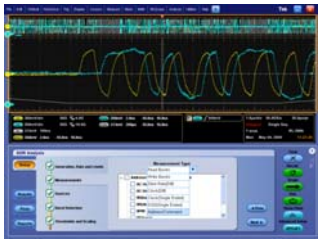
Signal Acquisition & Measurements

Option DDRA: Oscilloscope-based DDR tool that accelerates the validation of high-speed DDR memory bus interfaces



- New Configuration Wizard Guides Easy Setup and Test Configuration
- Analyze All Read/Write Bursts in the Entire Acquisition
- Plot DQS and DQ Eye Diagrams for Reads and Writes
- Perform JEDEC Conformance Tests with Pass/Fail Limits
- Use Chip Select to Qualify Multirank Measurements
- Easily Move Between Conformance-test and Analysis/Debug Tools
- Automatically Produce Consolidated Reports with Pass/Fail Information, Statistical Measurement Results, and Test-setup Information

Validation of DDR, DDR2, DDR3, DDR4 and LP-DDR in one tool

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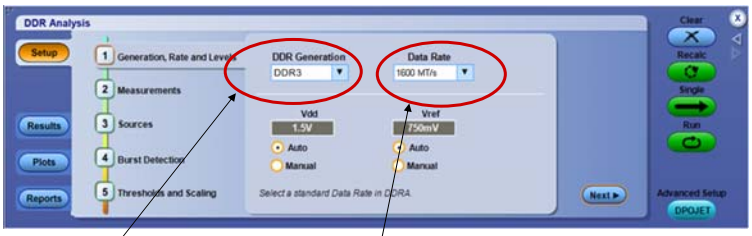
Automated Test Setup

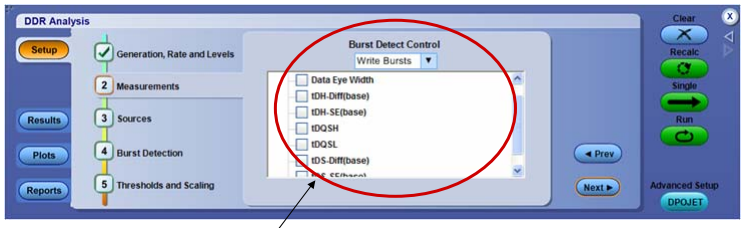
Step #1



Select DDR Generation

Select DDR Rate

Step #2



Choose measurements (Read / Write / CLK / Addr & Command)

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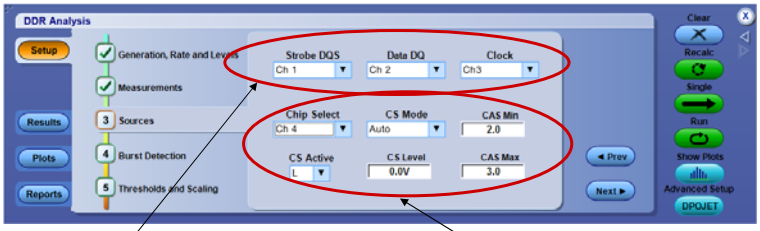
Source and Level Selection

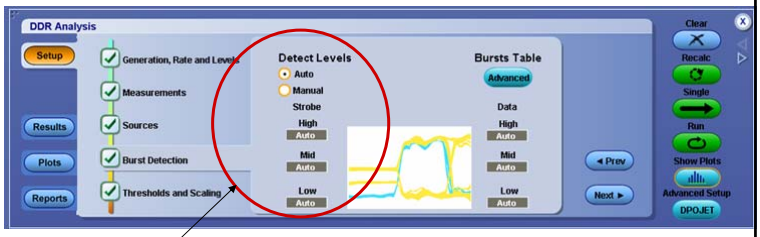
Step #3



Identify scope input channels for DQS, DQ, CLK, etc

Optional Chip Select qualifier

Step #4



Let DDRA set Read/Write Burst Detection Levels automatically, or customize if needed

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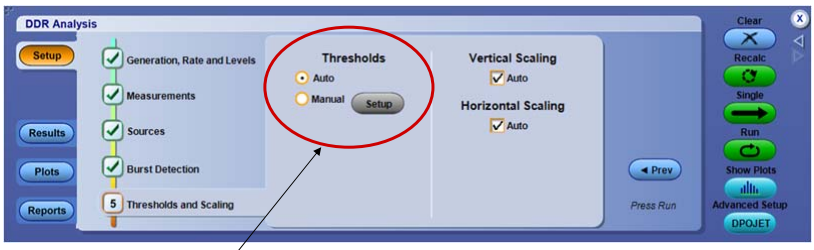
Measurement Thresholds and Auto Scaling

Step #5



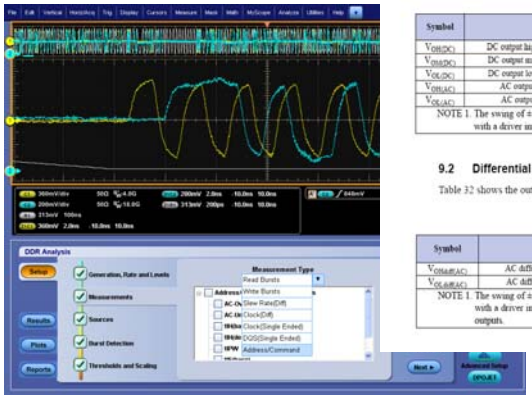
Let DDRA set Measurement Ref Levels automatically (per JEDEC), or customize if needed

Automatically isolate & mark all read or write bursts

- Easily Identify, mark & measure all Read / Write bursts
  - Scroll through marked reads / writes across the entire waveform record
  - Measurements performed on ALL reads/writes

Specialized Measurements for DDR

- JEDEC Standards specify measurements & methods



9 AC and DC Output Measurement Levels

9.1 Single Ended AC and DC Output Levels

Table 31 shows the output levels used for measurements of single ended signals.

Table 31 — Single-ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	$0.2 \times V_{DDQ}$	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	$V_{TT} + 0.1 \times V_{DDQ}$	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	$V_{TT} - 0.1 \times V_{DDQ}$	V	1

NOTE 1. The swing of $\pm 0.1 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $V_{TT} = V_{DDQ}/2$.

9.2 Differential AC and DC Output Levels

Table 32 shows the output levels used for measurements of differential signals.

Table 32 — Differential AC and DC Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit	Notes
$V_{OH(diff)(AC)}$	AC differential output high measurement level (for output SR)	$+0.2 \times V_{DDQ}$	V	1
$V_{OL(diff)(AC)}$	AC differential output low measurement level (for output SR)	$-0.2 \times V_{DDQ}$	V	1

NOTE 1. The swing of $\pm 0.2 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $V_{TT} = V_{DDQ}/2$ at each of the differential outputs.

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JEDEC Measurements Support in DDRA

Option DDRA supports a broad range of JEDEC-specified measurements for DDR, DDR2, DDR3, DDR4, LP-DDR

- Example measurements list for DDR2 :

- tCK(avg)
- tCK(abs)
- tCH(avg)
- tCH(abs)
- tCL(avg)
- tCL(abs)
- tHP
- tJIT(duty)
- tJIT(per)
- tJIT(cc)
- tERR(02)
- tERR(03)
- tERR(04)
- tERR(05)
- tERR(6 - 10 per)
- tERR(11 - 50 per)
- tDQSH
- tDS - diff (base)
- tDS - SE (base)
- tDS -diff - DERATED
- tDS -SE - DERATED
- tDH - diff (base)
- tDH - SE (base)
- tDH -diff - DERATED
- tDH -SE - DERATED
- tDIPW
- tAC - diff
- tDQSCK -diff
- tDQSCK - SE
- tDQSQ - diff
- tDQSQ - SE
- tQH
- tDQSS
- tDSS
- tDSH
- tIPW
- tIS (base)
- tIH (base)
- tIS - DERATED
- tIH - DERATED
- Vid - diff (AC)
- Vix (AC) - DQS
- Vix (AC) - CLK
- Vox (AC) - DQS
- Vox (AC) - CLK
- Input Slew-Rise (DQS),
- Input Slew-Fall (DQS),
- Input Slew-Rise (CLK),
- Input Slew-Fall (CLK),
- AC - Overshoot Amplitude - diff
- AC -Undershoot Amplitude - diff
- AC - Overshoot Amplitude - SE
- AC - Undershoot Amplitude - SE
- Data Eye Width

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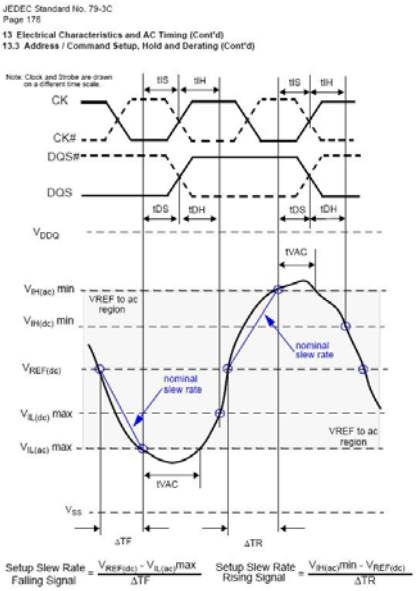
Measurement De-rating

• JEDEC stipulates de-rating of DDR2 and DDR3 pass / fail limits for Setup & Hold measurements based on signal slew rate*

• Option DDRA automatically calculates slew rates and applies the appropriate de-rating values to the measurement limits.

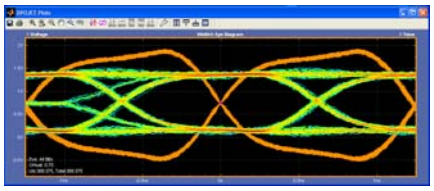
- tDS - diff (base)
- tDS -diff - DERATED
- tDS - SE (base)
- tDS -SE - DERATED
- tDH - diff (base)
- tDH -diff - DERATED
- tDH - SE (base)
- tDH -SE - DERATED
- tIS (base)
- tIS - DERATED
- tIH (base)
- tIH - DERATED



* JESD79-2E, JESD79-3C specifications

Signal Analysis & Debug
DDRA + DPOJET

- DDRA is not a closed tool – links directly to DPOJET for measurement details
- Opportunity to change or fine-tune settings, add new measurements as needed



DDR2 Write Eye Diagram – showing both DQ and DQS eyes

- DPOJET - powerful measurement engine for DDRA
- All settings are explicit – you can see them and change them.

"One Click" access to DPOJET & back

Memory Information Resources

- Tektronix
  - www.tektronix.com/memory
- Nexus Technology
  - www.nexustechnology.com
- Memory Implementers Forum
  - www.memforum.org
- JEDEC
  - www.jedec.org

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接　端　　测试

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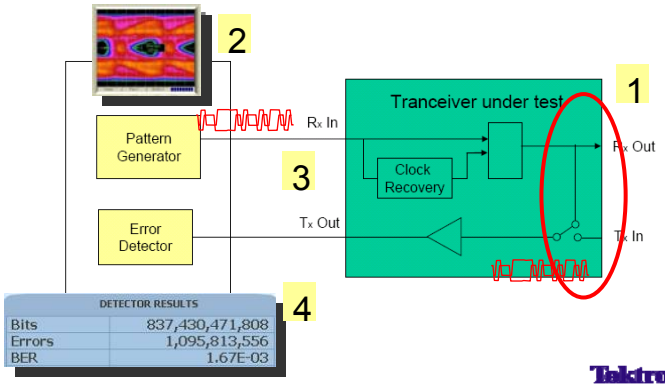
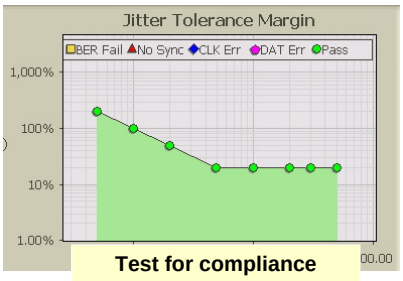
高速串行　　Rx接　端测试的

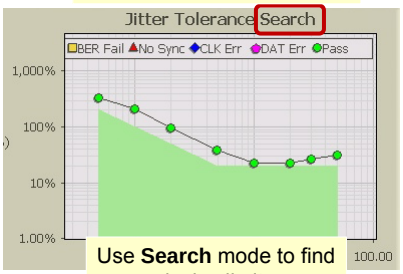
1. **DUT　Loopback　(Analog/Re-timing)**
2. **　　的　分　　的　分　　应的**
3. **stressed　　DUT Rx**
4. **计DUT Tx端发　的　　的**



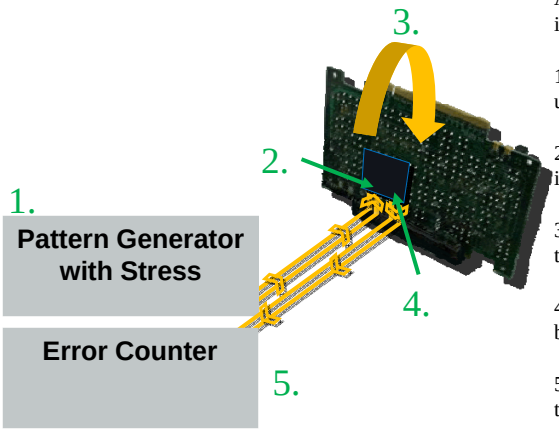
化Jitter Tolerance　　测试方案

- ✓PCIE GEN1,2,3
- ✓SATA I,II,III
- ✓USB3
- ✓Display Port
- ✓XFP/XFI
- ✓10GBase-KR
- ✓Optical
- ✓Serial Bus...





PCIe 3.0 Receiver Testing



At the simplest level, receiver testing is composed of:

1.Send impaired signal to the receiver under test

2.The receiver decides whether the incoming bits are a one or a zero

3.The chip loops back the bit stream to the transmitter

4.The transmitter sends out exactly the bits it received

5.An error counter compares the bits to the expected signal and looks for mistakes (errors)

PCIe 3.0 Stress Recipe

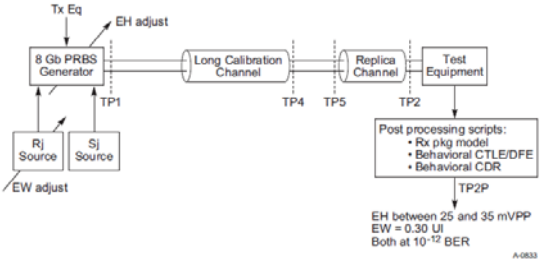


Figure 4-73: Layout for Calibrating the Stressed Jitter Eye

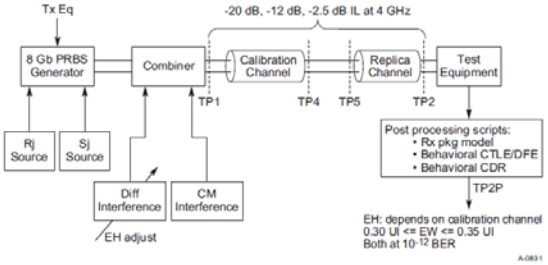


Figure 4-71: Setup for Calibrating the Stressed Voltage Eye

*From PCI Express Base Spec

Test Setup and Results

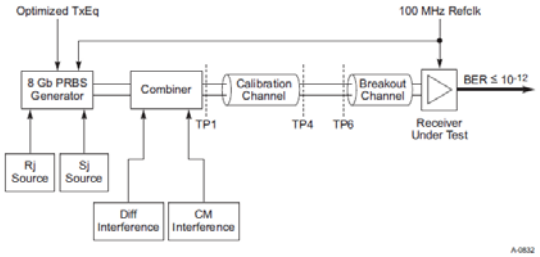


Figure 4-72: Layout for Stressed Voltage Testing of Receiver

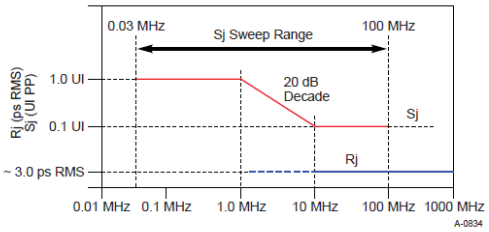


Figure 4-74: Swept Sj Mask

***From PCI Express Base Spec**

Components of a PCIe3 Receiver Test Solution

- BERTScope C Model
  - PG, stressed eye sources, ED
- New! DPP125C Option ECM
  - Eye opener, Clock doubler/Multiplier
- New! BSAITS125
  - CM/DM interference
  - ISI for Gen2 & Gen3
  - Option EXP for variable ISI
- New! CR125A Opt PCIE8G
  - PLL analysis for Gen1/2/3
    - New! BSAPCI3 SW
  - Auto calibration, Link training, and test
- Cables, adapters, compliance boards
- DPO/MSO70KC/DX Series Oscilloscope
  - Stressed Eye Calibration

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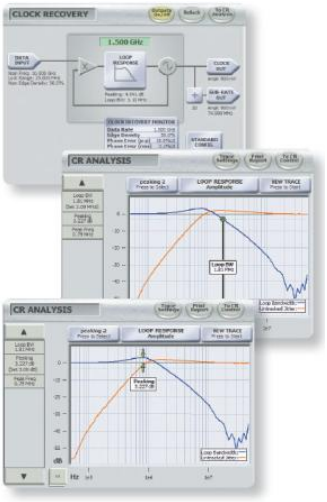
New! DPP125C with Option ECM

- Integrated reference clock multiplication to PCIe compliant 2.5 GHz, 5 GHz, and 8 GHz.
- Integrated eye opener functionality for testing DUTs with long channels.
- New microcontroller to provide more processing power.
- RS-232 interface enhancement to speed-up PCIe receiver equalization link training.
- SW to accommodate channel de-embedding and ISI fine adjustments.

New! BSAITS125 Interference Test Set

- Programmable, variable ISI for automated testing and precision setting
- Built-in compliant PCIe2 and PCIe3 Medium and Long ISI channels
- Integrated PCIe3 CM and DM interference combiner
- Integrated PCIe3 Base Spec CM interference calibration
- Continuously Variable, Expanded ISI for automated testing of multiple standards with Option EXP

New! CR125A Opt PCIE8G



- PLL Loop BW Analysis for Gen1/2/3
- Uses CR125A and Test SW
  - Similar to Gen1/2 PLL Loop BW solution

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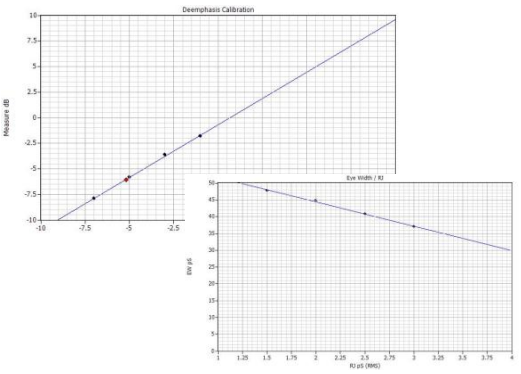
New! BSAPCI3 PCIe 3.0 Automation SW

- Automated calibration, link training, loopback initiation, and testing.
- BER Map feature for TxEQ optimization.
- Reduces the time and minimizes the skill-set required to perform the calibration and testing.
- Increases the reliability and accuracy by removing inconsistencies with manual calibration.



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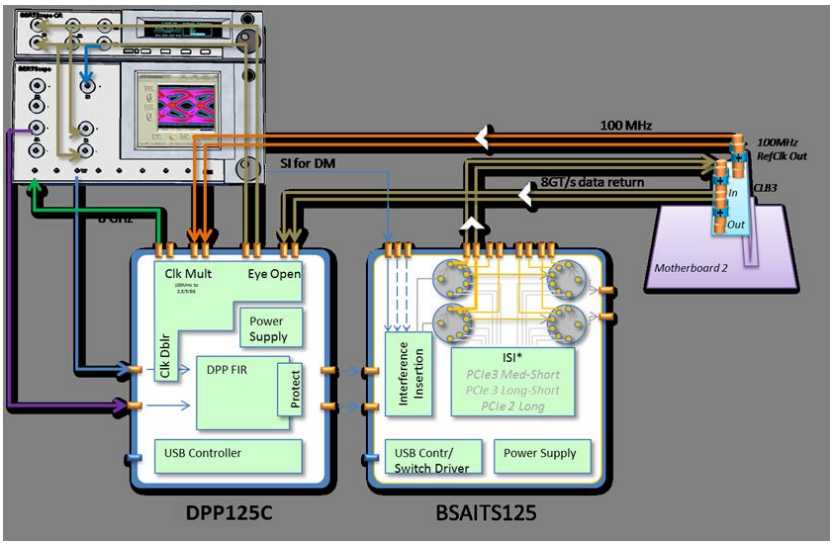
Typical PCIe3 Rx Test Configuration



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接　端　　测试SATA-RSG

- RSG-01 : Gen1 (1.5 Gbps) Receiver Jitter Tolerance Test
- RSG-02 : Gen2 (3 Gbps) Receiver Jitter Tolerance Test
- RSG-03 : Gen3 (6 Gbps) Receiver Jitter Tolerance Test
- RSG-05 : Receiver Stress Test at +350 ppm
- RSG-06 : Receiver Stress Test With SSC (Informative)

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SATA ECN 51: Change of receiver test pattern to FCOMP

The receiver tolerance test shall be conducted over variations in parameters SSC on and off, minimum and maximum amplitude, common mode interference over the specified frequency range, the test pattern **FCOMP** described in section 7.2.4.3.7, and jitter which includes the maximum random and deterministic jitter of various types: data dependent, periodic, duty cycle distortion.

7.2.4.3.7 Framed Composite Pattern (FCOMP)

The Framed Composite Pattern is equivalent to the COMP pattern in section 7.2.4.3.6 with the following structured changes:

1. In-line with section 7.2.4.2 the COMP pattern is framed. 2 ALIGN primitives inserted every 256 Dwords.
2. A short Inter Gap region is introduced before and after the SOF/EOF to ensure that when repeated sequentially by a generator the 256 Dword ALIGN primitives are perfectly and uniformly spaced 256 Dwords apart even after wrap-around by the generator.

1.1.1.1.1 Framed Composite Pattern (FCOMP)

Table FF – Framed Composite Pattern (FCOMP)

	Transmission Order →										
	K28.5(BCh)+		D10.2(4Ah)-		D10.2(4Ah)-		D27.3(7Bh)-				
+	1100	0001	0101	0101	0101	0101	0101	0111	0110	0011	+
	C	1	5	5	5	5	5	7	6	3	
	Above Dword is repeated a total of 2 times. 2 DW ALIGNp.										

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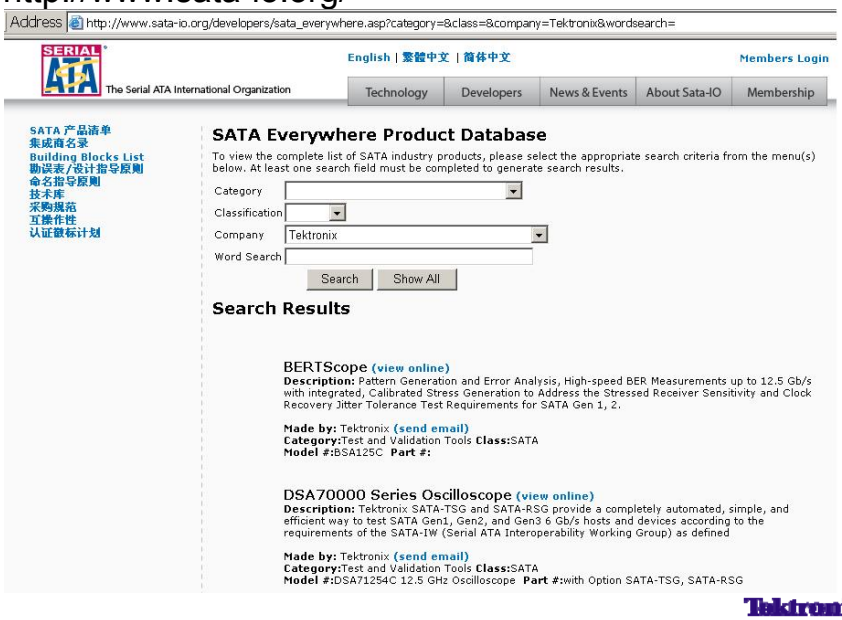
http://www.sata-io.org/



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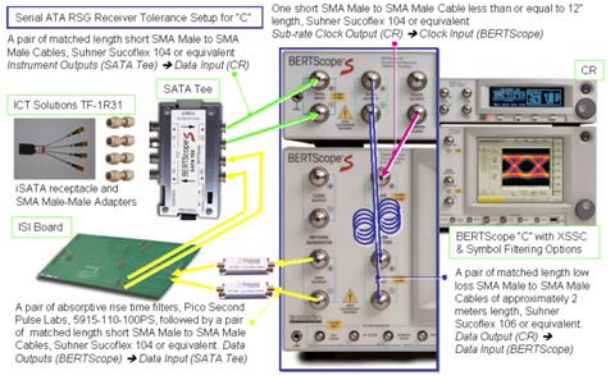
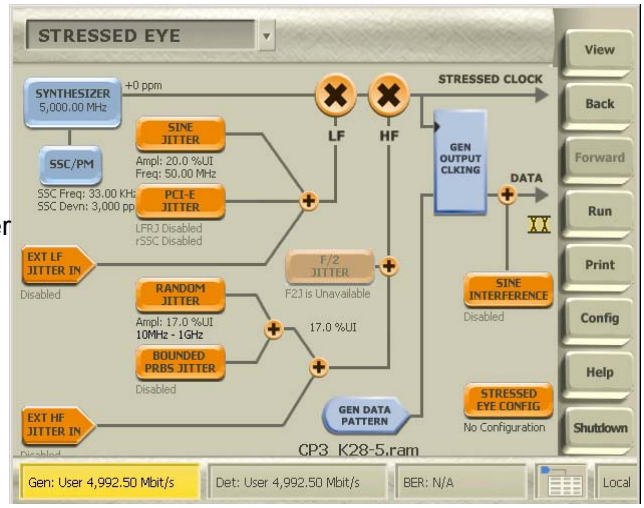
SATA接　端　　测试



- 测试工
  - BertScope BSA85C(STR　　测试)
  - CR125A
  - BSA12500ISI　分ISI
  - 100PSRTFILTER 100ps
  - 测试　　SATA-TPA-P/R
  -

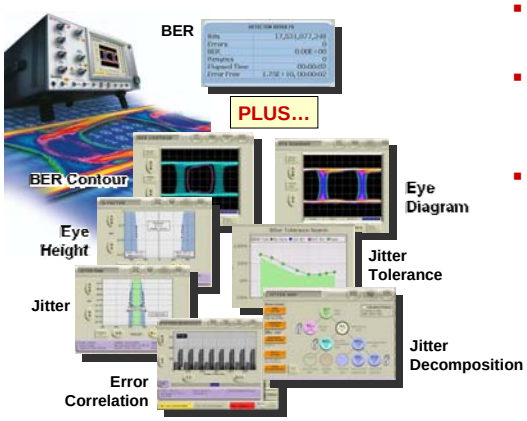
BERTScope

- Sine jitter
  - 1KHz~100MHz
  - max.1100ps
- Random jitter
  - f>1GHz
- Bounded PRBS jitter
- SSC
  - 12,500ppm
- Sine Interference



Beyond Compliance: BERTScope Analysis Tools

- Besides being a BERT, the BERTScope's **"Scope" functionality** brings benefits that complement those of the Tektronix scopes
- Analysis tools are full featured and easy to use



- Frees up the scope for other tasks
- **Eye diagram for quick diagnosis** of synchronization and BER failure issues
- **Debug** challenging **signal integrity problems**
  - Error Location Analysis
  - Pattern Capture
  - Jitter Map
  - BER Contour