DisplayPort Standard

12-04-2007

DisplayPort Standard
Tektronix MOI for Source Tests
(Real-Time DSO measurements for Source Devices)

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Modification Records

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Randy White, Ken Price, Keith Rule:
Changed test 3-14 Frequency Long Term Stability to Informative
Added spec range for test 3-14 Unit Interval to include SSC (+300ppm to -5300ppm)

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INTRODUCTION

The tests contained in this document are organized under Source tests only.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. This document outlines precise and specific procedures required to conduct Display Port tests. This document covers the following tests which are all Tektronix Real Time DPO/DSA oscilloscope based.

Formally, each test description contains the following sections:

- **Test Objective**
- **Interoperability statement**
- **Test conditions**
- **Measurement requirements and**
- **Pass/fail criteria covering:**
  - Source compliance tests (tests 3.1 – 3.17)
- **Equipment Preparation**

Prior to making any measurements, the following steps must be taken to assure accurate measurement:

1. Allow a minimum of 20 minutes warm-up time for oscilloscope.
2. Run scope SPC calibration routine. It is necessary to remove all probes from the scope before running SPC.
3. If using probes, perform the probe calibration defined for the specific probes being used.
4. Perform deskew to compensate for skew between measurement channels. Note that it is critical to select “Off” for the “Display Only” control on the Deskew setup window. This will assure that the deskew data is stored with any waveforms that are stored.

SOURCE COMPLIANCE TESTS

Test 3.1 – Eye Diagram testing (Normative)

1.1.1 Test Objective

To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall Display Port system objectives of Bit Error Rate in data transmission.

1.1.2 References

- Display Port Specification version 1.1 dated 19-Mar-2007 and errata 3 document dated 29-Aug-2007 and errata 4 document dated 6-Sep-2007.
- Display Port CTS draft 13 version 1 specifications dated 20-Jul-2007, section 3.1

1.1.3 Test Conditions

Tests shall be made on all Bit Rates supported without Pre-Emphasis and with non transition bit Voltage swing equal to or less than 800mV differential p-p.
Test Pattern: PRBS 7

1.1.4 Measurement Requirements

The following requirements must be met for each eye diagram measurement:
Clock Recovery as stipulated in section 2.1:

- The analysis equipment shall have the Bandwidth ≥ 8GHz
- When clock recovery is required, the implemented clock recovery technique shall follow the JT response curve (jitter Vs frequency).
- **Note:** Clock Recovery is of 2nd Order and Loop Damping Factor is 0.7*

Minimum Acquisition Time : 25x1/PLLBW* = 25 x (1/10MHz) = 2.5µS
(*Note: Where PLLBW = 10MHz and damping factor = 0.7 comes from JT response curve -Jitter Vs Frequency: Fig. 3-18 of errata doc)
Number of Edges measured: >100,000

- For HBR (high bit rate = 2.7Gbps): One UI = 370pS, for 100,000 UIs acquisition duration should be 100k * 370pS = 37µS (minimum for 100k edges)
- For RBR (reduced bit rate = 1.62Gbps): One UI = 617.3pS, for 100,000 UIs acquisition duration should be 100k * 617.3pS = 62µS (minimum for 100k edges)

The Eye Diagram will be displayed such that more than one full UI is shown but no more than 2.5UI.

1.1.5 Test equipment required

Refer to Appendix A of this MOI.

1.1.6 Connection Diagram

Refer to Appendix B of this MOI.

1.1.7 Detailed Test Procedure

Using DPOJET:

a. Set the Display Port Transmitter to generate the PRBS7 HBR (high bit rate=2.7Gbps) pattern with the required V_{swing} (400mV or 600mV or 800mV) and with no Pre-Emphasis.
b. Connect the differential input signals to Ch1 of the scope.
c. Enable the Tektronix display port solution application software (DPOJET – Jitter and Eye Diagram Analysis Tools) and load the appropriate <3.1-EyeDiag-HBR-DispPort.set> setup file. For recalling setup file: File menu → Recall → navigate to the appropriate setup file.

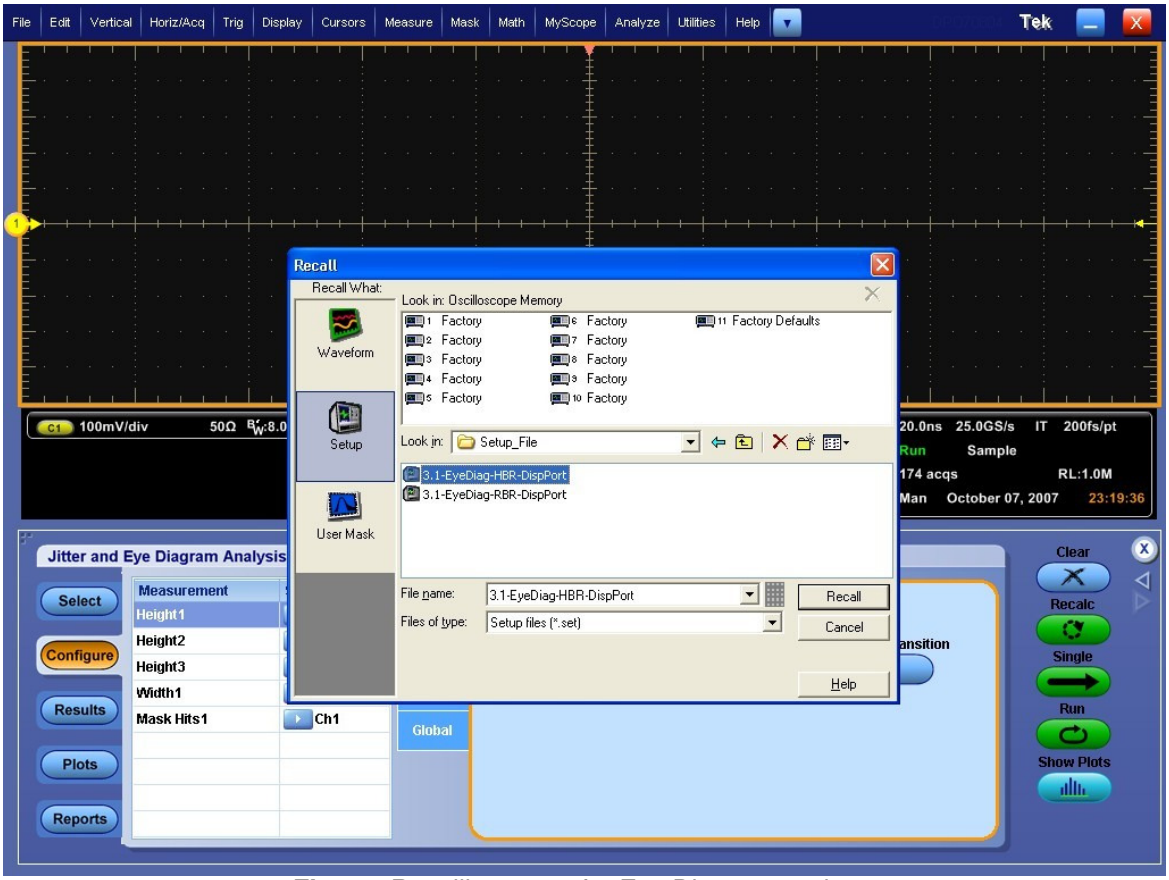


Figure: Recalling setup for Eye Diagram testing.

d. After setup recall, ensure that:
   - Correct Display port Eye masks <HBR_0dB_SRC_400.msk> and limit files <HBR_noPreEmph_ SRC_400.xml> are loaded.

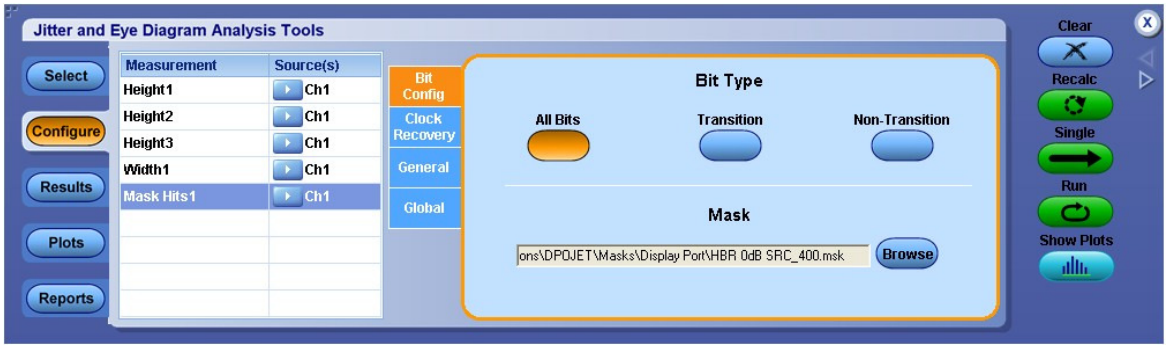


Figure: Eye diagram plot configuration – Setting mask file for eye diagram.

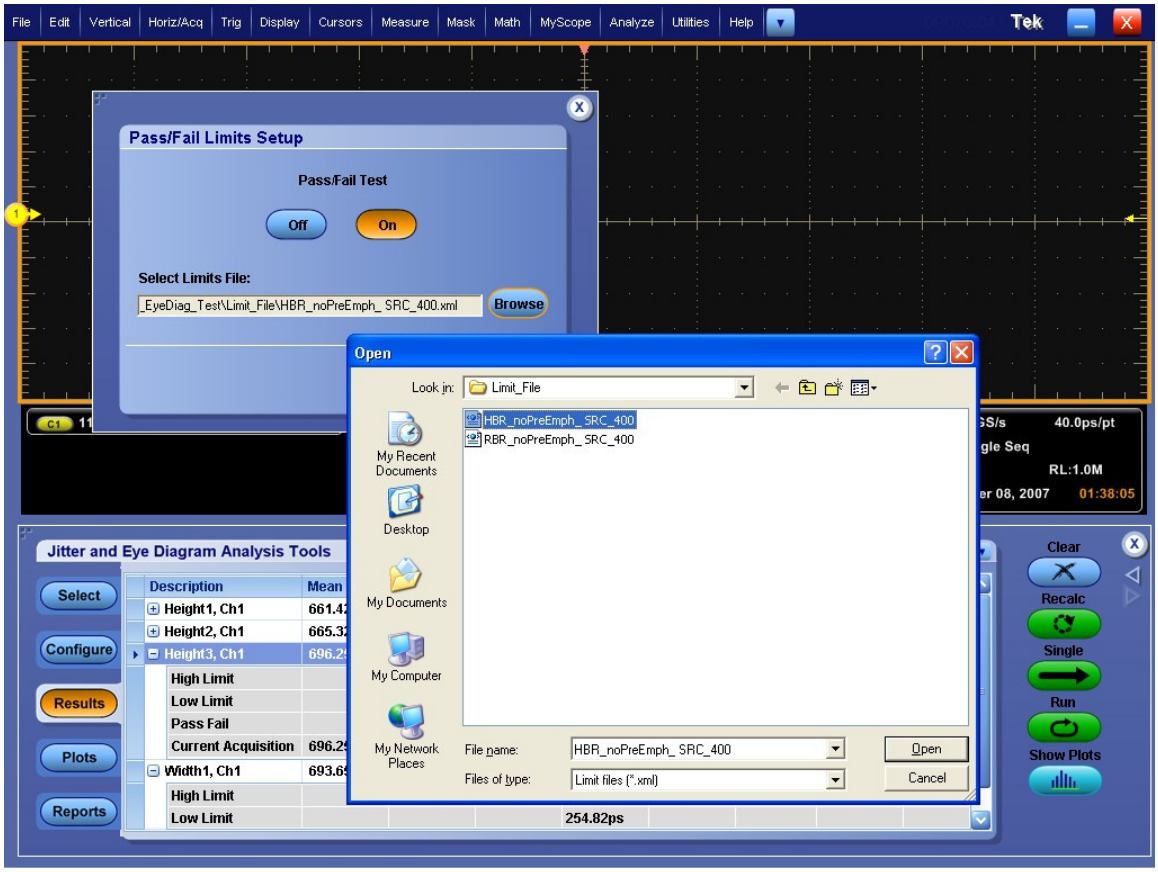


Figure: Pass/Fail limit setting – Navigate through Analyze > Jitter and Eye Analysis > Limits.

   - The scope time base is 4µS/div and hence the acquisition duration is 40µS.
   - Measurements selected are: Eye Height, Eye width and Mask hits.
   - The application measurements are configured for proper configuration parameters and sources (Ch1)

- The vertical scale for the source (Ch1) is such that it occupies >= 6 vertical divisions in the graticule.
- Clock recovery configuration is correct (PLL-Custom BW, PLL model = type II, Damping = 0.7, PLL Loop BW = 10MHz).

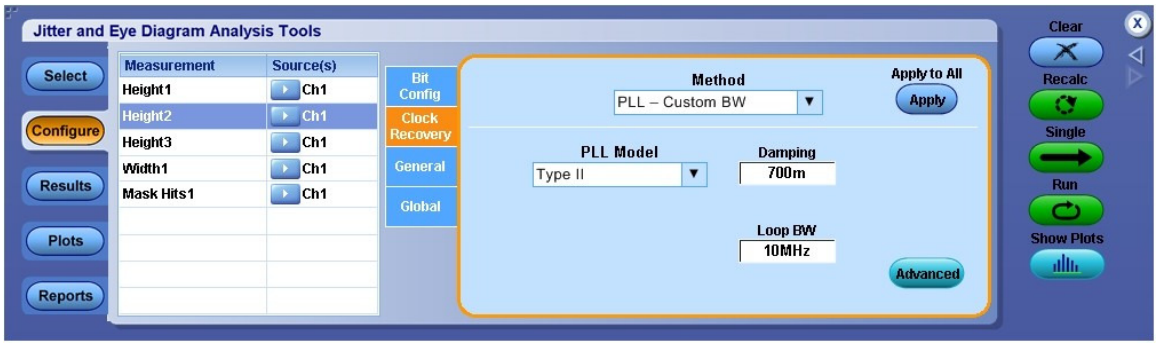


Figure: Measurement configuration – Setting clock recovery parameters.

- Eye diagram plot is added for Mask hits measurement- All bits.

e. In case setup files are not available above mentioned setting should be done manually.
f. Press Single to run the measurements.
g. As shown in figure below, results will be displayed with pass/fail limits, in the result panel. Eye diagram plots with mask will be displayed in the plot window. Eye Height measurements 1, 2, and 3 correspond to All, Transition, and Non-Transition bits respectively.
h. Click on the 'options' arrow button on the result panel and uncheck "Display Units – Absolute" to change the units of 'Width' measurement from seconds to UI.

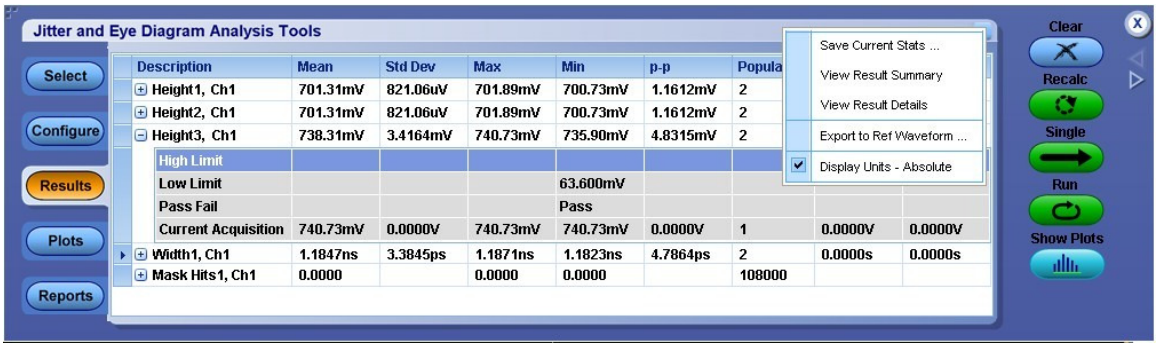


Figure: Configuring the results for showing Eye Width in terms of UI (than absolute value in sec.)

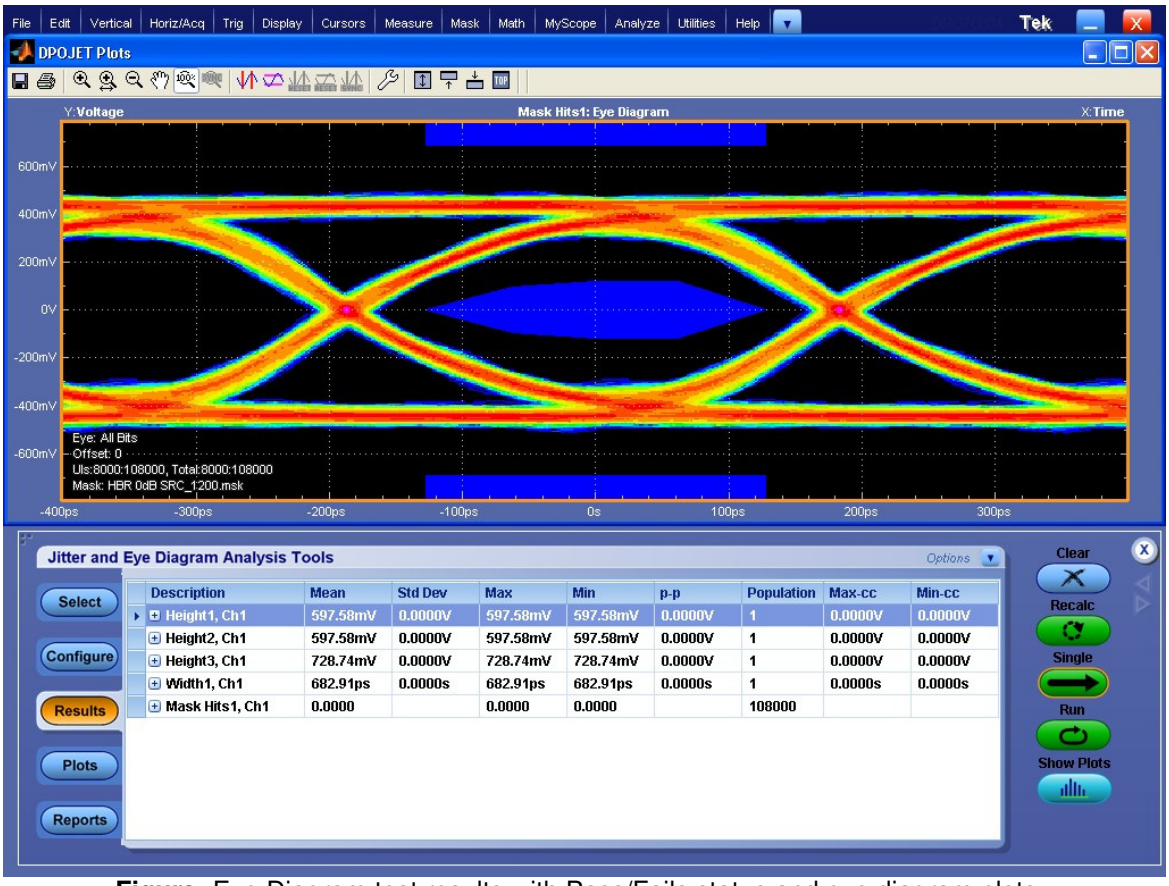


Figure: Eye Diagram test results with Pass/Fails status and eye diagram plots.

i. Do the similar exercise for measurement on PRBS7 RBR signal (Reduced bit rate 1.62Gbps). However, the horizontal time base setting will be 8µS/div and mask <RBR_0dB_SRC_400.msk> and limit files <RBR_noPreEmph_SRC_400.xml> should be chosen corresponding to RBR signal. These settings are defined in the setup file <3.1-EyeDiag-RBR-DispPort.set>.

j. If the signal of 400mV amplitude swing passes, then the device passes the compliance test- if not, repeat the test using a 600mV signal. If the 600mV signal passes, then the device passes - if not, repeat the test using a 800mV signal.

Using RT-Eye:

a. Set the Display Port Transmitter to generate the PRBS7 pattern with the required Vswing (400mV or 600mV or 800mV) and with no Pre-Emphasis.
b. Enable the Tektronix display port solution application software (RT-Eye Serial Analysis) and load the appropriate setup file < 3.1_EyeDiag_HBR_setup.ini>.

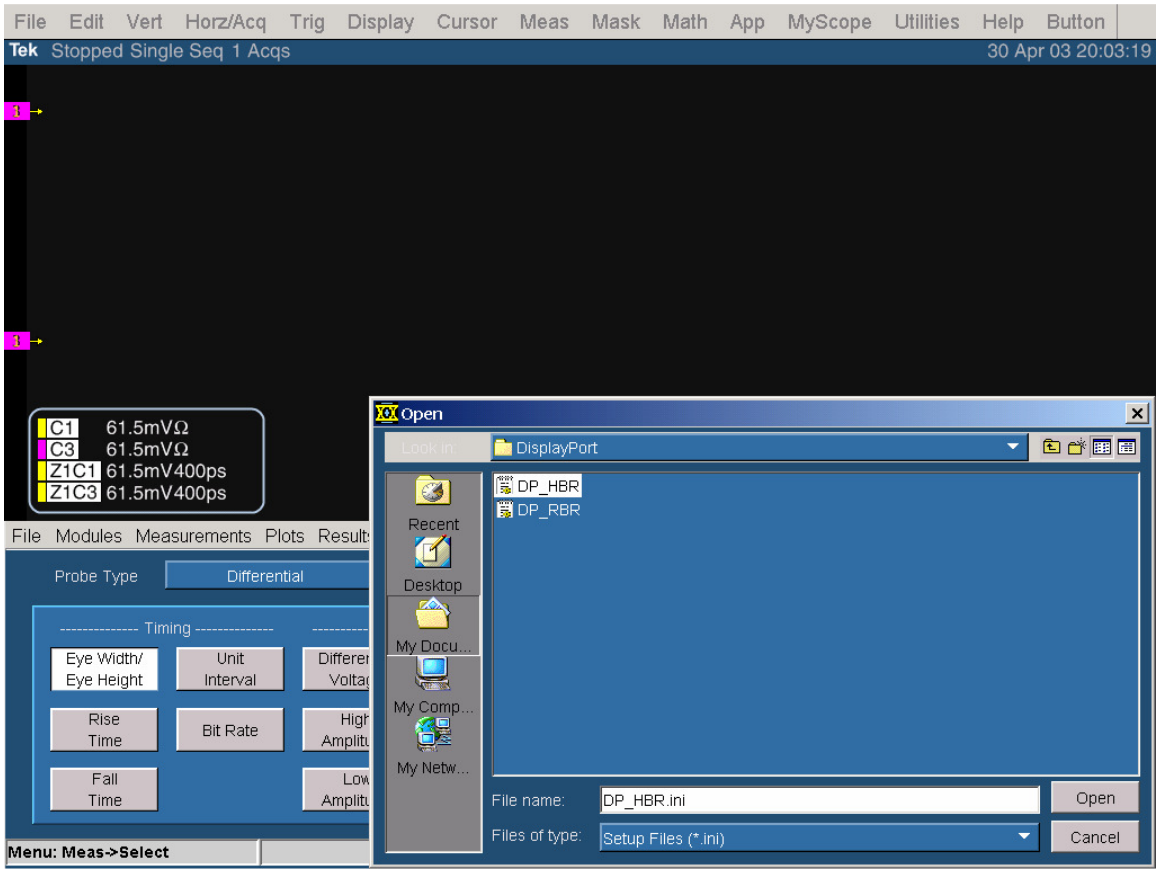


Figure: Recalling setup for Eye Diagram measurement on RT-Eye application.

c. Ensure that the correct Display port Eye masks and limit files will be loaded. Configure the application for proper channel, PLL, number of UI and RL settings.

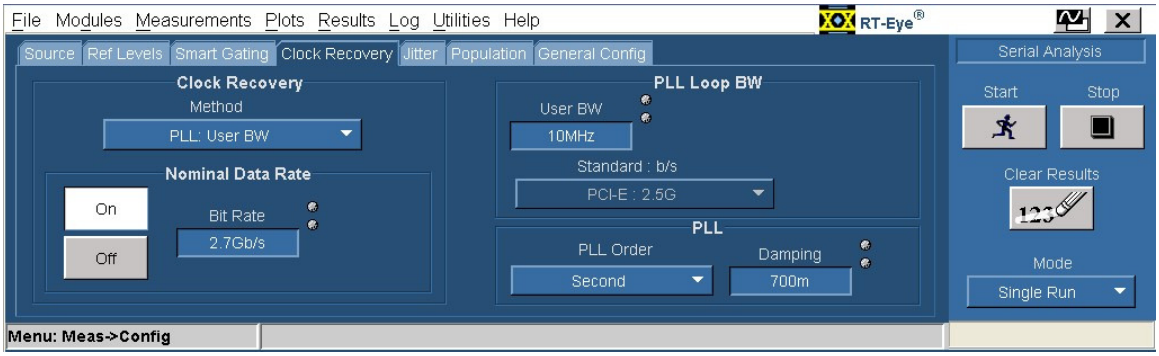


Figure: Configuring the clock recovery parameters for Eye Diagram measurement.

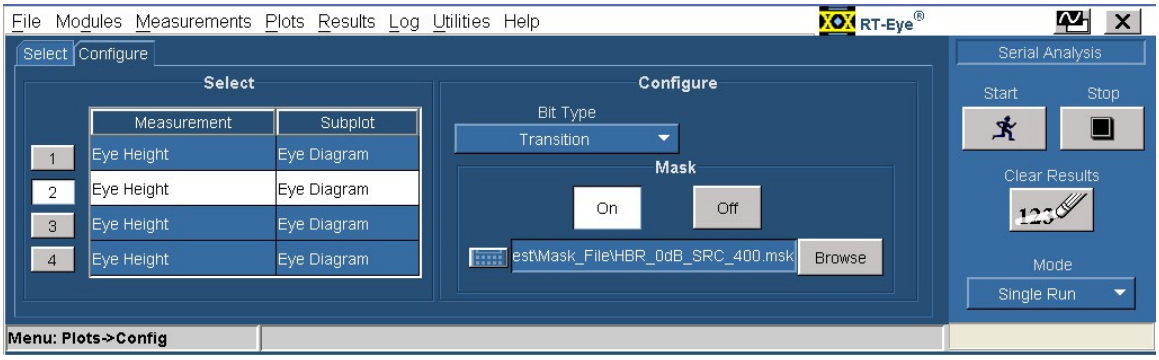


Figure: Configuring the plots and Eye diagram mask files for Eye Diagram measurement.

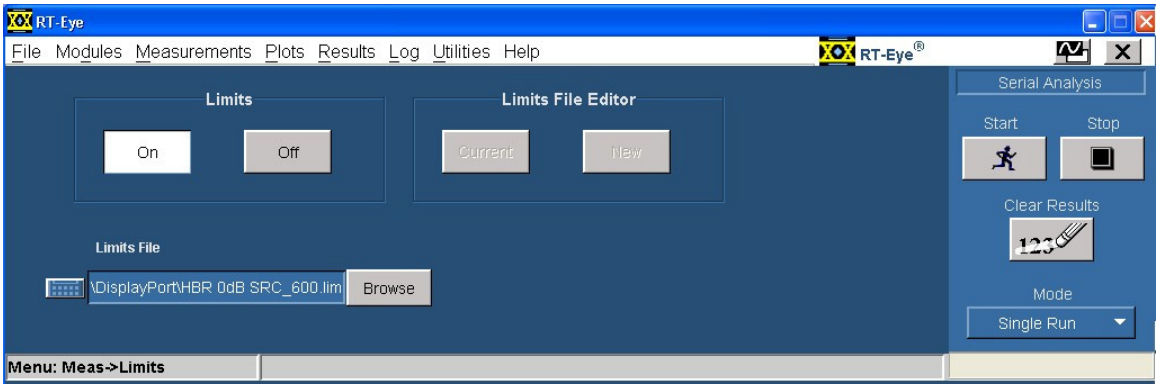


Figure: Configuring the limits for Eye Diagram measurement.

d. Click on start and Run the test.
e. Result will display the eye diagram with Mask and Pass/ Fail status.

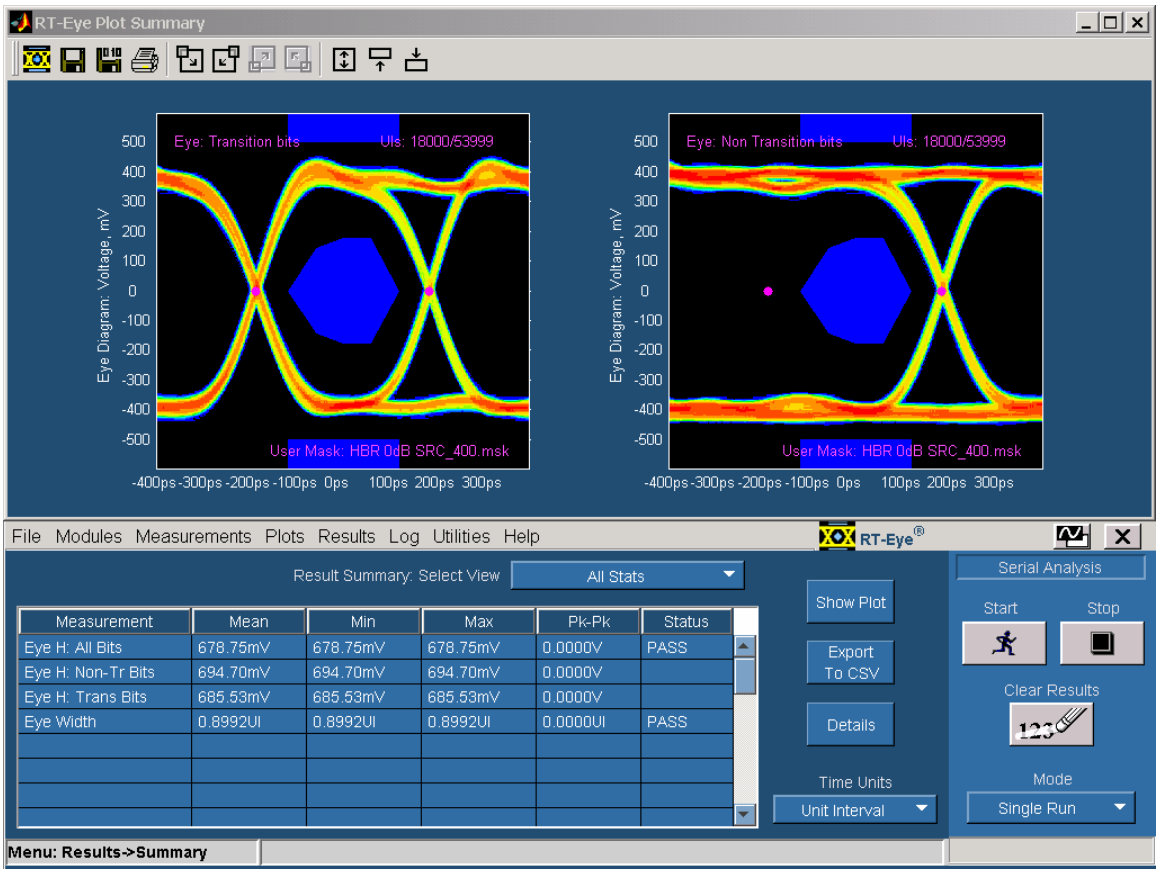


Figure: Eye Diagram measurement result with plots and pass/fail status.

f. If the signal of 400mV amplitude swing passes, then the device passes the compliance test- if not, repeat the test using a 600mV signal. If the 600mV signal passes, then the device passes - if not, repeat the test using an 800mV signal.

1.1.8 Pass/Fail Criteria

There can be no signal trajectories entering into the mask. As long as one or more differential voltage swing settings meet the eye mask specification, the source device is considered to be compliant. *(Reference: Errata draft 4 document, Sept 6, 2007)*

TEST 3.2 - Non Pre-Emphasis Level Verification Testing (Normative)

1.2.1 Test Objective

To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven. [Reference: Table 3.10 VESA Display Port Standard]

1.2.2 References

- Display Port specification version 1.1 dated 19-Mar-2007 and errata 3 document dated 29-Aug-2007 and errata 4 document dated 6-Sep-2007.
- Display Port CTS draft 13 version 1 specifications dated 20-Jul-2007, Section 3.2.

1.2.3 Test Conditions

Tests shall be made on all Bit Rates supported without Pre-Emphasis for all differential voltage swings supported.
Test Pattern: PRBS 7

1.2.4 Measurement Requirements

The following requirements shall be met for each level measurement:
Number of Edges measured >1000 (***Note:** Set the trigger to acquire the required portion of the waveform and then wait for scope to have > 1000 acquisitions)
Amplitude measurement will be performed using $V_N = MAX(V_H,V_L)$ where V_H and V_L have the following definitions:

- V_H is the Mode of the High or 'one' voltage over the last two UIs when three or more successive one's are transmitted.
- VL is the Mode of the Low or 'zero' voltage over the last two UIs when three or more successive 0's are transmitted.
  Note: Triggering is set in such a way that three consecutive 1's or 0's are captured in the acquisition for the measurement of voltage levels.

Voltage Peak-Peak = VH-VL

1.2.5 Test equipment required

Refer to Appendix A of this MOI. (****DSA/DPO 70804 with DPOJET analysis module and P7380SMA probe)

1.2.6 Connection Diagram

Refer to Appendix B of this MOI.

1.2.7 Detailed Test Procedure

a. Connect the respective channel of the Display port signal output to the scope CH1 using P7380SMA probe and Efficere Display Port Fixture.
b. Recall the setup <3.2_NonPreEmph_Level_HBR_VL_mea.set> or Do scope autoset and then do following setting:
   - Horizontal / Acquisition setup → Horizontal Tab: Mode = Automatic; Scope time base 400pS/div; Sampling Rate = 250GS/s
   - Horizontal / Acquisition setup → Acquisitions Tab: Sampling Mode = Equivalent; Acquisition mode = Sample

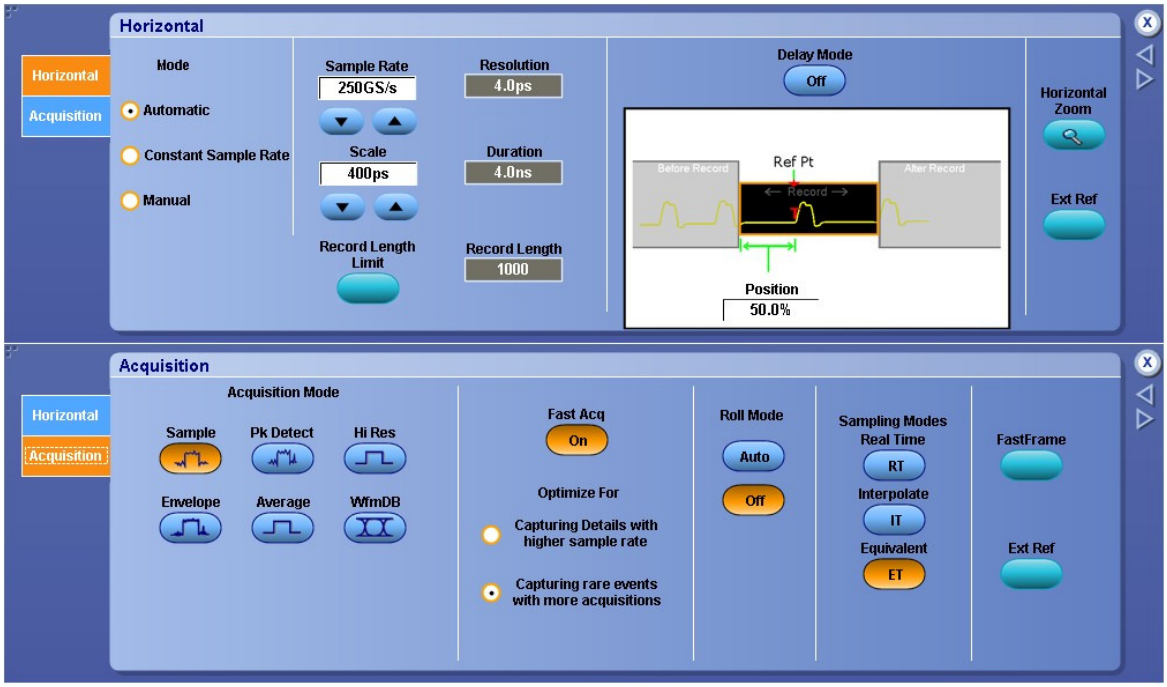


Figure: Scope horizontal and acquisition setting for V_H and V_L measurements.

   - Trigger setup → Trigger type = Timeout; Timer = 3UI period (1.11nS for HBR data, 1.875nS for RBR data) and 'Trigger When' = Stays low.

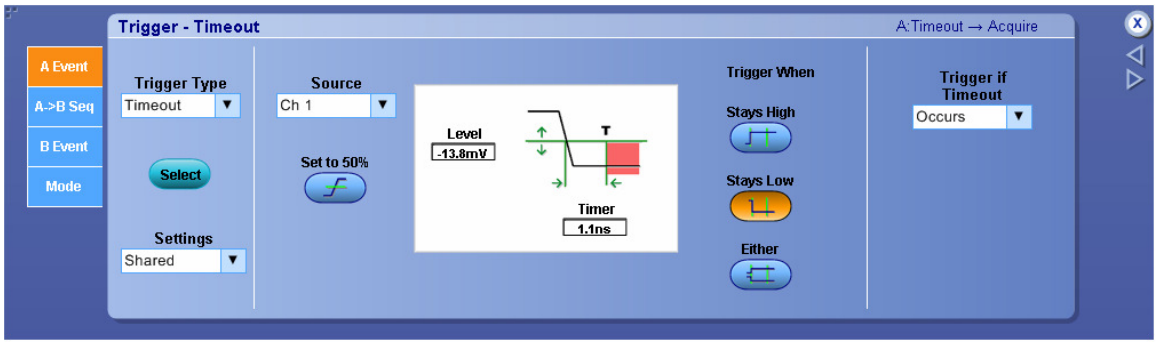


Figure: Scope trigger setting for V_H and V_L measurements.

c. Enable the DPO acquisition mode (FastAcq mode) and wait for > 1000 triggers completion

d. Enable the cursor gating and place the cursor-1 at approximately one unit interval after the falling edge as shown below (close to where the signal enters the 'low' or 'zero' level)
e. Place second cursor at around two UI (740ps) away from the first cursor.
f. Add the scope built in 'Low' measurement with cursor gating enabled to measure the signal level between the cursor gating and note down this as V_L.

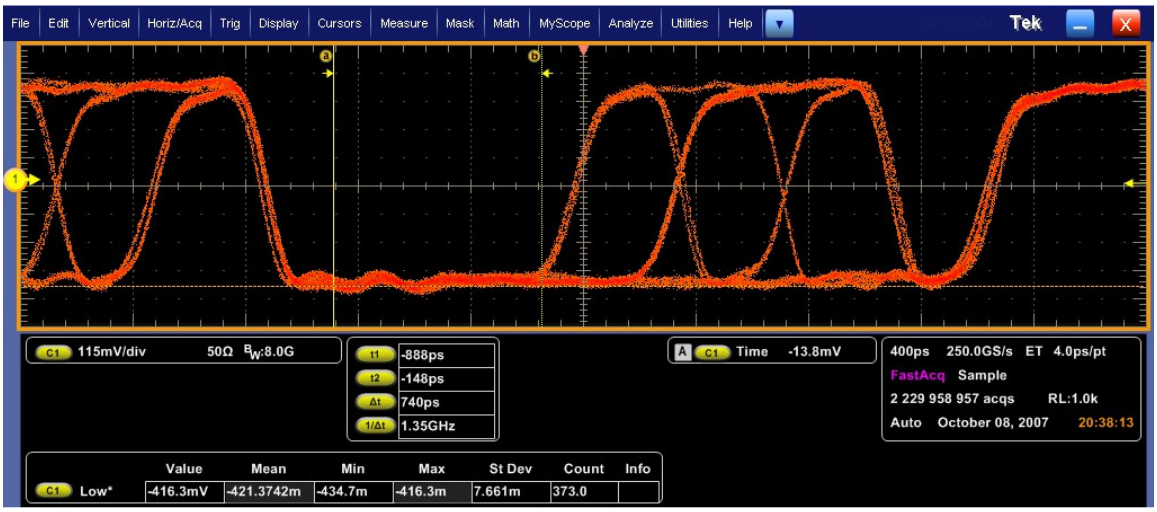


Figure: Screen showing measurement of V_L with cursor gating enabled

g. <u>MeasuringV_H:</u> Now recall the setup <3.2_NonPreEmph_Level_HBR_VH_mea.set> or change the 'Trigger when' to 'Stays high' in the trigger setup. Ensure that signal captured between the two cursors is now the 'high' or 'one' level.
h. Now note down the 'High' measurement value as V_H.

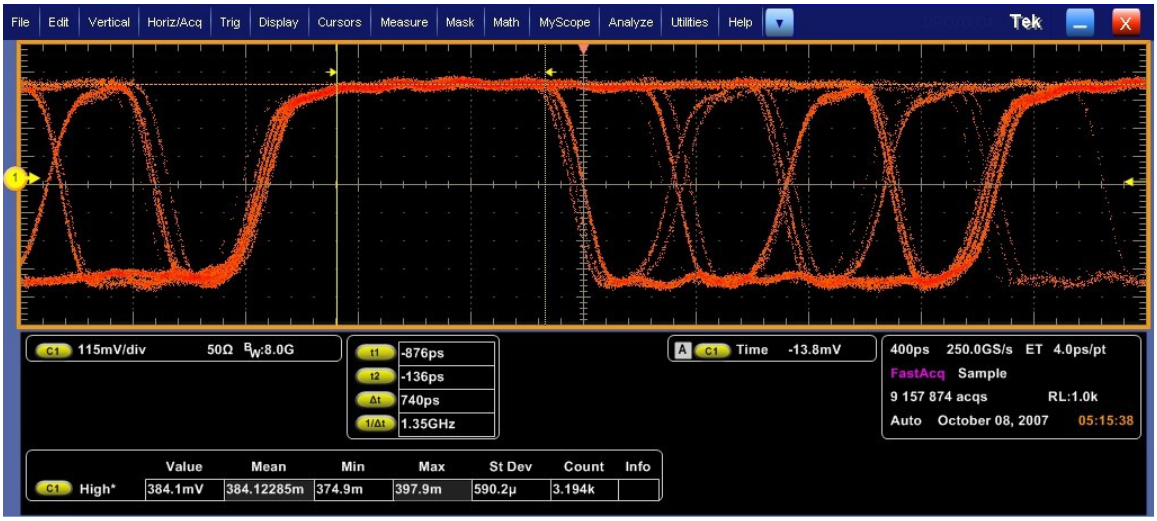


Figure: Screen showing measurement of V_H with cursor gating enabled

i. Find the difference V_H-V_L. With the screenshots shown here V_H = 384.1mV and V_L = -411.7mV and the difference V_H-V_L = 795.8mV peak-to-peak (or 0.7958V).

1.2.8 Pass/Fail Criteria

Voltage Peak to Peak will fall in the range:

Output Level 1: 0.34≤ Result ≤0.46
Output Level 2: 0.51≤ Result ≤0.68
Output Level 3: 0.69≤ Result ≤0.92
Output Level 4: 1.02≤ Result ≤1.38

Nominal Setting is 400, 600, 800 and 1200mVolts peak-peak

3.3 Pre-Emphasis Level Verification Testing (Normative)

1.3.1 Test Objective

This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting. [Reference: Table3.10 VESA Display Port Standard]

1.3.2 References

- Display Port Specification version 1.1 dated 19-Mar-2007 and errata 3 document dated 29-Aug-2007 and errata 4 document dated 6-Sep-2007.
- Display Port CTS draft 13 version 1 specifications dated 20-Jul-2007, section 3.3.

1.3.3 Test Conditions

Tests shall be made on all Bit Rates supported with Pre-Emphasis for all differential voltage swings supported.
Test Pattern=PRBS 7

1.3.4 Measurement Requirements

The following requirements shall be met for each level measurement:
Number of Edges measured >1,000 (**Note:** Set the trigger to acquire the required portion of the waveform and then wait for scope to have > 1000 acquisitions).

V_{swing} measurements shall be taken using an average of a histogram of level ($V_{swing} = V_{top} - V_{base}$). The Histogram will window the 45% to 55% locations of the analyzed bit (**Note:** Histogram based 'mean' measurements will be enabled with waveform histogram box spanning over 45% to 55% of the analyzed bit UI). The analyzed bit is defined as:

- For transition bits, the analyzed bit is over the first bit interval past a transition (**Note:** From transition put the cursors on 1st bit UI).
- For non transition bits the analyzed bit is the third bit interval past a transition (**Note:** From transition put the cursors on 3rd bit UI).

At every voltage setting and pre-emphasis setting subject to constraints in Table 3-12 of the Display Port Standard, the following measurement sequence shall be followed:

1. Set DUT with no pre-emphasis (0dB)
   a. Measure the transition bit voltage swing, rail-to-rail: Vswing_transition_0dB
   b. Measure the non-transition bit voltage swing (third bit of consecutive 0's or 1's):Vswing_nontransition_0dB
   c. RATIO_0dB = Vswing_transition_0dB/Vswing_nontransition_0dB
2. Set DUT with pre-emphasis (PE dB=3.5, 6, or 9.5 dB)
   a. Measure the transition bit voltage swing, rail-to-rail: Vswing_transition_PEdB
   b. Measure the non-transition bit voltage swing (third bit of consecutive 0's or 1's): Vswing_nontransition_PEdB

c. RATIO_PEdB = Vswing_transition_PRdB / Vswing_nontransition_PEdB
3. Calculate Pre-Emphasis Ratio = RATIO_PEdB / RATIO_0dB.

1.3.5 Test equipment required

Refer to Appendix A of this MOI. (**DSA/DPO 70804 with DPOJET analysis module and P7380SMA probe)

1.3.6 Connection Diagram

Refer to Appendix B of this MOI.

1.3.7 Detailed Procedure

a. Connect the respective channel of the Display port signal output to the scope CH1 using P7380SMA probe and Efficere Display Port Fixture. The signal has **no** pre-emphasis.
b. Do the steps mentioned in 1.2.7a to 1.2.7c (Procedure for test 3.2 – Non Pre-Emphasis level verification test) using setup files <3.3_Pre-Emph_Level_Vh_measSetup.set> & <3.3_Pre-Emph_Level_VL_measSetup.set> for measuring V_H and V_L and hence the voltage swing.
c. Recall the specified setup files or do following scope setting manually:
    - Horizontal / Acquisition setup → Horizontal Tab: Mode = Automatic; Scope time base 200pS/div; Sampling Rate = 500GS/s
    - Horizontal / Acquisition setup → Acquisitions Tab: Sampling Mode = Equivalent (ET); Acquisition mode = Sample
    - Trigger setup → Trigger type = Timeout; Timer = 3UI period (1.11nS for HBR data, 1.875nS for RBR data) and 'Trigger When' = Stays low (for V_L and Stays High for V_H measurement).

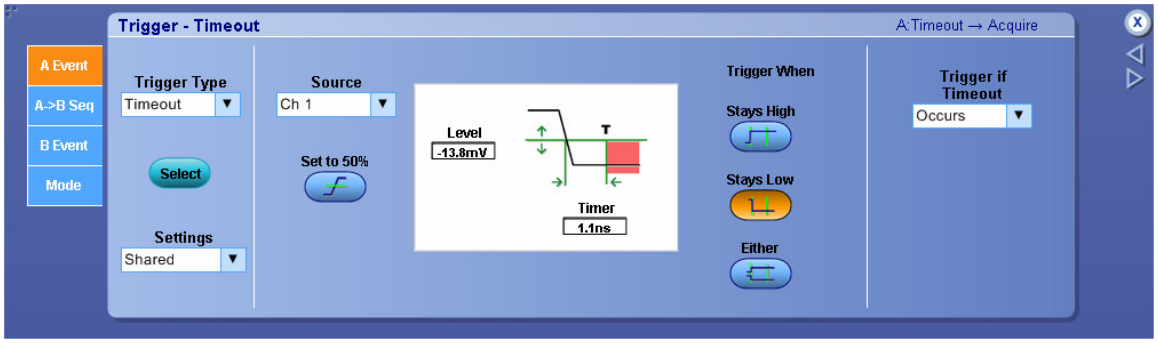


Figure: Scope trigger setting to measure V_L for transition and non-transition bit.

d. Enable the DPO acquisition mode (FastAcq mode) and wait for > 1000 triggers completion
e. Measure → Waveform Histogram → Waveform histogram setup window: Define the histogram box span (45% - 55% of the UI) over analyzed bit. Add Histogram Mean by navigating through Measure → Histogram Measurements → Mean.

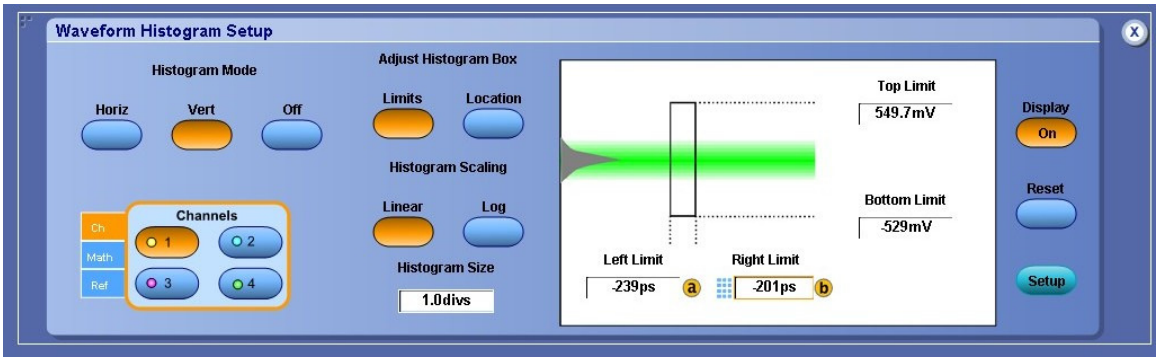


Figure: Waveform histogram setting to measure V_H and V_L for transition and non-transition bit.

f. Define the histogram box left and right limit corresponding to 45% and 55% respectively of 1st bit UI just after the transition. Note down the 'Hs Mean*' measurement as V_L of Transition bit.

Figure: Measurement of V_L for Transition bit.

g. Now shift the histogram box on the 3rd bit UI from the transition maintaining the same box width i.e., left limit is at 245% of UI and right limit is at 255% of UI from the transition. The 'Hs Mean*' measurement reading this time will give V_L for non-transition bit.

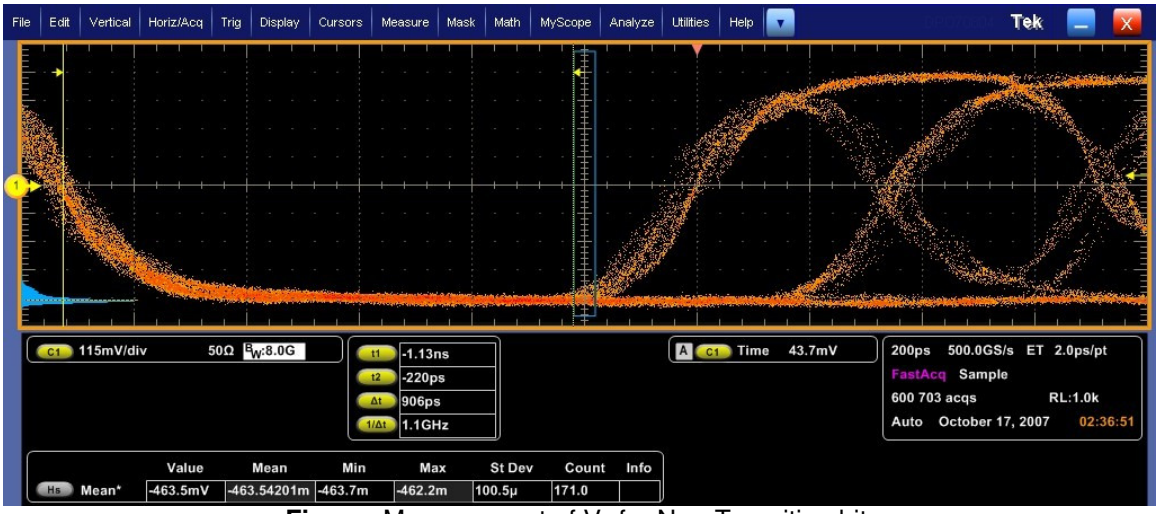


Figure: Measurement of V_L for Non-Transition bit.

h. Now change the trigger setting to capture three consecutive 1's by making the parameter 'Trigger when' as 'Stays high'.

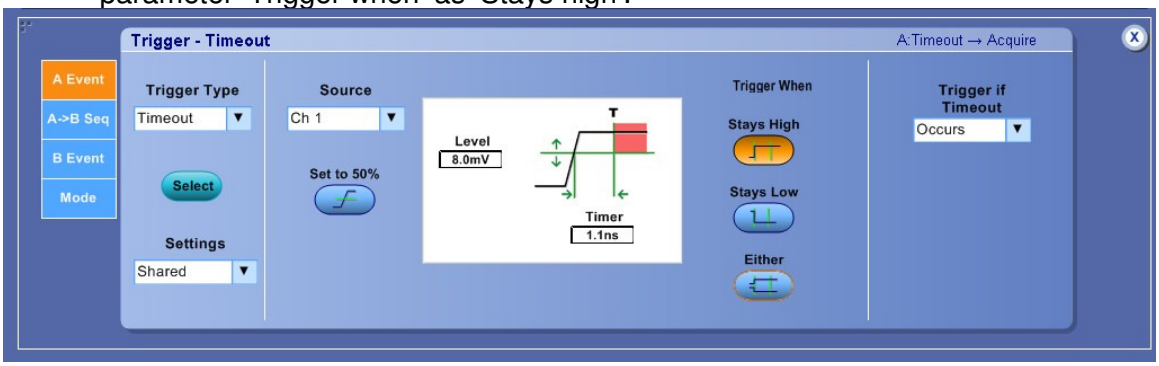


Figure: Screen showing trigger setting for measurement of V_H for transition and non-transition bit.

i. Place histogram box as described in step (f) and (g) to measure V_H for transition and non-transition bits respectively.

Figure: Measurement of V_H for Transition bit.

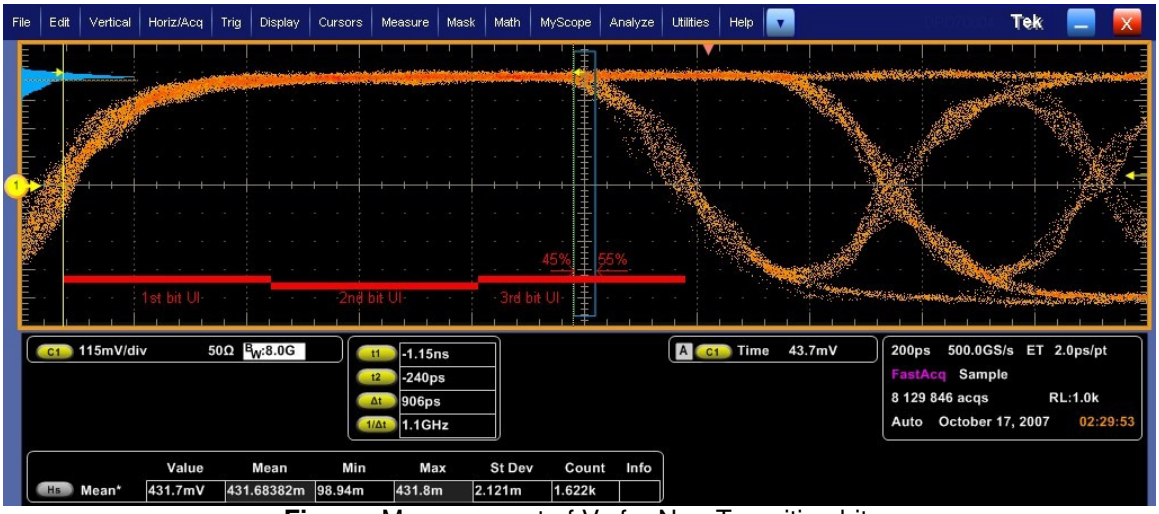


Figure: Measurement of V_H for Non-Transition bit.

j. Calculate the voltage swing ratio for signal without pre-emphasis
   - Vswing_transition_0dB = $V_H - V_L$ (for transition bits)
   - Vswing_nontransition_0dB = $V_H - V_L$ (for Non-transition bits)
   - RATIO_0dB = Vswing_transition_0dB/Vswing_nontransition_0dB

k. Now feed signal with pre-emphasis and repeat the similar exercise, from step (a) to (j), to calculate voltage swing ratio for signal with Pre-Emphasis.
   RATIO_PEdB = Vswing_transition_PRdB / Vswing_nontransition_PEdB

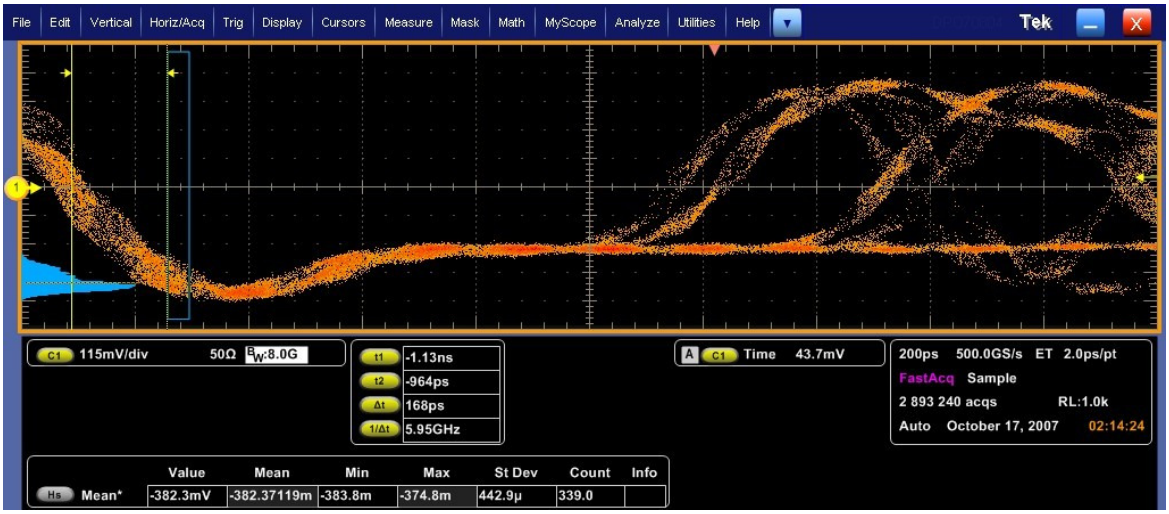


Figure: Measurement of V_L for Transition bit of signal with pre-emphasis.

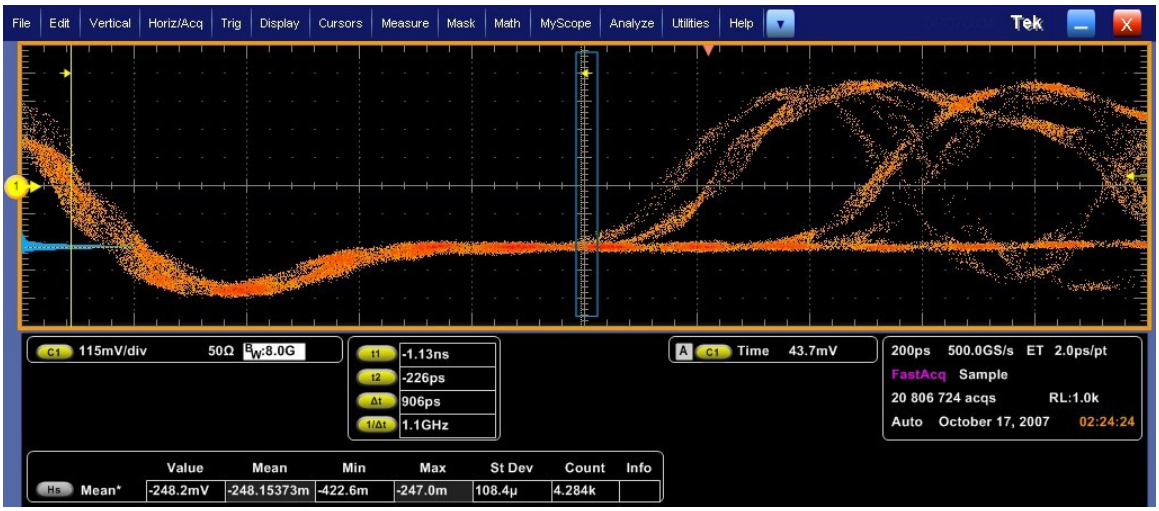


Figure: Measurement of V_L for Non-Transition bit of signal with pre-emphasis.

Figure: Measurement of V_H for Transition bit of signal with pre-emphasis.

Figure: Measurement of V_H for Non-Transition bit of signal with pre-emphasis.

l. Finally calculate the Pre-Emphasis ratio = RATIO_PEdB / RATIO_0dB

1.3.8 Pass/Fail Criteria

1. Pre-Emphasis Calculation shall meet the following range for the appropriate levels [Reference Table 3-10]:

For 3.5 dB setting: 1.2 ≤ Pre-Emphasis Ratio ≤ 1.8
For 6.0 dB setting: 1.6 ≤ Pre-Emphasis Ratio ≤ 2.4
For 9.5 dB setting: 2.4 ≤ Pre-Emphasis Ratio ≤ 3.6

2. The values of pre-emphasis must monotonically increase as pre-emphasis setting is increased. Specifically, pre-emphasis values of 1.6 to 1.8 are valid for either the 3.5 dB setting or the 6 dB setting but **NOT** both.

3.4 Inter-Pair Skew Test (Normative)

1.4.1 Test Objective

To evaluate the skew, or time delay, between respective differential data lanes in the Display Port interface. [Reference Table 3.10 VESA Display Port Standard]

1.4.2 References

- Display Port specification version 1.1 dated 19-Mar-2007 and errata 3 document dated 29-Aug-2007 and errata 4 document dated 6-Sep-2007.
- Display Port CTS draft 13 version 1 specifications dated 20-Jul-2007, Section 3.4

1.4.3 Test Conditions

Tests shall be made on highest Bit Rate supported without Pre-Emphasis for 400mV differential voltage swing.
Test Pattern: PRBS 7
Sources with 2 and 4 lane operation only (Each combination applicable).

1.4.4 Measurement Requirements

The following requirements shall be met for the inter-skew measurement:
De-skewed measurement channels
Number of Edges measured: 100
Waveform maximized on screen: More than half vertical screen used, Horizontal covers ~ 8 UI
Capture waveforms on two lanes simultaneously on two measurement channels.
Search both waveforms for common point in PRBS 7 sequence and measure time difference between the corresponding edges. Find the time of transition by determining when the waveform crosses the transition amplitude.
For each signal, find V_H and V_L using similar method as prescribed in section 3.1.4.
$V_{Transition} = \{V_H + V_L\} / 2$
Inter-Lane Skew = $\{1/NumEdges\} * \Sigma [T_{Transition\_LaneA} - T_{Transition\_LaneB}]$
Note: Basically find inter-lane skew for one acquisition and then average it over number of acquisitions.

1.4.5 Test equipment required

Refer to Appendix A of this MOI.

1.4.6 Connection Diagram

Refer to Appendix B of this MOI.

1.4.7 Detailed procedure (See note after the detailed procedure)

a. Deskew the scope channels.
b. Connect the two differential signals under test to the 2 scope channels using two P7380SMA probes.
c. Repeat the steps mentioned in 1.2.7(a) to 1.2.7(i) of this MOI to determine V_H and V_L of the signal. Average of these levels i.e., $V_{Transition} = (V_H + V_L)/2$ will be used as reference data level in the trigger setting.
d. Do scope autoset and set the vertical scale to ensure the waveform covers more than half the screen. Set the horizontal scale to capture 8UI of the signals (horizontal time base = 400pS/div, Sampling rate = 25GS/s, RL =1k).
e. Set the trigger on Ch1→ Trigger type = Serial, Bit Rate = 2.7Gbps, Trigger on pattern = 01111001, Data level = $V_{Transition}$ (mid of V_H and V_L).

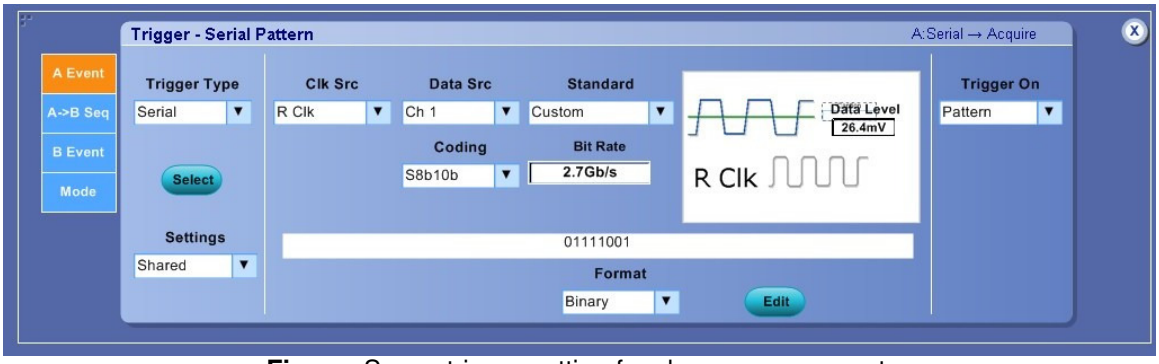


Figure: Scope trigger setting for skew measurement.

f. Locate the same pattern on second channel. Measure the time difference between transitions on two channels using cursors.

Figure: Skew measurement using cursors by triggering on specific pattern.

g. The cursor delta will give the skew between the two measured lanes.

1.4.8 Pass/Fail Criteria

-2UI ≤ Inter-Lane Skew – Nominal Skew setting ≤ 2UI.
i.e., for HBR signal: -740pS ≤ Inter-Lane Skew – Nominal Skew setting ≤ 740pS
And for RBR signal: -1234pS ≤ Inter-Lane Skew – Nominal Skew setting ≤ 1234pS

The Display Port Standard prescribes 20UI (7.4nS for HBR and 12.34nS for RBR) offset from Lane 0 to Lane 1, Lane 1 to Lane 2 and from Lane 2 to Lane 3. Between Lane 0 and Lane 2, the Nominal Skew setting will be 40UI (14.8nS for HBR and 24.68nS for RBR Signal).

3.5 Intra-Pair Skew Test (Normative)

1.5.1 Test Objective

To evaluate the skew, or time delay, between respective sides of a differential data lane in a Display Port interface. [Reference Table 3.10 VESA Display Port Standard]

1.5.2 References

- Display Port specification version 1.1 dated 19-Mar-2007 and errata 3 document dated 29-Aug-2007 and errata 4 document dated 6-Sep-2007.
- Display Port CTS draft 13 version 1 specifications dated 20-Jul-2007, Section 3.5

1.5.3 Test Conditions

Tests shall be made on highest Bit Rate supported without Pre-Emphasis for 400mV differential voltage swing.
Source / Test Pattern: PRBS 7
Applies to 1, 2 and 4 lane operation (All functional lanes to be tested).
Intra-pair measurement implies two single ended probed points on a given differential data lane.

1.5.4 Measurement Requirements

The following requirements shall be met for the intra-skew measurement:
De-skew the measurement channels
Number of edges measured: Num_Edges = 100
Waveform maximized on screen: More than half vertical screen used, Horizontal covers at least two UI for good transition identification.
Capture signals on two lanes simultaneously on two single ended measurement channels. Find falling edges of one channel that is aligned with corresponding rising edges of signal on other channel. Find the time of transition by determining when the waveform crosses the transition amplitude.
For each lane composed of 2 single ended signals D+ and D-, find V_H and V_L using similar method as prescribed in section 3.1.4.
Keep $V_{Transition}$= 0 volts
Intra-Lane Skew = {1/NumEdges} * Σ [D+Transition_High - D-Transition_Low]

1.5.5 Test equipment required

Refer to Appendix A of this MOI. (**DSA/DPO 70804 with DPOJET analysis module)

1.5.6 Connection Diagram

Refer to Appendix B of this MOI – NO PROBE USED FOR THIS TEST.

1.5.7 Detailed Procedure

a. Deskew the scope channels.
b. Connect the two single-ended signals of a lane under test to scope channels CH1 and CH2 using matched cable pair.
c. Do Auto set and Set the vertical scale to ensure the waveform covers more than half the screen. Set the horizontal scale to capture 2UI of the signals (Horizontal time base = 100pS/div for HBR signal).
d. Set the trigger type to edge trigger.

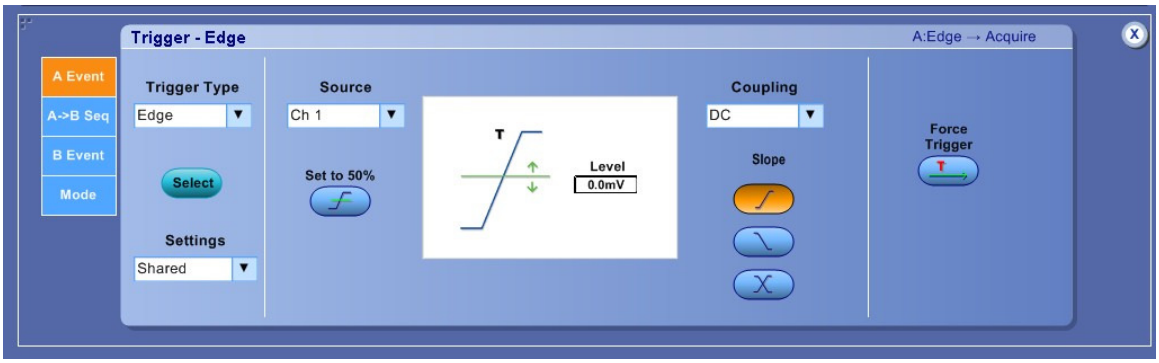


Figure: Trigger setting for intra-pair skew measurement.

e. Go to measurement menu, select time tab and then configure delay measurement. Select setup in delay measurement and configure source1 as lane A+ (Ch1) and source 2 as lane A- (Ch2). Configure ref level as 50%, Delay Edge1 = rise time and Delay Edge2 = fall time.

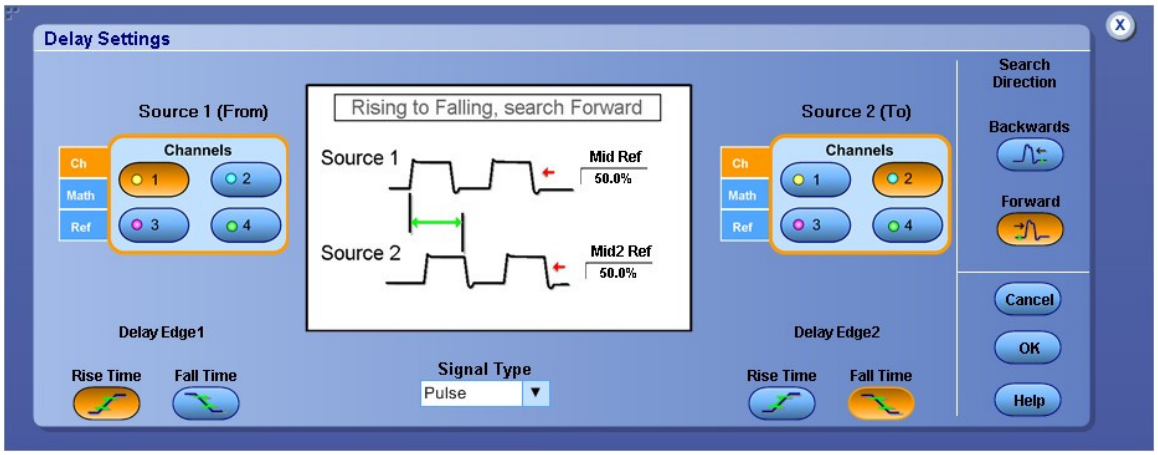


Figure: Delay measurement setting for intra-pair skew measurement.

f. Right click on the delay measurement result in the grid area to select statistics under delay measurement menu and configure weight factor (n=) as 100 edges.
g. Take the averaged delay value after 100 edges as the intra-pair skew value. For the example shown, the skew is 27.1pS.

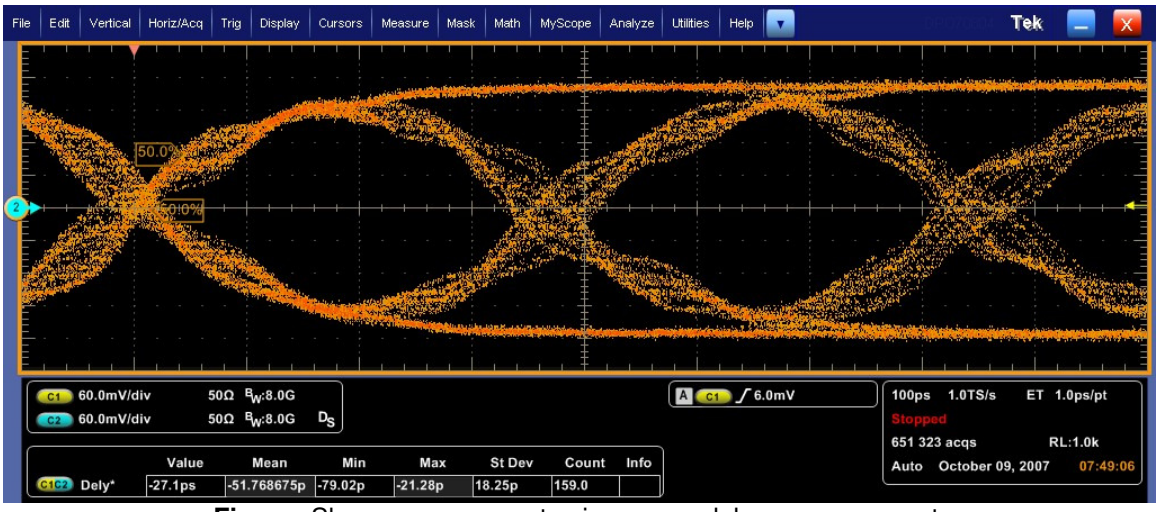


Figure: Skew measurement using scope delay measurement.

1.5.8 Pass/Fail Criteria

Intra-Lane Skew ≤ 30 ps.

3.6 Differential Transition Time Test (Informative)

- Informative test, not included in this version.

3.7 Single Ended Rise & Fall Time Mismatch Test (Informative)

- Informative test, not included in this version.

3.8 Overshoot and Undershoot Test (Informative)

- Informative test, not included in this version.

3.9 Frequency Accuracy (Normative)

1.9.1 Test Objective

To evaluate that the clock distribution network of the source device conform to within an acceptable tolerance of the nominal operating frequency. [Reference Table 3.10 VESA Display Port Standard]

1.9.2 References

- Display Port Specification version 1.1 dated March 19 2007 and errata 3 document dated 29th Aug 2007 and errata 4 document dated Sept 6 2007.
- Display Port CTS draft 13 version 1 specifications dated July 20 2007 Section 3.9.

1.9.3 Test Conditions

Tests shall be made on all Bit Rates supported.
Transmitter set to 0dB pre-emphasis and differential swing to 1.2V
Test Pattern=D10.2

1.9.4 Measurement Requirements

The following requirements must be met for each frequency measurement:
Minimum Acquisition Time: 33usec

1.9.5 Test equipment required

Refer to Appendix A of this MOI.

1.9.6 Connection Diagram

Refer to Appendix B of this MOI.

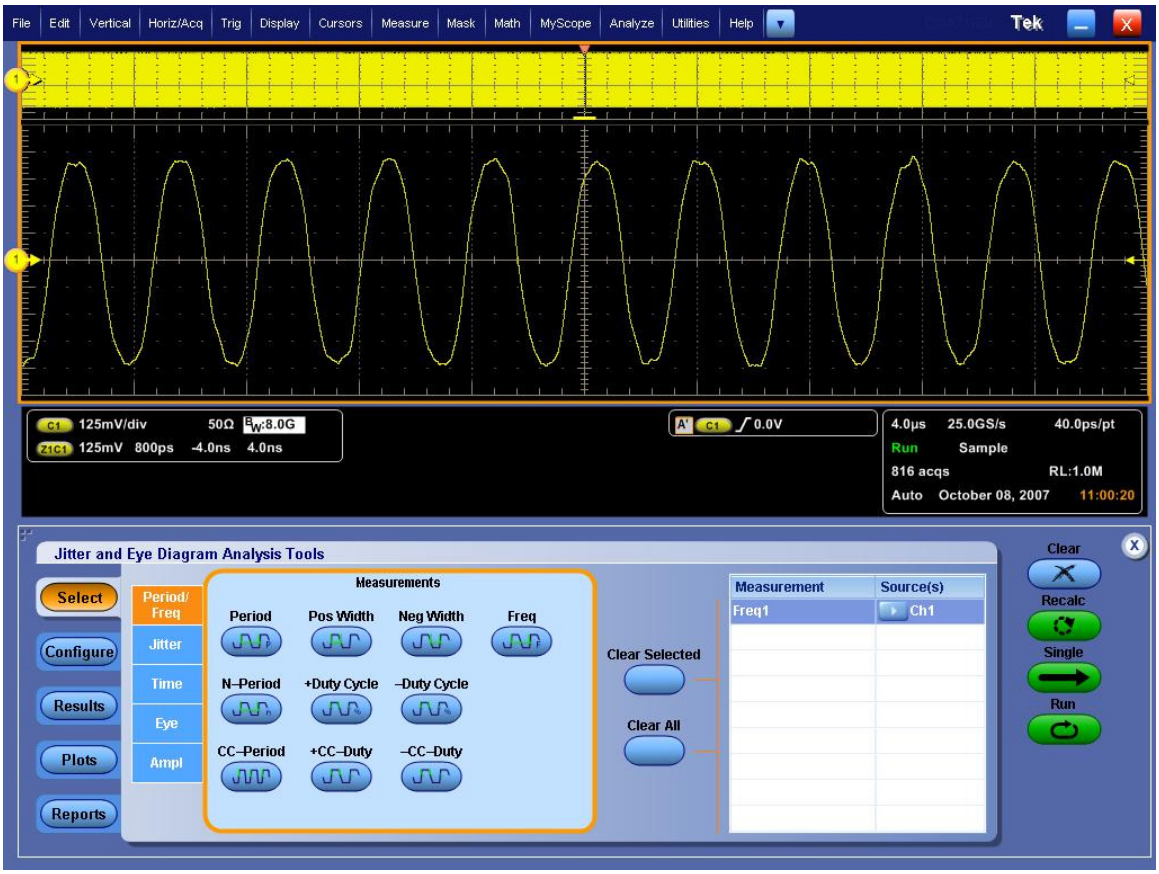
1.9.7 Detailed Procedure

Using DPOJET:

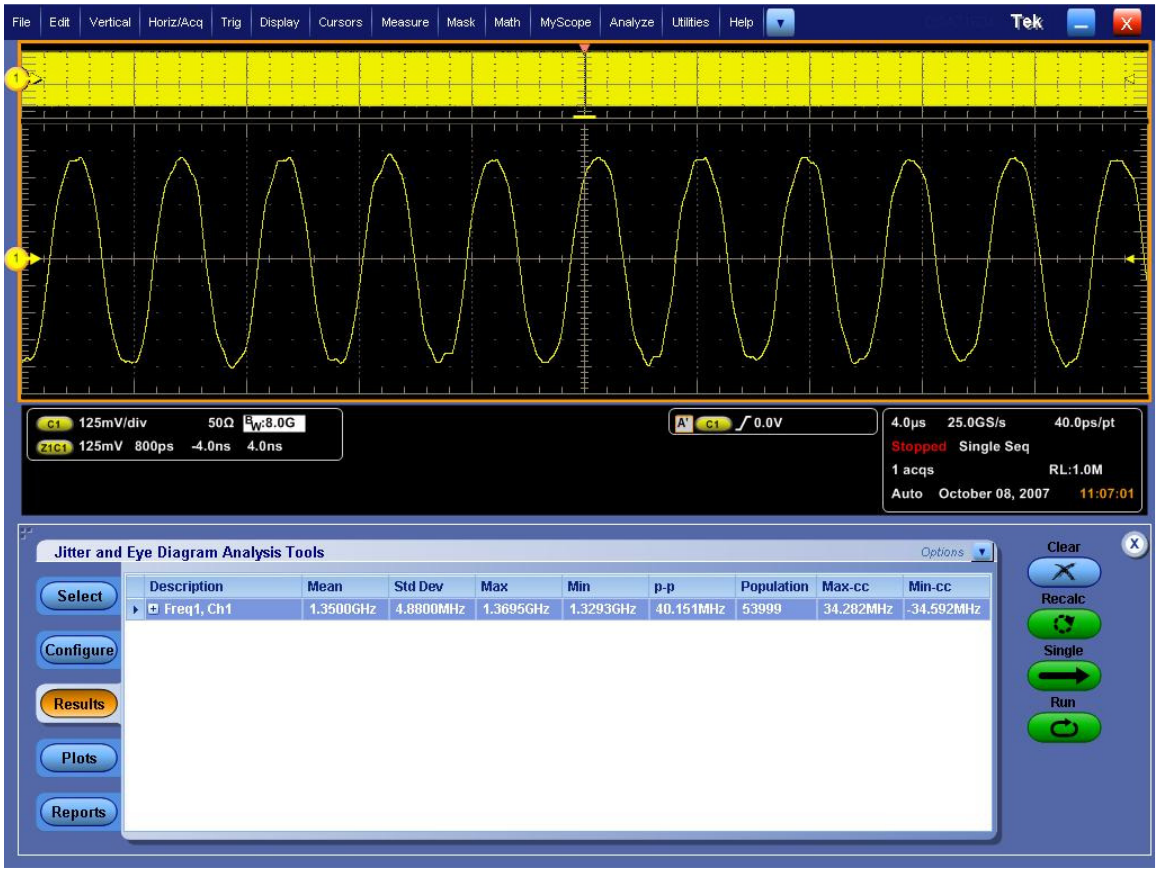
In the scope recall the setup 'Frequency Accuracy'<3.9_Frequency_Accuracy.set and open the DPOJET application in Analyze → DPOJET → Select

Scope setup: 4µs/div, 40ps/pt (40µs acquisition time)

Select Measurement: Data Period on Math1 = Ch1-Ch3 or Ch1 (SMA probe)

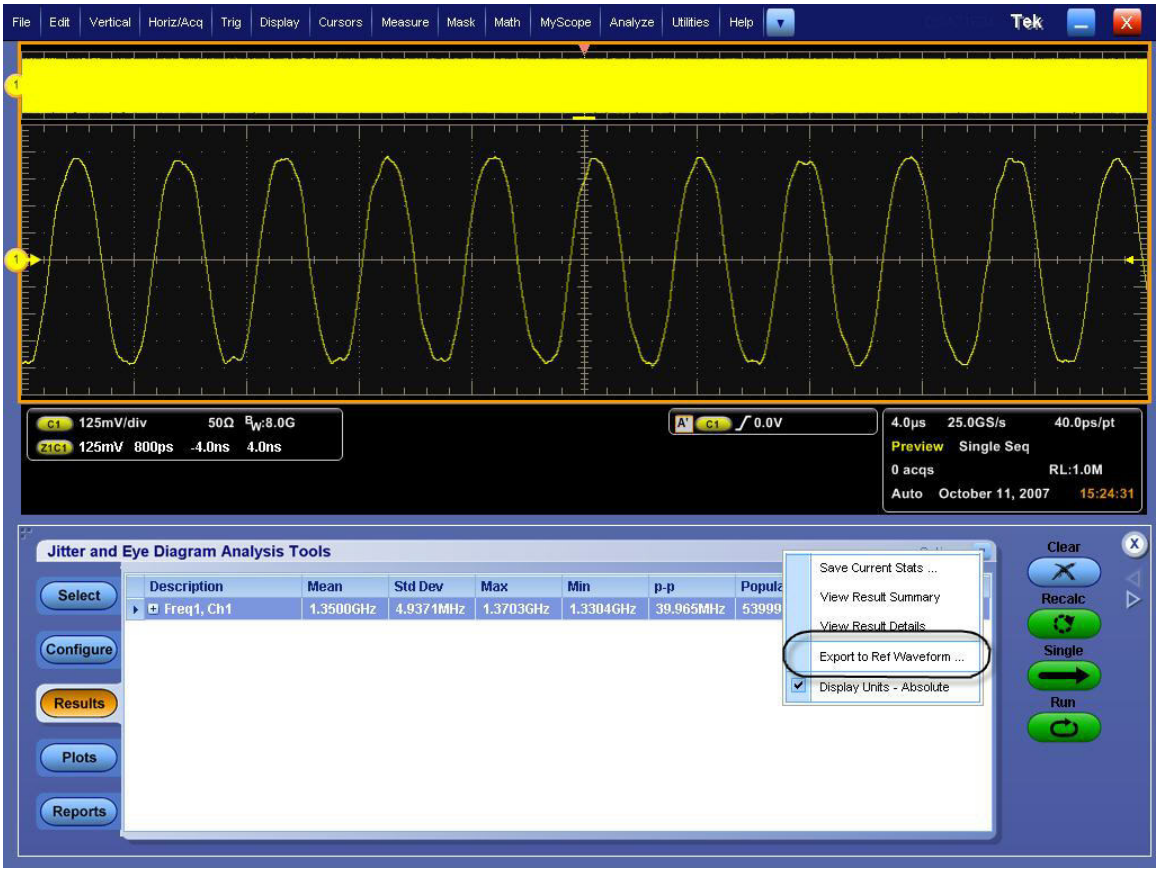

File
Edit
Vertical
Horiz/Acq
Trig
Display
Cursors
Measure
Mask
Math
MyScope
Analyze
Utilities
Help
Tek
C1 125mV/div 50Ω BW:8.0G
Z1C1 125mV 800ps -4.0ns 4.0ns
A C1 0.0V
4.0µs 25.0GS/s 40.0ps/pt
Run Sample
816 acqs RL:1.0M
Auto October 08, 2007 11:00:20
Jitter and Eye Diagram Analysis Tools
Select
Configure
Results
Plots
Reports
Period/ Freq
Jitter
Time
Eye
Ampl
Measurements
Period
Pos Width
Neg Width
Freq
N–Period
+Duty Cycle
–Duty Cycle
CC–Period
+CC–Duty
–CC–Duty
Clear Selected
Clear All
Measurement
Source(s)
Freq1
Ch1
Clear
Recalc
Single
Run

Click on Single to run the application. When complete, the statistics table will contain the results.

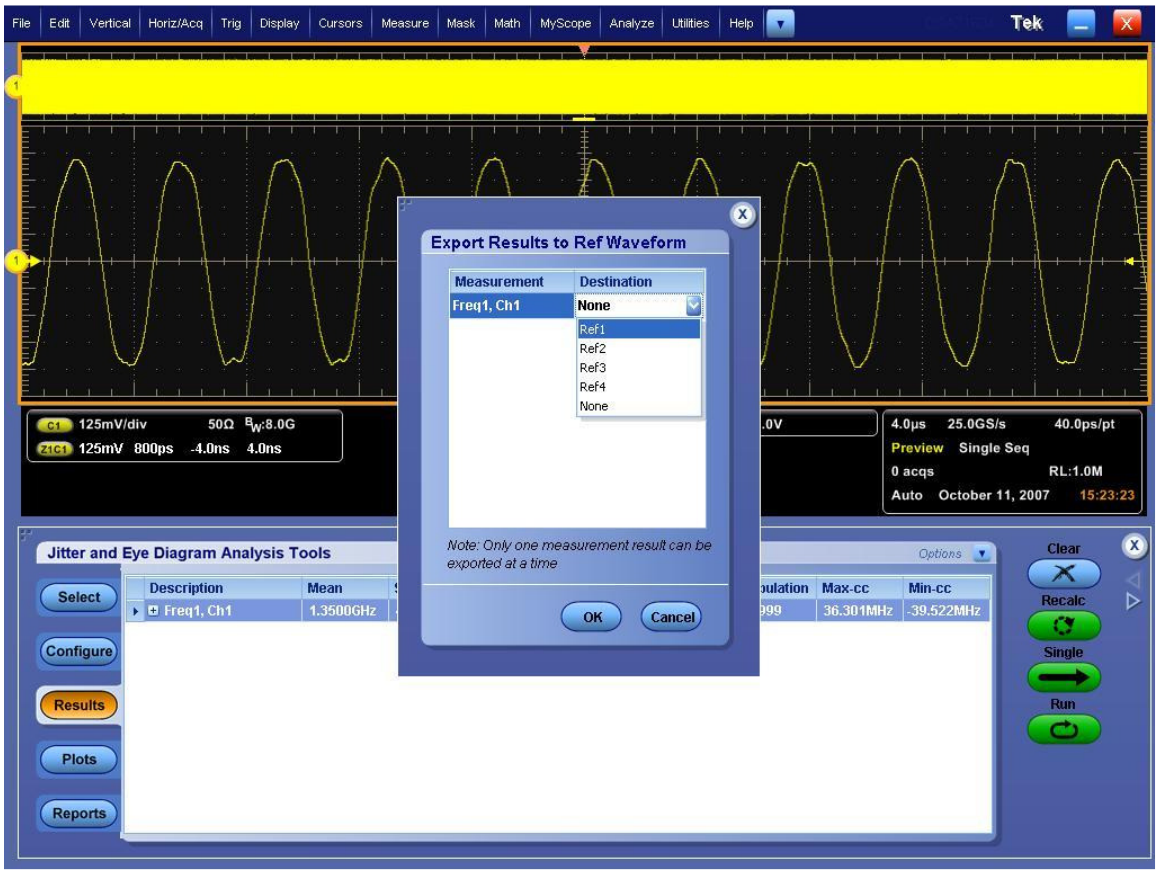


Note that this measurement is rounded up from an internal representation of 9 digits. For measurements that are near the limit, it is possible to use the following procedure to view additional resolution on the measurement.

Select “Export to Ref Waveform” in the Options menu



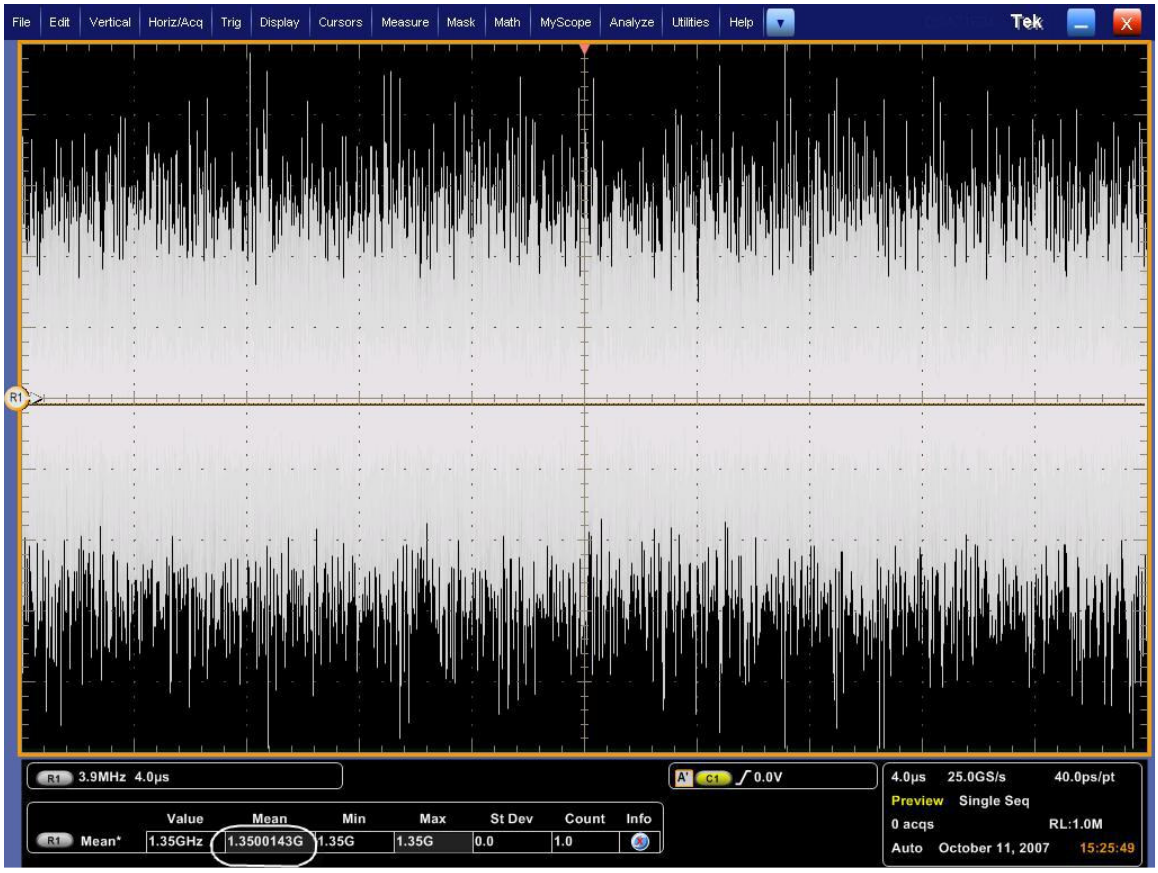
Select Ref1 as the Destination. This transfers the Period profile into the scope's Ref waveform memory.



Once the reference waveform is transferred into the scope's storage, minimize the DPOJET screen so that only the scope UI is displayed.

Enable Mean amplitude measurement. Despite the fact that these are called amplitude measurements, in this case the measurements will be showing mean frequency.

Read the value of the current acquisition (ref waveform) following the µ: symbol.



Using TDSJIT3:

Start the JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 recall the setup <3.9_Frequency_Accuracy.set>.

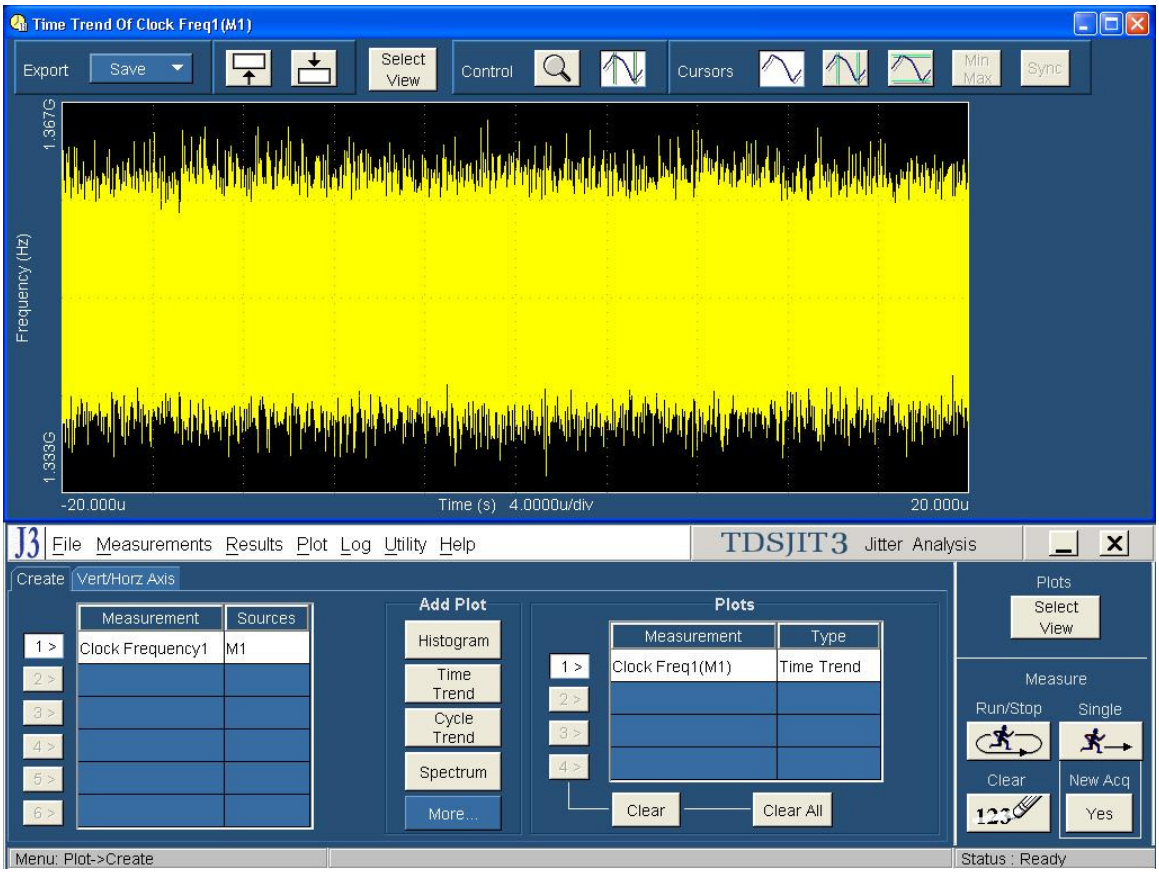
Scope setup: 4µs/div, 40ps/pt

Select Measurement: Data Period on Math1 = Ch1-Ch3 or Ch1 (SMA probe)

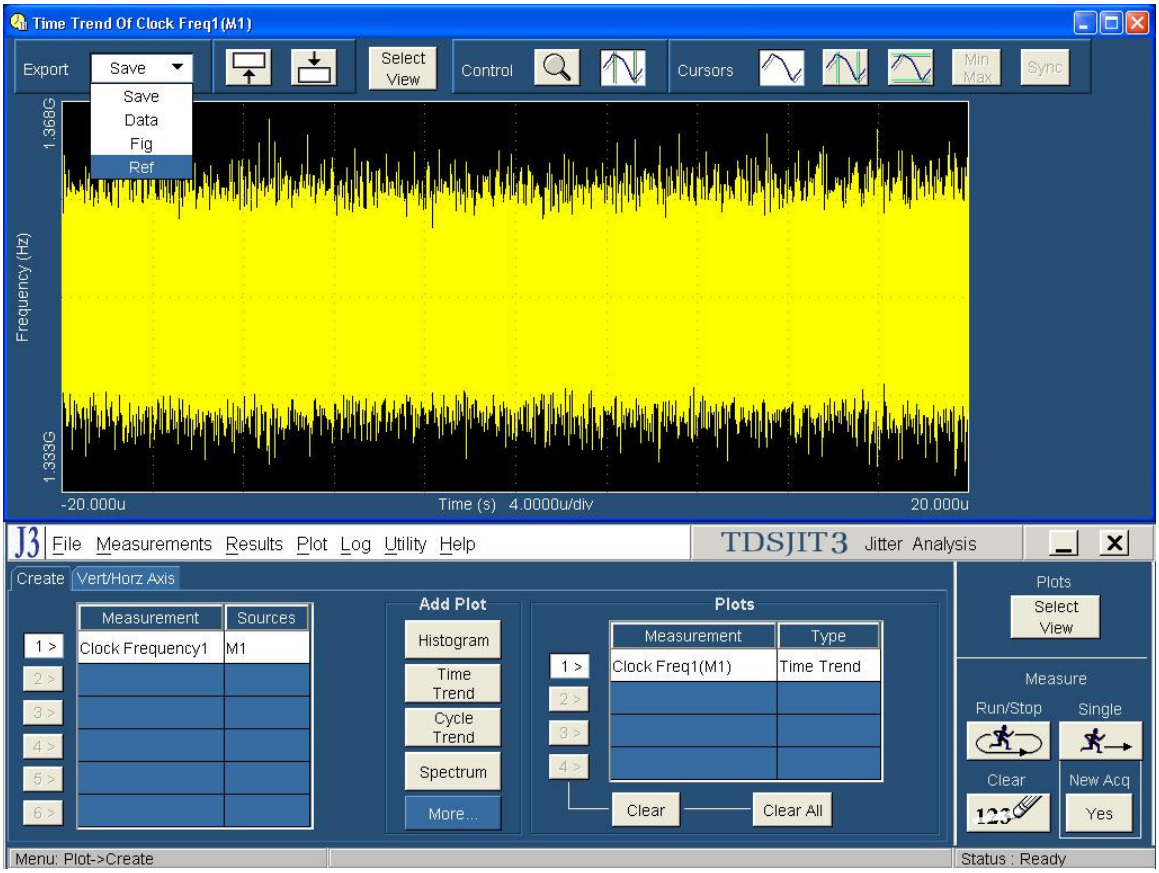
Click on Single to run the application. When complete, the statistics table will contain the results.

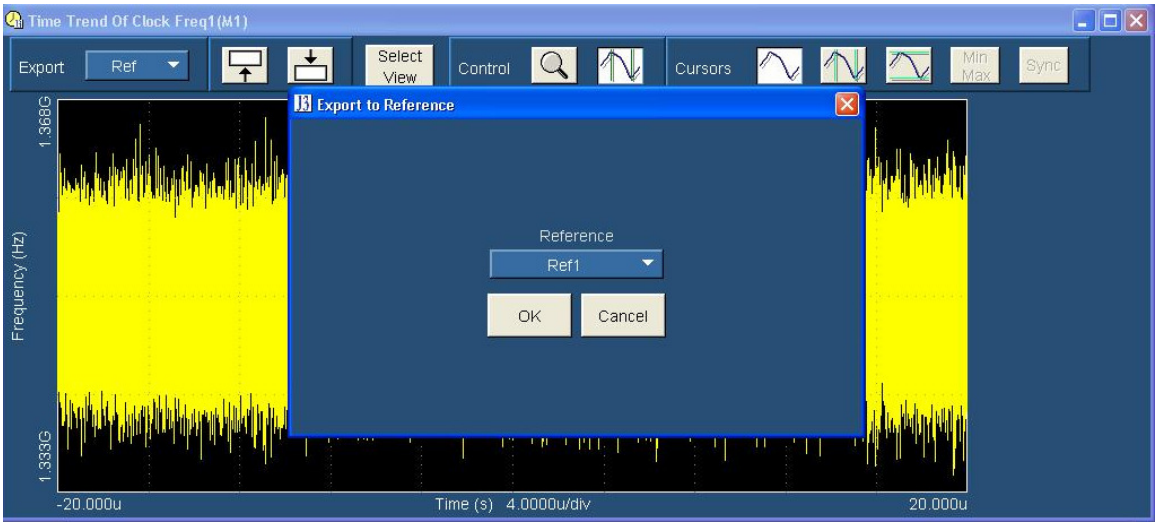
Note that this measurement is rounded up from an internal representation of 9 digits. For measurements that are near the limit, it is possible to use the following procedure to view additional resolution on the measurement.

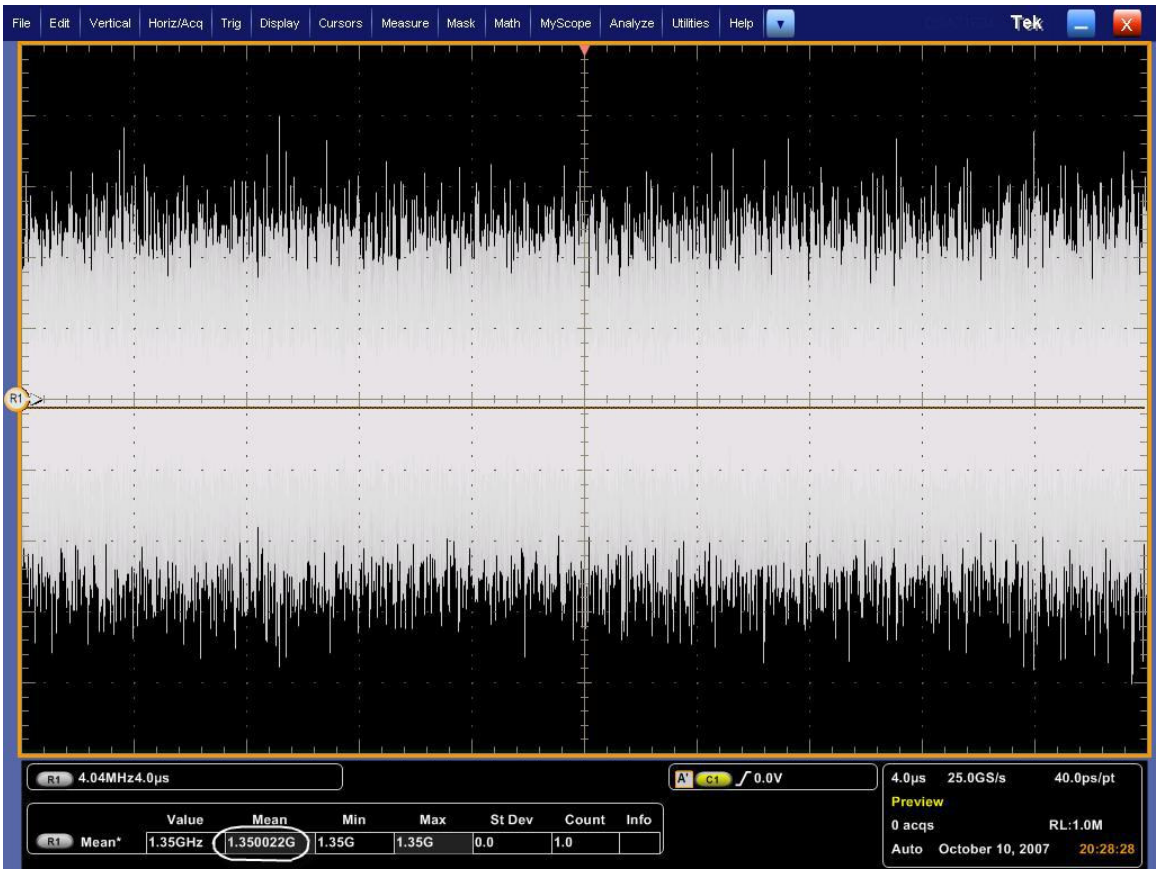
Select “Plot” from JIT3 main menu bar, and create a time trend plot of the period.


Time Trend Of Clock Freq1(M1)
Export
Save
Select View
Control
Cursors
Min Max
Sync
1.367G
Frequency (Hz)
1.333G
-20.000u
Time (s) 4.0000u/div
20.000u
File Measurements Results Plot Log Utility Help
TDSJIT3 Jitter Analysis
Create
Vert/Horz Axis
Measurement
Sources
Clock Frequency1
M1
Add Plot
Histogram
Time Trend
Cycle Trend
Spectrum
More...
Plots
Measurement
Type
Clock Freq1(M1)
Time Trend
Clear
Clear All
Plots
Select View
Measure
Run/Stop
Single
Clear
New Acq
Yes
Menu: Plot->Create
Status : Ready

To get more measurement resolution, use the Export: Save function in JIT3's plot screen, and select "Ref" from the pull-down menu. This transfers the Period Profile into the scope's Ref waveform memory.







Once the reference waveform is transferred into the scope's storage, minimize the JIT3 screens, so that only the scope UI is displayed.

Enable Mean amplitude measurement. Despite the fact that these are called amplitude measurements, in this case the measurements will be showing mean frequency (amplitude of the waveform).

Read the value of the current acquisition (ref waveform) following the µ: symbol.

1.9.8 Pass/Fail Criteria

The mean frequency shall be within the bounds set by the bit rate +/- 300ppm not accounting for the effects of SSC which is 1.349595 GHz to 1.350405 GHz for HBR devices and 809.7570 MHz to 810.2430 MHz for RBR devices.

[Reference Table 3.10 VESA Display Port Standard]

3.10 AC Common Mode Noise (Normative)

1.10.1 Test Objective

To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a Display Port interface. [Reference Table 3.10 VESA Display Port Standard]

1.10.2 References

- Display Port Specification version 1.1 dated March 19 2007 and errata 3 document dated 29th Aug 2007 and errata 4 document dated Sept 6 2007.
- Display Port CTS draft 13 version 1 specifications dated July 20 2007 Section 3.10.

1.10.3 Test Conditions

Tests shall be made on **all** Bit Rates supported **with** and **without** Pre-Emphasis for all differential voltage swings supported.
Test Pattern=PRBS7

1.10.4 Measurement Requirements

The following requirements must be met for each measurement:
Appropriately de-skew measurement channels
Number of Edges measured: >100,000
Minimum Acquisition Time : 25x1/PLLBW, (=2.5µS for PLLBW = 10MHz)
VTX-AC-CM = $(V_{TX\text{-}Plus} + V_{TX\text{-}Minus})/2$

1.10.5 Test equipment required

Refer to Appendix A of this MOI.

1.10.6 Connection Diagram

Refer to Appendix B of this MOI.

1.10.7 Detailed Procedure

Using DPOJET:

In the scope recall the setup <3.10_AC_Common_Mode_Noise.set> and open the DPOJET application in Analyze → DPOJET→ Select

Scope setup: 4µs/div, 40ps/pt (>100,000 UI)
Select Measurement: Ampl → Common Mode Noise on Ch1, Ch3


File
Edit
Vertical
Horiz/Acq
Trig
Display
Cursors
Measure
Mask
Math
MyScope
Analyze
Utilities
Help
Tek
C1 60.0mV/div 50Ω BW:16.0G
C3 60.0mV/div 50Ω BW:16.0G
Z(C1) 60.0mV 800ps -4.0ns 4.0ns
Z(C3) 60.0mV 800ps -4.0ns 4.0ns
A C1 0.0V
4.0µs 25.0GS/s 40.0ps/pt
Stopped Single Seq
1 acqs RL:1.0M
Auto October 08, 2007 11:15:54
Jitter and Eye Diagram Analysis Tools
Select
Configure
Results
Plots
Reports
Period/ Freq
Jitter
Time
Eye
Ampl
Measurements
Period
Pos Width
Neg Width
Freq
N–Period
+Duty Cycle
–Duty Cycle
CC–Period
+CC–Duty
–CC–Duty
Clear Selected
Clear All
Measurement
Source(s)
Common Mode1
Ch1,Ch3
Clear
Recalc
Single
Run

Click on “Start” to run the test. Record the Mean Common Mode voltage as shown below.

If pre-emphasis is used to compensate for cable loss then the same procedure as above can be used.

Click on “Start” to run the test. Record the Mean Common Mode voltage as shown below.

Using RT-Eye:

Start RT-Eye application on Scope. Select File => Recall => <3.10_AC_Common_Mode_Noise.ini>. Select AC CM Voltage in Amplitude frame. Make sure Probe type is Single Ended.

Click on “Start” to run the test. Record the StdDev Common Mode Voltage from the Results → Details section as shown below.

1.10.8 Pass/Fail Criteria

The measured AC common mode noise shall not exceed 20mV (RMS).

Note: This test limit is subject to further evaluation. The current value reflects TP1 specified performance so this limit does not derate the performance through a connector. [Reference Table 3.10 VESA Display Port Standard]

3.11 Non ISI Jitter Measurements (Normative)

1.11.1 Test Objective

To evaluate the amount of Non-ISI jitter accompanying the data transmission. [Reference the Figure 3.18 and figure 3.19 in the VESA Display Port Standard]

1.11.2 References

- Display Port Specification version 1.1 dated March 19 2007 and errata 3 document dated 29th Aug 2007 and errata 4 document dated Sept 6 2007.
- Display Port CTS draft 13 version 1 specifications dated July 20 2007 Section 3.11.

1.11.3 Test Conditions

Tests shall be made on **all** Bit Rates supported for all output levels.
Pre-emphasis is allowed to be set for best performance. The rationale for this flexibility is the understanding that some devices may have substantial copper trace lengths to the output receptacle. In these cases, being allowed pre-emphasis to overcome the loss is reasonable.
Test Pattern = PRBS7

1.11.4 Measurement Requirements

The following requirements shall be met for each frequency measurement:
Number of Edges measured: >1E6
Measurement PLL: Refer to section 2.1
Transition points in the signal (Zero crossings when signal transitions from low to high or from high to low) are found. Signal processing techniques are used to evaluate the underlying clock for the signal and the transition points are compared in time versus this time reference. Sophisticated algorithms are applied to evaluate jitter components from arrays of time deltas so determined.

1.11.5 Test equipment required

Refer to Appendix A of this MOI.

1.11.6 Connection Diagram

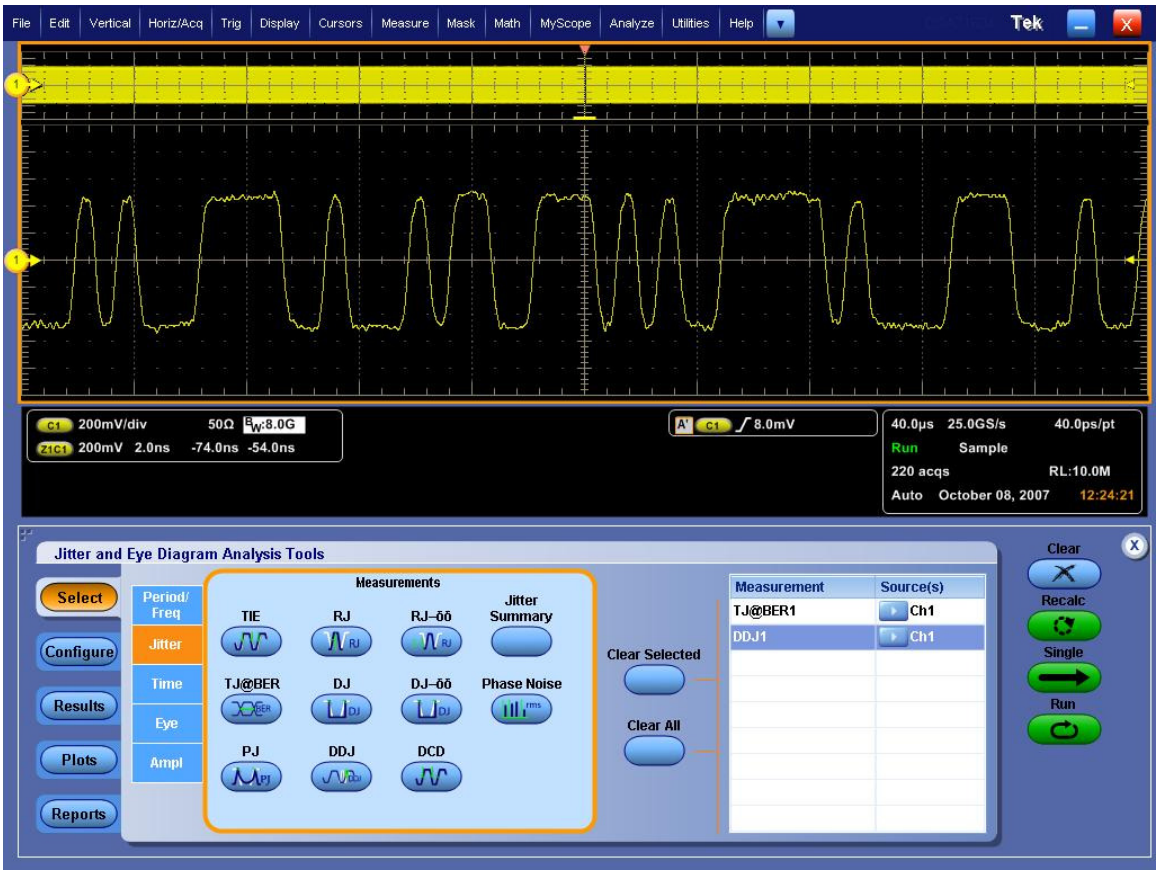
Refer to Appendix B of this MOI.

1.11.7 Detailed Procedure

In the scope recall the setup <3.11_Non_ISI_Jitter.set> and open the DPOJET application in Analyze→ DPOJET → Select

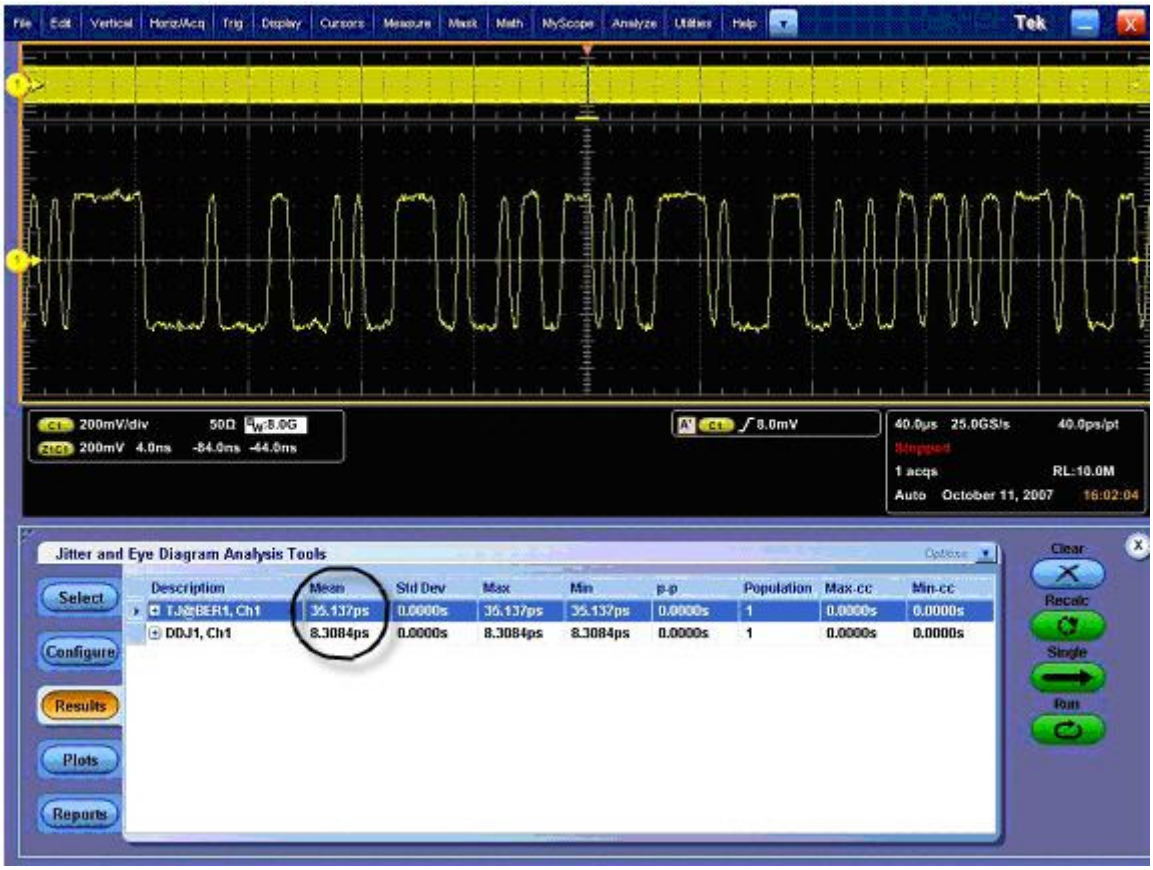
Scope setup: 40µs/div, 40ps/pt (>1e6 UI)

Select Measurement: TJ@BER and DDJ1 on Math1 = Ch1-Ch3 or Ch1 (SMA probe)



Click on Single to run the application. When complete, the statistics table will contain the results.

Calculate Non-ISI jitter = Tj(BER) – DDJ



If using pre-emphasis the same setup can be used.

Using TDSJIT3:

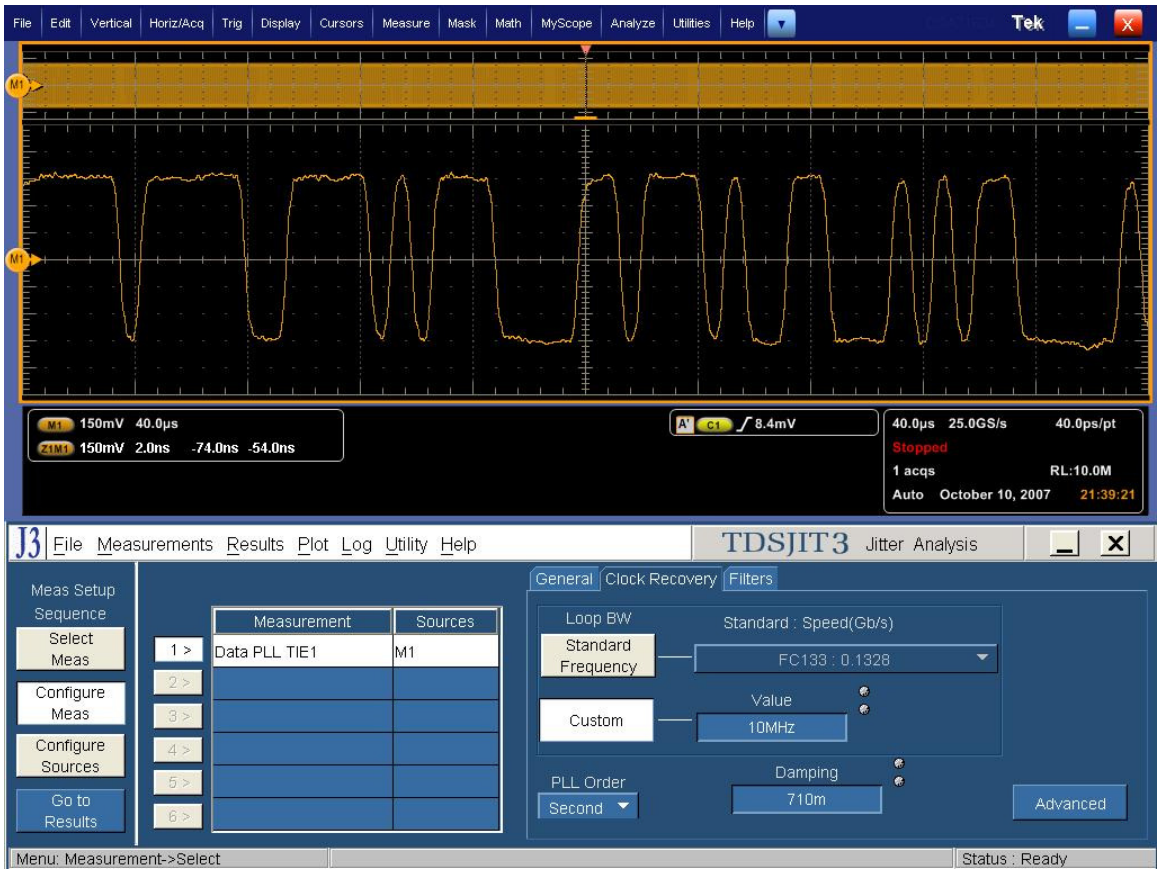
Start the JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 recall the setup <3.11_Non_ISI_Jitter.ini>

Scope setup: 40µs/div, 40ps/pt (>1e6 UI)

Select Measurement: Data PLL TIE on Math1 = Ch1-Ch3 or Ch1 (SMA probe)

In the Configure enable RjDj analysis with a repeating pattern length of 127 and BER-9.

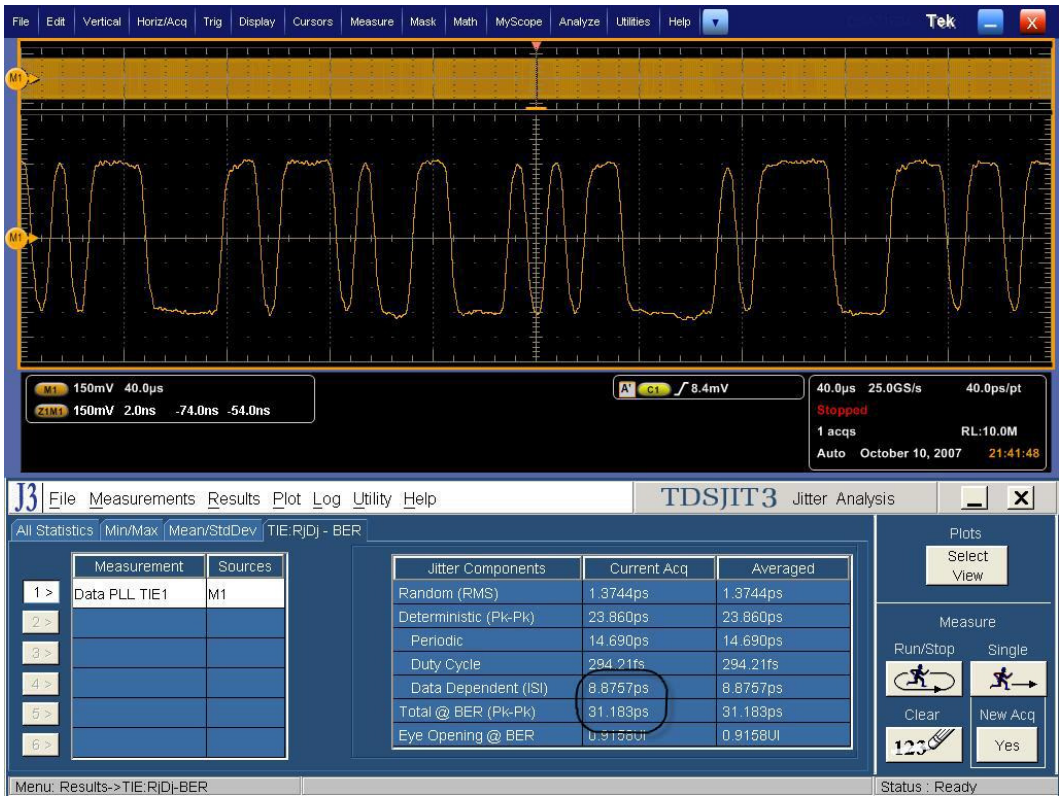
Configure Clock Recovery with 10MHz Loop BW, 2nd Order PLL, and a damping factor of 0.707



Press Go to Results button and click on “Start” to run the test. When complete, the statistics table will contain the results.

Calculate Non-ISI jitter = Tj(BER) – DDJ

If using pre-emphasis the same setup can be used.



The Non-ISI Jitter maximum values are as follows:

	Tx pins	TP2	TP3	Rx pins
	Non-ISI (ps)	**Non-ISI (ps)**	**Non-ISI**	**Non-ISI**
HBR				
A_{TXp-p}	96.296	96.296	122.222	125.556
RBR				
A_{TXp-p}	98.765	98.765	272.840	287.037

1.11.8 Pass/Fail Criteria

The maximum deterministic jitter at the compliance points is outlined in the following table:

	Transmitter package pins[1]	Transmitter Connector (TP2)	Receiver Connector (TP3)	Receiver package pins[2]
	Non-ISI	**Non-ISI**	**Non-ISI**	**Non-ISI**
High-Bit Rate (2.7Gb/s per lane)				
A_{TXp-p}	0.26	0.26	0.330	0.339
Reduced-Bit Rate (1.62Gb/s per lane)				
A_{TXp-p}	0.16	0.16	0.442	0.465

From Table 3-13 VESA DisplayPort Standard, consult spec for updates.

3.12 Total Jitter (TJ) Measurements (Normative)

1.12.1 Test Objective

To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10E9 or through an approved estimation technique1. This measurement is a data time interval error (Data-TIE) jitter measurement. [Reference the Table 3.13 VESA Display Port Standard]

1.12.2 References

- Display Port Specification version 1.1 dated March 19 2007 and errata 3 document dated 29th Aug 2007 and errata 4 document dated Sept 6 2007.
- Display Port CTS draft 13 version 1 specifications dated July 20 2007 Section 3.12.

3.12.3 Test Conditions

Tests shall be made on **all** Bit Rates supported.
Pre-emphasis is allowed to be set for best performance.
All voltage levels verified.
Test Pattern = PRBS7

3.12.4 Measurement Requirements

The following requirements shall be met for each Total Jitter measurement:
Number of Edges measured: >1E6
Measurement PLL: Refer to section 2.1)
Use Dual Dirac Model to estimate jitter to a 10-9 BER.
Transition points in the signal (Zero crossings when signal transitions from low to high or from high-to-low) are found. Signal processing techniques are used to evaluate the underlying clock for the signal and the transition points are compared in time versus this time reference. Sophisticated algorithms are applied to evaluate jitter components from arrays of time deltas so determined.

1.12.5 Test equipment required

Refer to Appendix A of this MOI.

1.12.6 Connection Diagram

Refer to Appendix B of this MOI.

3.12.7 Detailed Procedure

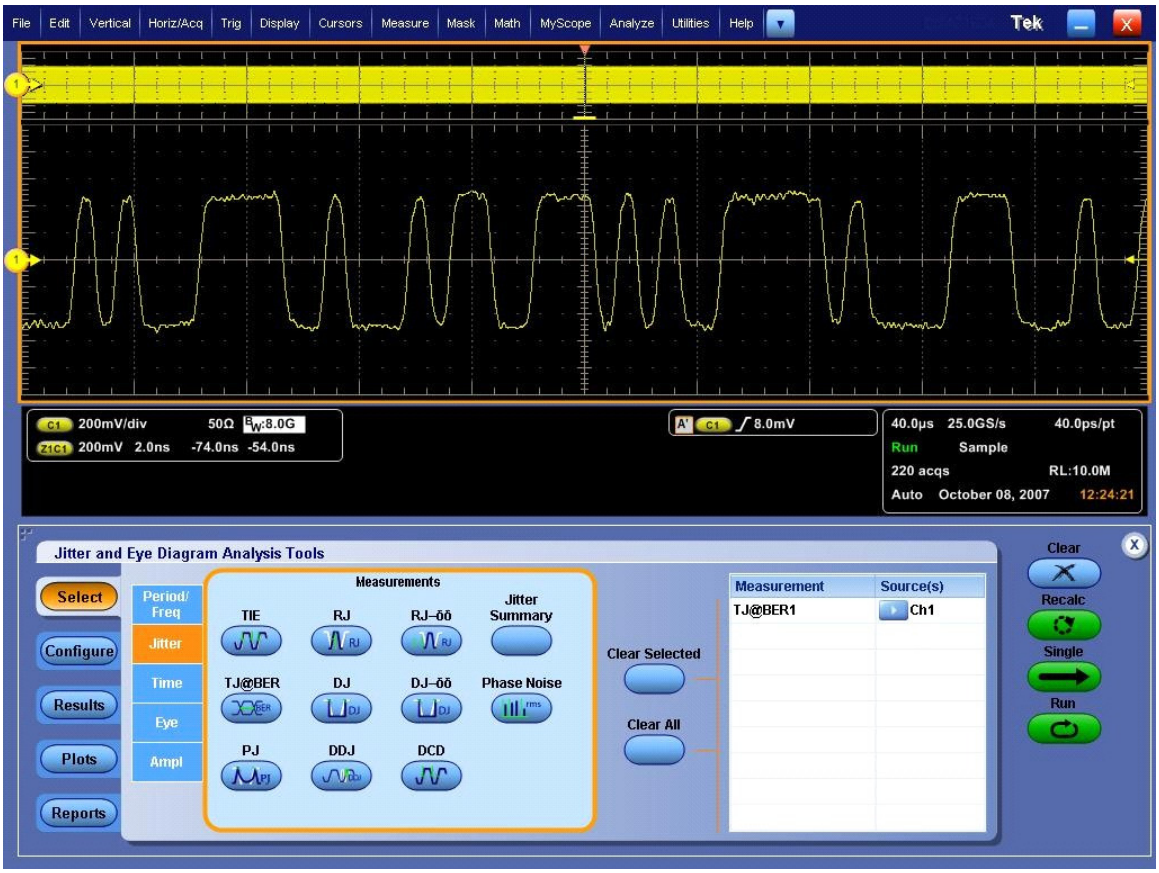
Using DPOJET:

In the scope recall the setup <3.12_Total_Jitter.set> and open the DPOJET application in Analyze → DPOJET→ Select

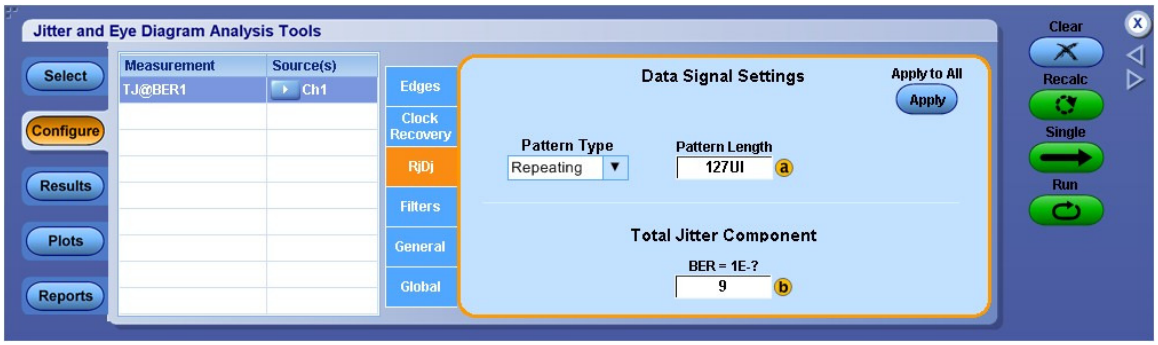
Scope setup: 40µs/div, 40ps/pt (>1e6 UI)

Select Measurement: TJ@BER on Ch1 (P7380SMA probe)

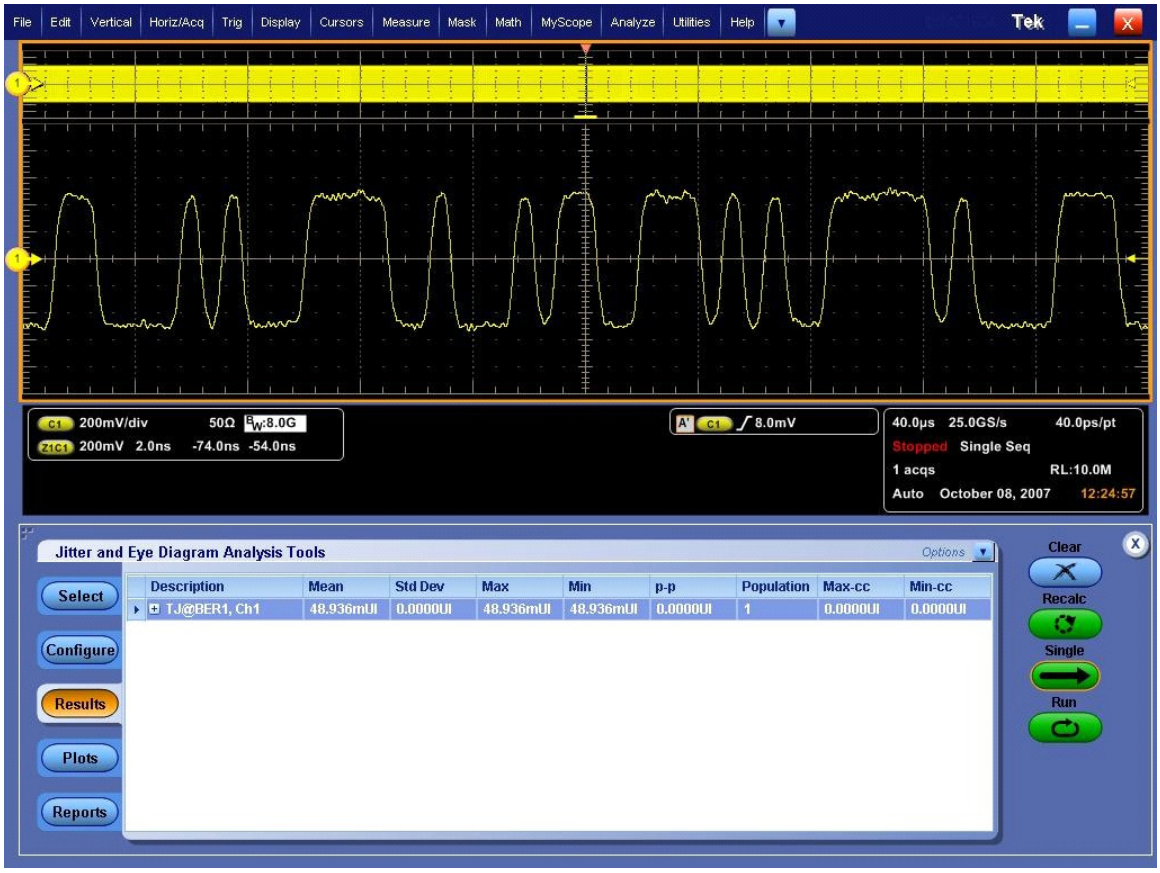
(Alternatively, the test can be performed using matched cable pair; in this case select Measurement as Math1 = Ch1-Ch3)



Configure the measurement as shown below:
Pattern type= repeating, Length =127UI, BER = 1e-9



Click on Single to run the application. When complete, the statistics table will contain the results.



If pre-emphasis is applied the same setup as above can be used to measure Total Jitter.

4. Compare Tj(BER) to Table 3-13 below

	Tx pins	TP2	TP3	Rx pins
	Non-ISI (ps)	**Non-ISI (ps)**	**Non-ISI**	**Non-ISI**
HBR				
$A_{TX(p-p}$	96.296	134.815	181.852	196.296
RBR				
$A_{TX(p-p}$	98.765	137.654	332.716	358.025

Table 3-13

Using TDSJIT3:

Start the JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 recall the setup <3.12_Total_Jitter.ini>

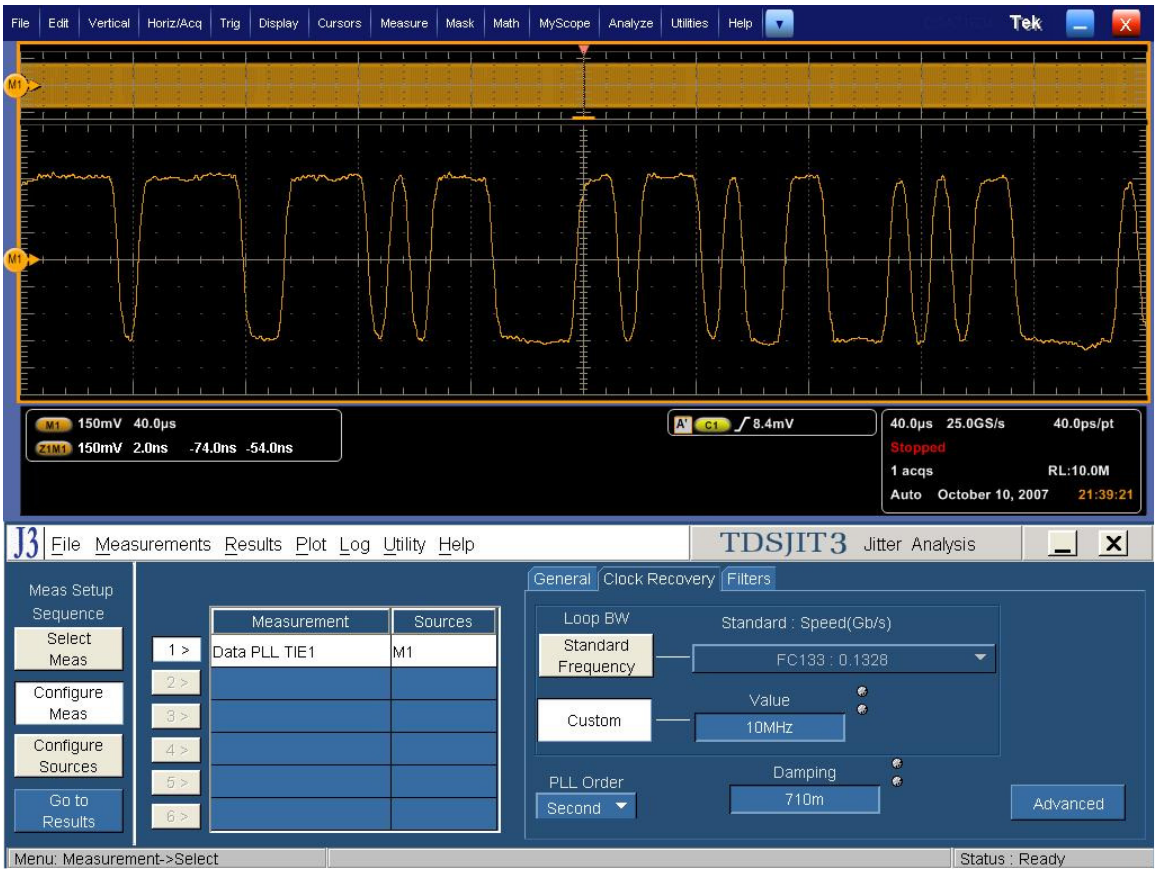
Scope setup: 40µs 40ps/pt (>1e6 UI)

Select Measurement: Data PLL TIE on Ch1 (P7380SMA probe)

(Alternatively, the test can be performed using matched cable pair; in this case select Measurement as Math1 = Ch1-Ch3) – shown in illustration below.

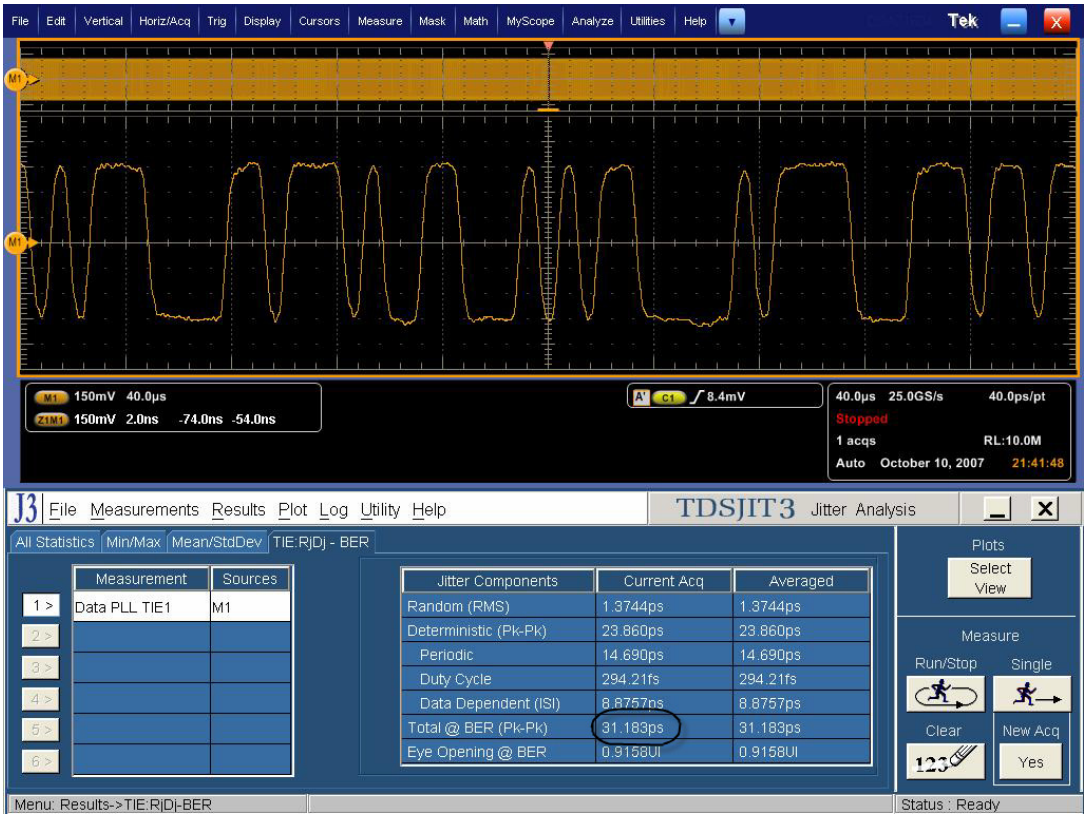
In the Configure enable RjDj analysis with a repeating pattern length of 127 and BER-9.

Configure Clock Recovery with 10MHz Loop BW, 2nd Order PLL, and a damping factor of 0.707.



Press Go to Results button and click on “Start” to run the test. When complete, the statistics table will contain the results.

If pre-emphasis is applied the same setup as above can be used to measure Total Jitter.



The Total Jitter maximum values are as follows:

	Tx pins	TP2	TP3	Rx pins
	Non-ISI (ps)	**Non-ISI (ps)**	**Non-ISI**	**Non-ISI**
HBR				
A_{TXp-p}	96.296	134.815	181.852	196.296
RBR				
A_{TXp-p}	98.765	137.654	332.716	358.025

3.12.8 Pass/Fail Criteria

The maximum total jitter at the compliance points is outlined in the following table.

	Transmitter package pins[1]	Transmitter Connector (TP2)	Receiver Connector (TP3)	Receiver package pins[2]
	TJ	TJ	TJ	TJ
High-Bit Rate (2.7Gb/s per lane)				
A_{TXp-p}	0.26	0.364	0.491	0.53
Reduced-Bit Rate (1.62Gb/s per lane)				
A_{TXp-p}	0.16	0.223	0.539	0.58

From Table 3.13 VESA DisplayPort Standard

3.13 Unit Interval (Normative)

1.13.1 Test Objective

To evaluate the overall variation in the Unit Interval width over at least one full SSC cycle to ensure it stays within the spec limit of 300PPM

1.13.2 References

- Display Port Specification version 1.1 dated March 19 2007 and errata 3 document dated 29th Aug 2007 and errata 4 document dated Sept 6 2007.
- Display Port CTS draft 13 version 1 specifications dated July 20 2007 Section 3.13.

1.13.3 Test Conditions

Tests shall be performed on a PRBS7 signal, with SSC enabled. An evaluation of at least 100K Unit Intervals or 1 Full SSC cycle is required to ensure that any SSC modulation on the signal does not violate the time base accuracy specifications.

1.13.4 Measurement Requirements

This measurement should be evaluated over 100K Consecutive Unit intervals.

1.13.5 Test equipment required

Refer to Appendix A of this MOI.

1.13.6 Connection Diagram

Refer to Appendix B of this MOI.

1.13.7 Detailed Procedure

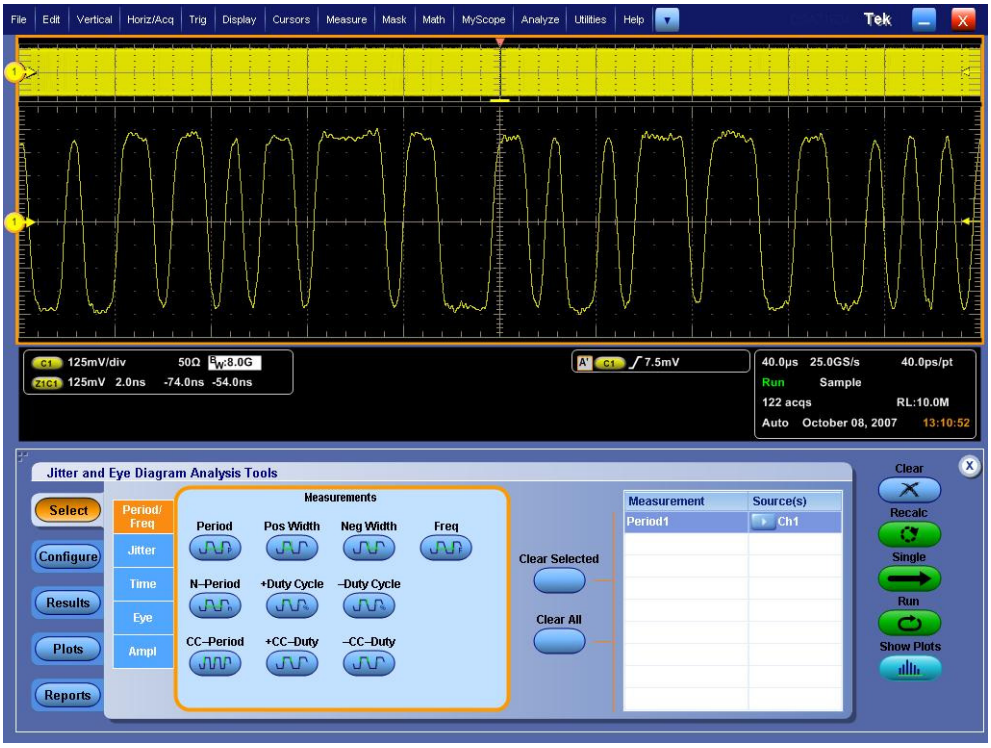
Using DPOJET:

In the scope recall the setup <3.13_Unit_Interval.set> and open the DPOJET application in Analyze→ DPOJET → Select

Scope setup: 40µs/div, 40ps/pt (>1e6 UI)

Select Measurement: Data Period on Ch1 (P7380SMA probe)

(Alternatively, the test can be performed using matched cable pair; in this case select Measurement as Math1 = Ch1-Ch3)


File
Edit
Vertical
Horiz/Acq
Trig
Display
Cursors
Measure
Mask
Math
MyScope
Analyze
Utilities
Help
Tek
C1 125mV/div 50Ω BW:8.0G
ZtC1 125mV 2.0ns -74.0ns -54.0ns
A' C1 7.5mV
40.0µs 25.0GS/s 40.0ps/pt
Run Sample
122 acqs RL:10.0M
Auto October 08, 2007 13:10:52
Jitter and Eye Diagram Analysis Tools
Select
Configure
Results
Plots
Reports
Period/ Freq
Jitter
Time
Eye
Ampl
Measurements
Period
Pos Width
Neg Width
Freq
N–Period
+Duty Cycle
–Duty Cycle
CC–Period
+CC–Duty
–CC–Duty
Clear Selected
Clear All
Measurement
Source(s)
Period1
Ch1
Clear
Recalc
Single
Run
Show Plots

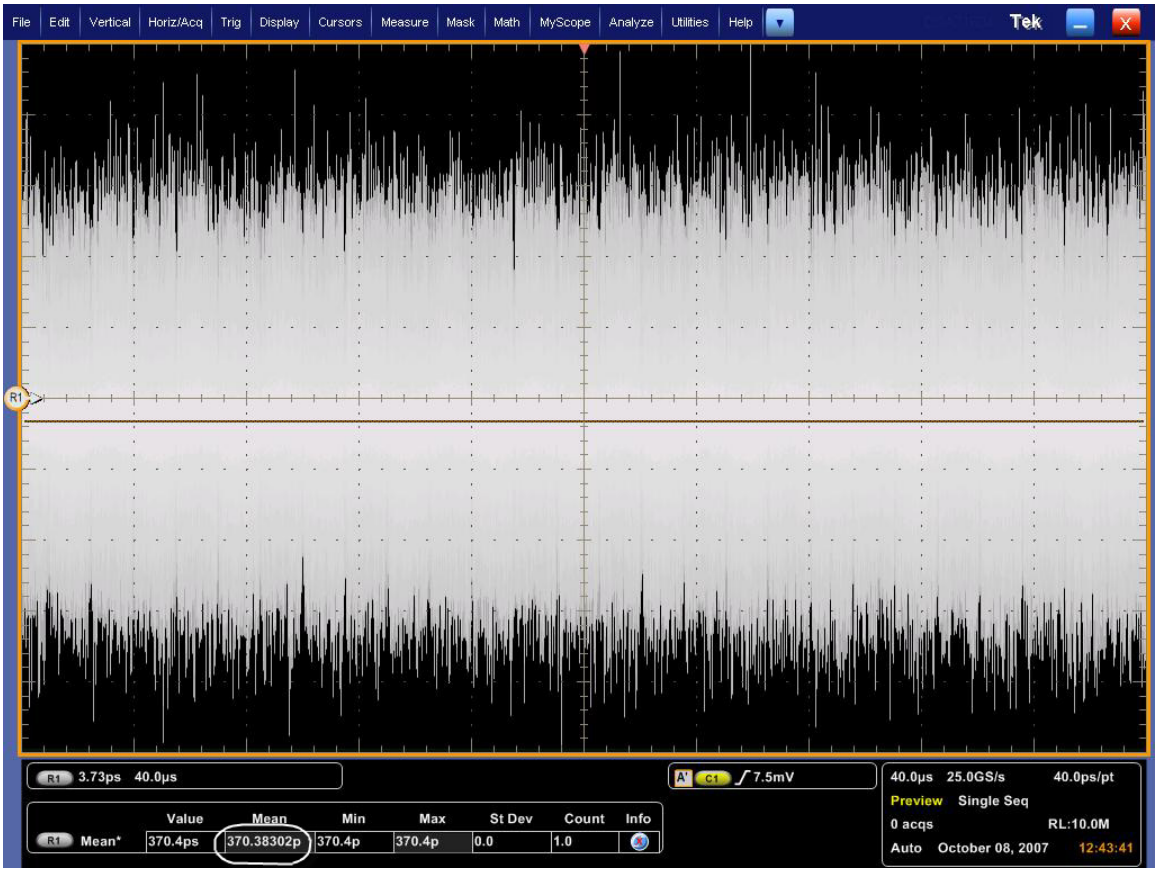
Set the Signal Type: Data

lick on Single to run the application. When complete, the statistics table will contain the results.

Note that this measurement is rounded up from an internal representation of 9 digits. For measurements that are near the limit, it is possible to use the following procedure to view additional resolution on the measurement.

Select “Export to Ref Waveform” in the Options menu

Select Ref1 as the Destination. This transfers the Period profile into the scope's Ref waveform memory.



Once the reference waveform is transferred into the scope's storage, minimize the DPOJET screen so that only the scope UI is displayed.

Enable Mean amplitude measurement. Despite the fact that these are called amplitude measurements, in this case the measurements will be showing mean period.

Read the value of the current acquision (ref waveform) following the µ: symbol.

Using TDSJIT3 :

Start the JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 recall the setup <3.13_Unit_Interval.ini>.

Scope setup: 4µs/div, 40ps/pt (>100,000 UI)

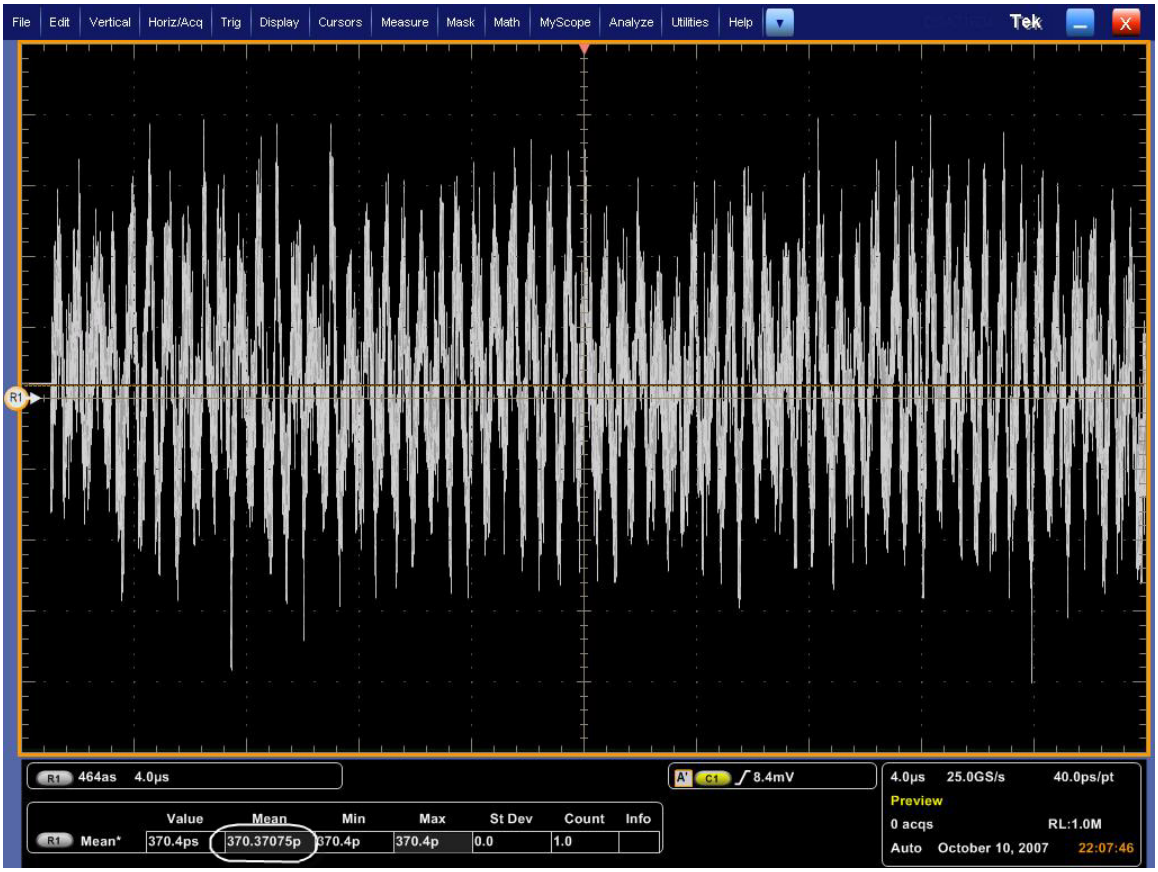
Select Measurement: Data Period on Ch1 (P7380SMA probe)

(Alternatively, the test can be performed using matched cable pair; in this case select Measurement as Math1 = Ch1-Ch3) – shown in illustration below.

Click on Single to run the application. When complete, the statistics table will contain the results.


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
M1 125mV 4.0µs
ΔM1 125mV 800ps -10.4ns -2.4ns
A' C1 8.4mV
4.0µs 25.0GS/s 40.0ps/pt
Stopped
1 acqs RL:1.0M
Auto October 10, 2007 21:56:47
J3 File Measurements Results Plot Log Utility Help
TDSJIT3 Jitter Analysis
All Statistics Min/Max Mean/StdDev TIE:RjDj - BER
Measurement Sources
1 > Data Period1 M1
Statistic Current Acq All Acqs
Population 105266 105266
Mean 370.37ps 370.37ps
Std Dev 203.05fs 203.05fs
Max 370.66ps 370.66ps
Min 370.08ps 370.08ps
Pk-Pk 575.89fs 575.89fs
Max + Δ 1.5077fs 1.5077fs
Max - Δ -1.5059fs -1.5059fs
Plots
Select View
Measure
Run/Stop
Single
Clear
New Acq
Yes
Menu: Results->All Statistics
Status : Ready

Note that this measurement is rounded up from an internal representation of 9 digits. For measurements that are near the limit, it is possible to use the following procedure to view additional resolution on the measurement.



1.13.8 Pass/Fail Criteria

The mean Unit Interval must satisfy the following criteria:

- Mean Unit Interval measured between 617.0987.ps (min) to 617.4691 ps (max) with SSC disabled and 614.1975 ps (min) to 617.4691 ps (max) with SSC enabled (for products running at RBR).

- Mean Unit Interval measured between 370.2592 ps (min) to 370.4815 ps (max) with SSC disabled and 368.5185 ps (min) to 370.4815 ps (max) with SSC enabled (for products running at HBR).

Note there are two spec limits corresponding to either SSC disabled or enabled (+0ppm to -5000ppm deviation)

3.14 Frequency Long Term Stability (Informative)

1.14.1 Test Objective

To evaluate the overall variation in source time base accuracy over a measurement interval of no fewer than 10 SSC cycles, ensuring the device stays within the required +-300PPM limit.

1.14.2 References

- Display Port Specification version 1.1 dated March 19 2007 and errata 3 document dated 29th Aug 2007 and errata 4 document dated Sept 6 2007.
- Display Port CTS draft 13 version 1 specifications dated July 20 2007 Section 3.14.

1.14.3 Test Conditions

Tests shall be performed on a PRBS7 signal, with SSC enabled.
An evaluation of at least 10 full SSC cycles is required.

1.14.4 Measurement Requirements

As SSC in Display Port is mandatory, the reported result must be the mean of ten measured maximum values from the range of SSC modulation deviation. The execution of this test must include use of the filter to remove the low frequency SSC components of phase modulation. This filter is a High Pass filter with a 20dB/Decade roll off with a corner frequency 60X that of the highest SSC frequency allowed. (1.98MHz).
(Note: this procedure uses a Low pass filter with a cutoff frequency of 1.98MHz)

1.14.5 Test equipment required

Refer to Appendix A of this MOI.

1.14.6 Connection Diagram

Refer to Appendix B of this MOI.

1.14.7 Detailed procedure

Using DPOJET :

In the scope recall the setup <3.14_Frequency_Stability.set> and open the DPOJET application in Analyze → DPOJET → Select

Scope setup: 40µs/div, 40ps/pt (>1e6 UI)

Select Measurement: Data Period on Ch1 (P7380SMA probe)

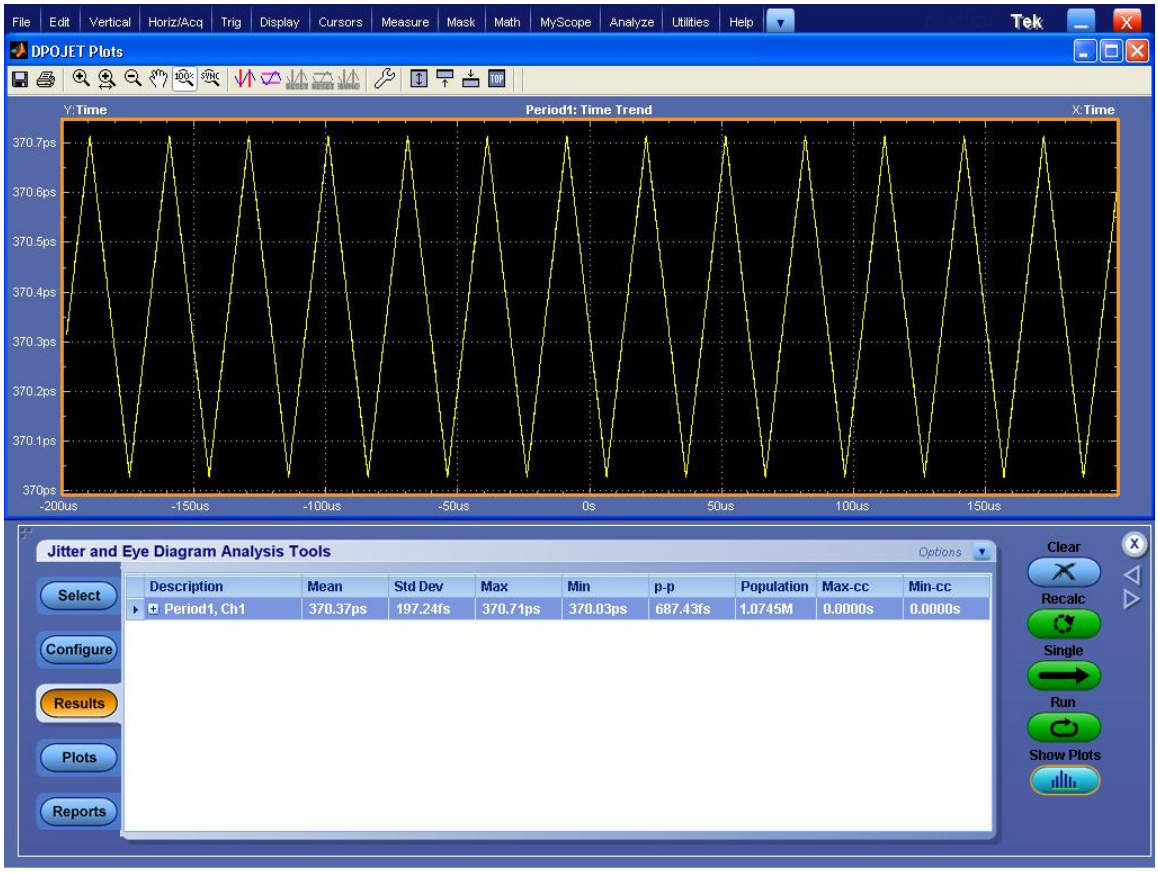
(Alternatively, the test can be performed using matched cable pair; in this case select Measurement as Math1 = Ch1-Ch3)

Configure Signal Type: Data

Configure filters: 2nd order low pass, 1.98MHz

Click on Single to run the application. When complete, the statistics table will contain the results.

A Period time trend profile similar to the following will be acquired with SSC ON.

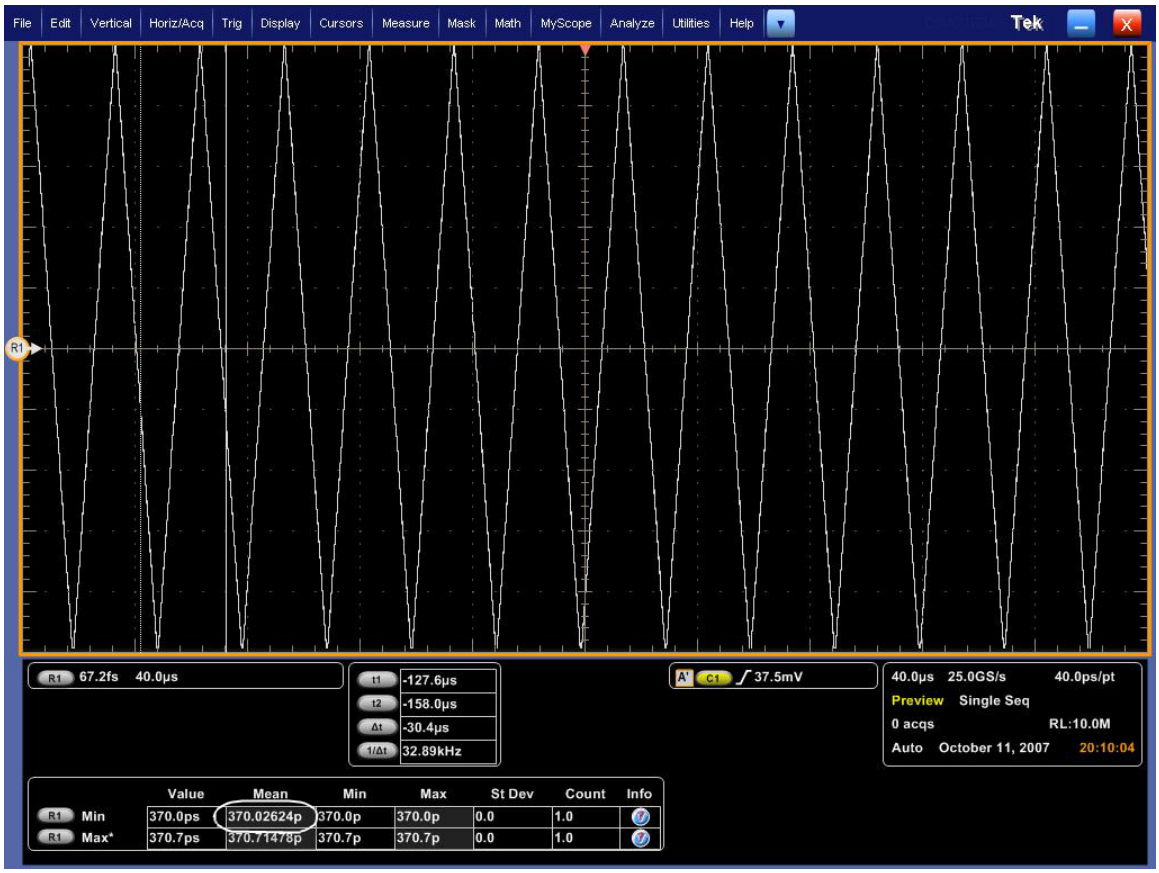


NOTE: The DPOJET software provides the ability to do cursor measurements directly on the profile plot. However, the 4 digits of resolution obtained when using DPOJET cursor measurements (1000 ppm) is not sufficient for this test.
The value can also be read directly from the statistics table as seen in the previous figure. This data is shown as 5 digits, and provides a 100 ppm resolution, which is marginally adequate for the 300ppm measurement tolerance. For test 3-14, use the Min value (min period=max freq)..

To get 8 digits of resolution, select “Export to Ref Waveform” from the Options pull-down menu. This transfers the Period Profile into the scope’s Ref waveform memory.

Create a Max and Min measurement (Max will be used for test 3-16). In the Meas menu select Gating using the Cursor method.

Use the Cursor Position knob to place cursors around the first of the 10 peaks. Record the Min period, which is shown as (µ). Repeat the process of moving the cursors to each subsequent peak, and record the Min period for each cycle. Average the 10 recorded values to produce the Measured Mean Min period. In addition, the data for test 3-16 can be taken at the same time by recording the Max period values for each of the 10 minimum peaks.


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
R1
R1 67.2fs 40.0µs
t1 -127.6µs
t2 -158.0µs
Δt -30.4µs
1/Δt 32.89kHz
C1 37.5mV
40.0µs 25.0GS/s 40.0ps/pt
Preview Single Seq
0 acqs RL:10.0M
Auto October 11, 2007 20:10:04
Value Mean Min Max St Dev Count Info
R1 Min 370.0ps 370.02624p 370.0p 370.0p 0.0 1.0
R1 Max* 370.7ps 370.71478p 370.7p 370.7p 0.0 1.0

Using TDSJIT3 :

Start the JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 recall the setup <3.14_Frequency_Stability.ini>.

Scope setup: 40µs/div, 40ps/pt (>1e6 UI)

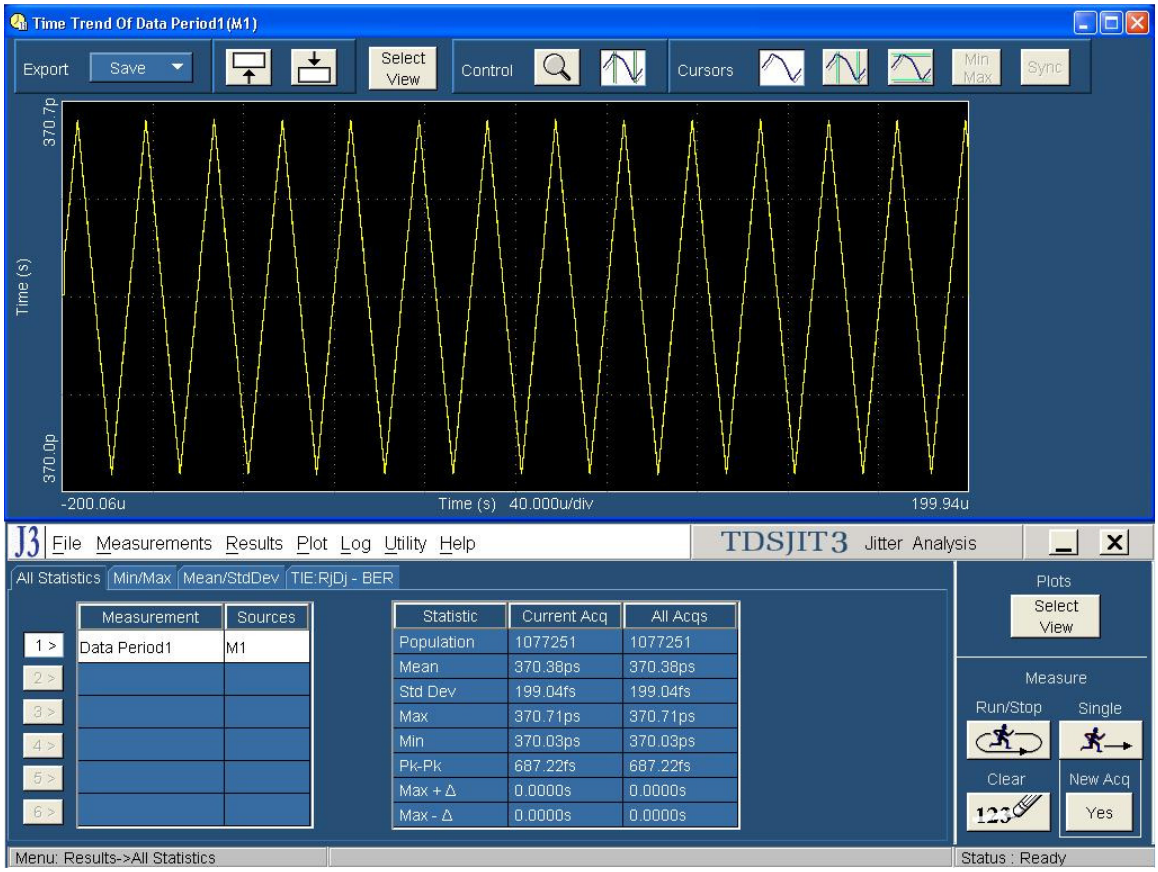
Select Measurement: Data Period on Ch1 (P7380SMA probe)

(Alternatively, the test can be performed using matched cable pair; in this case select Measurement as Math1 = Ch1-Ch3) – shown in illustration below.

Configure Measurement: Filters Low Pass second order 1.98 MHz

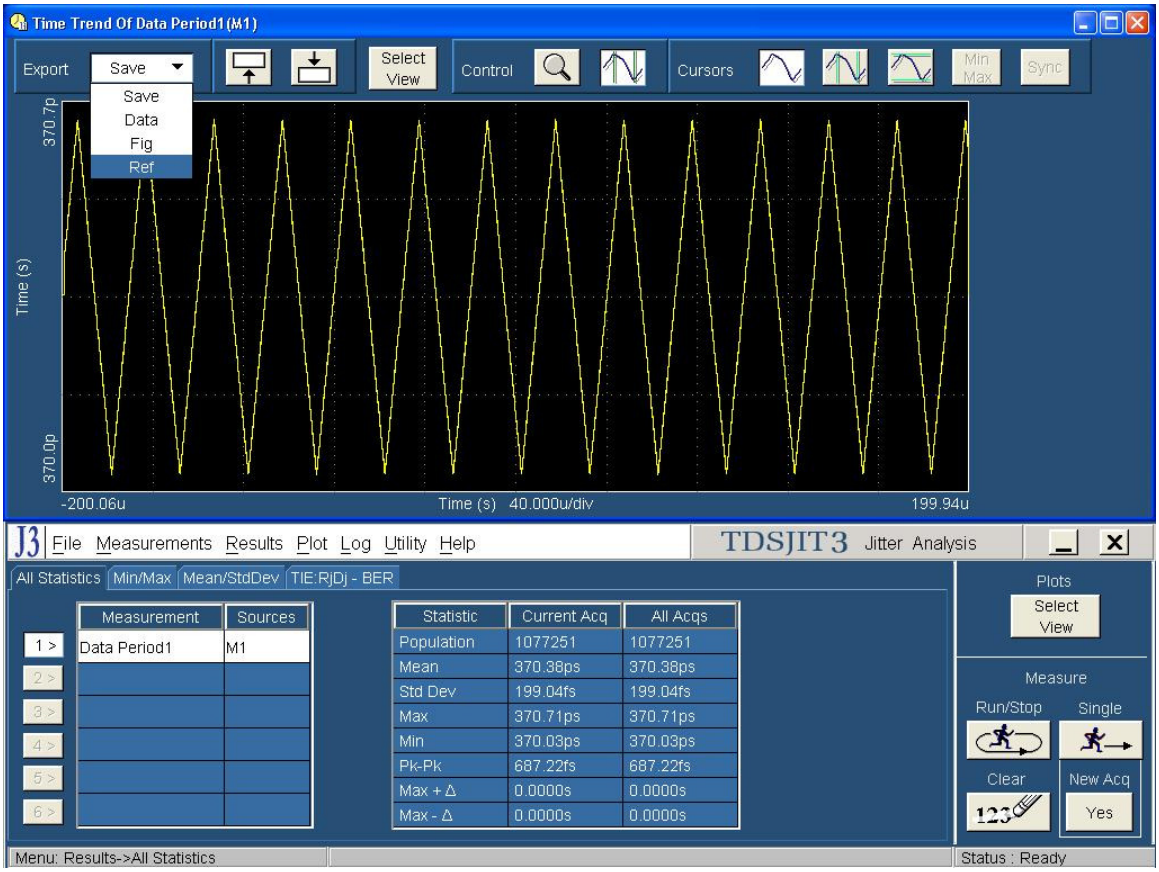
Click on Single to run the application. When complete, the statistics table will contain the results.

A Period time trend profile similar to the following will be acquired with SSC ON.



NOTE: The TDSJIT3 software provides the ability to do cursor measurements directly on the profile plot. However, the 4 digits of resolution obtained when using JIT3 cursor measurements (1000 ppm) is not sufficient for this test.
The value can also be read directly from the statistics table as seen in the previous figure. This data is shown as 5 digits, and provides a 100 ppm resolution, which is marginally adequate for the 300ppm measurement tolerance. For test 3-14, use the Min value (min period=max freq) shown in the "Current Acq" column.

To get 8 digits of resolution, use the Export: Save function in JIT3's plot screen, and select "Ref" from the pull-down menu. This transfers the Period Profile into the scope's Ref waveform memory.



Once the reference waveform is transferred into the scope's storage, minimize the TDSJIT3 screens, so that only the scope UI is displayed.

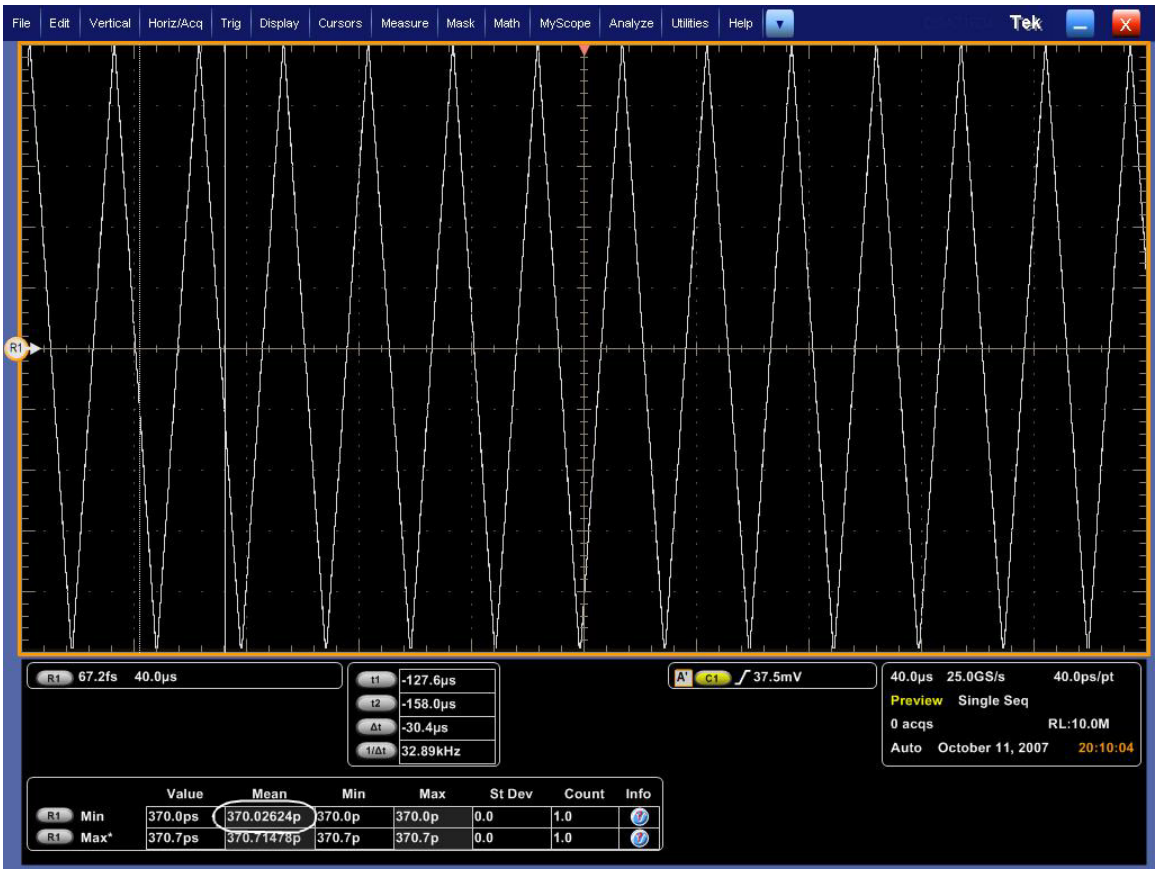
Under the Meas menu item, click on Gating. Select Cursor for the gating method.

Set the cursors for approximately 1 SSC cycle coverage.

Under the Cursor menu item, click on Cursor Setup. Select Tracking for the Track Mode.

Enable Max and Min amplitude measurements (Max is used for test 3-16). Despite the fact that these are called amplitude measurements, in this case the measurements will be showing period.

Use the Cursor Position knob to place cursors around the first of the 10 peaks. Record the Min period, which is shown as (μ). Repeat the process of moving the cursors to each subsequent peak, and record the Min period for each cycle. Average the 10 recorded values to produce the Measured Mean Min period. In addition, the data for test 3-16 can be taken at the same time by recording the Max period values for each of the 10 minimum peaks.



Calculate deviation = (Nominal – Measured Mean Min Period)/Nominal * 1e6 ppm where Nominal is 370.3704 ps for HBR devices and 617.2840 ps for RBR devices.

1.14.8 Pass/Fail Criteria

Pass/Fail Criteria f_{tol} measured between -300ppm and 300ppm.

3.15 Spread Spectrum Modulation Frequency (Normative)

3.15.1 Test Objective

To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.

3.15.2 References

- Display Port Specification version 1.1 dated March 19 2007 and errata 3 document dated 29th Aug 2007 and errata 4 document dated Sept 6 2007.
- Display Port CTS draft 13 version 1 specifications dated July 20 2007 Section 3.15.

3.15.3 Test Conditions

The SSC frequency will be evaluated at the highest bit rate the transmitter supports. Tests shall be performed on a PRBS7 signal, with SSC enabled. An evaluation of at least 10 full SSC cycles is required (Mean value reported).

3.15.4 Measurement Requirements

As SSC in Display Port is mandatory, the reported result must be the mean of ten measured maximum values from the range of SSC modulation deviation.

1.15.5 Test equipment required

Refer to Appendix A of this MOI.

1.15.6 Connection Diagram

Refer to Appendix B of this MOI.

3.15.7 Detailed Procedure

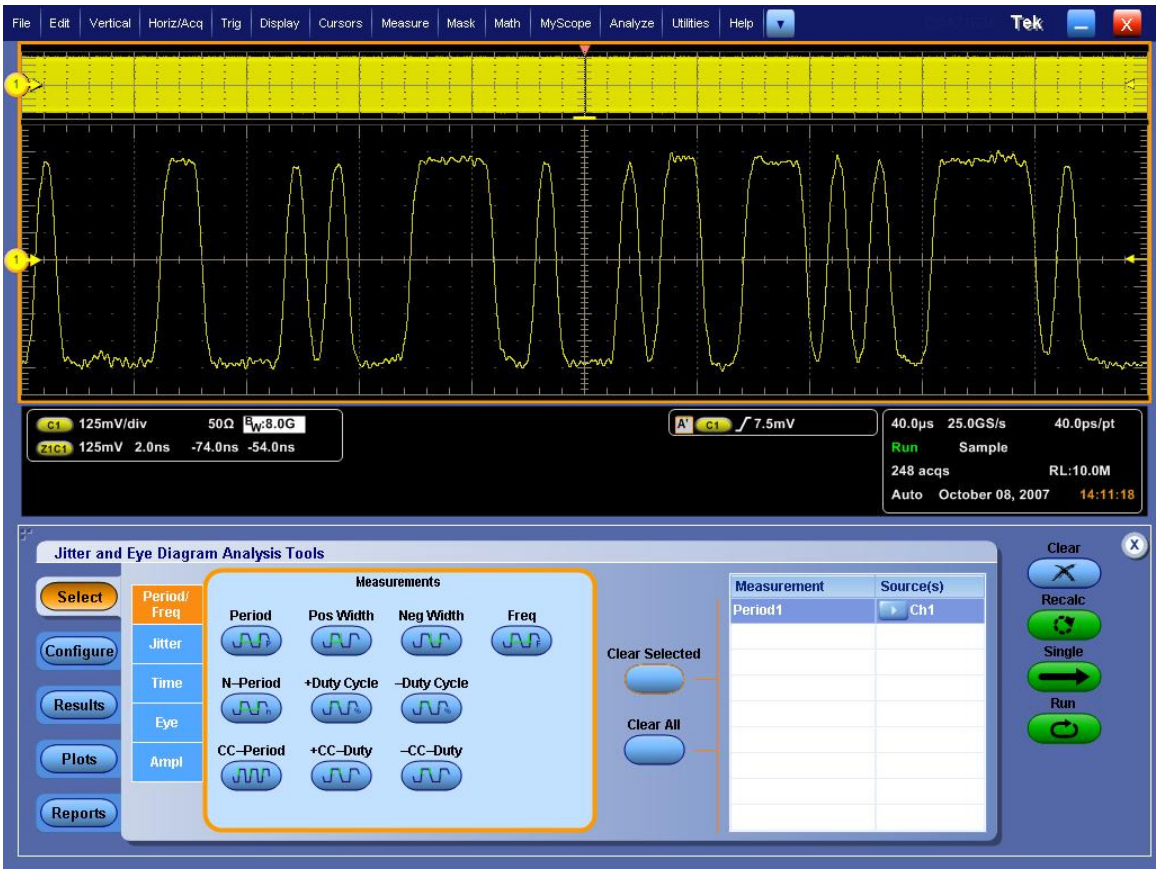
Using DPOJET :

In the scope recall the setup 'Frequency Stability' <3.15_SSC_Frequency.set> and open the DPOJET application in Analyze → DPOJET → Select

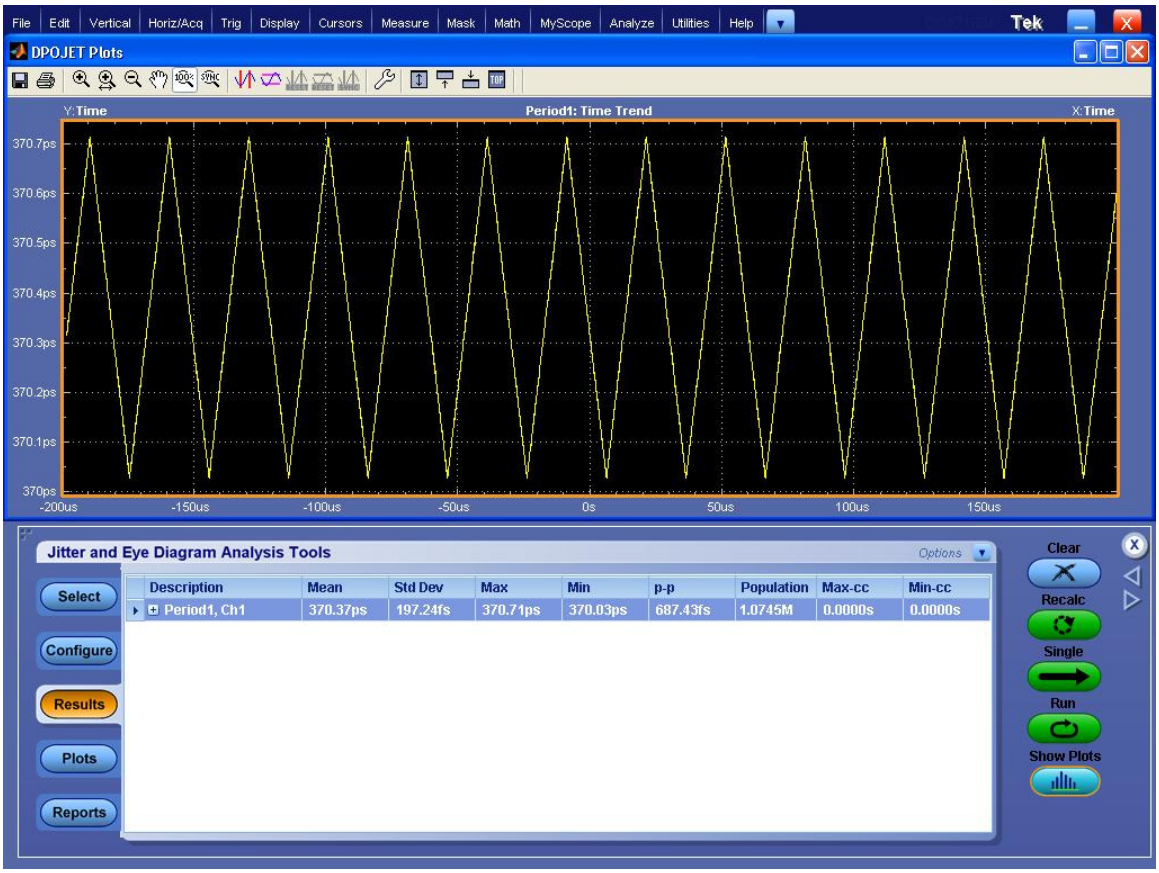
Scope setup: 40µs/div, 40ps/pt (>1e6 UI)

Select Measurement: Data Period on Ch1 (P7380SMA probe)

(Alternatively, the test can be performed using matched cable pair; in this case select Measurement as Math1 = Ch1-Ch3)


File
Edit
Vertical
Horiz/Acq
Trig
Display
Cursors
Measure
Mask
Math
MyScope
Analyze
Utilities
Help
Tek
C1 125mV/div 50Ω BW:8.0G
Z1C1 125mV 2.0ns -74.0ns -54.0ns
A C1 7.5mV
40.0µs 25.0GS/s 40.0ps/pt
Run Sample
248 acqs RL:10.0M
Auto October 08, 2007 14:11:18
Jitter and Eye Diagram Analysis Tools
Select
Configure
Results
Plots
Reports
Period/ Freq
Jitter
Time
Eye
Ampl
Measurements
Period
Pos Width
Neg Width
Freq
N–Period
+Duty Cycle
–Duty Cycle
CC–Period
+CC–Duty
–CC–Duty
Clear Selected
Clear All
Measurement
Source(s)
Period1
Ch1
Clear
Recalc
Single
Run

Follow the procedure described for test 3-14, up to the point where the profile has been created.

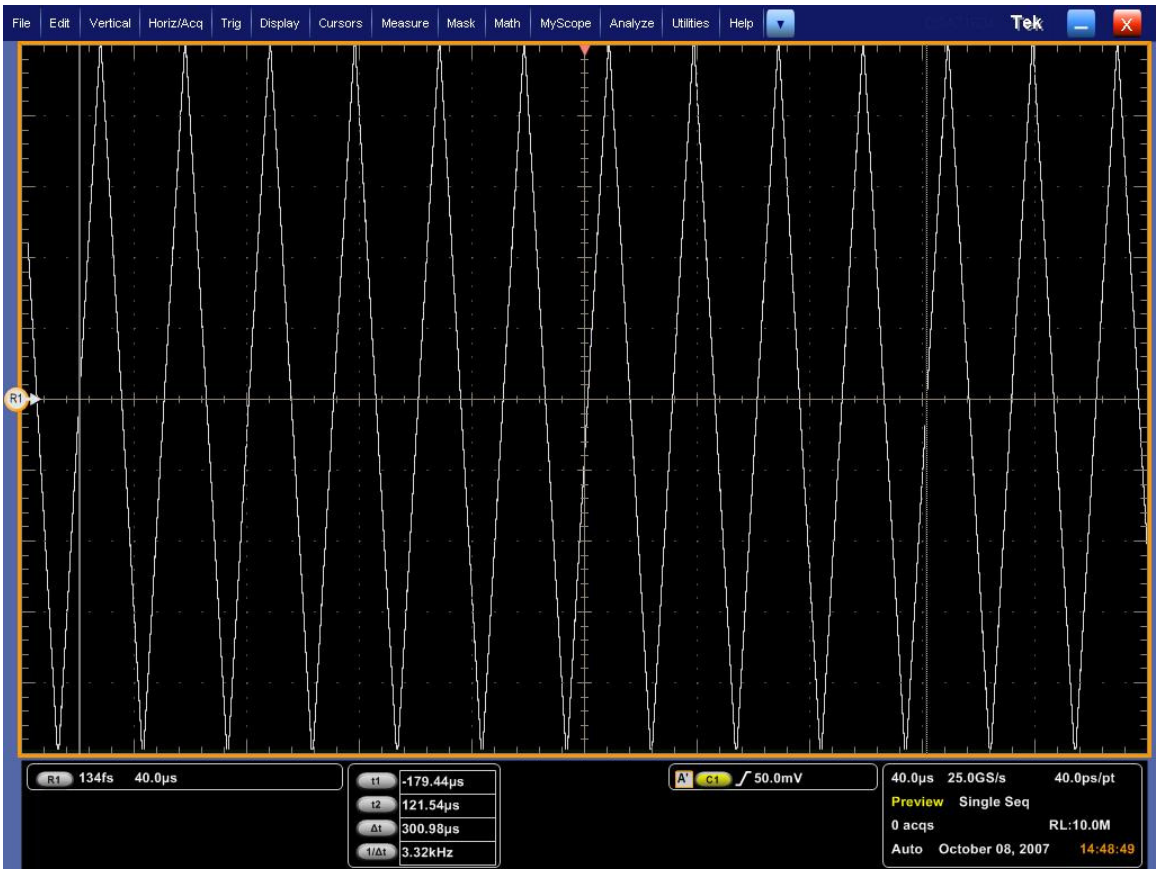


In some cases, it will be adequate to make the measurements using the cursor capability in DPOJET to measure the modulation frequency. Set cursors at the X axis crossing across 10 cycles. To arrive at the modulation frequency, take the delta time value, divide by 10, and invert to get frequency.

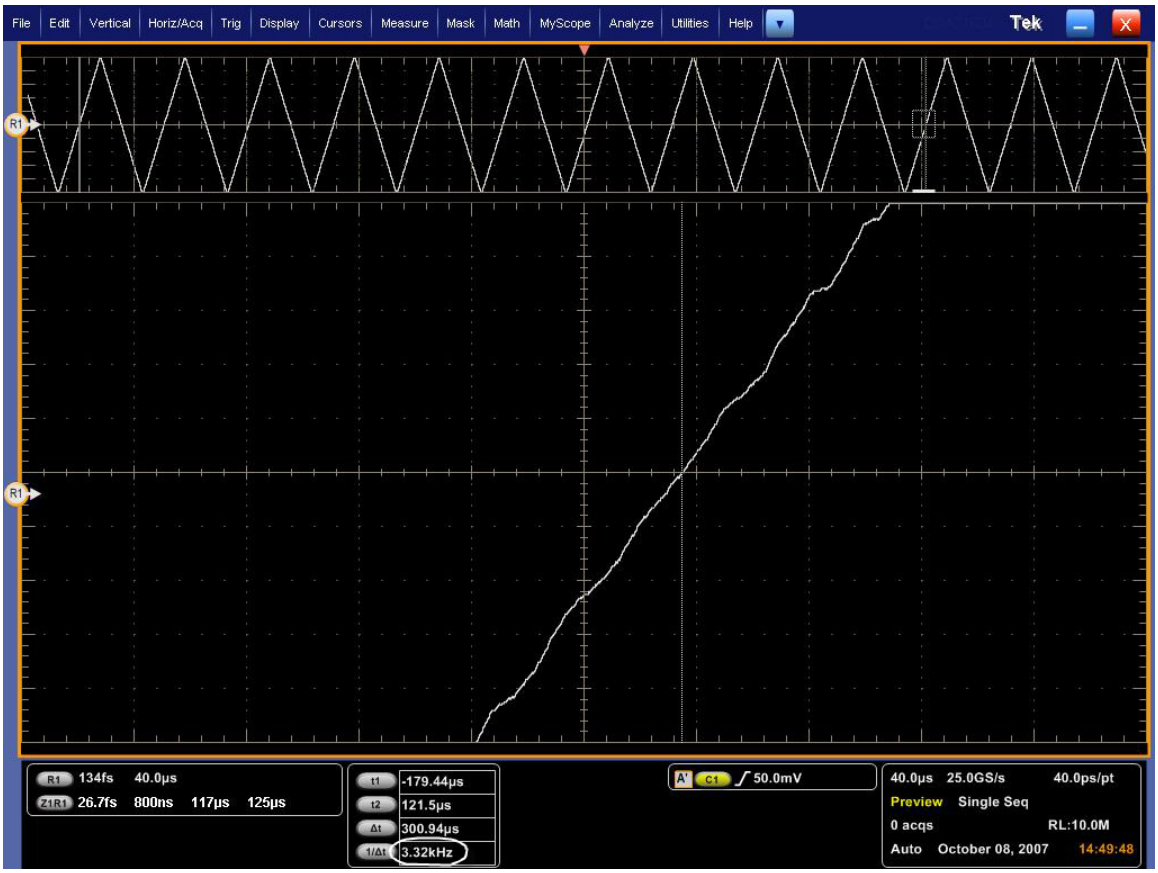
Note that there is often substantial higher frequency noise on this profile, and it may be difficult to discern the X axis measurement points on the profile. This is especially critical if the device is close to either limit. In this case, it may be preferable to move the waveform into the scope's reference waveform storage, and perform a more critical inspection there. This can be accomplished by using the following process:

Select “Export to Ref Waveform” from the Options pull-down menu.

Once the reference waveform is transferred into the scope’s storage, minimize the DPOJET screens, so that only the scope UI is displayed. Turn on the scope cursors, and place across 10 cycles of the profile, as shown.



Using the scope's zoom function, it is possible to more closely inspect the placement of the cursors in making the measurement, as shown in the following image.



Again, it is necessary to divide the period by 10, then invert to get the modulation frequency, or alternatively multiply the 1/Δt value by 10 to get the modulation frequency.

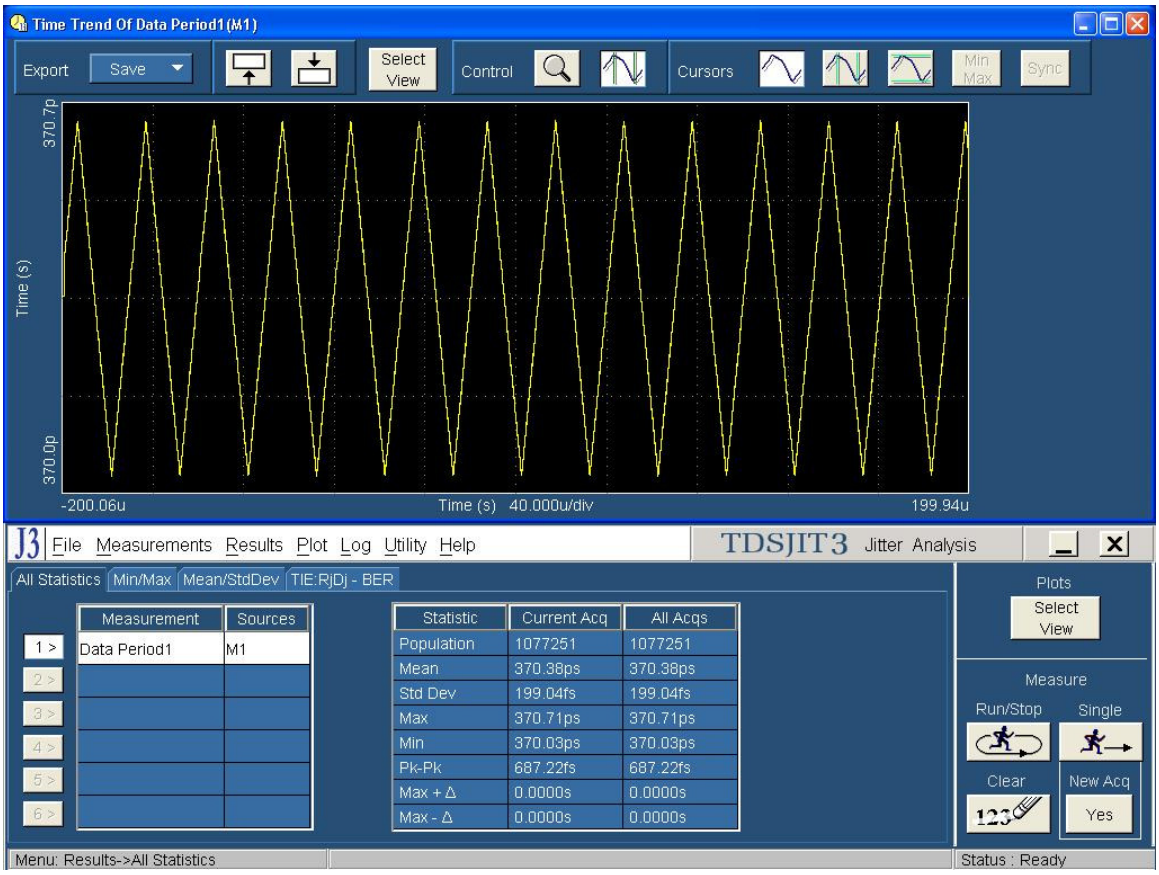
Using TDSJIT3:

Start the JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 recall the setup <3.15_SSC_Frequency.ini>.

Scope setup: 40µs/div, 40ps/pt (>1e6 UI)

Select Measurement: Data Period on Ch1 (P7380SMA probe)

(Alternatively, the test can be performed using matched cable pair; in this case select Measurement as Math1 = Ch1-Ch3) – shown in illustration below.

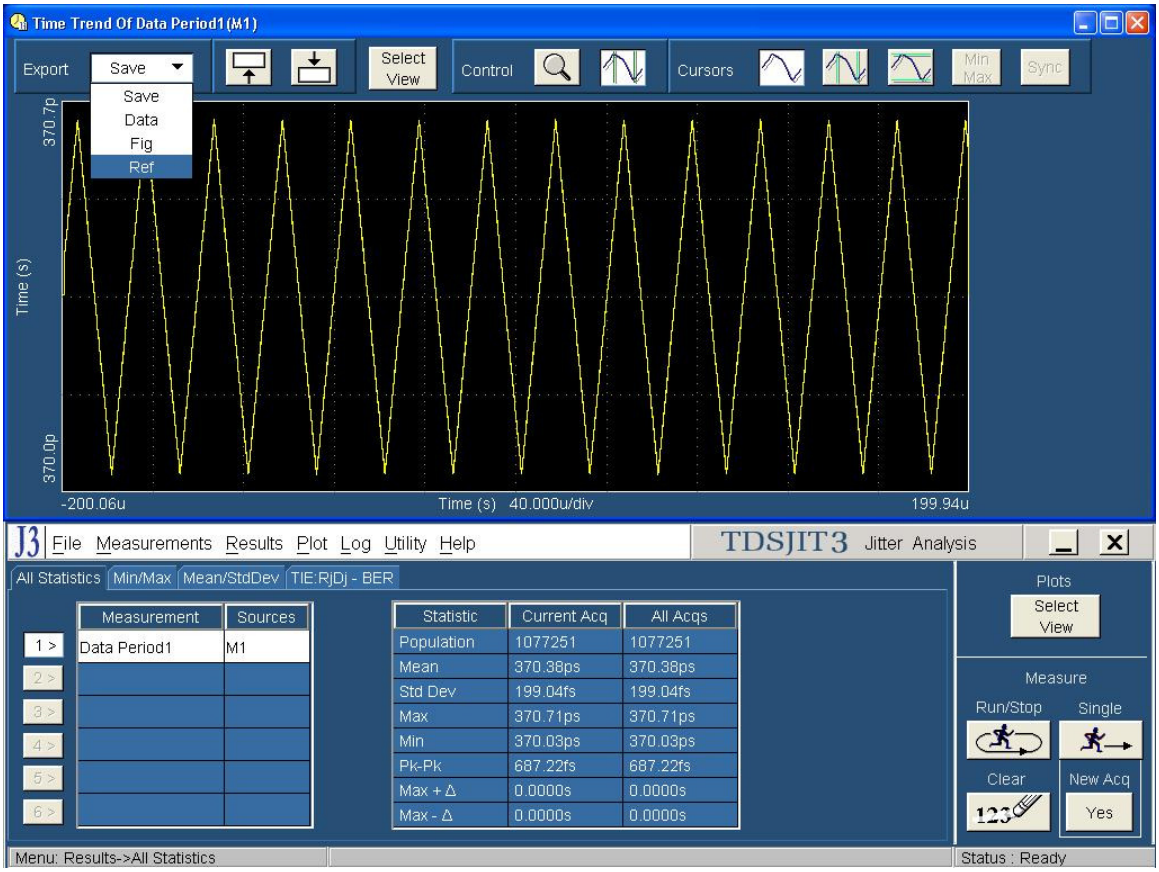


In some cases, it will be adequate to make the measurements using the cursor capability in JIT3 to measure the modulation frequency. Set cursors at the X axis crossing across 10 cycles. To arrive at the modulation frequency, take the delta time value, divide by 10, and invert to get frequency.

Note that there is often substantial higher frequency noise on this profile, and it may be difficult to discern the X axis measurement points on the profile. This is especially critical if the device is close to either limit. In this case, it may be preferable to move the

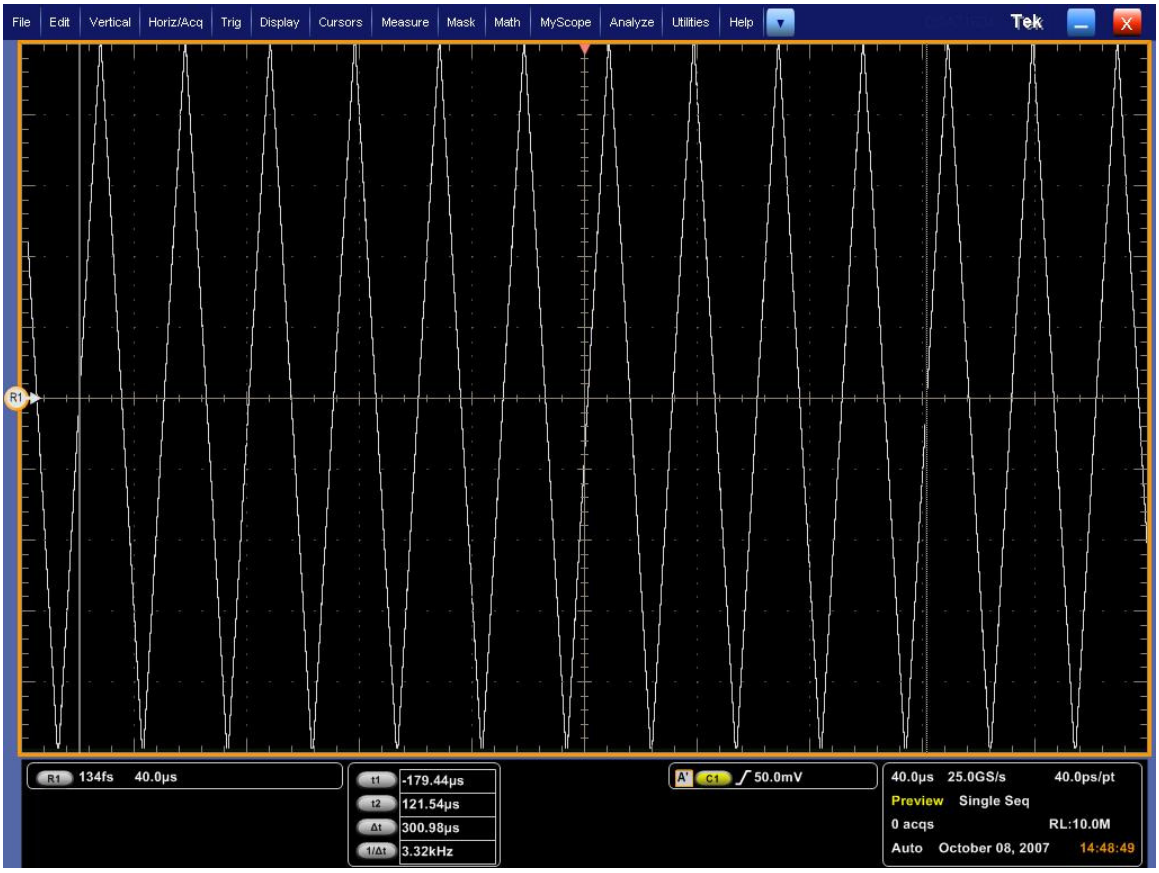
waveform into the scope's reference waveform storage, and perform a more critical inspection there. This can be accomplished by using the following process:

Use the Export: Save function in JIT3's plot screen, and select "Ref" from the pull-down menu.

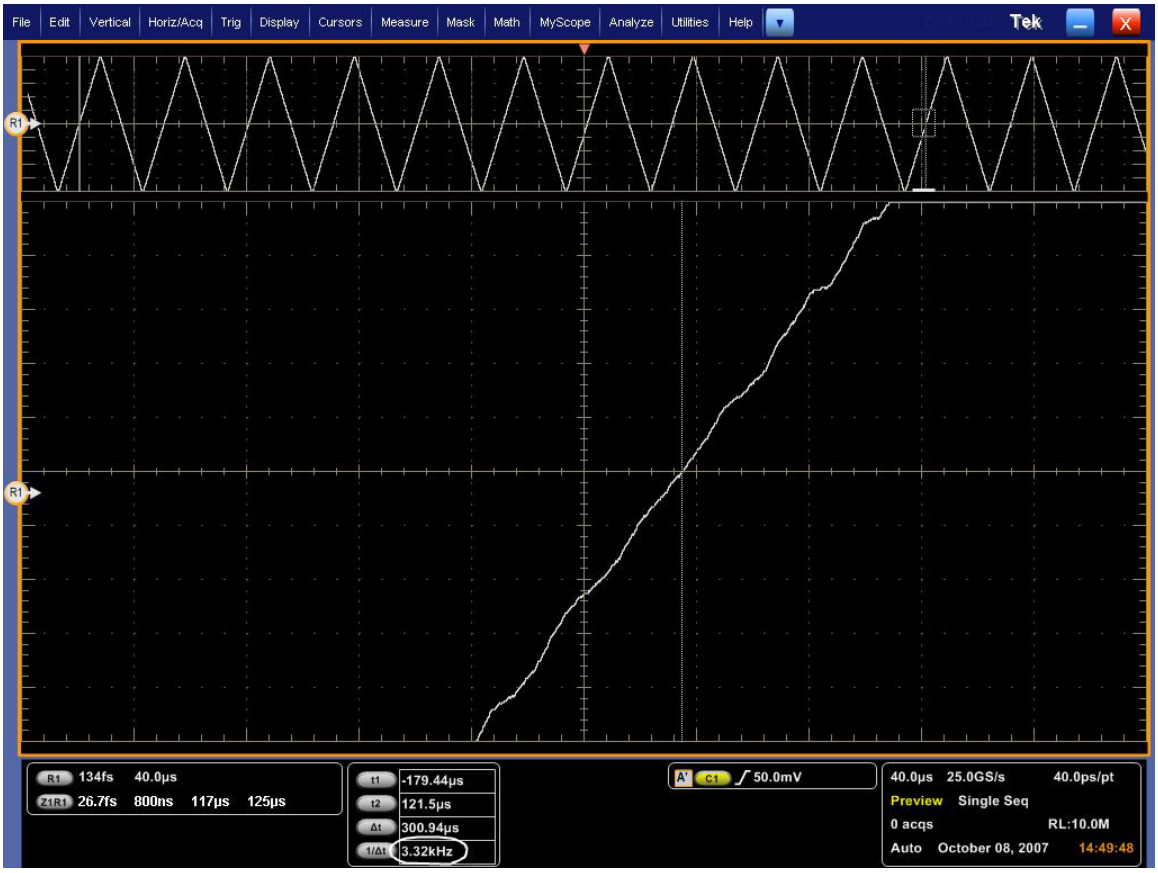


Once the reference waveform is transferred into the scope's storage, minimize the JIT3 screens, so that only the scope UI is displayed.

Turn on the scope cursors, and place across 10 cycles of the profile, as shown.



Using the scope's zoom function, it is possible to more closely inspect the placement of the cursors in making the measurement, as shown in the following image.



Again, it is necessary to divide the period by 10, and then invert to get the modulation frequency, or alternatively multiply the 1/Δt value by 10 to get the modulation frequency.

3.15.8 Pass/Fail Criteria:

f_{SSC} measured between 30kHz and 33kHz The value above shall be based on a mean of at least 10 complete SSC cycles

3.16 Spread Spectrum Modulation Deviation (Normative)

1.16.1 Test Objective

To evaluate the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [The device must] operate in the region of 0 to -5000PPM.

1.16.2 References

- Display Port Specification version 1.1 dated March 19 2007 and errata 3 document dated 29th Aug 2007 and errata 4 document dated Sept 6 2007.
- Display Port CTS draft 13 version 1 specifications dated July 20 2007 Section 3.16.

1.16.3 Test Conditions

The SSC Modulation Deviation will be evaluated at the highest bit rate the transmitter supports.

Tests shall be performed on a PRBS7 signal, with SSC enabled.
An evaluation of at least 10 full SSC cycles is required (Mean value reported).

1.16.4 Measurement Requirements

As SSC in Display Port is mandatory, the reported result must be the mean of ten measured maximum values from the range of SSC modulation deviation.
The value reported as the result must be the single total range value relative to nominal of the SSC modulation deviation, using the equation below, where “Max” is the mean of 10 recorded values of the maximum peaks.
Calculate deviation = (Measured Max – Nominal)/Nominal * 1e6 ppm
(Note: this procedure uses the “Max” value instead of “Min”)

1.16.5 Test equipment required

Refer to Appendix A of this MOI.

1.16.6 Connection Diagram

Refer to Appendix B of this MOI.

1.16.7 Detailed Procedure

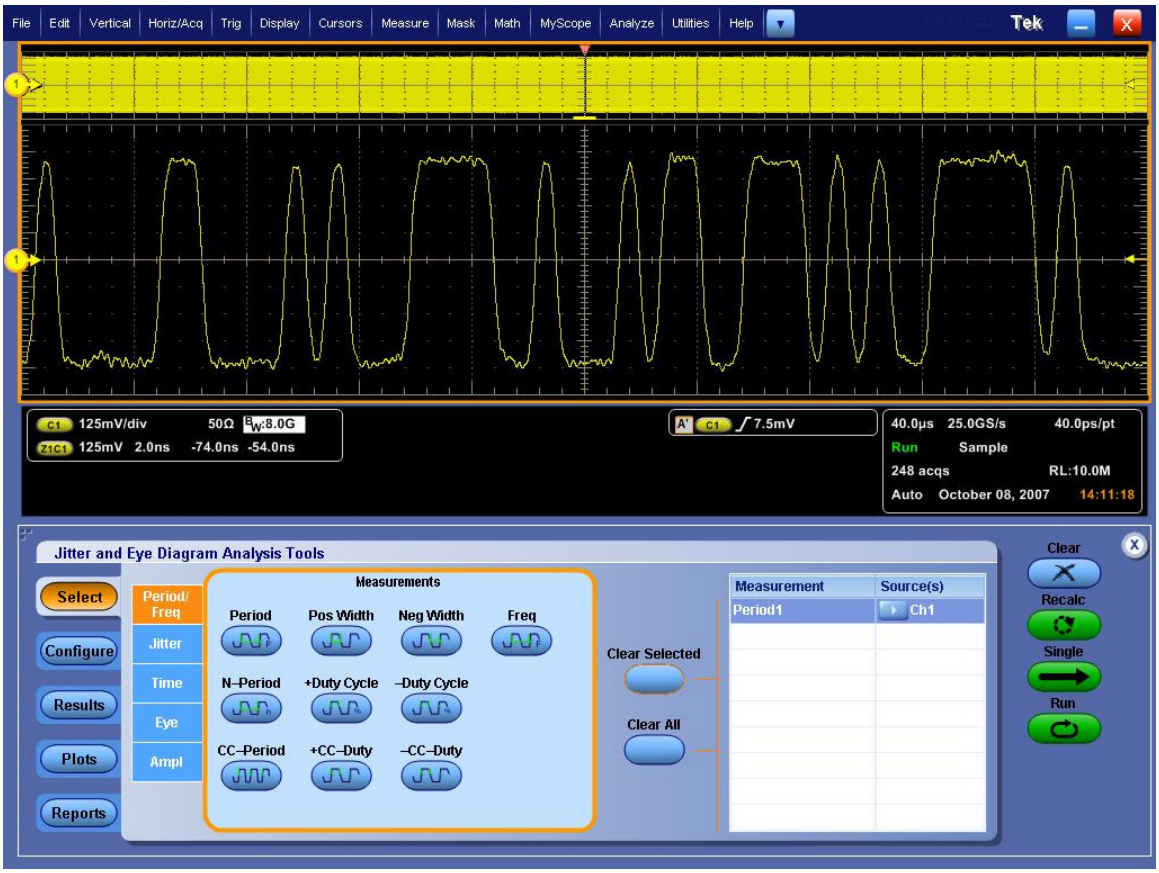
Using DPOJET:

In the scope recall the setup 'Spread Spectrum Modulation Deviation' <3.16_SSC_Deviation.set> and open the DPOJET application in Analyze → DPOJET → Select

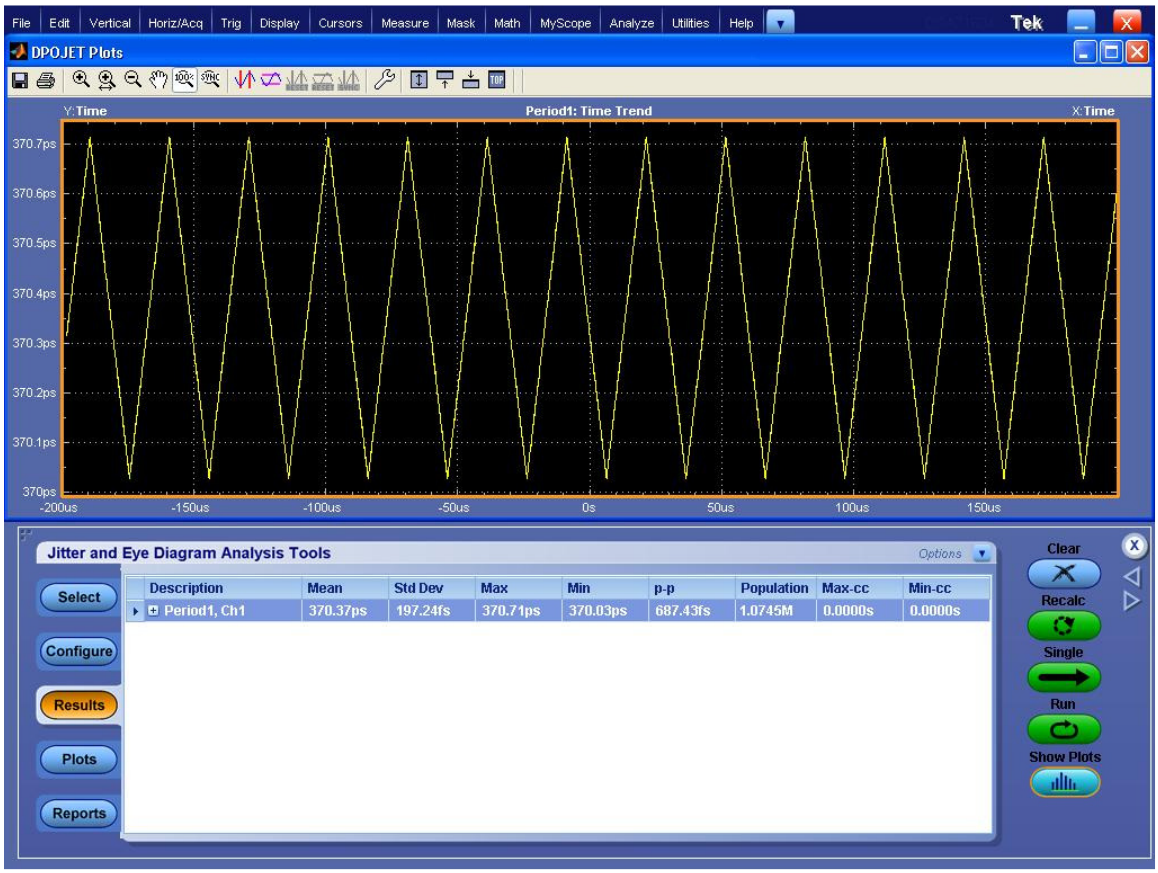
Scope setup: 40µs/div, 40ps/pt (>1e6 UI)

Select Measurement: Data Period on Ch1 (P7380SMA probe)

(Alternatively, the test can be performed using matched cable pair; in this case select Measurement as Math1 = Ch1-Ch3)



Follow the procedure described for test 3-14, up to the point where the profile has been created.

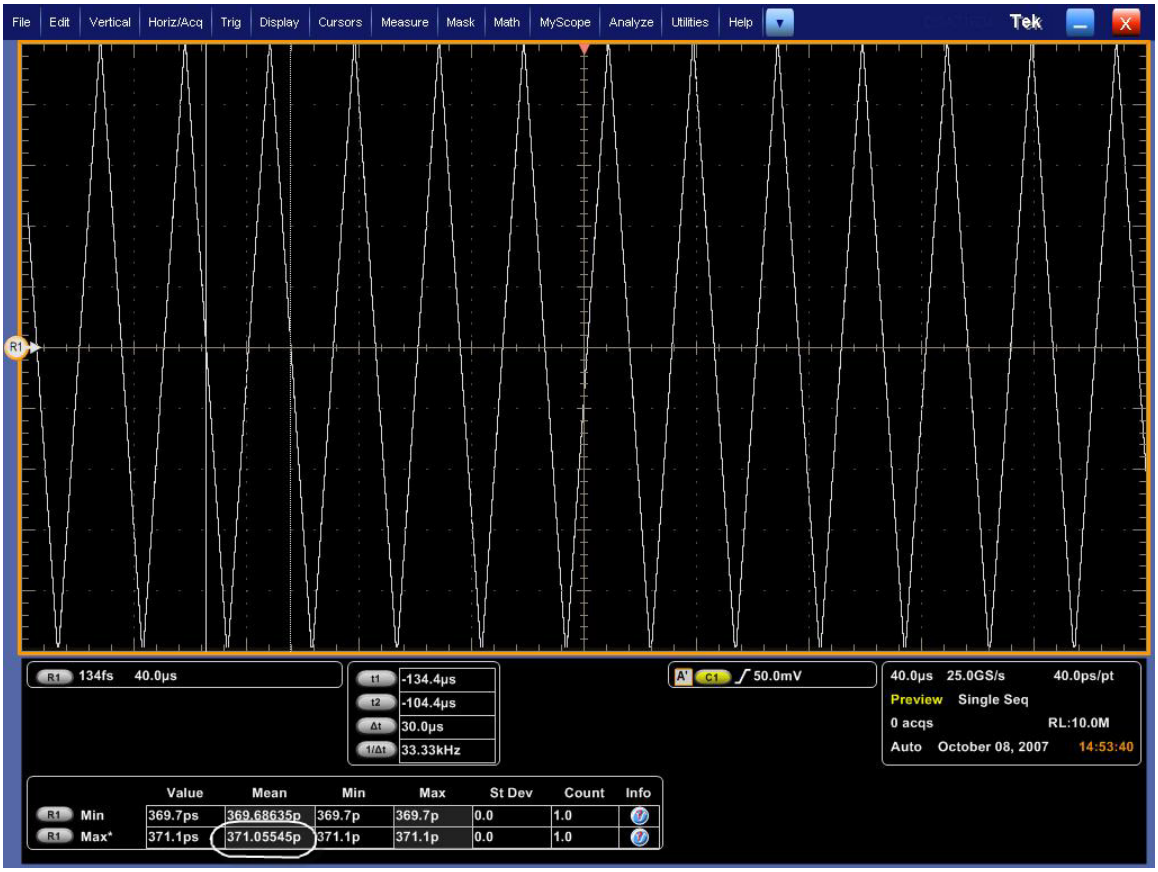


NOTE: The DPOJET software provides the ability to do cursor measurements directly on the profile plot. However, the 4 digits of resolution obtained when using DPOJET cursor measurements (1000 ppm) is not sufficient for this test.
The value can also be read directly from the statistics table as seen in the previous figure. This data is shown as 5 digits, and provides a 100 ppm resolution, which is marginally adequate for the 300ppm measurement tolerance. For test 3-14, use the Min value (min period=max freq)..

To get 8 digits of resolution, select “Export to Ref Waveform” from the Options pull-down menu.

This transfers the Period Profile into the scope’s Ref waveform memory.

Using the same technique described in test 3-14, record each of the 10 max period peak points. Average these values to determine the Measured mean Max period.



Using TDSJIT3:

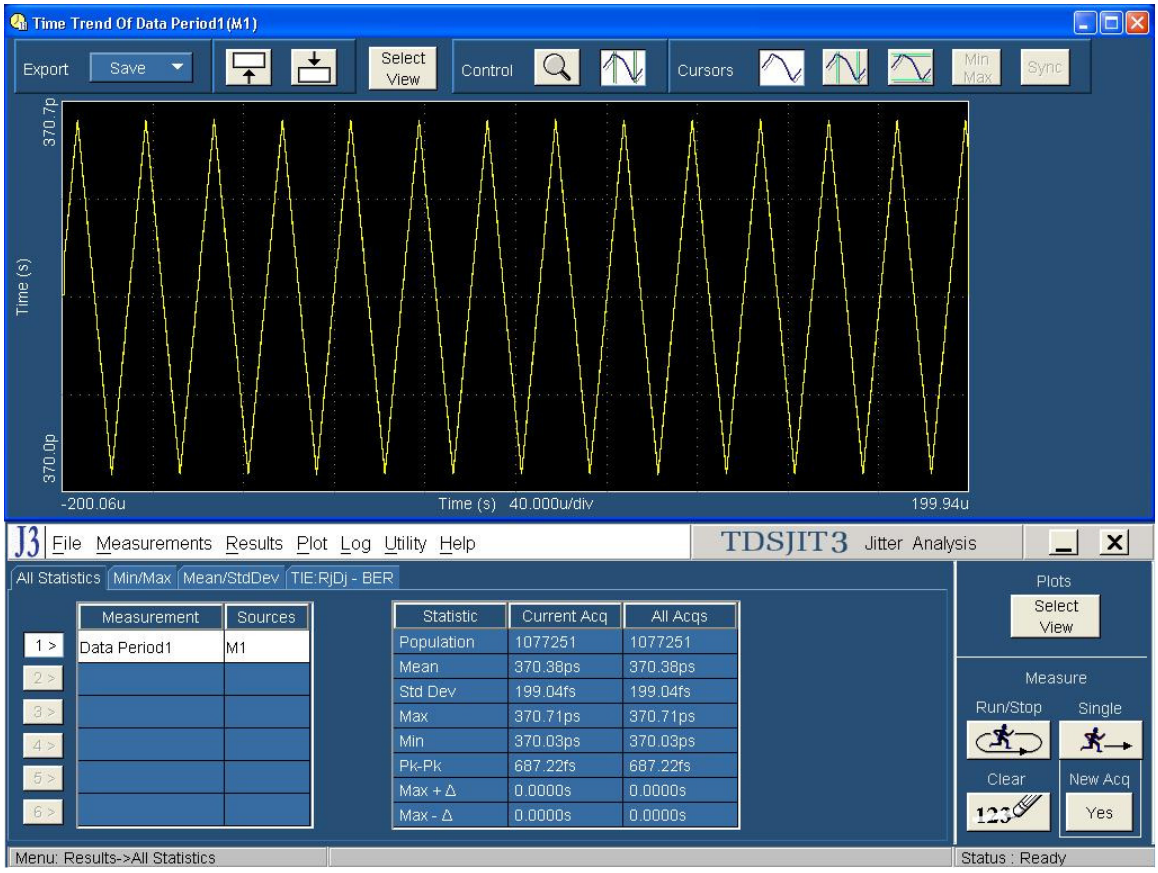
Start the JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 recall the setup <3.16_SSC_Deviation.ini>.

Scope setup: 40µs/div, 40ps/pt (>1e6 UI)

Select Measurement: Data Period on Ch1 (P7380SMA probe)

(Alternatively, the test can be performed using matched cable pair; in this case select Measurement as Math1 = Ch1-Ch3) – shown in illustration below.

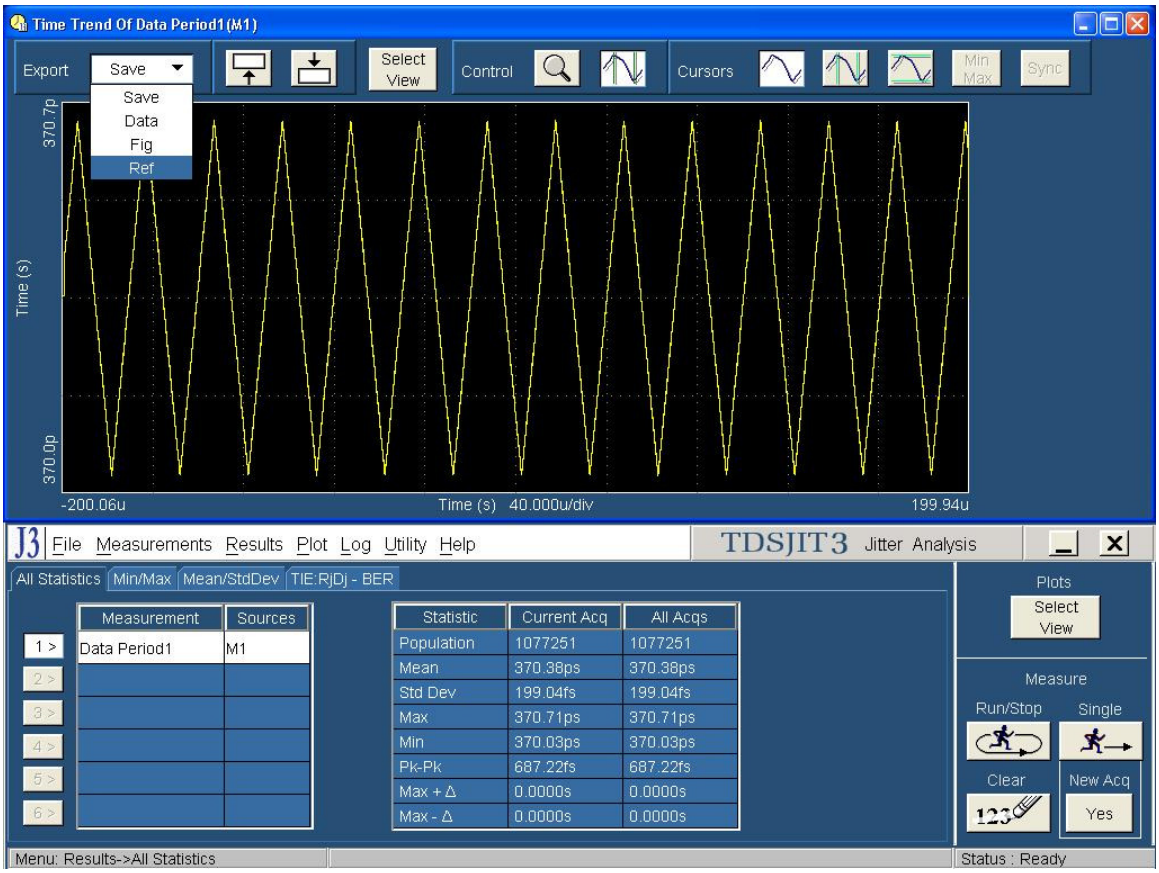
Follow the same procedure as described in test 3-14.



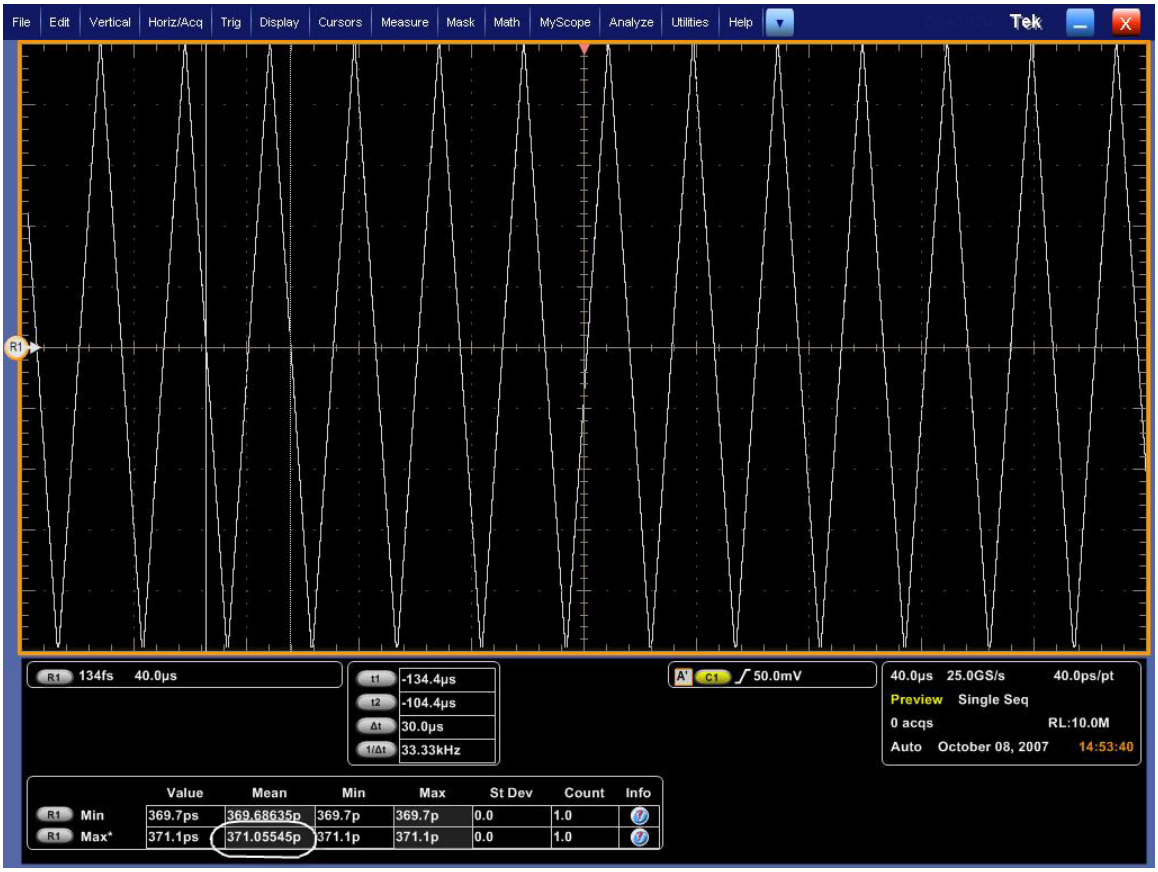
NOTE: The TDSJIT3 software provides the ability to do cursor measurements directly on the profile plot. However, the 4 digits of resolution obtained when using JIT3 cursor measurements (1000 ppm) is not sufficient for this test.

The value can also be read directly from the statistics table as seen in the previous figure. This data is shown as 5 digits, and provides a 100 ppm resolution, which is marginally adequate for the 300ppm measurement tolerance. For test 3-16, use the Max value shown in the "Current Acq" column.

To get 8 digits of resolution, use the Export: Save function in JIT3's plot screen, and select "Ref" from the pull-down menu. This transfers the Period Profile into the scope's Ref waveform memory.



Using the same technique described in 3-14, record each of the 10 max period peak points. Average these values to determine the Measured Mean Max period.



Calculate deviation = (Nominal – Measured Mean Max Period)/Nominal * 1e6 ppm where

Nominal is 370.3704 ps for HBR devices and 617.2840 ps for RBR devices.

1.16.8 Pass/Fail Criteria

SSC_{tol} measured (using mean of 10 recorded values) between -5000ppm and +0ppm.

3.17 dF/dt Spread Spectrum Deviation HF Variation (Informative)

- Informative test, not included in this version.

APPENDIX A:

Test Equipment list

Product	Description	Quantity
Oscilloscope	Tektronix Real Time DSA/DPO70000 or TDS6804B/TDS6124C/TDS6154C 8GHz or above (required bandwidth as per the Compliance Test Specification) captures the 5th harmonic of the 1.35GHz fundamental	1
Software [1, 2]	DPOJET Jitter and Eye Diagram Analysis Tool or RT-Eye Serial Data Compliance and Analysis Software and TDSJIT3 Advanced Jitter Timing and Analysis software	1
SMA Probe [3]	P7380SMA	1
Test Fixtures	TPA-P and TPA-R fixtures from Efficere Technologies. Order a set as ET-DP-TPA-S	1 set

[1] DPOJET Advanced required for eye diagram test analysis.

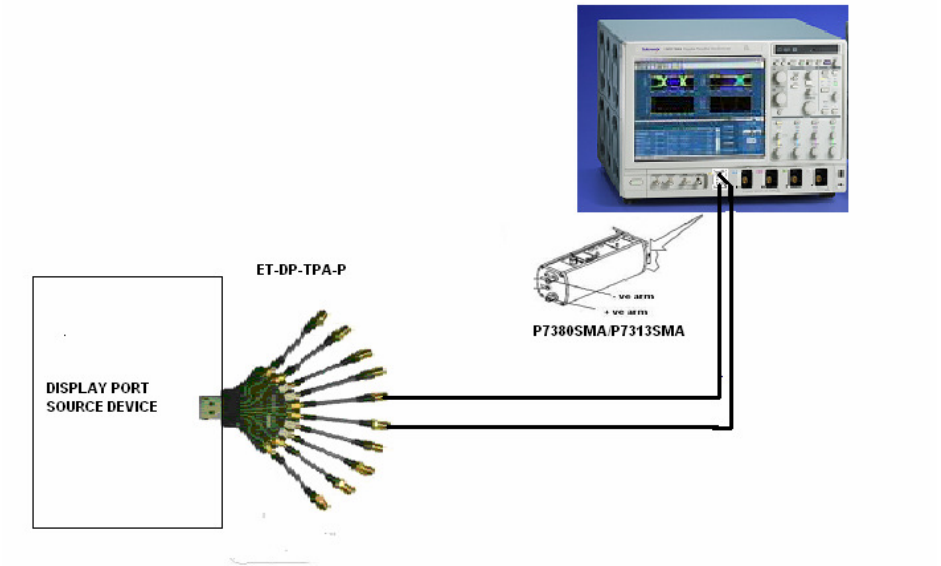
[2] DSA70000 includes TDSRT-Eye and TDSJIT3 Advanced standard whereas both are optional on the DPO70000/TDS6000 series.

[3] P7380SMA required for test 3-2 and 3-3 (Non Pre-emphasis and Pre-emphasis level verification).

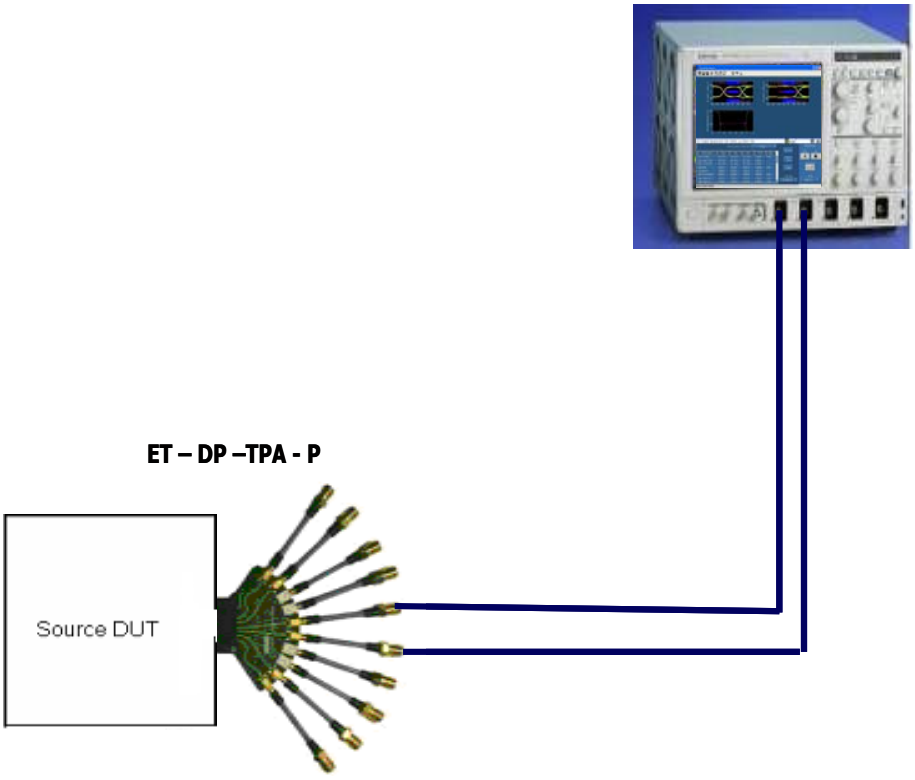
APPENDIX B:

Connection Diagram

Transmitter Test Setup 1 (with diff probe):



Transmitter Test Setup 2 (with matched cable set):



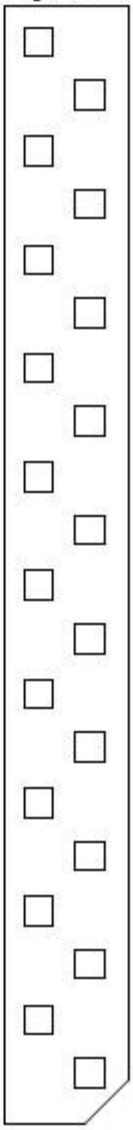
DP fixture pin-out details

Connector Pin Assignments

Display Port Plug & Receptacle Pin Assignments		
Pin Description	Connector Pin Number	Destination Number
ML_Lane 0 (p) - Source ML_Lane 3 (n) - Sink	1	J1
Ground	2	Ground
ML_Lane 0 (n) - Source ML_Lane 3 (p) - Sink	3	J2
ML_Lane 1 (p) - Source ML_Lane 2 (n) - Sink	4	J3
Ground	5	Ground
ML_Lane 1 (n) - Source ML_Lane 2 (p) - Sink	6	J4
ML_Lane 2 (p) - Source ML_Lane 1 (n) - Sink	7	J5
Ground	8	Ground
ML_Lane 2 (n) - Source ML_Lane 1 (p) - Sink	9	J6
ML_Lane 3 (p) - Source ML_Lane 0 (n) - Sink	10	J7
Ground	11	Ground
ML_Lane 3 (n) - Source ML_Lane 0 (p) - Sink	12	J8
Ground	13	Ground
Ground	14	Ground
AUX_CH (p) - Source AUX_CH (p) - Sink	15	J9
Ground	16	Ground
AUX_CH (n) - Source AUX_CH (n) - Sink	17	J10
Hot Plug Detect	18	P2 Pin 1
Return DP_PWR	19	P2 Pin 3
DP_PWR	20	P2 Pin 2
Ground	2, 5, 8, 11, 13, 14, 16	P2 Pin 4

Connector End View

Looking into connector



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