Multi-lane PCIe tester delivers results in minutes not hours

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PCIe testing normally requires complex test systems and engineers with deep expertise and knowledge. Moreover, it takes hours or even days of setup and testing, often stretching costs to seven figures. A new test solution claims to break the conventions of PCIe testing by delivering test results in minutes while offering a combination of plug-and-play setup and easy-to-use interface.

TMT4 Margin Tester—a specialized testing tool for the design and validation of PCIe Gen 3 and Gen 4 motherboards, add-in cards, and system designs—enables engineers at all levels of experience to evaluate the health of transmitter (Tx) and receiver (Rx) links faster than ever. It supports the majority of common PCIe form factors—including CEM, M.2, U.2, and U.3—with testing capabilities of up to 16 lanes across PCIe presets 0-9 while using a single standard connector.

Full Tx/Rx protocol capability enables link health evaluation of PCIe Gen 3 and Gen 4 communications on both sides of the link in a single box. Source: Tektronix

Tektronix's TMT4 Margin Tester is built on the Intel Stratix 10 FPGA with PCIe. Rina Raman, VP and GM of DCAI for Embedded Acceleration Division at Intel, acknowledges that the results are available substantially faster, in most cases, in minutes rather than hours. Raman also pointed to TMT4's ability to identify design issues much earlier in the design process.

Test engineers can conduct the earlier and more frequent evaluations of board- or system-level link health during design and validation. According to Chris Witt, VP and GM of Portfolio Solutions at Tektronix, the TMT4 tester is intended to complement full validation and compliance testing systems consisting of oscilloscopes and BERTs. "It can uncover issues earlier in the design process before an in-depth examination using traditional equipment."

TMT4's simplified setup and configuration aim to minimize the need for senior-level engineers to perform link health evaluations. Next, its multi-lane testing capabilities enable users to significantly improve overall testing times by reducing the number of connection changes needed to perform testing.

In TMT4 Margin Tester, Quick Scan mode enables evaluation of link health for Gen 3 or Gen 4 devices for up to 16 lanes. Then there is Custom Scan mode that provides deeper insights by allowing users to scan Gen 3 or 4 devices for up to 16 lanes across PCIe presets 0-9 with up to 160 combinations in as little as 20 minutes.

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