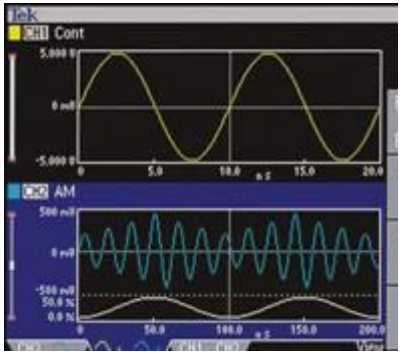
Compliance test method and detailed spec for USB3.0

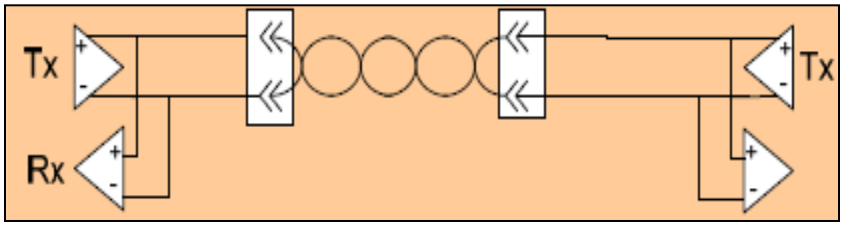


Tektronix Korea

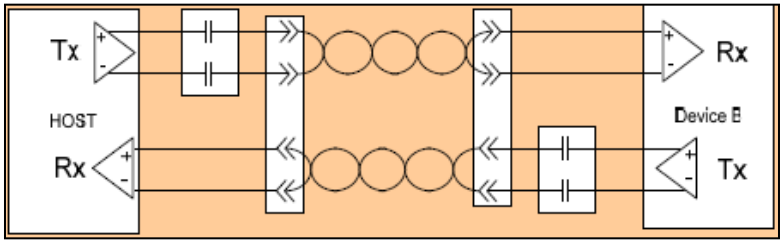
KEVIN.PARK

Differences from USB2.0

- High-Speed
  - 480MT/s
  - No-SSC
  - 2 wires for signaling
    - Tx and Rx use the same wire
    - 1 bi-directional link
  - DC coupled bus
  - NRZ encoding



- SuperSpeed
  - 5.0GT/s (10X speed increase)
  - SSC is required
  - Equalization/CTLE are required
  - 4 wires for signaling
    - 2 for Tx and 2 for Rx
    - Each Uni-directional
  - AC Coupled bus
  - 8b/10b Encoded

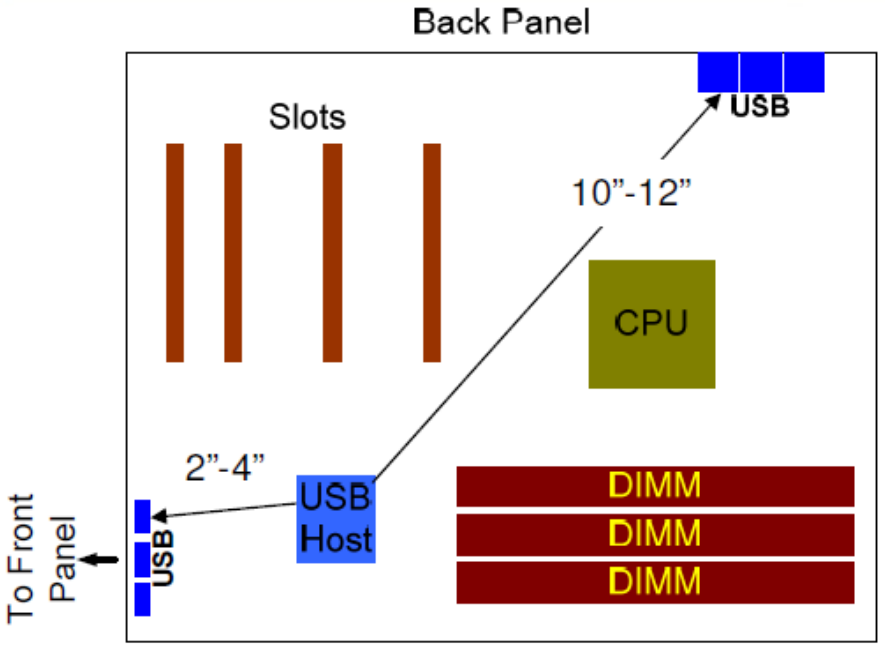


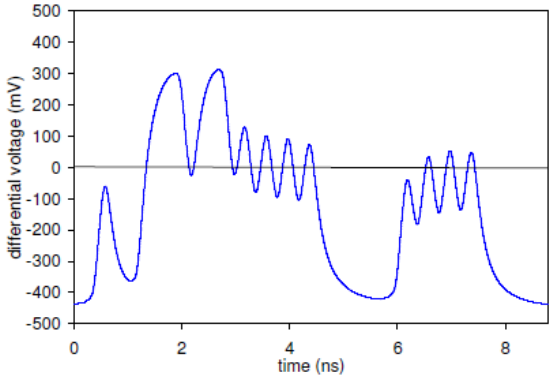
Source: USB-IF

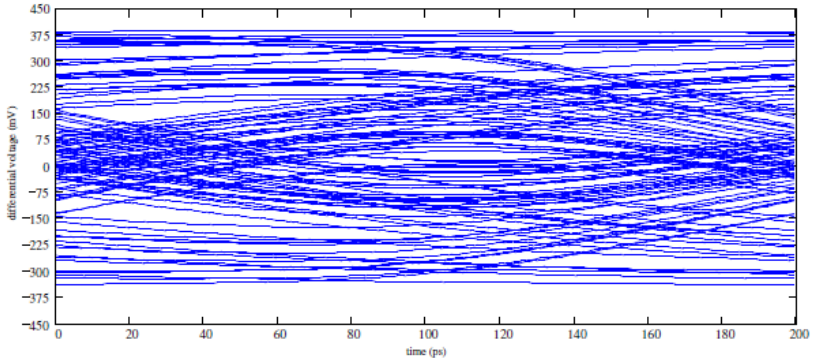
Tektronix

USB 3.0 Key Considerations – Long Channel

- Channel characteristics
  - 2” ~ 12” Host channel
  - 1” ~ 6” Device channel
  - 0m ~ 3m Cable
- Cause Frequency dependent loss (ISI) and Crosstalk
- Close the 5Gb/s eye



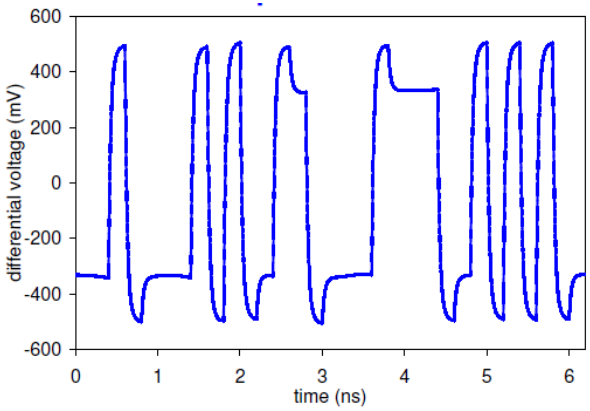


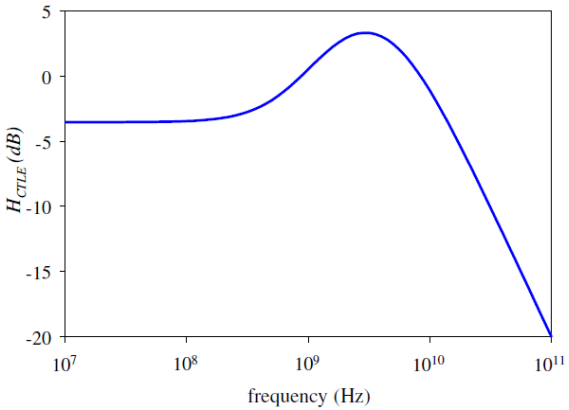


Source: USB DevCon

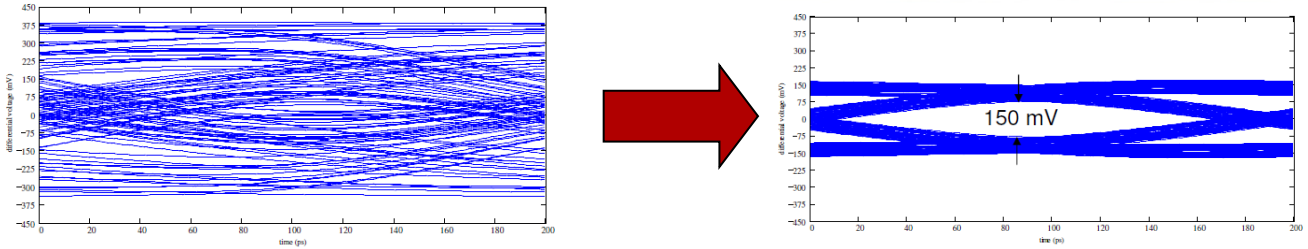
Tektronix

USB 3.0 Key Considerations – Equalization





- Transmitter Equalization
  - 3.5±0.5dB de-emphasis
- Receiver Equalization
  - Continuous Time Linear Equalizer (CTLE)



- Enable to open the Receiver eye

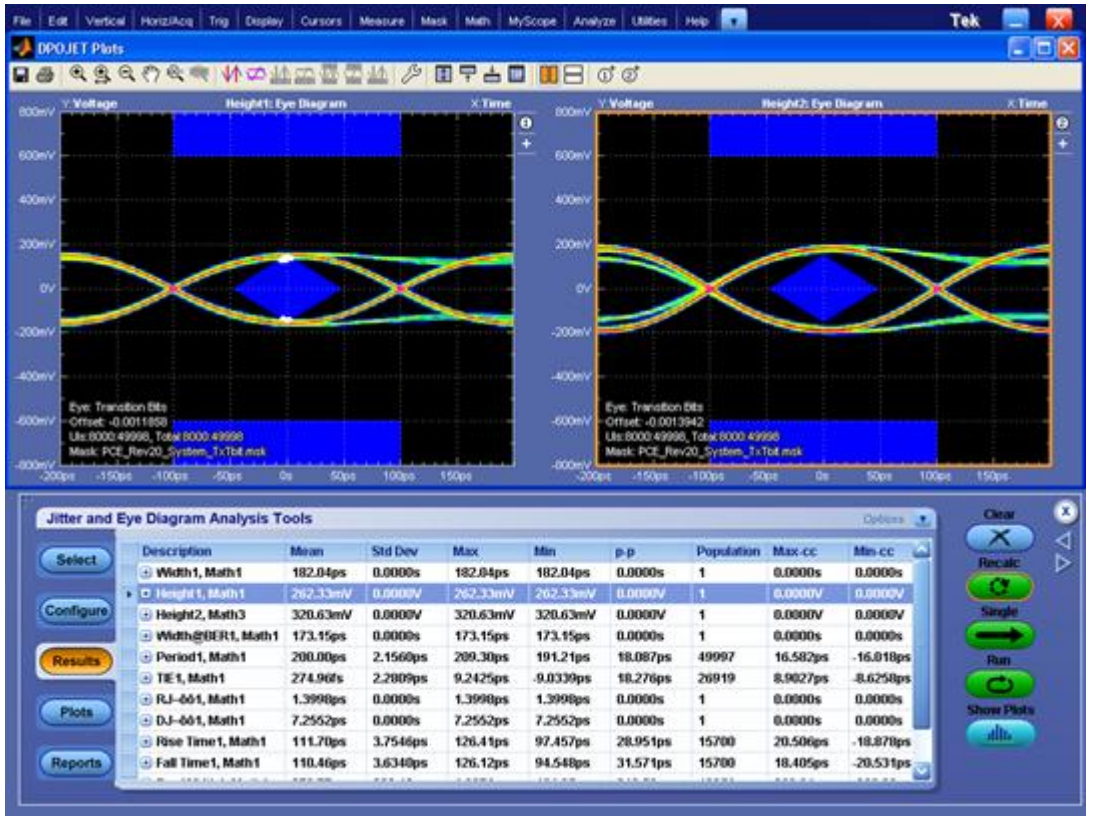
Source: USB DevCon

Tektronix

Fixture and Channel De-Embedding

- Why de-embed- Improve Margin
  - Removes fixture effects that are not present in a real system
  - Remove the effects of the channel and connector for measurements defined at the TX pins
- De-Embedding Process
  - Characterize channel with TDR or Simulator to create S-parameters
  - Create de-embed filter with SDLA software

Before → **After**



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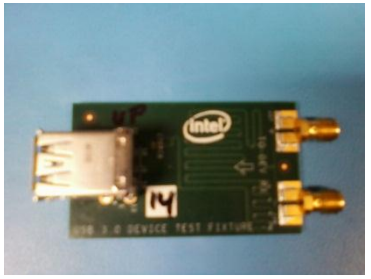
Channel Embedding

- Compliance Testing is done by embedding the compliance channel, but many designers want to validate other channel models
  - Understand transmitter margin given worst case channels
  - Model channel and cable combinations beyond compliance requirements
  - Create interconnect models with SDLA software to analyze channel effects



USB-IF Host & Device HW Channels

Transmit Channel

Universal Serial Bus 3.0 Specification, Revision 0.9

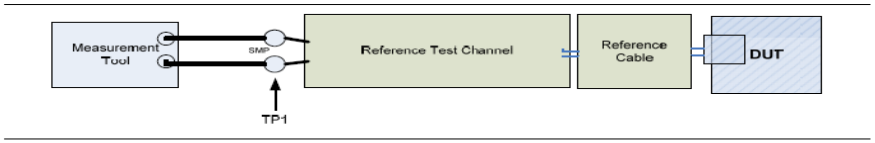


Figure 6-14. Tx Normative Setup with Reference Channel

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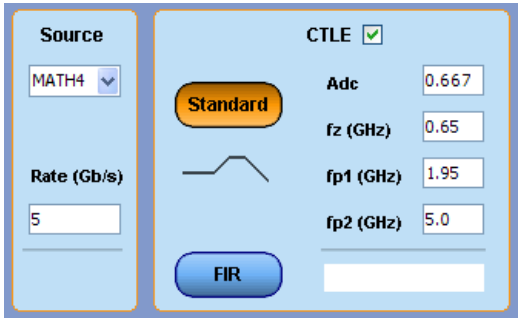
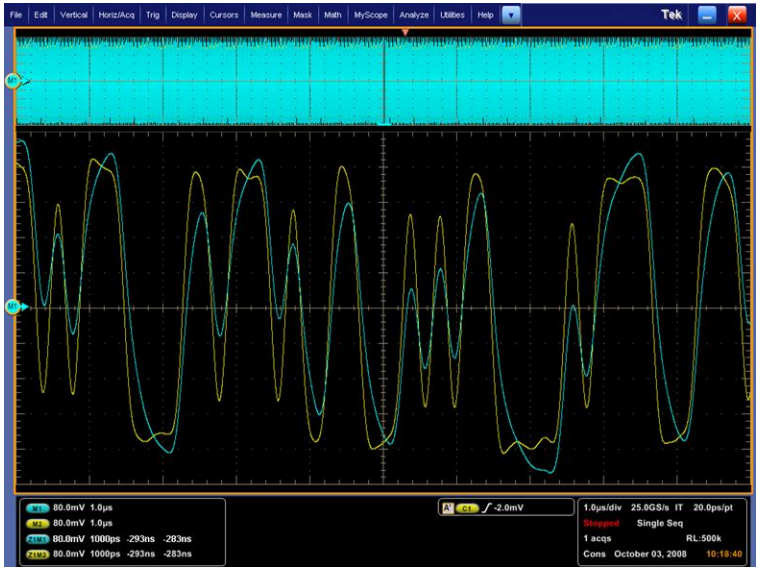
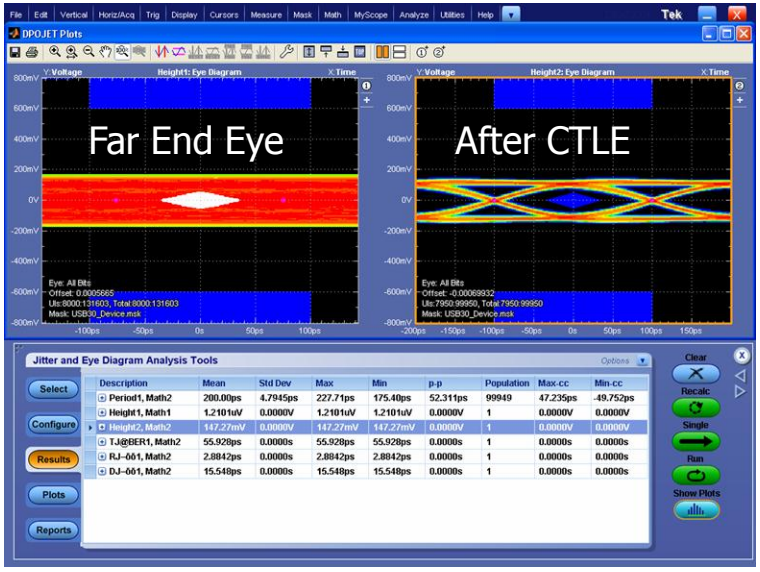
Receiver Equalization

- Tektronix USB Solutions ships with the USB Specification defined CTLE Function
- Customizing CTLE functions and creating filters for use with Tektronix' USB Solution is easily achieved with SDLA (Serial Data Link Analysis Software)







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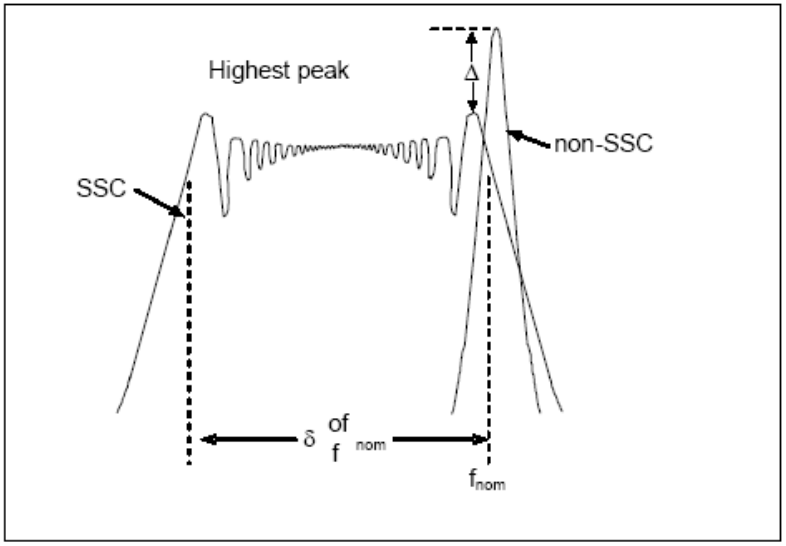
USB 3.0 Key Considerations – SSC

- SSC(Spread Spectrum Clocking)
  - The technique of modulating the operating frequency
  - Spread its radiated emissions over a range of frequencies
  - Reduction in the maximum emission for a given frequency
  - Meet radiated emission requirements

- EX) USB3.0, SATA, PCIe, DP, etc.
  - 30~33KHz, 0.5% Down Spread
  - 200.0psec~201.0psec Period for 5Gbps USB3.0



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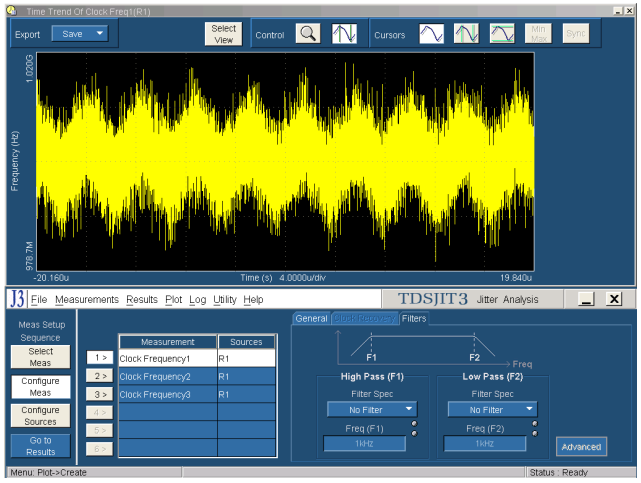
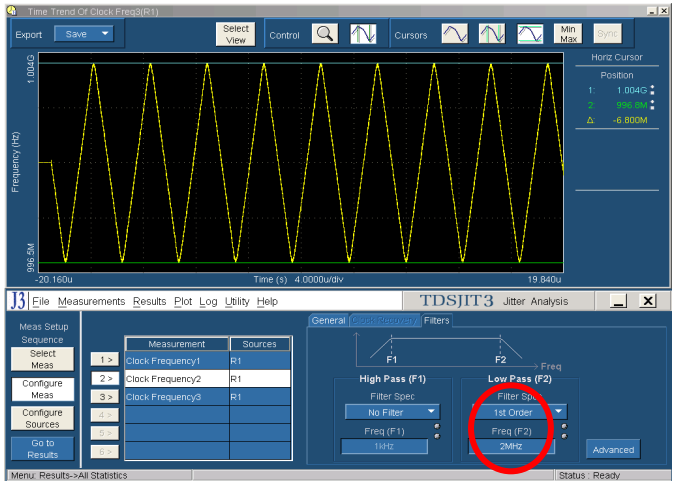
USB 3.0 Key Considerations – SSC

- FM modulation with Jitter
  - Can not see modulation feature because of the HF noise
  - Modulation Rate? Modulation Center Frequency?
  - Implement 2MHz 1st order LPF

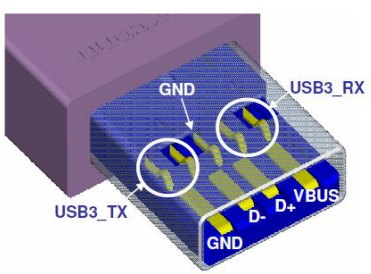


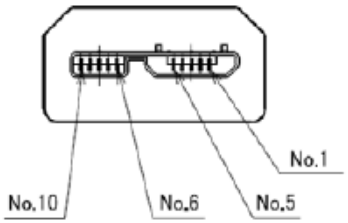


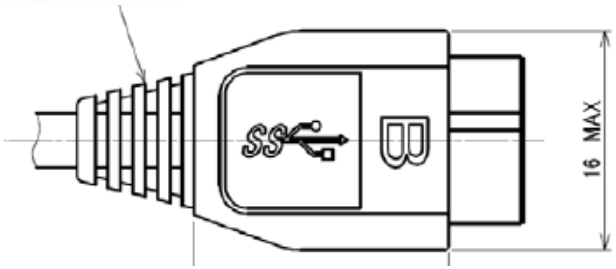
Tektronix

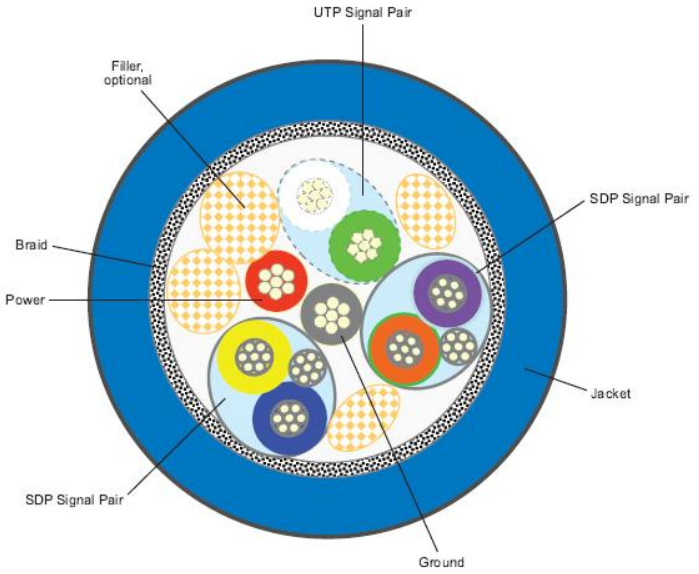
USB 3.0 Key Considerations – Connector & Cable

- Connector objective
  - Support 5Gbps
  - Backward compatible with USB2.0
- Connector Type
  - USB3.0 Standard-A Plug and Receptacle
  - USB3.0 Standard-B Plug and Receptacle
  - USB3.0 Powered-B Plug and Receptacle
  - USB3.0 Micro-B Plug and Receptacle
  - USB3.0 Micro-A Plug (OTG only)
  - USB3.0 Micro-AB Receptacle (OTG only)
- New Feature
  - 2 additional Differential Pairs and one GND
  - Blue color housing for Standard-A
  - Powered-B enable device to provide a power (Ex. Printer with Wireless USB adapter)
- Cable
  - UTD for USB2.0
  - SDP (Shielded Differential Pair) for SuperSpeed









Source: USB 3.0 Rev 1.0 Specification

Connecting to the Host/Device Under Test

- For Host Tx/Rx Testing
  - Host Test Fixture 1
  - Host Test Fixture 2
  - General cable(Tx test)
  - 3m cable(Rx Test)

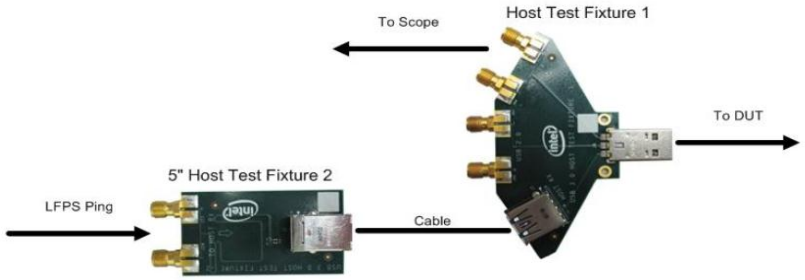


Figure 6: Host Tx Test Topology

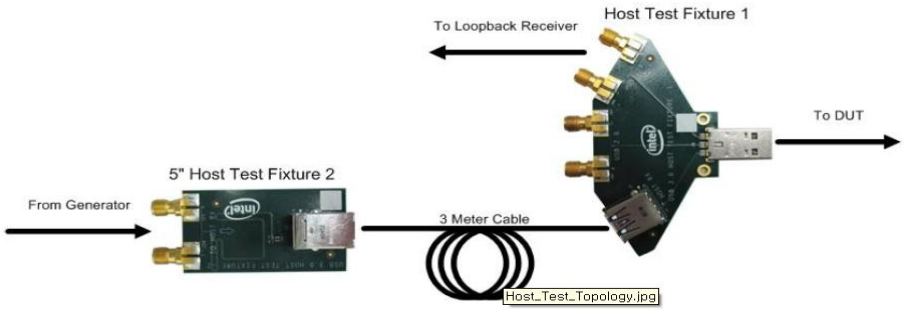


Figure 3: Host Rx Test Topology

- For Device Tx/Rx Testing
  - Device Test Fixture 1
  - Device Test Fixture 2
  - General cable&8”cable (Tx Test)
  - 3m cable, 8”cable(Rx Test)
  - 5V Dc Voltage Adapter

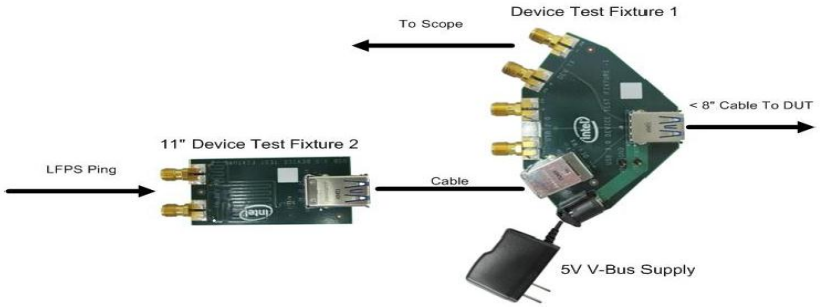


Figure 5: Device Tx Test Topology

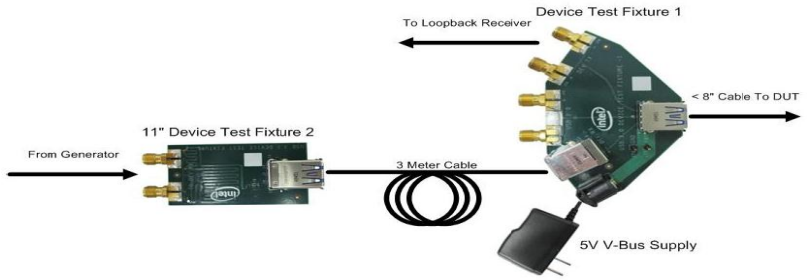


Figure 4: Device Rx Test Topology

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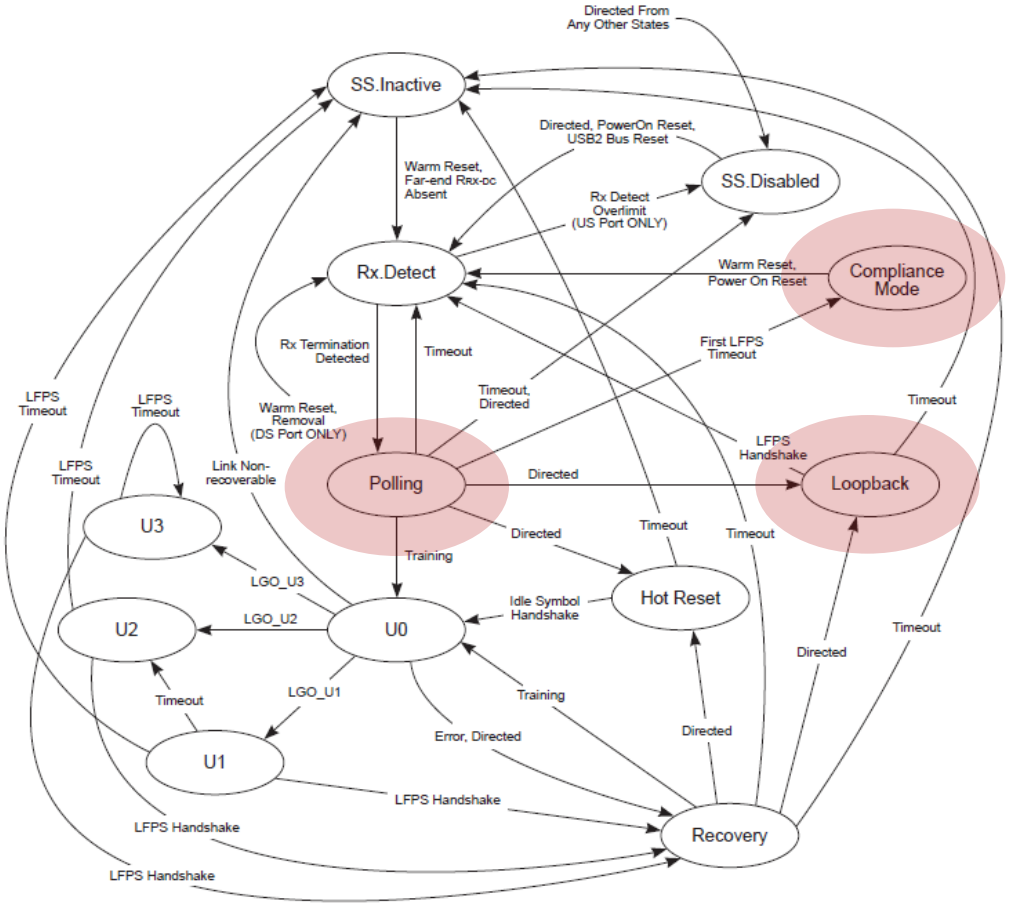
LTSSM – Link Training and Status State Machine



Note: Transition conditions are illustrative only. Not all of the transition conditions are listed.

U-047

Figure 7-13. State Diagram of the Link Training and Status State Machine

- 12 different link states
- U0/U1/U2/U3
  - Link enabled/disabled/suspended states
- Rx.Detect/Polling/Recovery/Hot Reset
  - Link initialization/Training/Reset
- Loopback/Compliance
  - Rx/Tx Loopback/compliance test
- SS.Inactive/SS.Disabled
  - Link Error/USB2.0

Tektronix

Entering to Compliance Mode for Transmitter

- Polling is a state for Link Training
- Bit lock/Symbol lock/Rx equalization training using TSEQ/TS1/TS2
- Polling.LFPS is a substate to synchronize the operation
- Exit to Polling.RxEQ
  - 16 Polling.LFPS are sent
  - 2 Polling.LFPS are received
  - 4 Polling.LFPS are sent
- Exit to Compliance Mode
  - Doesn't complete Polling.LFPS during 360msec timeout

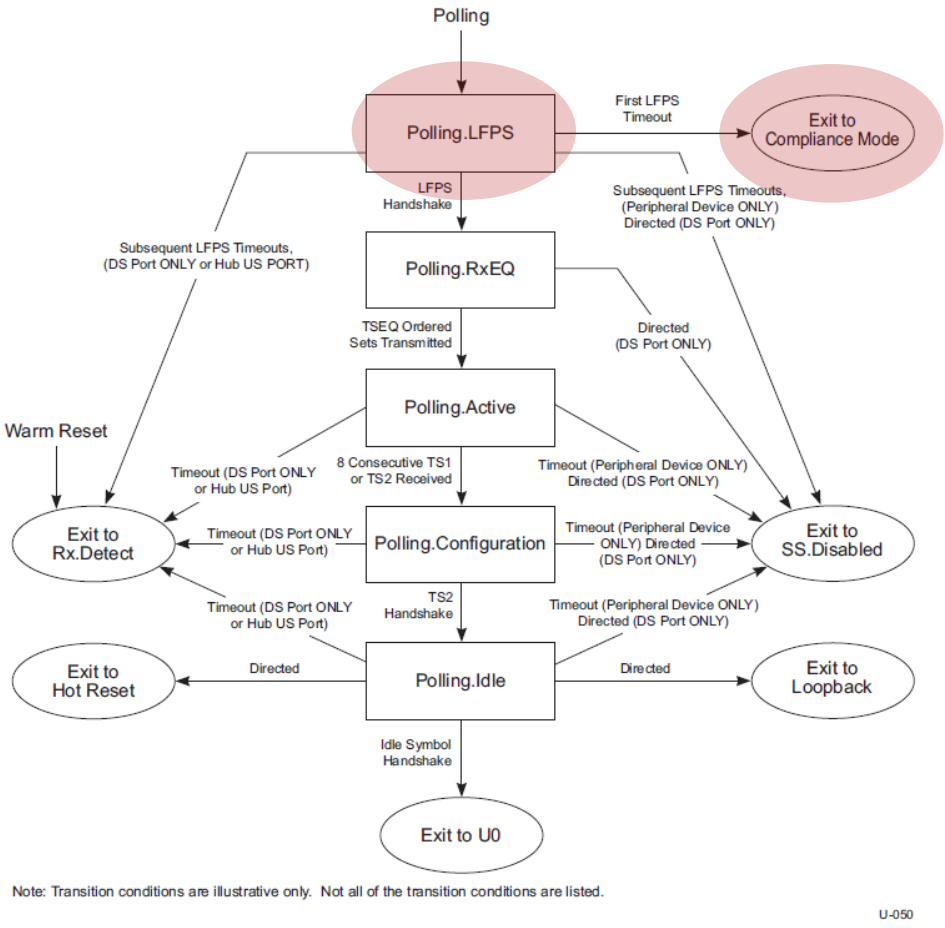


Figure 7-16. Polling Substate Machine

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Compliance Pattern

Table 6-7. Compliance Pattern Sequences

Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1's and 0's	With de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP8	50-250 1's and 0's	With without de-emphasis. Repeating 50-250 1's and then 50-250 0's.

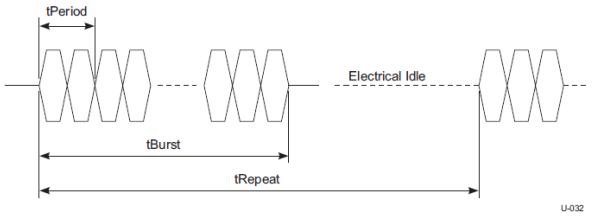


Figure 6-20. LFPS Signaling

Table 6-21. LFPS Transmitter Timing[1]

	tBurst				tRepeat		
	Min	Typ	Max	Minimum Number of LFPS Cycles[2]	Min	Typ	Max
Polling.LFPS	0.6 µs	1.0 µs	1.4 µs		6 µs	10 µs	14 µs
Ping.LFPS	40 ns		200 ns	2	160 ms	200 ms	240 ms
tReset[3]	80 ms	100 ms	120 ms				
U1 Exit[4,5]	300 ns		900 ns/2 ms[6]				
U2 / Loopback Exit[4,5]	80 µs[7]		2 ms				
U3 Wakeup[4,5]	80 µs[7]		10 ms				

Symbol	Minimum	Typical	Maximum	Units	Comments
tPeriod	20		100	ns	

- 360msec timeout initiates CP0 scrambled D0.0 PRBS pattern
- With Ping.LFPS, pattern shall advance to the next pattern
- Tx compliance requests CP0 and CP1
- AWG or Scope Trigger-output generate Ping.LFPS

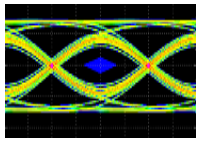
Tektronix

SuperSpeed Tx compliance

- Measurements at TP1
- Requires HW Reference Cable and Test Channel
- …or TP1' with Transmit Path Channel Emulation

Table 6-12. Normative Transmitter Eye Mask at Test Point TP1

Signal Characteristic	Minimal	Nominal	Maximum	Units	Note
Eye Height	100		1200	mV	2, 4
Dj			0.43	UI	1,2,3
Rj			0.23	UI	1,2,3, 5
Tj			0.66	UI	1,2,3



CTLE

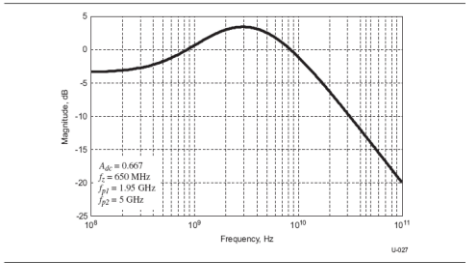


Figure 6-17. Tx Compliance Rx EQ Transfer Function

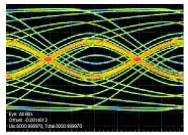
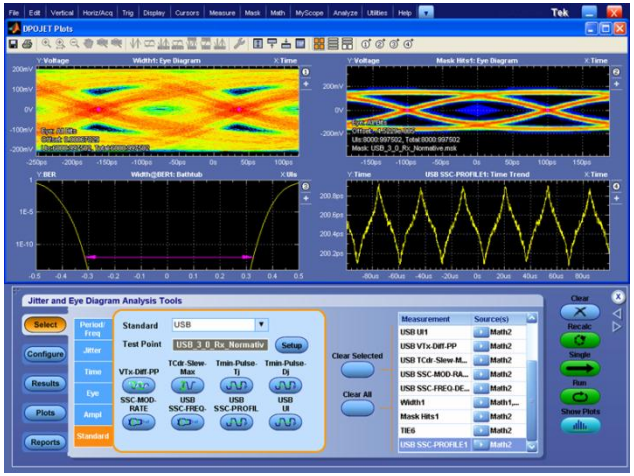


Figure 6-14. Tx Normative Setup with Reference Channel

Tektronix

SuperSpeed Tx compliance

- TX Normative Electrical Parameter
  - UI-Unit interval
  - VTx-Diff-PP-Differential PP TX voltage swing
  - TCRD_Slew_Max-Maximum slew Rate
  - Tx random jitter - Dual Dirac
  - Mask Hits
- Normative Spread Spectrum Clocking
  - SSC Modulation Rate
  - SSC Freq Deviation-Max,Min
  - SSC- USB Profile
- TX-Normative Eyemask
  - Tx total jitter - Dual Dirac at 10-12BER
  - Tx deterministic Jitter - Dual Dirac
  - Eye Height -Transmitter Eye Mask
  - Width@BER
- LFPS measurement
  - LFPS Duty Cycle
  - LFPS fall time
  - LFPS Rise time
  - LFPS Period
  - LFPS Vcm-AC
  - LFPS Vtx-DIFF-PP
  - LFPSTBurst
  - LFPS TRepeat



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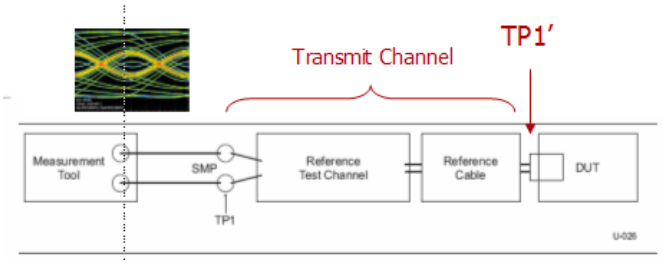
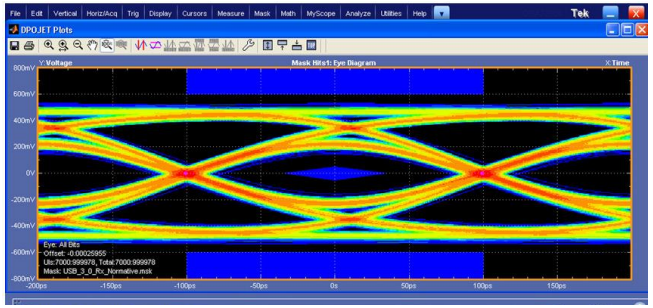
SuperSpeed Tx Key Test – Eye Diagram

- Enable compliance pattern CP0(PRBS) with SSC
- Measure 10^6UI(200usec) @ TP1 or TP1'
- Over 40Gs/sec
- 4.9MHz 2nd order PLL Clock Recovery
- Emulate Tx Channel to TP1 with FIR Filter or TP1' with H/W channel
- Host test : 3 meter cable + 5" device PCB trace.
- Device test : 3 meter cable + 11" host PCB trace.
- Apply CTLE in S/W(DPOJET or Tekexpress)
- Require >= 12.5GHz B/W scope for TP1' – DSA71254B





Spec	Min	Max	Units
Eye Height	100	1200	mV
Dj		86	ps
Rj		46	ps
Tj		132	ps

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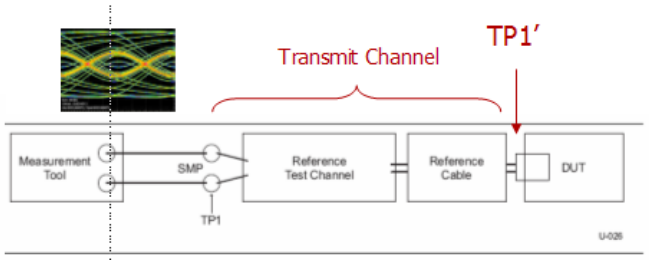
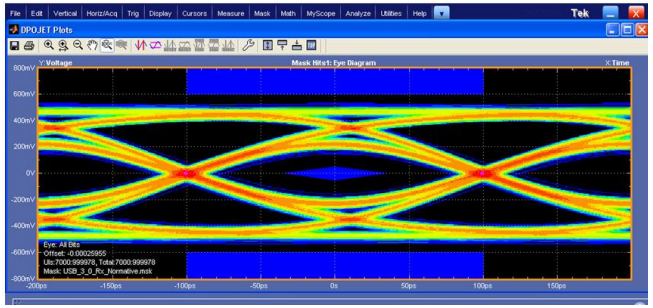
SuperSpeed Tx Key Test – Dj, Rj & Tj @ BER

- Enable compliance pattern CP0(PRBS) with SSC
- Change compliance pattern to CP1 with SSC
- Measure 10^6UI(200usec) @ TP1 or TP1'
- Over 40Gs/sec
- 4.9MHz 2nd order PLL Clock Recovery
- Emulate Tx Channel to TP1 with FIR Filter or TP1' with H/W channel
- Host test : 3 meter cable + 5" device PCB trace.
- Device test : 3 meter cable + 11" host PCB trace.
- Apply CTLE in S/W(DPOJET or Tekexpress)
- Dj from CP0 & Rj from CP1
- Calculate T j @BER E-12 using Dual-Dirac method





Spec	Min	Max	Units
Eye Height	100	1200	mV
Dj		86	ps
Rj		46	ps
Tj		132	ps

$$TJ(BER) = 2Q(BER) \times RJ_g + DJ_{dd}$$

- Q is 7 when BER=10^{-12}

Source: USB 3.0 Rev 1.0 Specification

Tektronix

SuperSpeed Tx Key Test – SSC

- Enable compliance pattern CP1 with SSC
- Measure 10^6UI(200usec) @ TP1 or TP1'
- Over 40Gs/sec
- Period measurement
- 1.98MHz Low pass filter
- Emulate Tx Channel to TP1 with FIR Filter or TP1' with H/W channel
- Host test : 3 meter cable + 5" device PCB trace.
- Device test : 3 meter cable + 11" host PCB trace.
- Apply CTLE in S/W(DPOJET or Tekexpress)
- $T_{SSC-MOD-RATE}$: 30KHz ~ 33KHz
- $T_{SSC-MOD-DEVIATION}$: between + 300/−3700 and + 300/−5300PPM

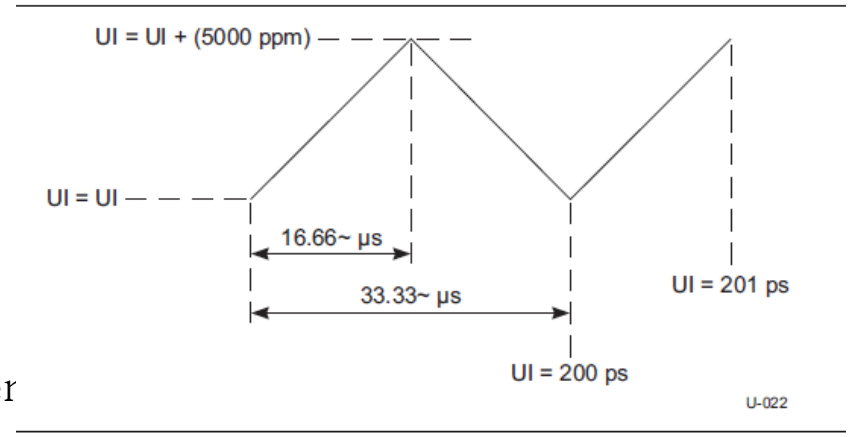
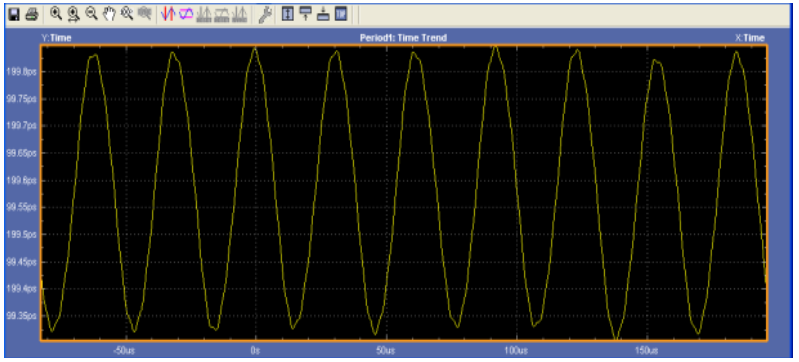


Figure 6-10. Period Modulation from Triangular SSC

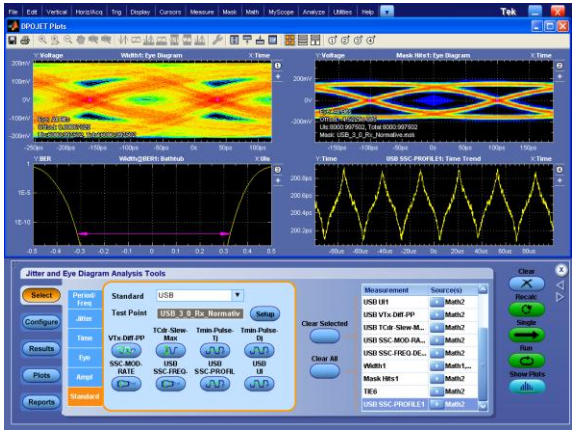


Source: USB 3.0 Rev 1.0 Specification

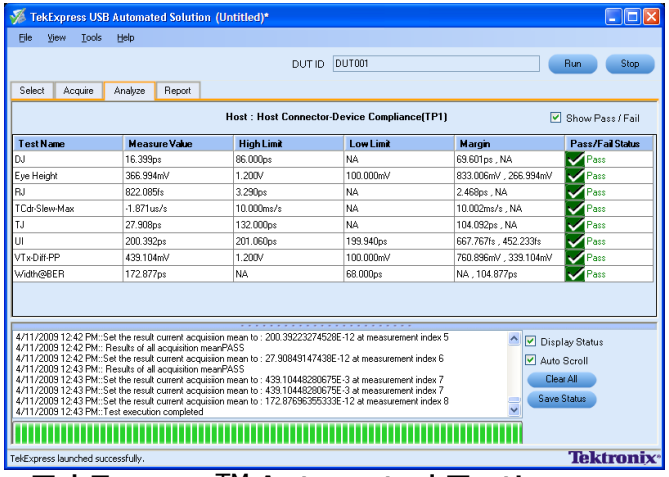
Tektronix

Automated USB 3.0 Transmitter Solution

- Automated all normative and informative transmitter tests
- PING.LFPS from AWG or Scope Trigger output
- Executed in less than five minutes
- Pre-defined CTLE filter provided as per the USB 3.0 specification
- Software channel emulation models
  - Host Channel Back Panel + Cable
  - Host Channel Front Panel + Cable
  - Device Channel + Cable
- comprehensive reports detailing test margins and pass / fail results
- Will Integrates SigTest for Compliance Test



DPOJET
Validation/Debug

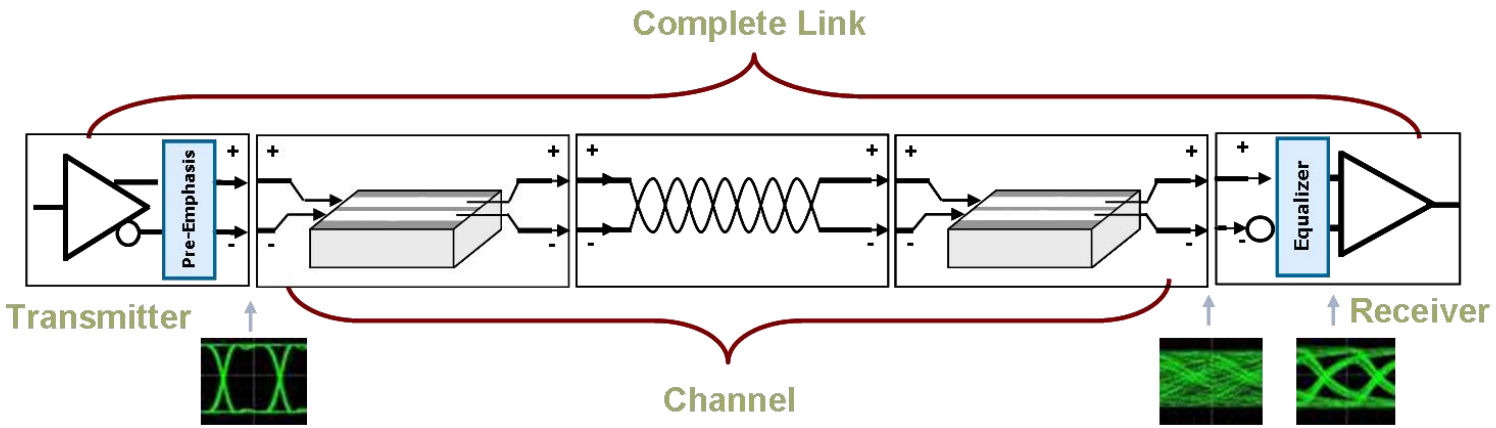


TekExpress™ Automated Testing

Tektronix

USB 3.0 Receiver Testing Overview

- A jitter tolerance test is required for certification, though debug and characterization capabilities are needed to ensure that receivers will work in real world conditions
  - Send specific test data patterns to the device-under-test (DUT) through a known channel (fixtures and cables)
  - Add a specific "recipe" of stresses and de-emphasis
  - Command the DUT into loopback mode
  - Return "echoed" data to a BERT
  - Detected errors are inferred to be a result of bad DUT receiver decisions



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USB3.0 Normative Receiver Test

- External BERT detect using “Scope Error Detect” or Protocol analyzer
  - required for compliance test
- Using ‘built-in Loopback BERT’ feature
  - optional
- Impairment CP0 Scrambled D0.0
- Transmit the BDAT total $3*10^{10}$ bits
- De-Emphasis Level is set to -3dB
- Voltage Level is set to 145mV(Ex. Device)
- SSC on
- Requires HW Reference Cable and Test Channel for TP1 test
- …or TP1’ with Receive Path Channel Emulation

Source: USB 3.0 Specification

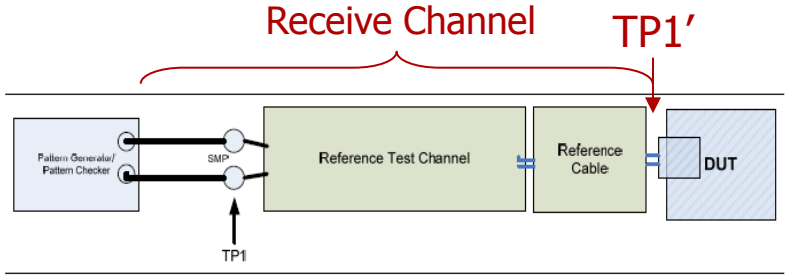
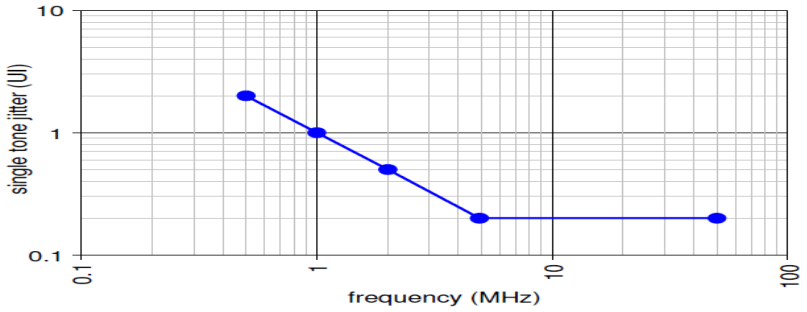


Figure 6-18. Rx Tolerance Setup

Frequency	SJ	RJ
500kHz	400ps	2.42ps
1MHz	200ps	2.42ps
2MHz	100ps	2.42ps
4.9MHz	40ps	2.42ps
50MHz	40ps	2.42ps
10MHz	40ps	2.42ps
20MHz	40ps	2.42ps
33MHz	40ps	2.42ps
50MHZ	40ps	2.42ps



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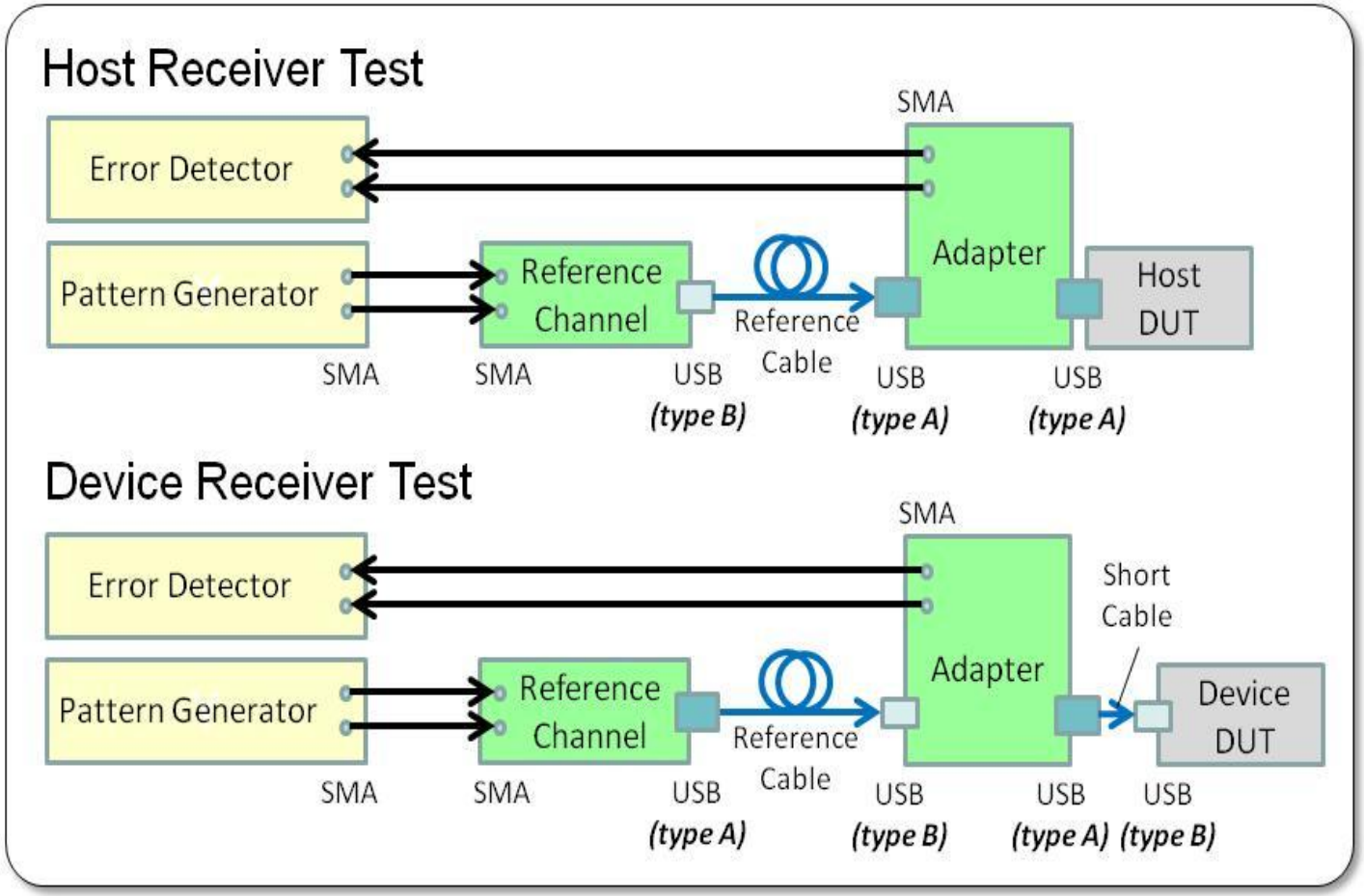
Generic USB 3.0 RX Test Configuration



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Entering to Loopback for Receiver Test

- Bit lock/Symbol lock/Rx equalization training using TSEQ/TS1/TS2
- Transmit 200 Polling.LFPS (2ms)
- Transmit 65536 TSEQ.
- Transmit 256 TS1.
- Transmit 256 TS2 with loopback bit set.

Table 6-3. TS1 Ordered Set

Symbol Number	Encoded Values	Description
0-3	K28.5	COM (Comma)
4	D0.0	Reserved for future use
5	See Table 6-5	Link Functionality
6-15	D10.2	TS1 Identifier

Table 6-4. TS2 Ordered Set

Symbol Number	Encoded Values	Description
0-3	K28.5	COM (Comma)
4	D0.0	Reserved
5	See Table 6-5	Link Functionality
6-15	D5.2	TS2 Identifier

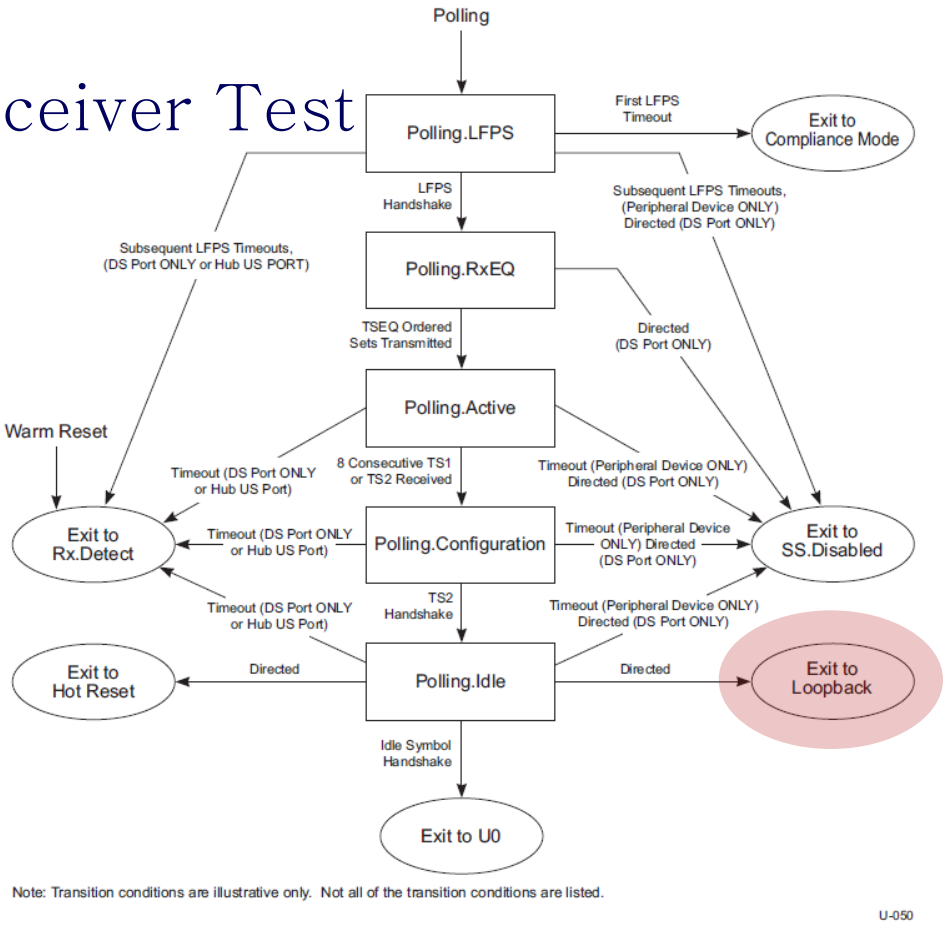


Figure 7-16. Polling Substate Machine

Table 6-5. Link Configuration Field

Bit	TS1 Symbol 5	Description
Bit 0	0 = Normal Training 1 = Reset	Reset is set by the Host only in order to reset the device.
Bit 1	Set to 0	Reserved for future use.
Bit 2	0 = Loopback de-asserted 1 = Loopback asserted	When set, the receiving component enters digital loopback.
Bit 3	0 = Disable Scrambling de-asserted 1 = Disable Scrambling asserted	When set, the receiving component disables scrambling.
Bit 4:7	Set to 0	Reserved for future use.

Tektronix

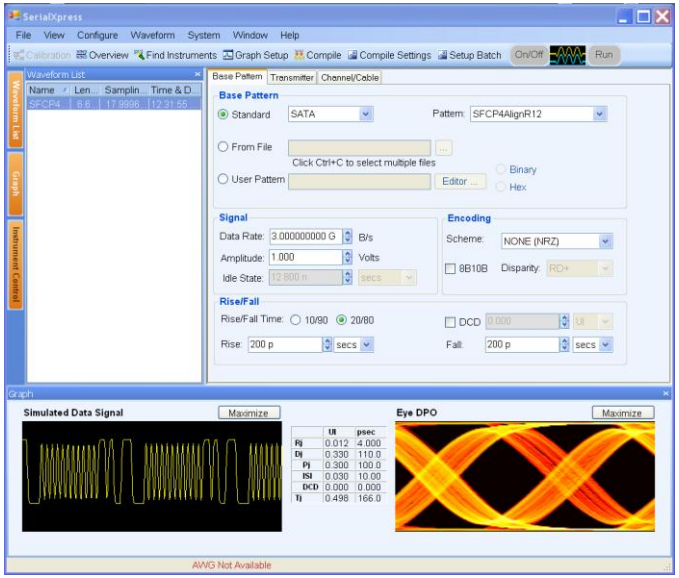
Two Solutions for USB 3.0 Receiver Testing
BERTScope BSA85C and AWG7122C

- Tektronix has the right solution to meet your needs
  - Both provide fully automated Receiver Compliance and Jitter Tolerance Testing
  - Both offer advanced impairments to debug problems caused by SSC or other anomalies
  - Both support a wide range of HSS Standards
  - Both support asynchronous clocking (SKP order set rejection)
- BERTScope
  - Performance that you need up to 26Gb/s for next generations standards including DisplayPort 1.2, SATA/SAS, 10G KR, PCI Express 3.0
  - Impairments can be changed on the fly to see the effect of increasing or reducing jitter
  - Debug and analysis tools enable quick identification of RX errors
  - True BER measurements
- Arbitrary Waveform Generator
  - Common platform for MIPI, HDMI, USB 3.0, and SATA
  - Only solution available that provides a common setup between transmitter and receiver testing without the need of RF switches and additional setup complexity
  - Easily apply sparameter models to verify designs under different channel conditions without the need of physical ISI channels
  - Generate SJ > 1Ghz to debug elusive problems caused by other system clocks

Complete USB 3.0 Receiver Solution

AWG7000 Arbitrary Waveform Generators with SerialXpress®

- No tradeoffs between any signal impairments
- Simulate any length of ISI channel
  - No need to wait for USB hardware compliance channels
- Model real-world complexities of SSC profiles to avoid system interoperability issues
- Minimize time needed for re-cabling
- Improved repeatability and portability of Receiver test configurations with setup files



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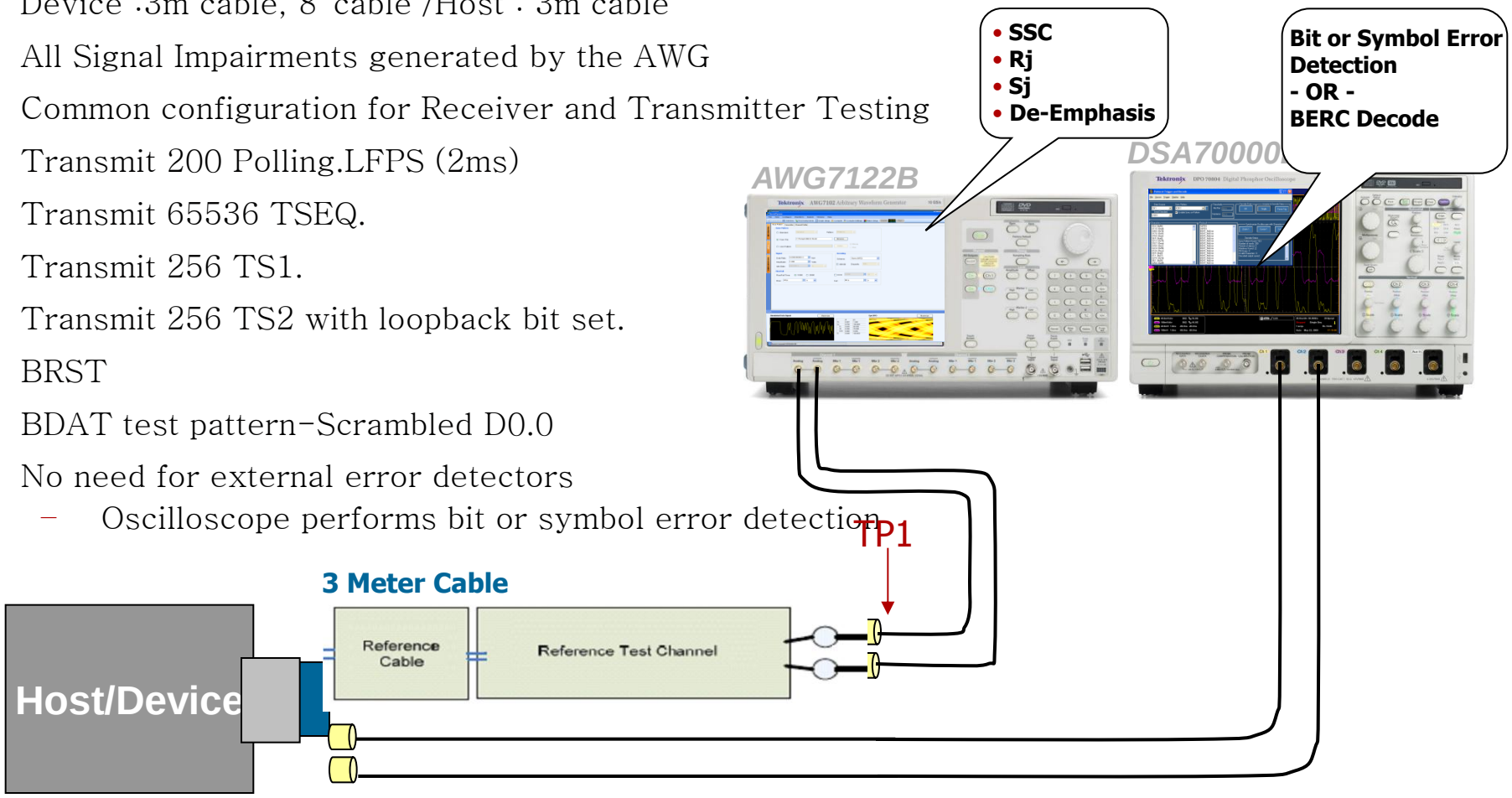
Scope Error Detector Demo

Tektronix

Receiver Test Setup (with HW Channel Emulation)

- USB-IF 'Compliance Channel'
- Device :3m cable, 8"cable /Host : 3m cable
- All Signal Impairments generated by the AWG
- Common configuration for Receiver and Transmitter Testing
- Transmit 200 Polling.LFPS (2ms)
- Transmit 65536 TSEQ.
- Transmit 256 TS1.
- Transmit 256 TS2 with loopback bit set.
- BRST
- BDAT test pattern-Scrambled D0.0
- No need for external error detectors
  - Oscilloscope performs bit or symbol error detection



USB3_Rx Configuration with AWG

Tektronix

Automation Jitter Tolerance with Tekexpress

- AWG7KC force BDATA(Bert DATA) to DUT Rx in Loopback BERT
- DSA70K acquires BCNT(BERT ERROR COUNT) from DUT Tx
- Scope ERRDT decode the BCNT
- Tekexpress control AWG & DSA and automate all Rx Jitter Tolerance
- Generate report

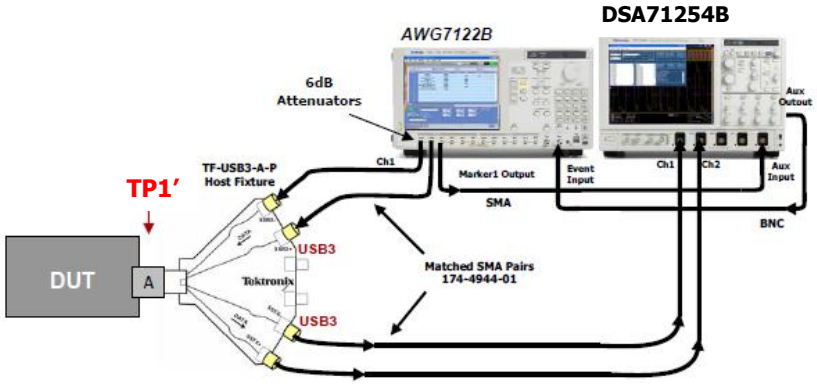
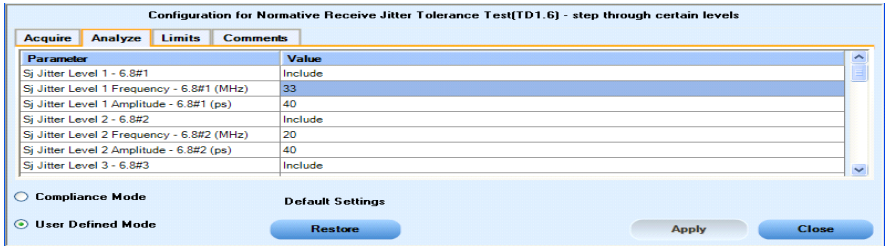
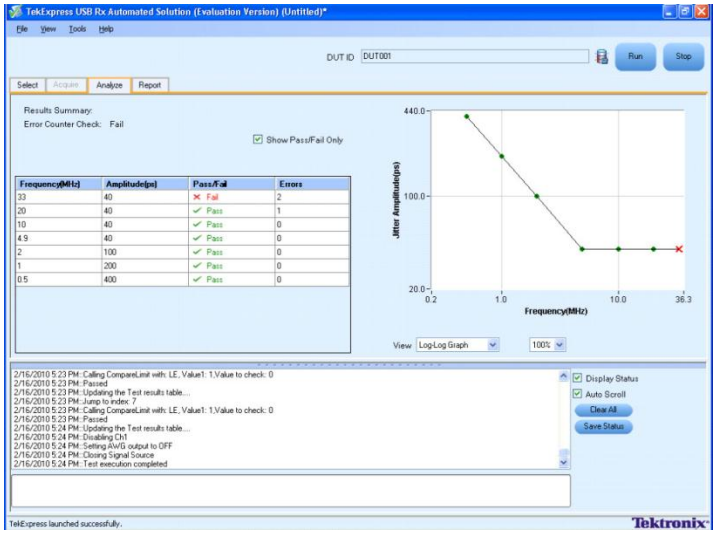
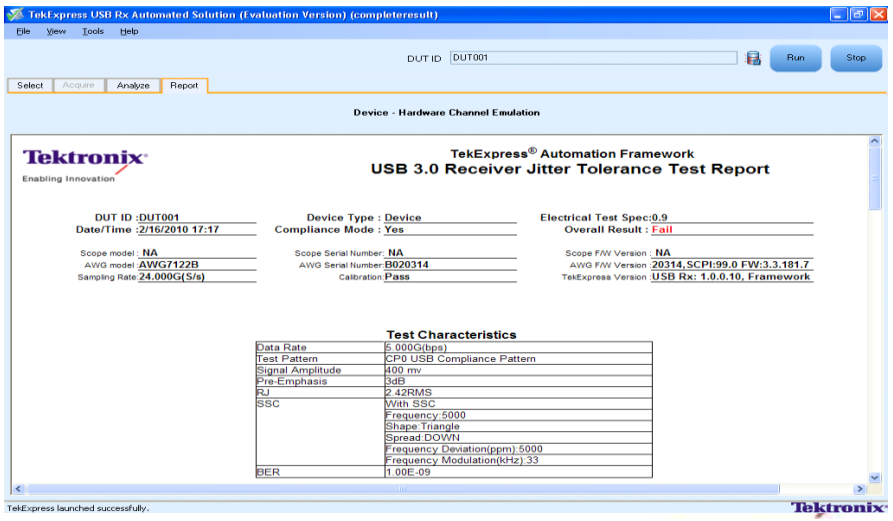


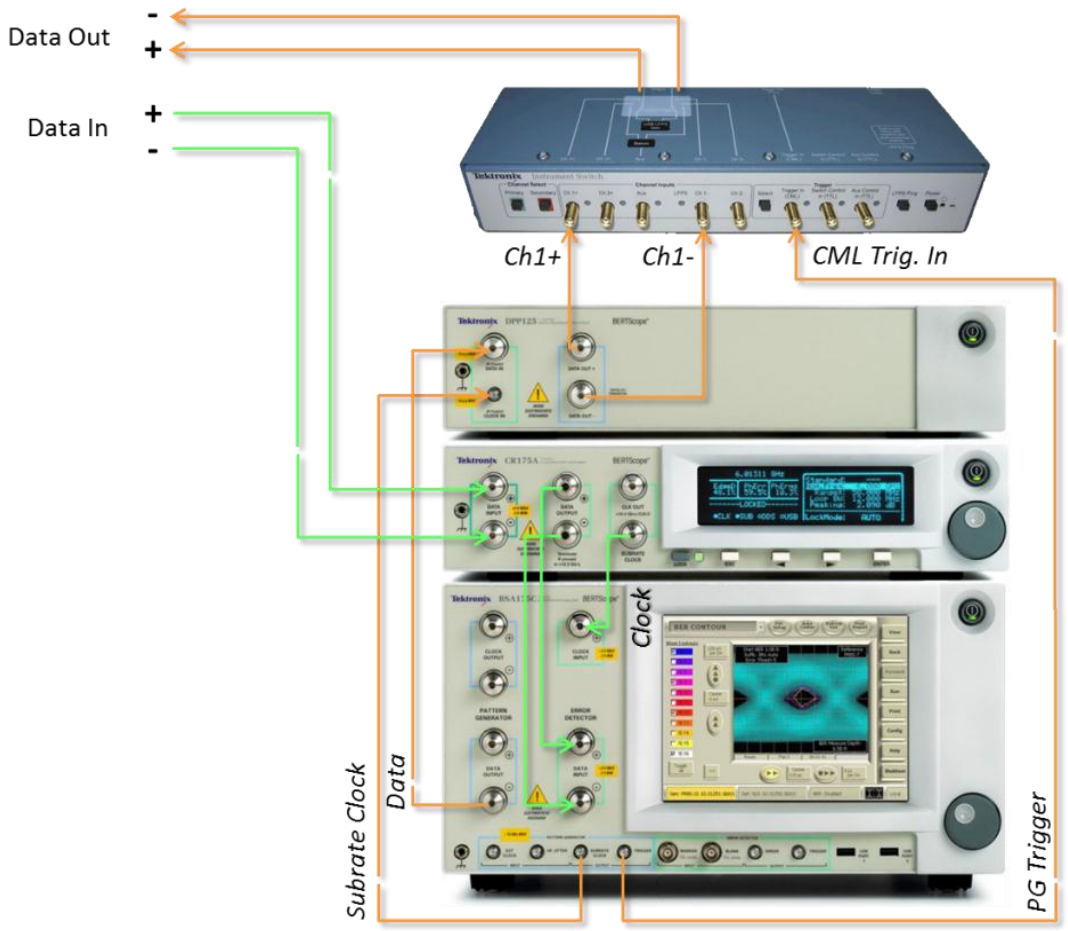
Figure 1: Setup for SW Channel Emulation







BERTScope USB 3.0 RX Test Configuration



- USB Switch

– creates the low-frequency periodic signaling (LFPS) required to initiate Loopback-mode

- DPP125B/C

– De-emphasis Processor

- CR125A

– Clock Recovery

- BSA85C

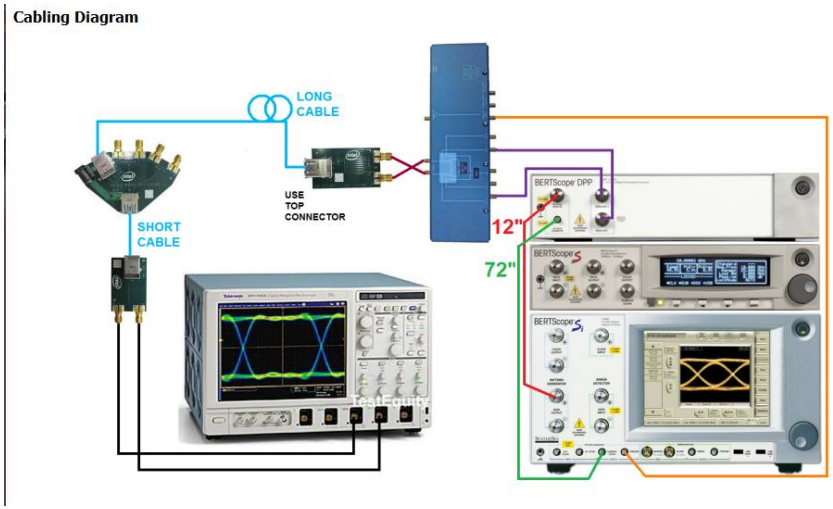
– BERTScope

Tektronix

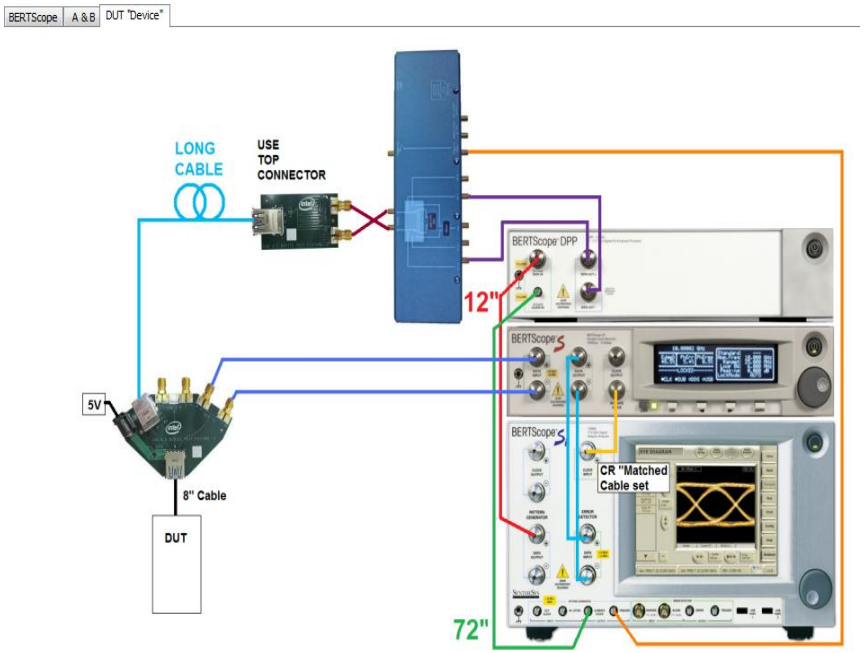
Super Speed Rx compliance

RX testing using BERTSCOPE

- USB-IF 'Compliance Channel
- Jitter tolerance testing using BERTSCOPE
- Auto Calibration & measurement Tools
- Powerful Jitter insertion function for Developers.



USB3_Rx Calibration Configuration with BERTScope



USB3_Rx Testing Configuration with BERTScope

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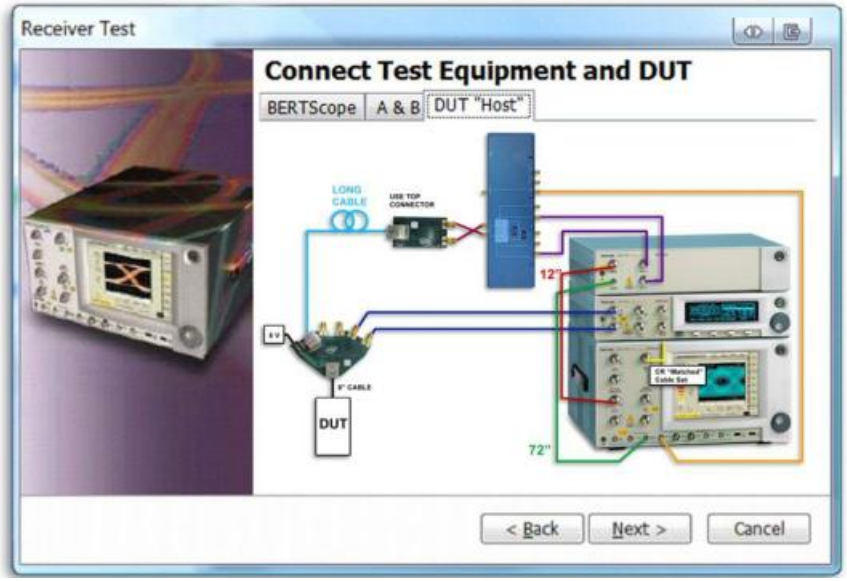
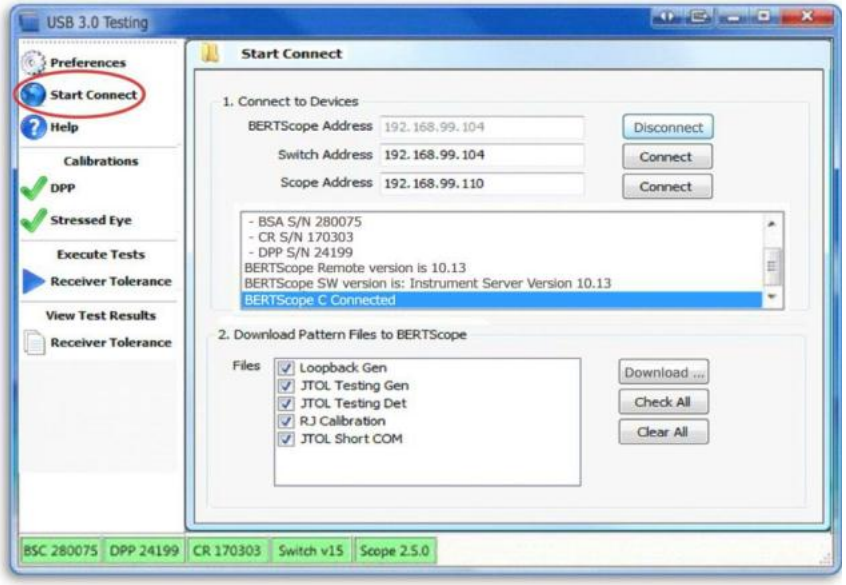
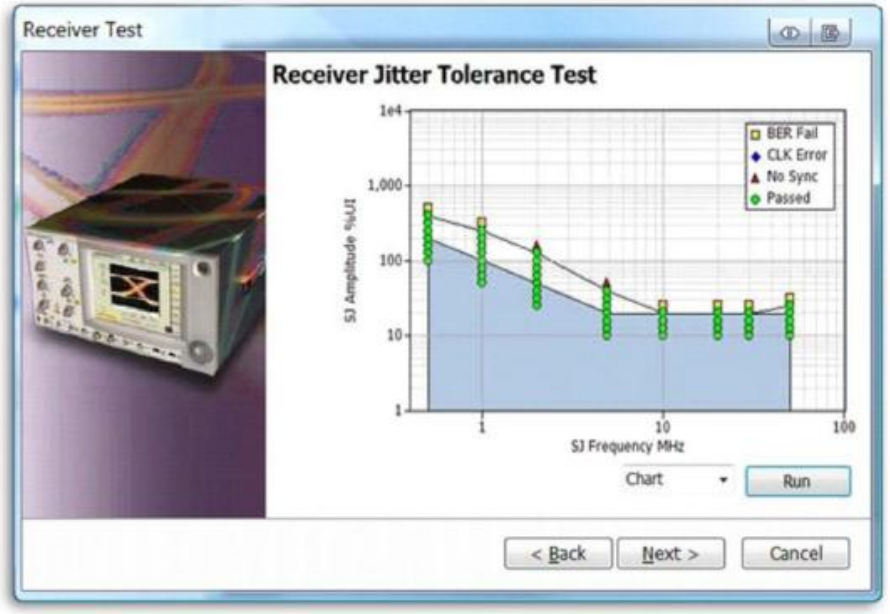
Super Speed Rx compliance
Automation S/W-BSAUSBSFT

- BERTSCOPE generates USB3 RX testing pattern
- CR Unit recover Receiver Clock
- BERTSCOPE Detector count error No.
- Template testing Application record result
- Automation S/W execute Report







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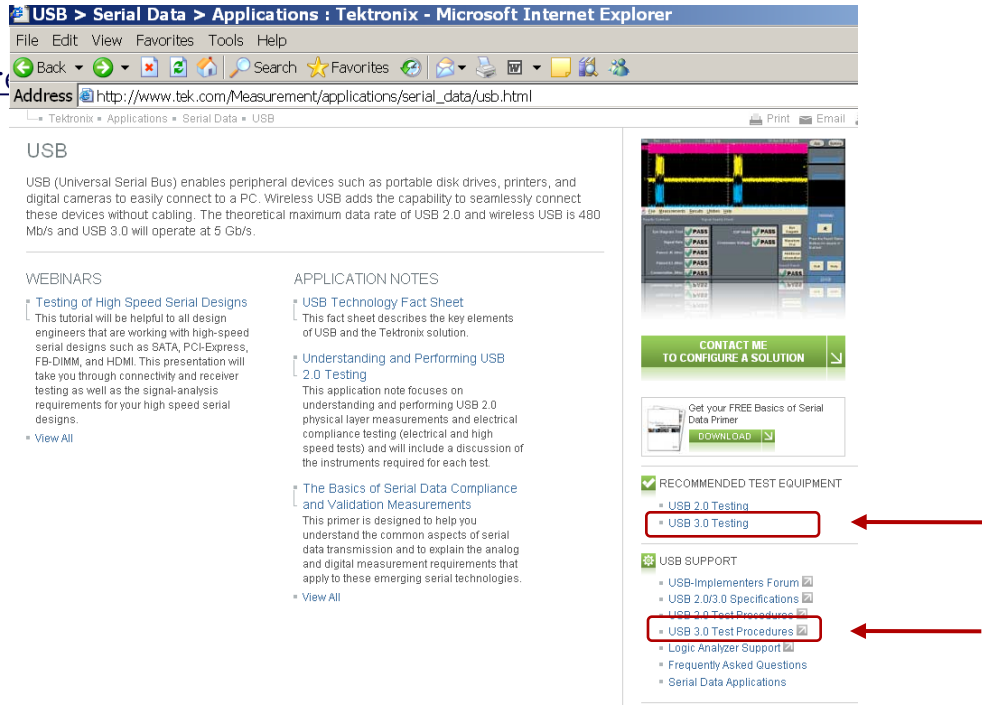
Resources

- Access to Specifications
  - Rev 1.0, http://www.usb.org/developers/docs/

- Tektronix USB Electrical PHY Tools
  - www.tektronix.com/usb
  - www.tektronix.com/softwar

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