Testing Challenges in Displayport

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Agenda

- DisplayPort Overview

- DisplayPort 1.2 updates
  - DisplayPort 1.2 Transmitter Testing
    - What’s New: T2, TP3, TP3EQ
    - Physical Layer Test Overview for DP1.2
    - DP-AUX: Control DUT parameters
  - Test Automation:
    - Full Main Link testing with DP12 Automated tool set
      - DP 1.2 Tx:
  - DisplayPort Sink/Receiver Testing
    - BSA125C configurations towards Rx testing

- eDP testing for eDP 1.4 specification

- MyDP update

Ref: VESA® DisplayPort® PHY Compliance Test Specification Version 1.2

10/15/2013
DisplayPort – Technology Overview

DisplayPort is expanding its footprint

- **Standard DisplayPort**
  - Specification Version 1.2
  - CTS Version 1.2b
  - Data Rates 1.62GBps, 2.7Gbps and 5.4Gbps
  - Box to Box (1, 2, 4 lanes)

- **eDP**
  - Specification Version 1.4
  - CTG in progress
  - Data Rates 1.62GBps to 5.4Gbps
  - Embedded (single box – Laptops) (1, 2, 4 lanes)

- **MyDP**
  - Specification Version 1.0
  - CTS Version 1.0 (in approval)
  - Data Rates 1.62GBps, 2.7Gbps and 5.4Gbps
  - Mobiles (1 lane)

- **iDP**
  - Specification Version 1.1
  - CTG
  - Data Rates 3.24, 3.78
  - LVDS replacement

10/15/2013
DisplayPort 1.2 Overview

- The DisplayPort PHY Compliance Test Specification establishes a test regimen to determine compliance of DisplayPort devices - segmented into:
  - Source
  - Receiver
  - Copper Cable
  - Hybrid devices
  - Tethered devices

- Test Point Definitions
  - TP1: at the pins of the transmitter device.
  - TP2: at the test interface on a test access fixture
  - TP3: at the test interface on a test access
  - TP3_EQ: TP3 with equalizer applied.
  - TP4: at the pins of a receiving device
Source Test Suite

1. EYE Diagram
2. Non Pre-Emphasis Level Verification
3. Pre-Emphasis Level Verification and Maximum Differential Pk-Pk Output Voltage
4. Inter-pair Skew
5. Intra-Pair Skew
6. Differential Transition Time
7. Single Ended Rise and Fall Time Mismatch
8. Overshoot and Undershoot Test
9. Frequency Accuracy
10. AC Common Mode Noise
11. Non ISI Jitter Measurement
12. Total Jitter and Random Jitter Measurement
13. Unit Interval
14. Main Link Frequency Compliance Stability
15. Spread Spectrum Modulation Frequency
16. Spread Spectrum Deviation
17. $\frac{dF}{dt}$ Spread Spectrum Deviation HF Variation
18. Dual-mode TMDS Clock (if supported)
19. Dual-mode EYE Diagram Testing (if supported)

DUT Configuration

- 1. Bit Rates: RBR, HBR or HBR2
- 2. Patterns: D10.2, PRBS7, COMP, PLTPAT, PCTPAT
- 3. FFE (Pre-Emphasis): 0dB, 3.5dB, 6dB, 9.5dB
- 4. Output Levels: 400mV, 600mV, 800mV, 1200mV
- 5. SSC (Spread Spectrum): On/Off
- 6. Post-Curser2: Level 0, 1, 2, 3
- 7. Lane Width, 1, 2, 4
Eye Diagram Test using Eye Compliance Pattern

An Eye diagram test for 800mV, 0dB pre-emphasis at TP2, TP3, TP3-EQ.
1.2 CTS requires adaptive application of one of three reference equalizers to the far end signal, to find a passing condition.

![Reference HBR2 Receiver Equalizer Transfer Functions](image)
1.2 CTS Requires Adaptive Eye Diagram
- Find the highest vertical eye point between .375 -- .625 UI at 10E-9BER
- Analytical tools which examine the vertical noise components project the Rn components to 10E9 BER. These tools have been proven in the field in SATA where they have been deployed for over two years.

Table 3-19: DisplayPort Main Link Transmitter (Main TX) TP3 EQ Parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Units</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXTE7_p_328p_HBR2</td>
<td>Maximum TX Total Jitter</td>
<td>0.62</td>
<td>UI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TXTE7_p_328p_HBR2</td>
<td>Maximum TX Deterministic Jitter</td>
<td>0.49</td>
<td>UI</td>
<td></td>
<td></td>
<td>For HBR2: Measured at 1E-9</td>
</tr>
<tr>
<td>TXTE7_p_328p_HBR2</td>
<td>Maximum TX Total Jitter</td>
<td>0.40</td>
<td>UI</td>
<td></td>
<td></td>
<td>BER using the HBR2</td>
</tr>
<tr>
<td>TXTE7_p_328p_HBR2</td>
<td>Maximum TX Deterministic Jitter</td>
<td>0.25</td>
<td>UI</td>
<td></td>
<td></td>
<td>Compliance EYE pattern</td>
</tr>
<tr>
<td>TXTE7_p_328p_HBR2</td>
<td>Maximum TX Random Jitter</td>
<td>0.23</td>
<td>UI</td>
<td></td>
<td></td>
<td>For HBR2: Measured at 1E-9</td>
</tr>
<tr>
<td>TXTE7_p_328p_HBR2</td>
<td>TX Differential Peak-to-Peak EYE Voltage</td>
<td>110</td>
<td>mV</td>
<td></td>
<td></td>
<td>BER using the HBR2</td>
</tr>
<tr>
<td>TXTE7_p_328p_HBR2</td>
<td>TX Differential Peak-to-Peak EYE Voltage Measurement Range</td>
<td>0.375</td>
<td>UI</td>
<td>0.625</td>
<td></td>
<td>Compliance EYE pattern</td>
</tr>
<tr>
<td>TXTE7_p_328p_HBR2</td>
<td>TX Differential Peak-to-Peak EYE Voltage</td>
<td>110</td>
<td>mV</td>
<td></td>
<td></td>
<td>For HBR2: Uses 0.5 CDF of</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the jitter distribution as 0UI</td>
</tr>
</tbody>
</table>

10/15/2013
Key Elements of DisplayPort 1.2 Transition: dFdT

While dFdT measurements have a unique origin emerging from the SATA and SAS specifications where the history of examining SATA dFdT has led this to become a highly recommend analysis. The dFdT contributing components will rarely appear in the normal Jitter budget due to their low frequency nature.
DisplayPort Auxiliary Channel Controller (DP-AUX)

Why use AUX channel controller in physical layer testing?

- Speeds Up Test Time - No User Interaction is Required to Change Source Output Signal or Validate Sink Silicon State or Error Count
- No Need to Learn Vendor-specific Software - A Single GUI Supports All Vendors
- View & Log Decoded AUX Traffic and Hot Plug Detect (HPD) Events from the Device under Test to the DP-AUX DisplayPort AUX Controller
- Ability to Read and Write DPCD Registers Supports Debug Activities
- Tektronix DP-AUX can serves as a DP1.2 Sink - Enables source to transmit the required patterns for testing.
Combination Parameters For DP1.2 Testing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>- 3</td>
</tr>
<tr>
<td>Lanes</td>
<td>- 4</td>
</tr>
<tr>
<td>Pre-Emphasis</td>
<td>- 4 Levels</td>
</tr>
<tr>
<td>Voltage Swing</td>
<td>- 4 Levels</td>
</tr>
<tr>
<td>Post Cursor2</td>
<td>- 4 Levels</td>
</tr>
<tr>
<td>SSC</td>
<td>- 2 Levels (SSC On and Off)</td>
</tr>
<tr>
<td>Patterns</td>
<td>- 5 Supported Patterns</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test</th>
<th>Waveforms (SSC, 4 Lanes Possible Combinations)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Diagram Test</td>
<td>80</td>
</tr>
<tr>
<td>Pre-Emphasis Test</td>
<td>240</td>
</tr>
<tr>
<td>Non-Pre-Emphasis</td>
<td>32</td>
</tr>
<tr>
<td>Total Jitter</td>
<td>80</td>
</tr>
</tbody>
</table>

~432 Acquired signals for DP1.2 Normative Measurements per lane. X4 lanes results in **1728 Automated** Acquisitions per DUT.

10/15/2013
TekExpress DisplayPort 1.2 Automation

- Comprehensive DisplayPort Version 1.2 Physical Layer Conformance and Compliance Verification Tool
  - All Core DP1.2 measurements
  - Keithley RF Switch and DP-AUX fully automated solution.
  - Selected measurements can be applied across all test permutations (SSC, CTLE’s, swing, rates, pre-emphasis, etc.) translates to **1728 measurements**. DP1.2 will provide full user intervention free, automated testing. This is the killer value proposition.
  - Factory Automation API for full product control in silicon automation systems.
  - Complimentary Fixtures and Compliance Interconnect Channel HW defined by VESA make this package a full customer solution with no compromises.

10/15/2013
DisplayPort 1.2

Test Selection

- DP1.2
  - Measurement selection is now provided as a function of the user specified test target capabilities.
  - If Post Cursor 2 capabilities are not present in the DUT, the measurement list will not show them.
  - Configuration schematics and online help available for all measurements.

10/15/2013
DisplayPort 1.2

Acquisitions

- DP1.2
  - Various signal interconnect methods are supported.
  - Direct TCA (SMA input) on user selected channels.
  - Differential Probe (P7313SMA) inputs for true 4 channel concurrent interconnect. (No single ended measurements)
  - 24:4 Keithley RF Switch allows fully automated control of all 8 single ended inputs for hands free comprehensive testing.

- Test Patterns
  - Automatic verification of test patterns (which can be disabled) ensures the correct patterns are used for the correct test under manual operation.
Keithley RF Switch Integration and Automation

DisplayPort transmitter has both Differential tests and Single ended tests and with the integration of RF switch we have complete automated solution without any user intervention for switching between lanes with both single ended and differential tests in sequential automated passes.
DisplayPort 1.2
User Preferences

- DP1.2
  - User defined test margin controls and auto highlighting of measurements within a user specified tolerance of either the standard spec limits or user defined custom limits.
  - Email controls allow notification of test conditions directly to users.
DisplayPort 1.2
Reporting

- DP1.2
  - Custom html reports which include user specified degrees of detail.
  - Reports and Session raw data are stored together allowing recalling a previous run and re-running the test (with different measurement configurations or limits) and re-generating a new report, **without the actual DUT present.**
Conventional DisplayPort Fixtures

- Partnership with Wilder Technologies to design and channel high performance DP fixtures

- Wilder TF-DP-TPA-PRC fixtures available from Tektronix also.
DisplayPort 1.2
Sink (Rx) Test Overview

Receiver testing is performed with a Tektronix BSA125C BertScope and Wilder HBR2 ISI Channel. BER observation times range from 37 seconds to 10.5 minutes depending on the data rate and jitter frequency being tested. The version 1.2 CTS outlines 17 Tx validation tests which are typically evaluated with a 12.5GHz or higher bandwidth oscilloscope.
DisplayPort 1.2
Sink (Rx) Test Observation Time

Four Principal Test Frequencies at 2, 10, 20 and 100 MHz SJ

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>Jitter Frequency</th>
<th>Number of Bits</th>
<th>Max Num of Bit Errors Allowable</th>
<th>Observation Time (^1) (seconds)</th>
<th>Data Rate Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>HBR2</td>
<td>2 MHz</td>
<td>(10^{12})</td>
<td>1000</td>
<td>HBR2 =185s</td>
<td>0</td>
</tr>
<tr>
<td>HBR</td>
<td></td>
<td></td>
<td></td>
<td>HBR =370s</td>
<td></td>
</tr>
<tr>
<td>RBR</td>
<td></td>
<td></td>
<td></td>
<td>RBR =620s</td>
<td></td>
</tr>
<tr>
<td>HBR2</td>
<td>10 MHz</td>
<td>(10^{11})</td>
<td>100</td>
<td>HBR2 =19s</td>
<td>+350ppm</td>
</tr>
<tr>
<td>HBR</td>
<td></td>
<td></td>
<td></td>
<td>HBR =37s</td>
<td>+350ppm</td>
</tr>
<tr>
<td>RBR</td>
<td></td>
<td></td>
<td></td>
<td>RBR =62s</td>
<td>+350ppm</td>
</tr>
<tr>
<td>HBR2</td>
<td>20 MHz</td>
<td>(10^{11})</td>
<td>100</td>
<td>HBR2 =19s</td>
<td>0</td>
</tr>
<tr>
<td>HBR</td>
<td></td>
<td></td>
<td></td>
<td>HBR =37s</td>
<td></td>
</tr>
<tr>
<td>RBR</td>
<td></td>
<td></td>
<td></td>
<td>RBR =62s</td>
<td></td>
</tr>
<tr>
<td>HBR2</td>
<td>100 MHz</td>
<td>(10^{11})</td>
<td>100</td>
<td>HBR2 =19s</td>
<td>0</td>
</tr>
<tr>
<td>HBR</td>
<td></td>
<td></td>
<td></td>
<td>HBR =37s</td>
<td></td>
</tr>
</tbody>
</table>

\[^1\text{To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: } 10^{11} \text{ bits at HBR = 370ps/UI} \times 10^{11} \text{ UI = 37 seconds}\]
BertScope Receiver Test Solution

Typical Configuration

- BertScope BSA85C
  - Option STR
- BSA12500ISI
- DP-AUX
- DSA12504C for calibration
  - SDLA Sw for CTLE filter creation
- 3 way Power dividers
- TTC Filters
- SMA cables
- Attenuators
- DC Block
Two Tone SJ, with Stationary HFSJ Parked at 200 MHz.

New HFSJ source for fixed 200 MHz SJ as required by DP1.2.
DisplayPort 1.2
Crosstalk Configuration

Generator page showing Patterns and capability of generation large amount Crosstalk with differential sub-rate Clock Outputs.
BSAITS125 generates multiple, fixed selections for ISI.

On BSAITS GUI, you can simply dial in the amount of ISI needed...and DPP and BSAITS will adjust to generate requested ISI...

Use BERTScope DPPB or DPPC to generate low pass filter to fine tune ISI.

- Can automate calibration when using BSAITS with DPP
- Can precisely tune ISI at all data rates
- Can generate additional ISI to test margin of DUT
RBR ISI created using BSAITS and DPP125B
DisplayPort 1.2 Compliance Testing

- GRL is the leading lab for DP 1.2 compliance testing and works with all key players in the DP standard
  - Mike Engbreton
    - Editor of DP 1.2b PHY Compliance Test Spec
    - Chairman of VESA DP Test Implementation Task Group
    - Author of Test Vendor Methods of Implementation (MOIs)

- GRL first to certify DP 1.2 source and sink products.

- DP 1.2b Test Program has been released for Self Testing
  - GRL is helping vendors develop their self test programs
PHY Documents Available from VESA Document Center

- DP 1.2b PHY CTS
- Vendor Methods of Implementation MOIs
  - Tek_DP_PHY12bCTS_Source_MOI_D2 01-14-2013
  - Tek_DP_PHY12bCTS_BERTScope_SINK_MOI_D2_01-14-13

Automation Needed!!
DP 1.2b Sink Test SW Solution
DPCD Automation Support

![DisplayPort Rx Auto Calibration](image-url)
Rev1.0 Planned Feature Set

- **Standard Features (Available from Tek or GRL directly)**
  - Calibration using BERTScope/TekScope
  - Support of Tek Variable ISI Solution
  - Traditional Jitter Margin Testing (Increase SJ until Fail)
  - Will track DP PHY CTS 1.2x VESA Updates
    - Current Rev is PHY CTS 1.2b
  - VESA Approved MOI using SW Automation

- **Upgrade Features (Available from GRL)**
  - Custom DUT Automation Support
    - If Sink does not support DPCD through DP-AUX
  - Multi-vendor Support
  - Others TBD
GRL DP 1.2b Sink Test Software

- **Schedule:**
  - Rev0.6 Beta Available in July 2013
  - Evolution into Rev1.0 Product delivery – Q3/Q4 of 2013

- **Pricing:**
  - TBD

- **Licensing:**
  - Orderable from Tektronix in Q3 (GR is SW OEM).
  - Upgrades and ‘Evergreen’ Support Available from GRL

- **SW Support:**
  - GRL
eDP source measurements:
Test 3.1 - Eye Diagram Test
Test 3.2 - Inter Pair Skew test
Test 3.3 - Non-ISI Jitter Measurements
Test 3.4 - Total Jitter
Test 3.5 - Deterministic jitter
Test 3.6 - Random Jitter
Test 3.7 - Main Link Frequency Stability
Test 3.8 - Spread Spectrum Modulation Frequency
Test 3.9 - Spread Spectrum Modulation Deviation
Oscilloscope Requirements
Option EDP requires a DPO/DSA/MSO 70K scope running firmware version 6.4.0 or higher and DPOJet version 6.0 or higher.
For customers testing RBR (1.62 Gb/sec) and HBR (2.7 Gb/sec) a minimum bandwidth of 8Ghz is required.
For customers testing HBR2 (5.4 Gb/sec) a minimum 12.5GHz BW is required.

Probing
For customers testing RBR (1.62 Gb/sec) or HBR (2.7 Gb/sec) Qty 4 P7380 or P7380SMA are required if testing more then two lanes at one time.
For customers testing HBR2 (5.4 Gb/sec) and HBR (2.7 Gb/sec) and RBR (1.62 Gb/sec) Qty 4 P7313 or P7313MA are required if testing more then two lanes at one time.
An optional eDP fixture is available on the Tektronix PAL:TF-EDP-TPA-PR
Embedded (eDP) Fixturing

- 20-Pin eDP Connector for CCFL Backlight (1 or 2 Lane eDP)
- 30-Pin eDP Connector for LED Backlight w/o LED Driver on PCB (1 or 2 Lane eDP)
- 30-Pin eDP Connector for LED Backlight with LED Driver on PCB (1 or 2 Lane eDP)
- 40-Pin eDP Connector for LED Backlight with LED Driver on PCB (up to 4 Lane eDP)
MyDP- PHY tests for Source

- Eye Diagram (Normative)
- Non Pre-Emphasis Level Verification (Normative)
- Pre-Emphasis Level Verification (Normative)
- Intra-Pair Skew (Informative)
- AC Common Mode Noise (Informative)
- Non ISI Jitter Measurements (Normative)
- Total Jitter (TJ) and Random Jitter (RJ/DJ) Measurements (Normative)
- HBR2 D10.2 Total/Random/Deterministic Jitter (TJ/RJ/DJ) Measurements (Normative)
- Main Link frequency Compliance (Normative)
- Spread Spectrum Modulation Frequency (Normative)
- Spread Spectrum Modulation Deviation (Normative)
- $Df/dt$ Spread Spectrum Deviation HF Variation (Informative)
- AUX Manchester – channel Eye Test (Normative)… Included in MyDP Specific.
- AUX Manchester – Channel Sensitivity test (Normative)
- Inrush (Normative)
- P_PWR DC Levels (Normative)

Most tests will be similar to standard DP 1.2 ONE LANE tests

10/15/2013
Sink Test will be similar to standard DP 1.2 ONE LANE tests

- BSAITS125 generates multiple, fixed selections for ISI...
- Use BERTScope DPPB or DPPC to generate low pass filter to fine tune ISI
- On BSAITS GUI, you can simply dial in the amount of ISI needed...and DPP and BSAITS will adjust to generate requested ISI...
- Can automate calibration when using BSAITS with DPP
- Can precisely tune ISI at all data rates
- Can generate additional ISI to test margin of DUT
## Complete Tektronix DisplayPort Instrument Portfolio

| **Receiver/Sink Tests**  
(Compliance/Characterization) | **BSA125C** with JMAP and SSC and HW Options DPP 125A and CR125A provide support for future bit-rates (12-26G) with a unique portfolio of Scope and Bert combined features. |
|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| **DP Channel Tests**          | **DSA8300**  
80E10 TDR Sampling Module for DSA8200 Sampling Scope  
S-Parameter Analysis Software 80SICON Software |
| **Cable Tests**               | **DSA8300**  
4X 80E08 TDR Sampling Module for DSA8300 Sampling Scope |
| **Transmitter/Source Tests**  | **DSA71254C**  
DPOJET Jitter Analysis software  
SMA Adapters TCA-SMA 2 per scope  
Differential SMA Probe P7313SMA (optional)  
+ DP-AUX controller + DP12 (Sw Option) |

Receiver Silicon characterization and compliance testing capability to 26Gbps.  
Source and Sink electrical channel performance, Crosstalk, Impedance and return loss. High Dynamic Range instrument.  
Cable crosstalk, skew and frequency domain measurements, sdd21, sdd11.  
Signal timing stability and SSC analysis, Transmitter AC parametric, Jitter, Amplitude.
THANK YOU