Mobile Storage Solution: eMMC Electrical Validation and Protocol Analysis S/W and UFS Protocol Decode S/W

Agenda

- eMMC technology overview
- Electrical measurements V4.41, V4.51
- eMMC Protocol overview
- PGY-MMC Electrical Validation and Protocol Analysis Software
- UFS Technology Overview
- UFS Protocol Analysis
- PGY-UPRO/UFS Protocol Decode Softwrae
- Demo
- Q&A

eMMC Technology Overview

- Multimedia card transfers data via configurable data bus signals
- Communication Signals
  - **CLK:** Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.
  - **CMD:** This signal is a bidirectional command channel used for card initialization and transfer of commands.
  - **DAT0-DAT7:** These are bidirectional data channels (1 bit/4 bit/8bit)

eMMC SDR Timing Data

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	f_{PP}	0	52[3]	MHz	$C_L \leq 30$ pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	Tolerance: +20KHz
Clock high time	t_{WH}	6.5		ns	$C_L \leq 30$ pF
Clock low time	t_{WL}	6.5		ns	$C_L \leq 30$ pF
Clock rise time[4]	t_{TLH}		3	ns	$C_L \leq 30$ pF
Clock fall time	t_{THL}		3	ns	$C_L \leq 30$ pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	$C_L \leq 30$ pF
Input hold time	t_{IH}	3		ns	$C_L \leq 30$ pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	$C_L \leq 30$ pF
Output hold time	tOH	2.5		ns	$C_L \leq 30$ pF
Signal rise time[5]	tRISE		3	ns	$C_L \leq 30$ pF
Signal fall time	tFALL		3	ns	$C_L \leq 30$ pF

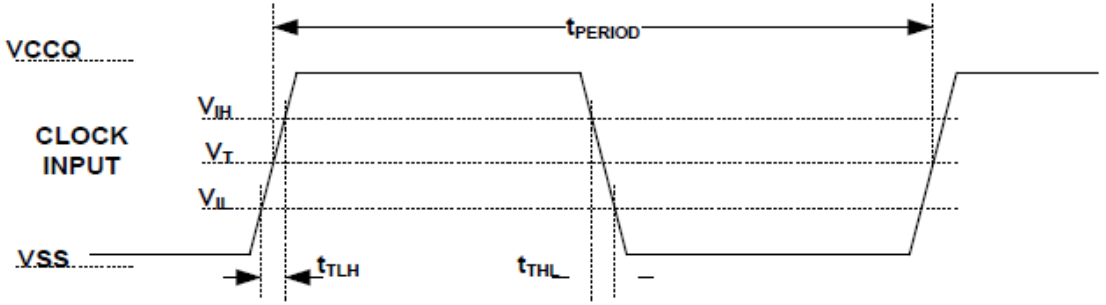
NOTE 1. CLK timing is measured at 50% of VDD.
NOTE 2. A *e*•MMC shall support the full frequency range from 0-26Mhz, or 0-52MHz
NOTE 3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.
NOTE 4. CLK rise and fall times are measured by min (VIH) and max (VIL).
NOTE 5. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).

eMMC DDR timing Data

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	f_{PP}	0	52[3]	MHz	$C_L \leq 30$ pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	Tolerance: +20KHz
Clock high time	t_{WH}	6.5		ns	$C_L \leq 30$ pF
Clock low time	t_{WL}	6.5		ns	$C_L \leq 30$ pF
Clock rise time[4]	t_{TLH}		3	ns	$C_L \leq 30$ pF
Clock fall time	t_{THL}		3	ns	$C_L \leq 30$ pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	$C_L \leq 30$ pF
Input hold time	t_{IH}	3		ns	$C_L \leq 30$ pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	t_{ODLY}		13.7	ns	$C_L \leq 30$ pF
Output hold time	t_{OH}	2.5		ns	$C_L \leq 30$ pF
Signal rise time[5]	t_{RISE}		3	ns	$C_L \leq 30$ pF
Signal fall time	t_{FALL}		3	ns	$C_L \leq 30$ pF

NOTE 1. CLK timing is measured at 50% of VDD.
NOTE 2. A *e*•MMC shall support the full frequency range from 0-26Mhz, or 0-52MHz
NOTE 3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.
NOTE 4. CLK rise and fall times are measured by min (VIH) and max (VIL).
NOTE 5. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).

eMMC v4.51 clock Timing Measurements



NOTE 1 V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).
NOTE 2 V_T=0.975V - Clock Threshold (V_{CCQ} = 1.8V) and V_T=0.65V - Clock Threshold (V_{CCQ} = 1.2V) , indicates clock reference point for timing measurements.

Symbol	Min.	Max.	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	0.2· t_{PERIOD}	ns	tTLH, tTHL < 1ns (max.) at 200MHz, C_{BGA}=12pF, The absolute maximum value of tTLH, tTHL is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

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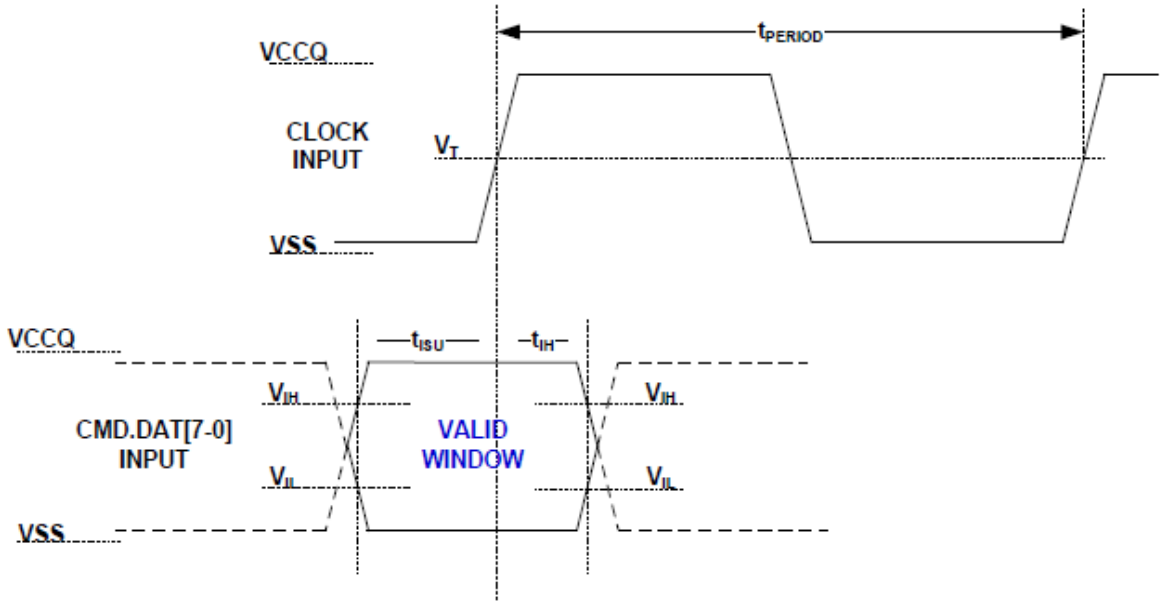
eMMC4.51 timing Measurements



Note1: t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
Note2: V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Symbol	Min.	Max.	Unit	Remark
t_{ISU}	1.40	-	ns	$5pF \leq C_{BGA} \leq 12pF$
t_{IH}	0.8		ns	$5pF \leq C_{BGA} \leq 12pF$

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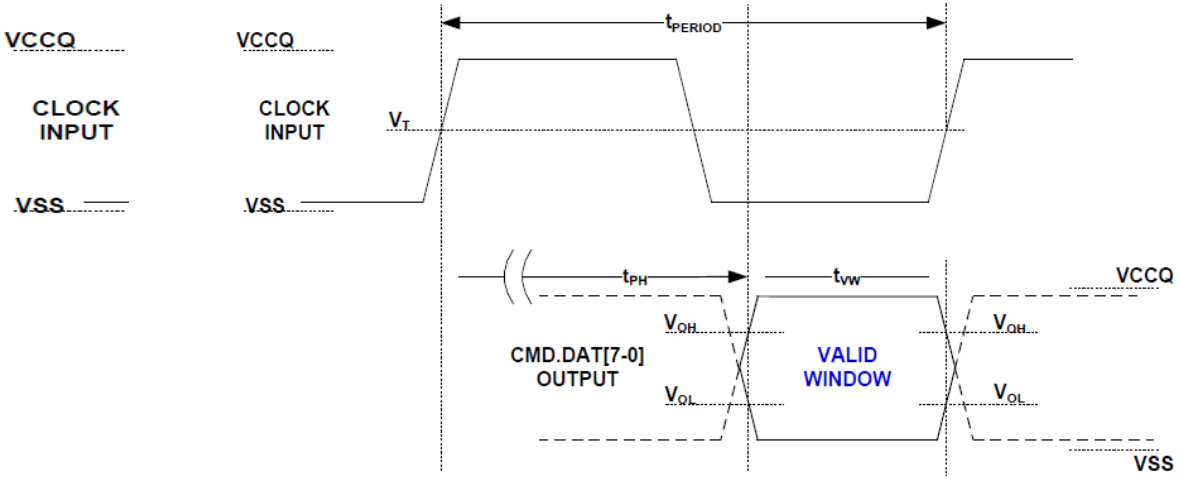
eMMC 4.51 timing measurements



NOTE V_{OH} denote NOTE V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

Table 172 — Output timing

Symbol	Min.	Max.	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
Δ_{TPH}	-350 (ΔT= -20 deg.C)	+1550 (ΔT= 90 deg.C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure Δ_{TPH} is 2600ps for ΔT from -25 deg.C to 125 deg.C during operation.
t_{VW}	0.575	-	UI	t_{VW}=2.88ns at 200MHz Using test circuit in Figure 72 including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected T_{VW} at Host input is larger than 0.475UI.

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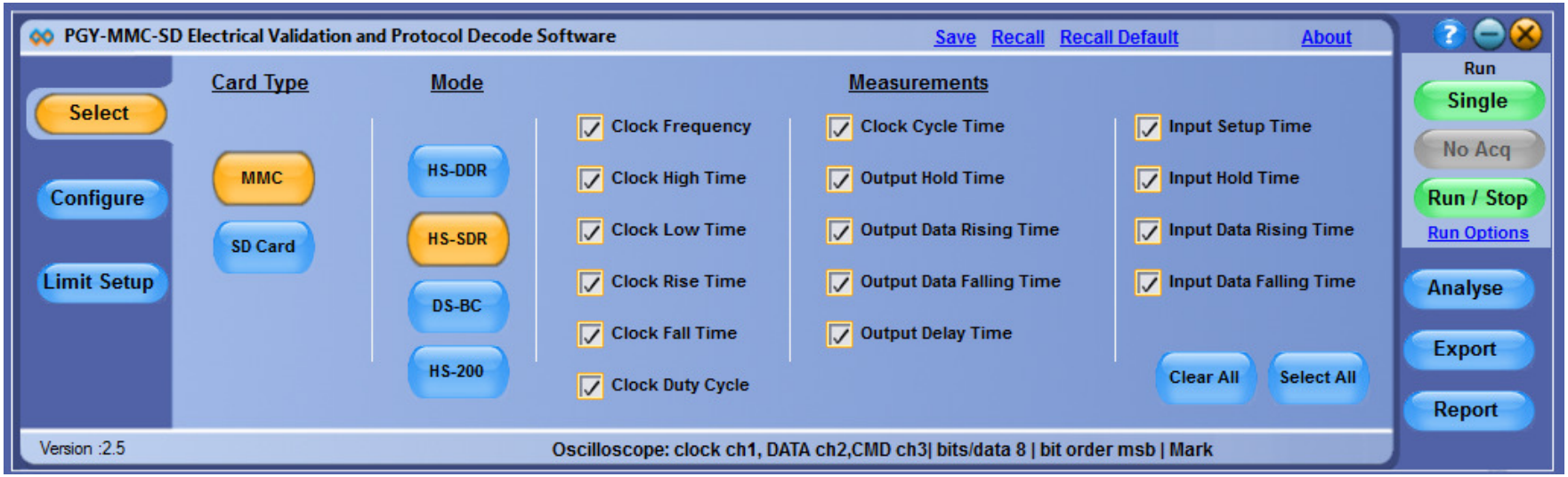
PGY-eMMC/Sd Electrical Validation and Protocol Decode Software- Select



- User can select eMMC type and select data mode
- eMMC Electrical measurements as specified in I2C Standard document are listed
- User has flexibility select few measurements or all measurements
- Supports electrical measurement for eMMC4.41 and 4.51

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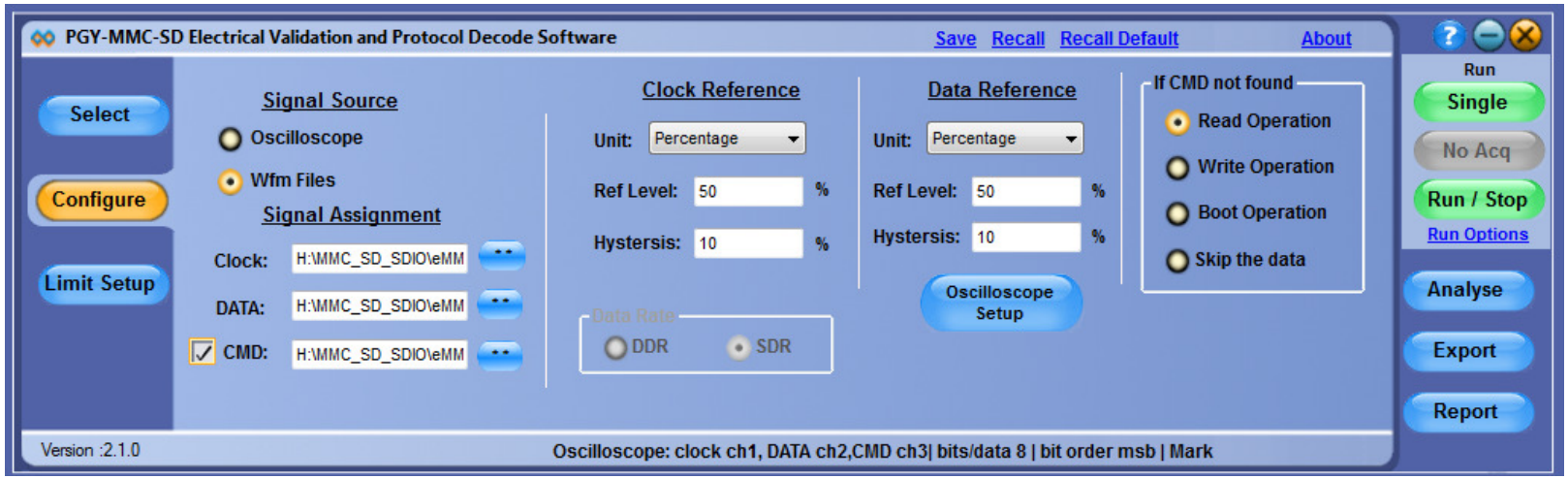
PGY-MMC-SD Electrical Validation and Protocol Decode Software- Configure



- Select the source of the signal from oscilloscope or saved files
- Use Clock and Data Reference by value. If signal is noisy set the hystersis at least 15% to avoid any intermittent transition as logic state

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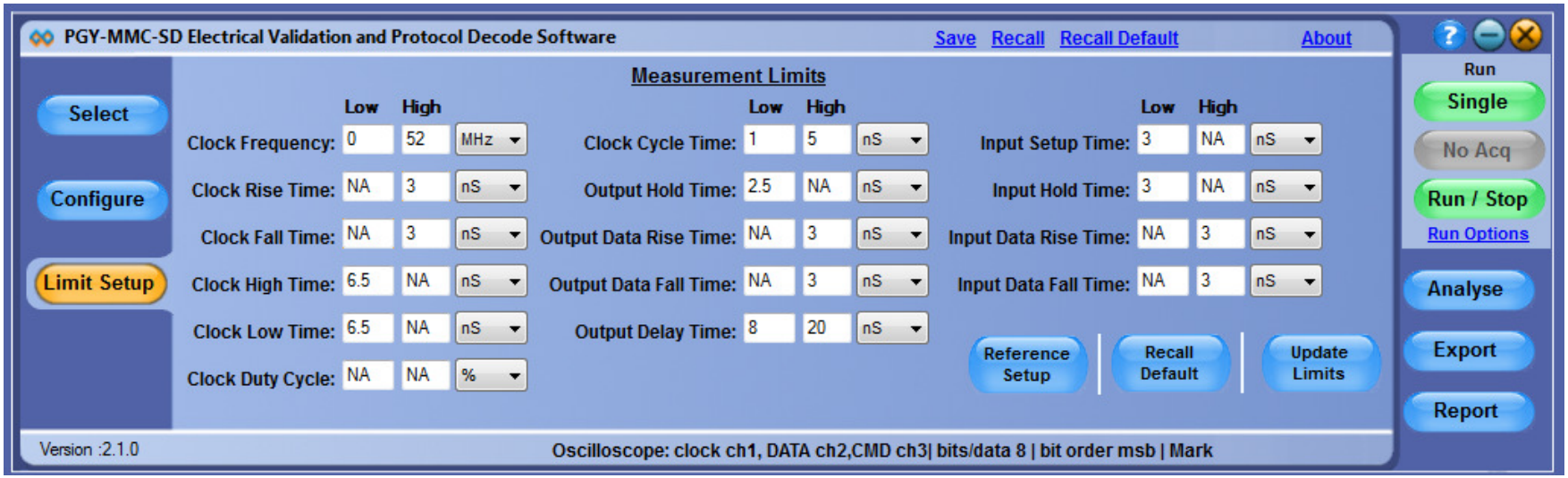
PGY-eMMC-SD Electrical Validation and Protocol Decode Software- Limit Setup



- Limits can be set to default limits as specified in standard document
- User defined Low and High Limits as per in-house specification
- Save and Recall the limits

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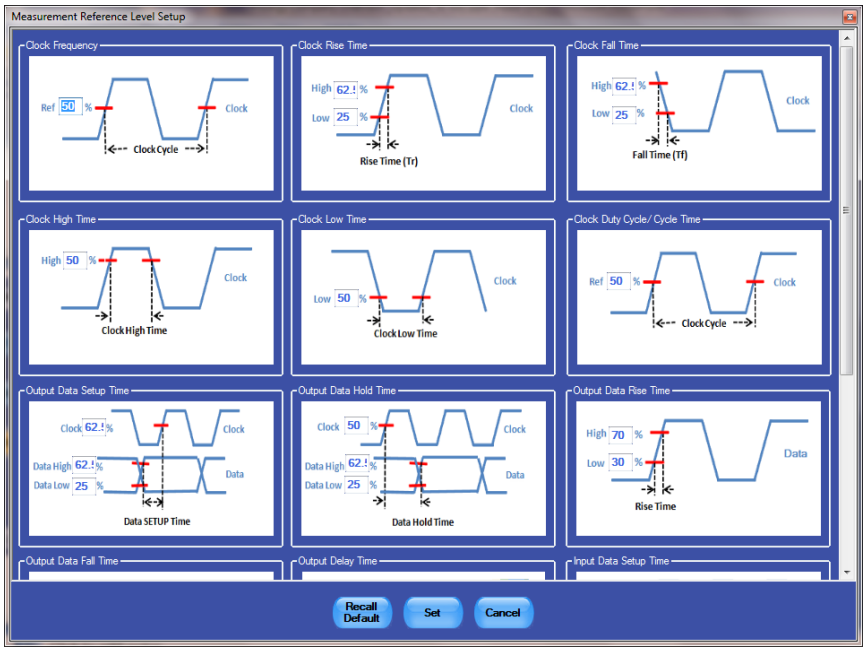
PGY-MMC-SD Electrical Validation and Protocol Decode Software- Reference Level Setup

- Graphical User Interface eases of reference level setup and avoid human errors
- User can view the default reference levels set for each of the electrical measurement
- Edit reference level setup for each of the measurements
- Save and recall of reference level setup



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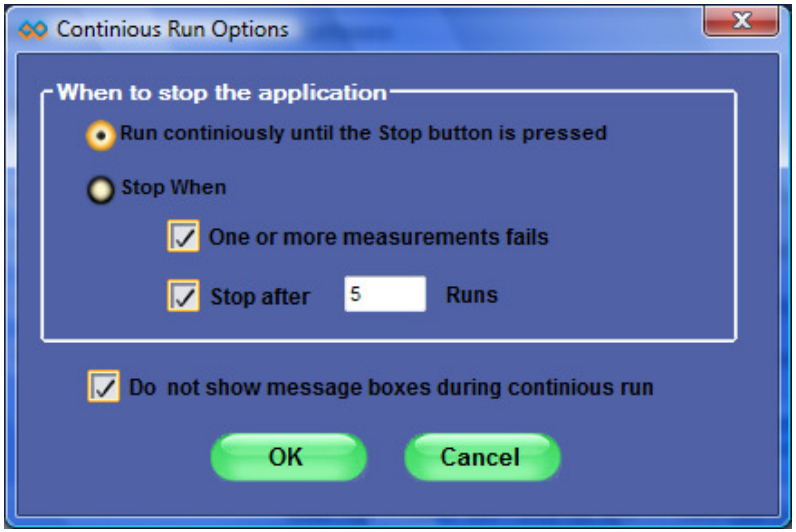
PGY-MMC-SD Electrical Validation and Protocol Decode Software- Run-Control



- Run Control captures the data and analyses it as per configure, limit values and reference level setup
- Analysis of signal using Single or Continuous acquisition
- Analysis of signals present in acquisition memory using **No Acq** mode
- Flexibility to stop the test if one or more measurement fails/ after running user defined number of tests

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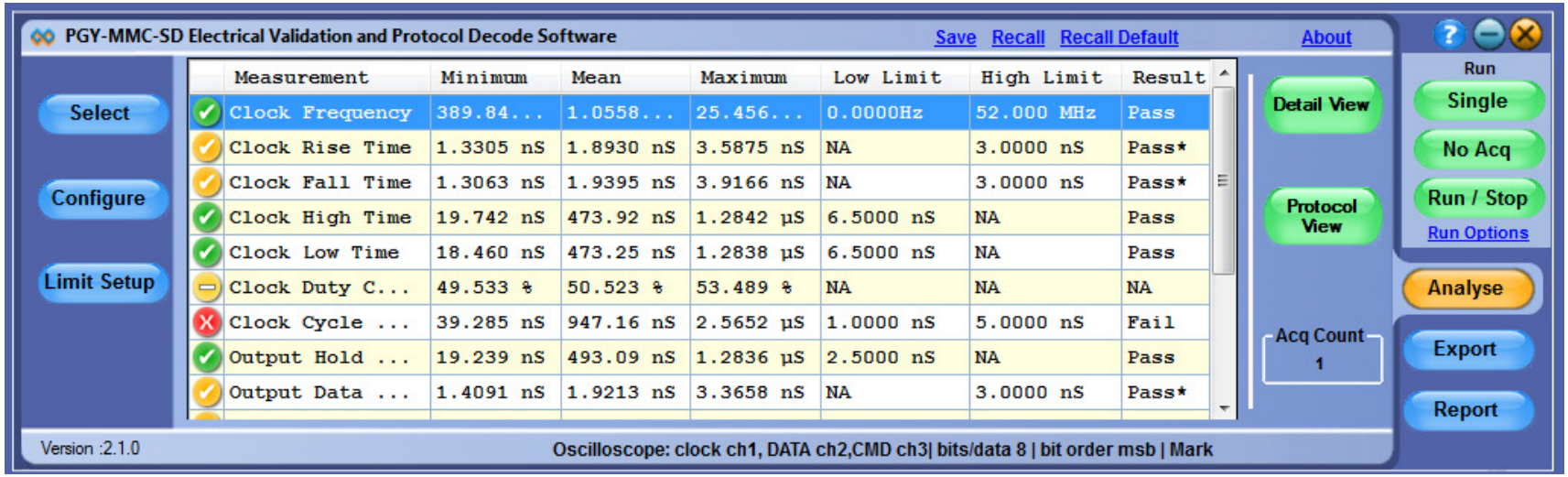
PGY-MMC-SD Electrical Validation and Protocol Decode Software- Analyze



- Displays measurement limits and annotation to indicate pass or fail
- Provides min, max and mean measurement values
- Detail View provides debugging environment
- Protocol view provides details of protocol transaction

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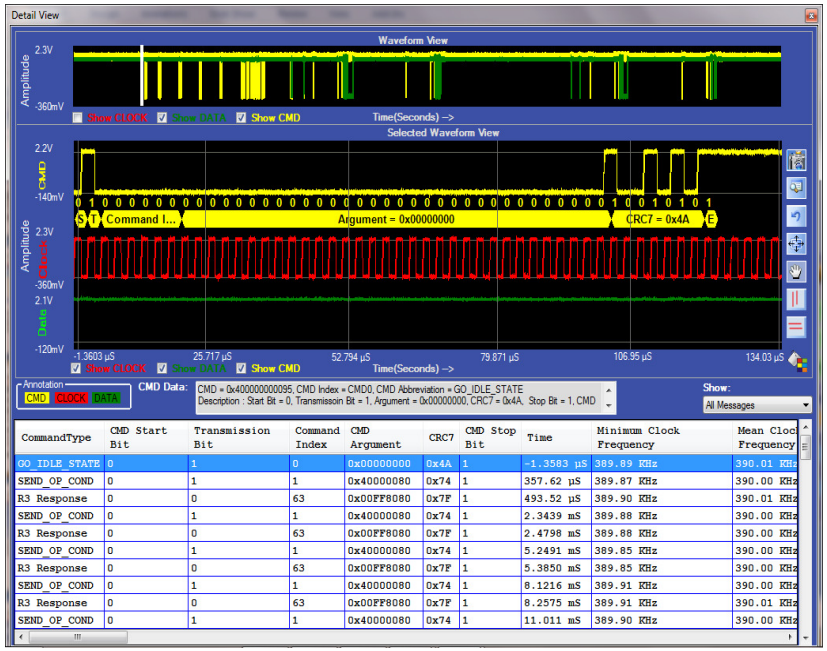
PGY-MMC-SD Electrical Validation and Protocol Decode Software- Detail View

- Provides powerful debug environment co-relating physical layer waveform, protocol decode data and electrical measurements
- Selected protocol decode message waveform is plotted in selected waveform window
- Reference cursor will be placed in acquired waveform window to indicate the position of the waveform in Acquired data
- Failed Electrical measurements selected in red color
- Cursor measurements for manual analysis
- Markers to indicate reference level for measurement
- Take snapshot of selected waveform image from detail view for report
- Decode tables list the Commands and responses from card
- Utility features for zooming the waveform, pan, cursors, reference set markers and image capture for report



CommandType	CMD Start Bit	Transmission Bit	Command Index	CMD Argument	CRC7	CMD Stop Bit	Time	Minimum Clock Frequency	Mean Clock Frequency
GO_IDLE_STATE	0	1	0	0x00000000	0x4A	1	-1.3583 µS	389.89 KHz	390.01 KHz
SEND_OP_COND	0	1	1	0x40000080	0x74	1	357.62 µS	389.87 KHz	390.00 KHz
R3 Response	0	0	63	0x00FF8080	0x7F	1	493.52 µS	389.90 KHz	390.01 KHz
SEND_OP_COND	0	1	1	0x40000080	0x74	1	2.3439 mS	389.88 KHz	390.00 KHz
R3 Response	0	0	63	0x00FF8080	0x7F	1	2.4798 mS	389.88 KHz	390.00 KHz
SEND_OP_COND	0	1	1	0x40000080	0x74	1	5.2491 mS	389.85 KHz	390.00 KHz
R3 Response	0	0	63	0x00FF8080	0x7F	1	5.3850 mS	389.85 KHz	390.00 KHz
SEND_OP_COND	0	1	1	0x40000080	0x74	1	8.1216 mS	389.91 KHz	390.00 KHz
R3 Response	0	0	63	0x00FF8080	0x7F	1	8.2575 mS	389.91 KHz	390.01 KHz
SEND_OP_COND	0	1	1	0x40000080	0x74	1	11.011 mS	389.90 KHz	390.00 KHz

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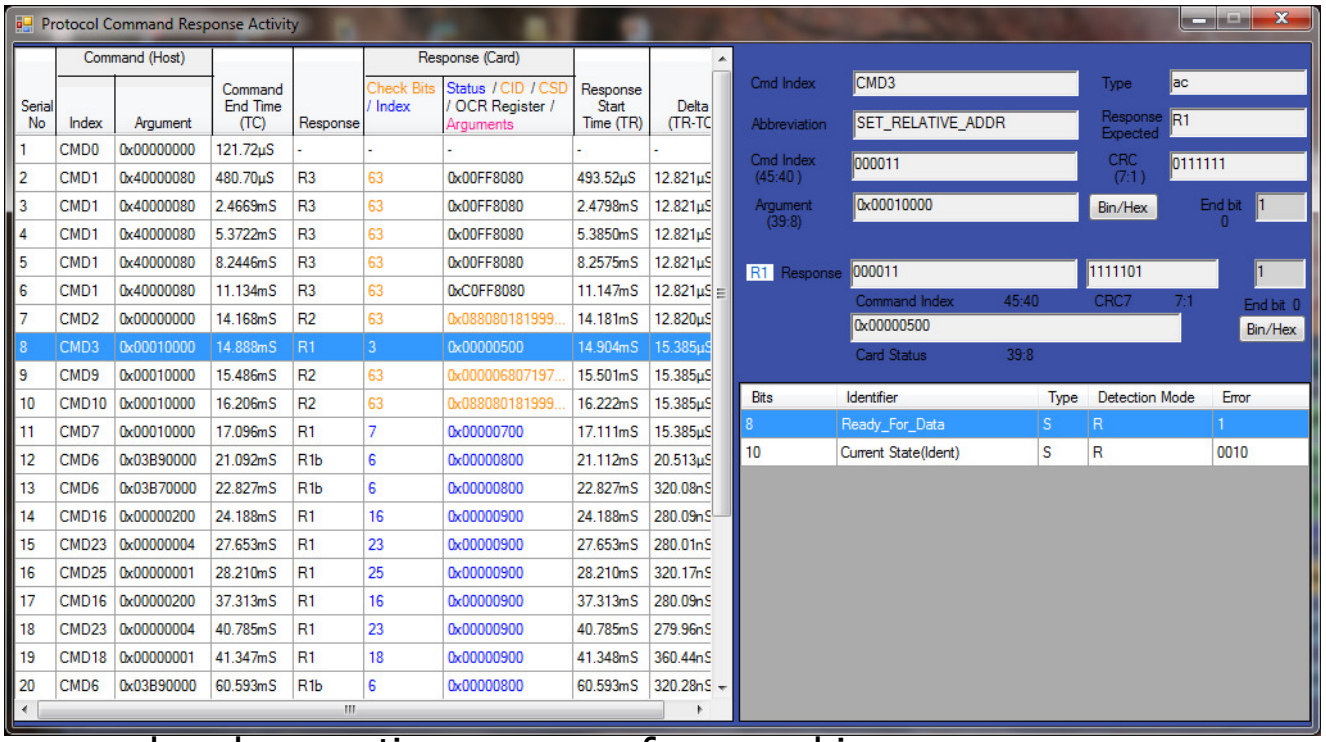
PGY-MMC-SD Electrical Validation and Protocol Decode Software- Protocol View



- List the command and respective response from card in same row
- Selected row's details of command and response are displayed at bottom the Protocol View table
- Time stamp at end of command frame and start of response
- Delta T column list the time lapsed between command and response

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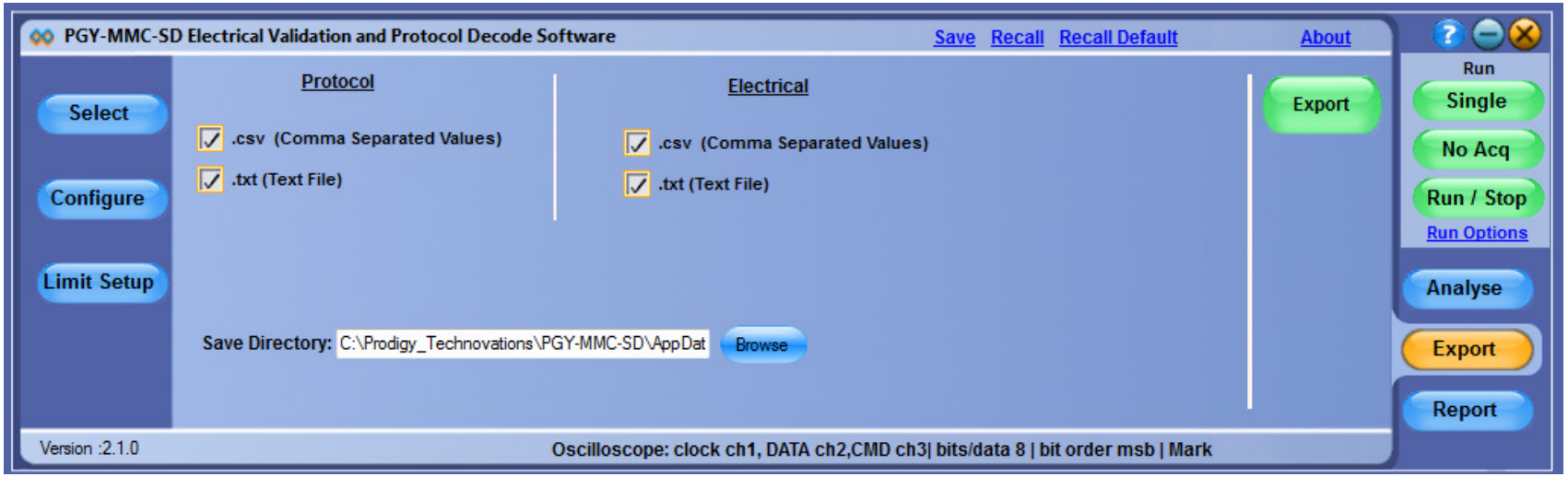
PGY-MMC-SD Electrical Validation and Protocol Decode Software- Export



- Export of Electrical measurements and Protocol Decode data to CSV and TXT file format
- Browser allows to place the data in desired location

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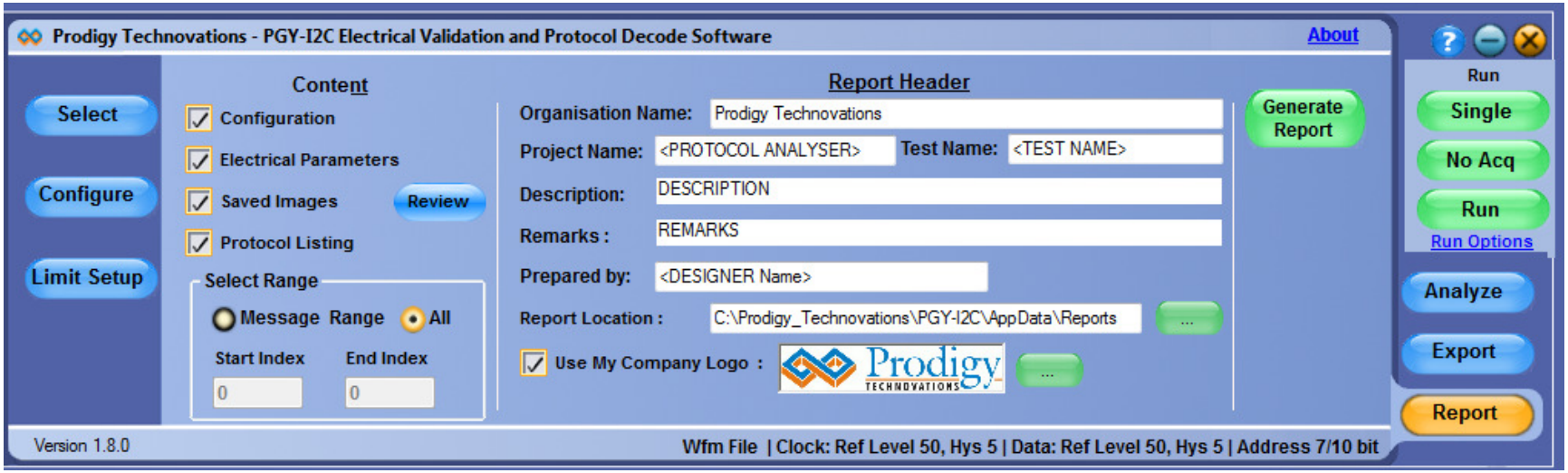
PGY-MMC-SD Electrical Validation and Protocol Decode Software- Report



- Supports customizable pdf format report generation
- Report can include electrical measurements, protocol decode, oscilloscope images, detail view images, and reference level setup
- Review of saved images allows the user to add title to image, description and delete the images

MPHY Protocol overview

<table>
<tr><th colspan="2">OSI Layer</th><th colspan="6">MIPI MPHY Protocols</th></tr>
<tr><td>Application (L7)</td><td rowspan="3">Application layer</td><td>UFS Protocol Layer</td><td>CSI-3/DSI-3 Layer</td><td>Application layer</td><td rowspan="6">SSIC Protocol</td><td rowspan="6">M-PCIe Protocol Layer</td><td rowspan="6">DigiRF Protocol</td></tr>
<tr><td>Presentation (L6)</td></tr>
<tr><td>Session (L5)</td></tr>
<tr><td>Transport (l4)</td><td>Transport</td><td colspan="2" rowspan="4">UniPRO Protocol Layer</td><td rowspan="4">LLI Protocol</td></tr>
<tr><td>Network (L3)</td><td>Network (L3)</td></tr>
<tr><td>Data Link (L2)</td><td>Data Link (L2)</td></tr>
<tr><td></td><td>PHY Adapter layer (L1.5)</td></tr>
<tr><td>Physical layer (L1)</td><td colspan="7">Physical layer (L1)</td></tr>
</table>

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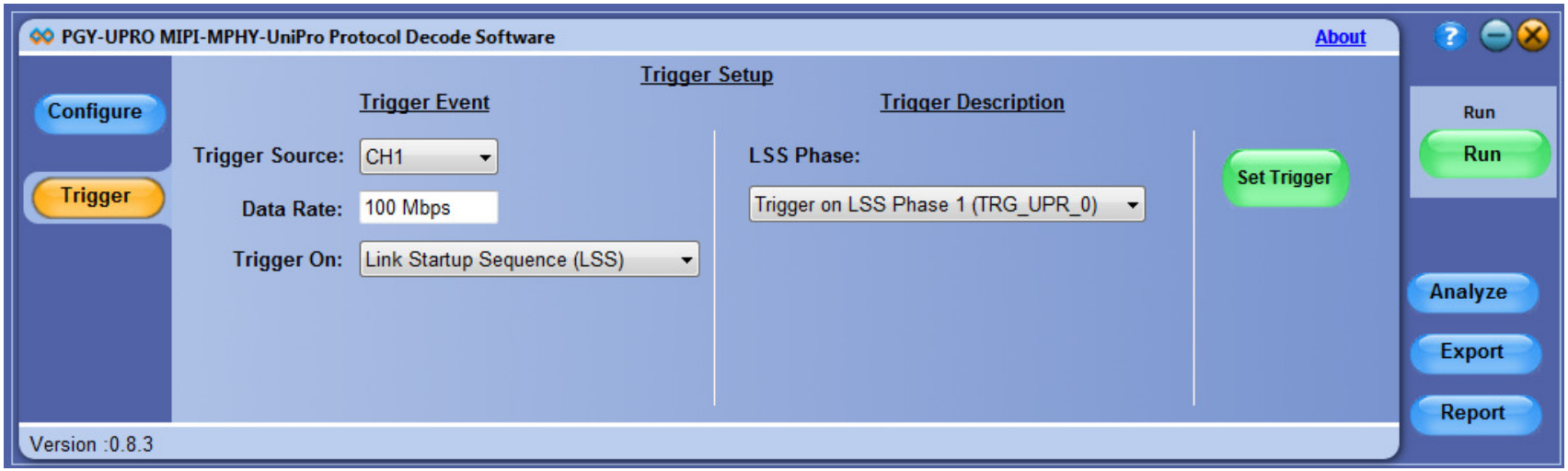
Trigger setup for UniPro/LLI



- Applications make use of serial trigger available in scope to trigger UniPRO/LLI Protocol content
- Requires Option ST6G option in the oscilloscope
- Trigger source could be any oscilloscope live channels
- Supports triggering using Link startup sequence, PA layer packet content and datalink layer packet content

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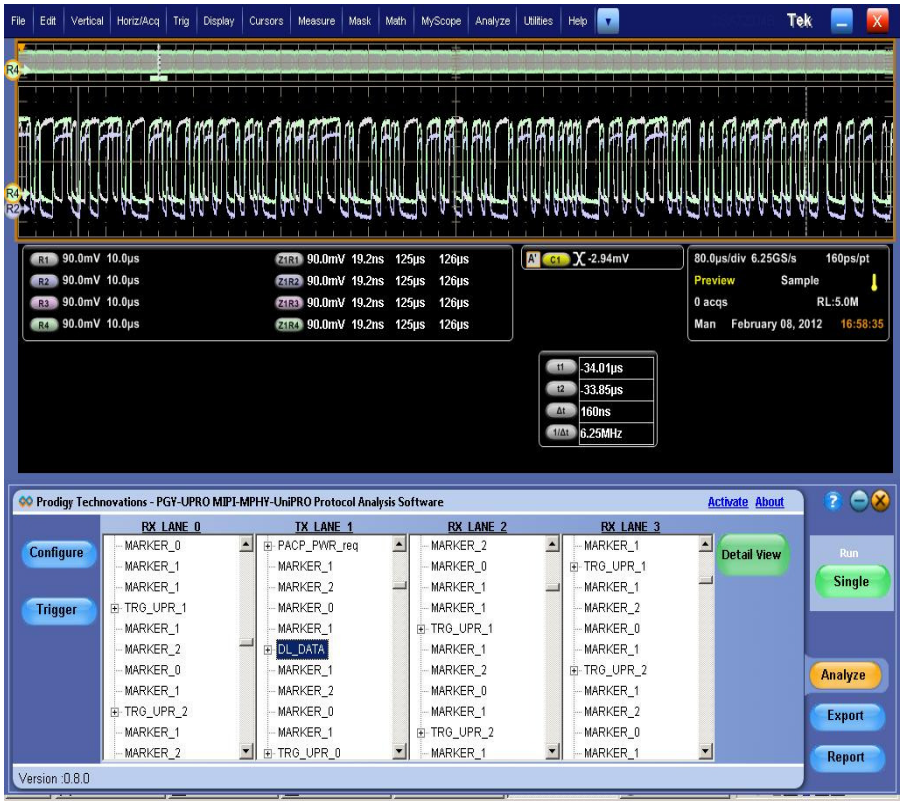
UniPro Trigger Features

Trigger Event	Trigger Content
Link Startup Sequence (LSS)	Trigger on LSS Phase 1 (TRG_UPR_0)
	Trigger on LSS Phase 2 (TRG_UPR_1)
	Trigger on LSS Phase 3 (TRG_UPR_2)
Phy Adapter layer Content	PACP_PWR_req
	PACP_PWR_cnf
	PACP_cap_ind
	PACP_EPR_ind
	PACP_TEST_MODE_req
	PACP_GET_req
	PACP_GET_cnf
	PACP_SET_req
	PACP_SET_cnf
	PACP_Test_Data
Data Link layer Content	Data_SOF
	Data_COF
	AFC (Acknowledgement)
	NAC (No Acknowledgement)

Seamless Integration of PGY-UniPro and Oscilloscope view

- Decoded data is displayed in bottom half of the scope display and scope waveform display on top
- Packet level info with flexibility to collapse the packet to view packet content
- Link the UniPro packet to oscilloscope waveform with cursors placement at start and end of the packet waveform



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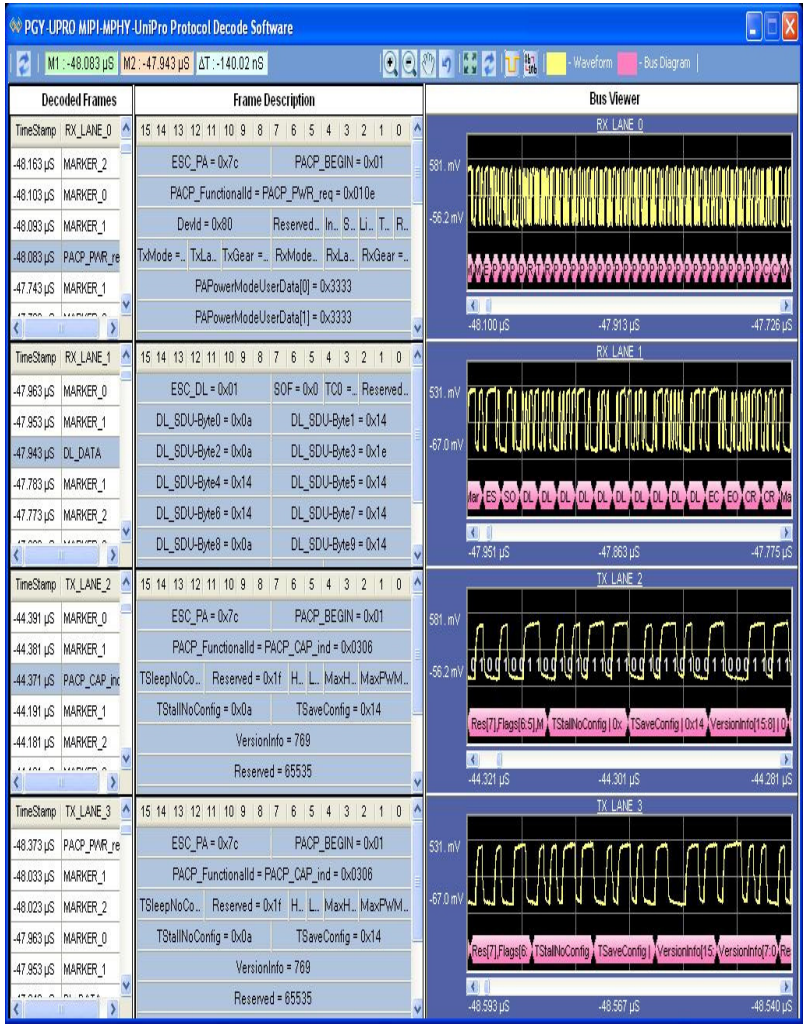
PGY-UniPro/LLI UniPro and LLI Protocol Decode S/W

- UniPro and LLI Protocol Decoder enables faster system level protocol debugging
- Conforms to UniPro Protocol Specification version 1.4 and LLI Protocol version 0.8
- Detail view provides a comprehensive protocol and physical layer data correlation
- Automated CRC computation to monitor CRC errors in protocol packet
- Trigger configuration leverages the Oscilloscope option ST6G serial trigger features and helps to trigger the UniPro and LLI specific events
- Generates comprehensive and customizable reports
- Ability to export the protocol and measurement details to txt and csv file formats



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UFS Protocol Overview

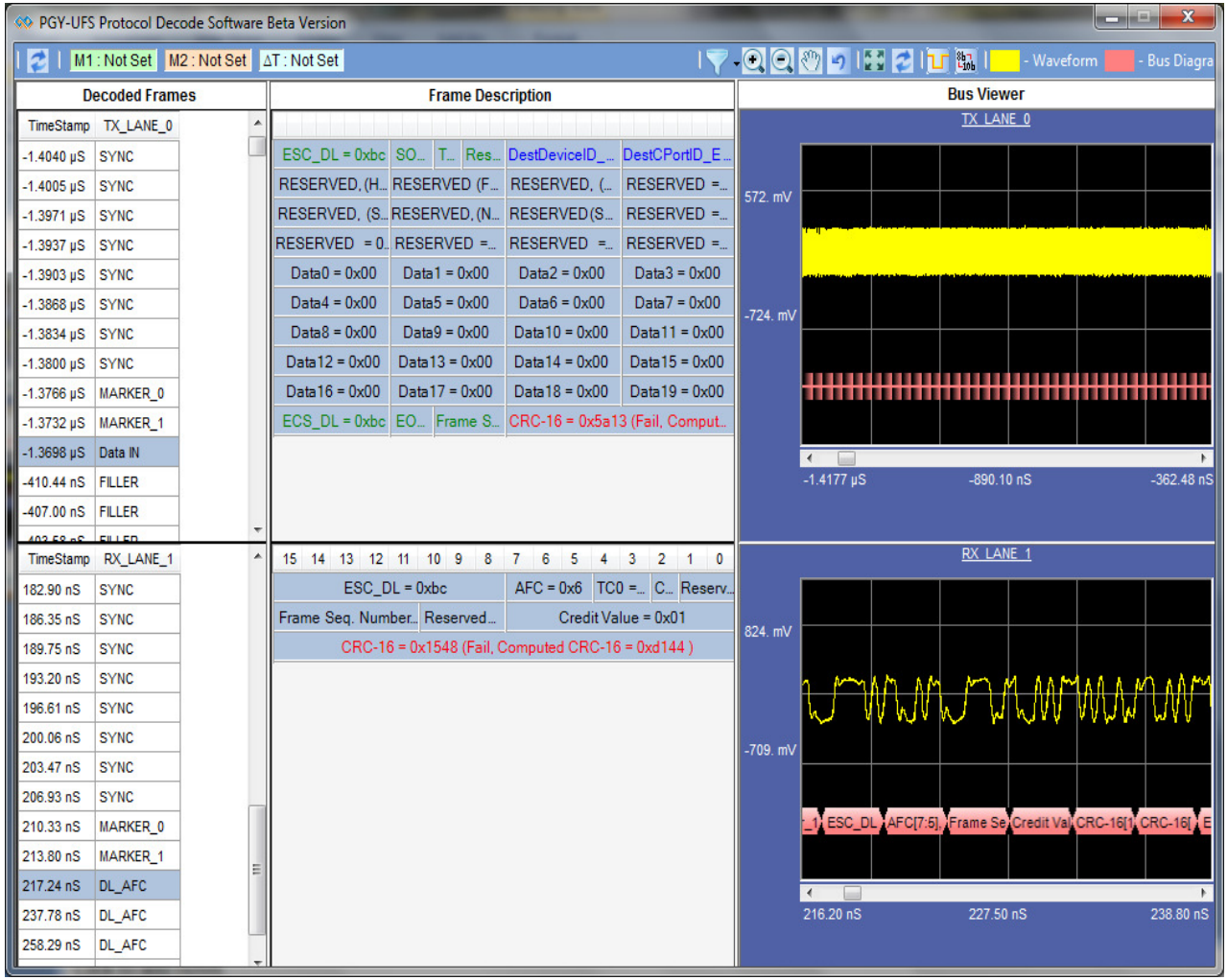
- UFS Protocol Information Units (UPIU) that travel between devices on the UniPRO bus
- All UFS UPIU's consist of a single basic header segment, possibly one or more extended header segments and zero or more data segments.
- A basic header segment has a fixed length of 12 bytes. The minimum UPIU size is 32 bytes which includes a basic header segment and transaction specific fields.

Details of UPIU

UPIU Data Structure	Description
NOP Out	The NOP Out transaction acts as a ping from an initiator to a target. It can be used to check for a connection path to a device and LUN.
NOP In	The NOP In transaction is a target response to an initiator when responding to a NOP In request.
Command	The Command transaction originates in the Initiator (host) and is sent to a logical unit within a Target device. A Command UPIU will contain a Command Descriptor Block as the command and the command parameters. When using the phase collapse feature the UPIU will also contain a data segment that would have been sent during the DATA OUT phase. This represents the COMMAND phase of the command.
Response	The Response transaction originates in the Target and is sent back to the Initiator (host). A Response UPIU will contain a command specific operation status and other response information. When using the phase collapse feature, the UPIU will also contain a data segment that would have been sent during the DATA IN phase. This represents the STATUS phase of the command.
Data Out	The Data Out transaction originates in the Initiator (host) and is used to send data from the Initiator to the Target (device). This represents the DATA OUT phase of a command.
Data In	The Data In transaction originates in the Target (device) and is used to send data from the Target to the Initiator (host). This represents the DATA IN phase of a command.
Task Management Request	This transaction type carries SCSI Architecture Model (SAM) task management function requests originating at the Initiator and terminating at the Target. The standard functions are defined by the SAM-5 specification. Addition functions might be defined by UFS.
Task Management Response	This transaction type carries SCSI Architecture Model (SAM) task management function responses originating in the Target and terminating at the Initiator.
Ready To Transfer	The Target device will send a Ready To Transfer transaction when it is ready to receive the next Data Out UPIU and has sufficient buffer space to receive the data. The Target can send multiple Ready To Transfer UPIU if it has buffer space to receive multiple Data Out UPIU packets. The maximum data buffer size is negotiated between the Initiator and Target during enumeration and configuration. The Ready To Transfer UPIU contains a DMA context and can be used to setup and trigger a DMA action within a host controller.
Query Request	This transaction originates in the Initiator and is used to request descriptor data from the Target. This transaction is defined outside of the Command and Task Management functions and is defined exclusively by UFS.
Query Response	This transaction originates in the Target and provides requested descriptor information to the Initiator in response of the Query Request transaction. This transaction is defined outside of the Command and Task Management functions and is defined exclusively by UFS.

Simultaneous view of UniPro and UFS Protocol

- Application supports simutaneous view of UniPRO and UFS Protocol
- In this screenshot you can UFS-Data-in packet info as well ACK packet using UniPRO-UFS View



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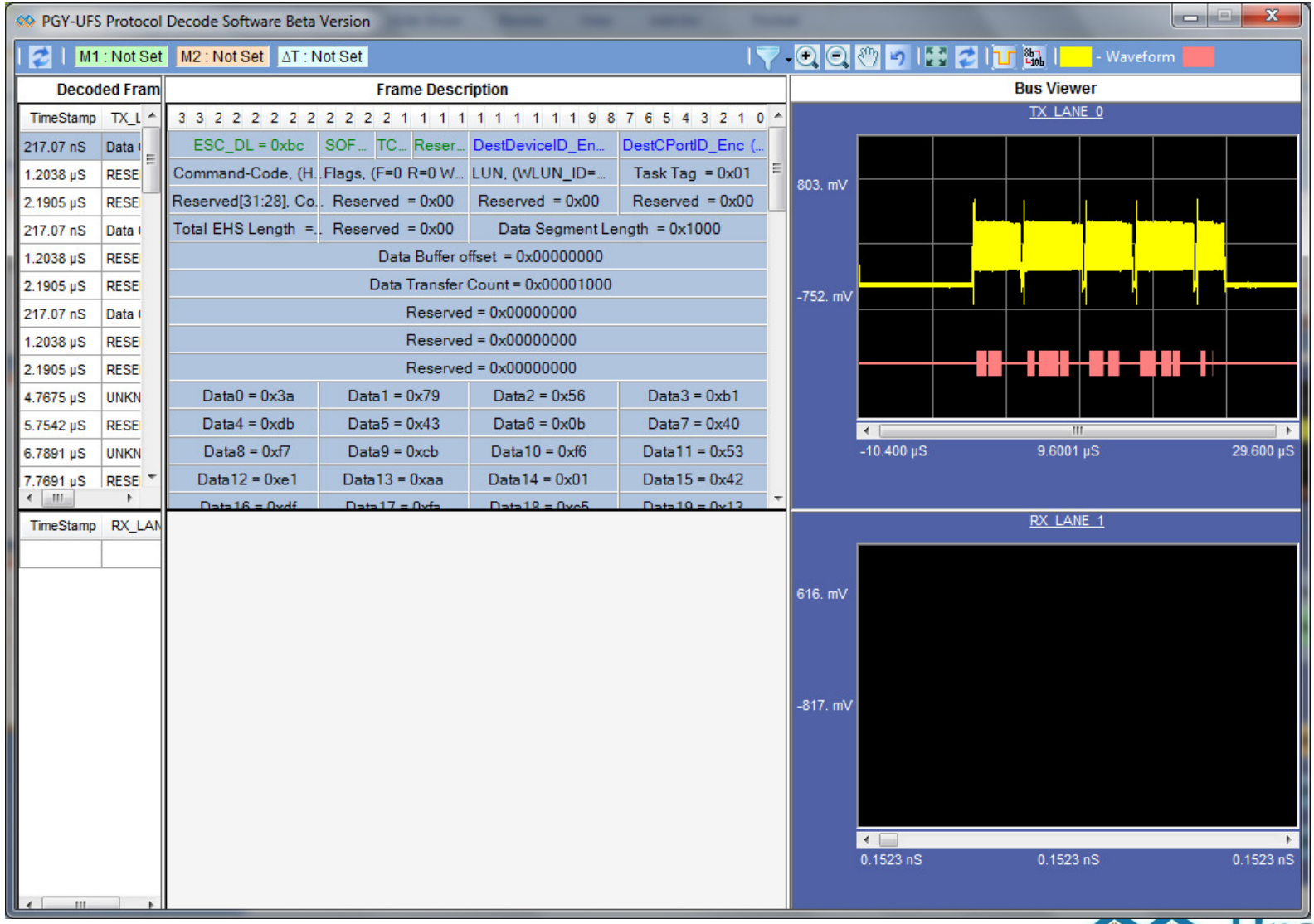
UFS Protocol view of data-out



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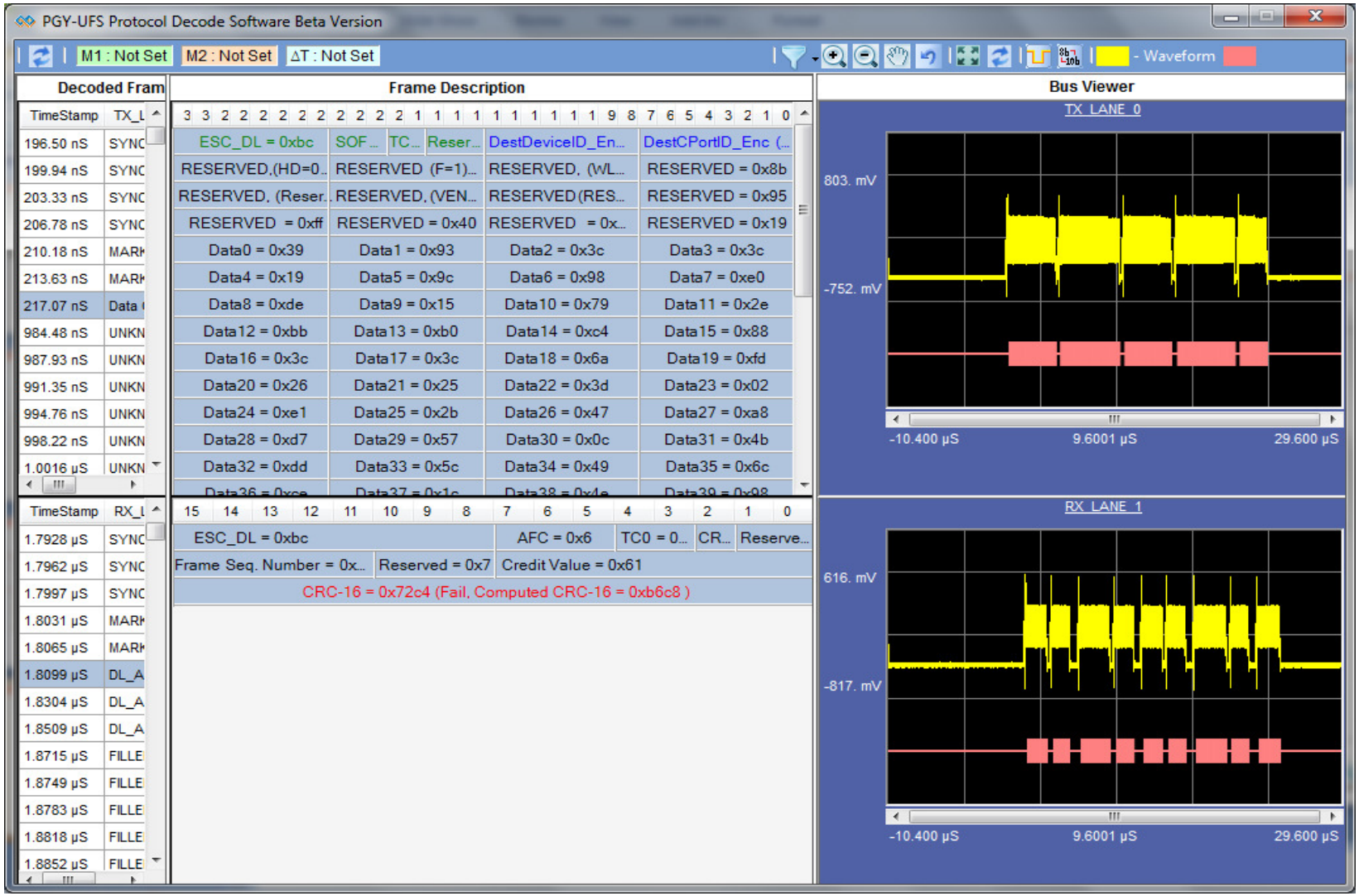
UniPRO-UFS Protocol View



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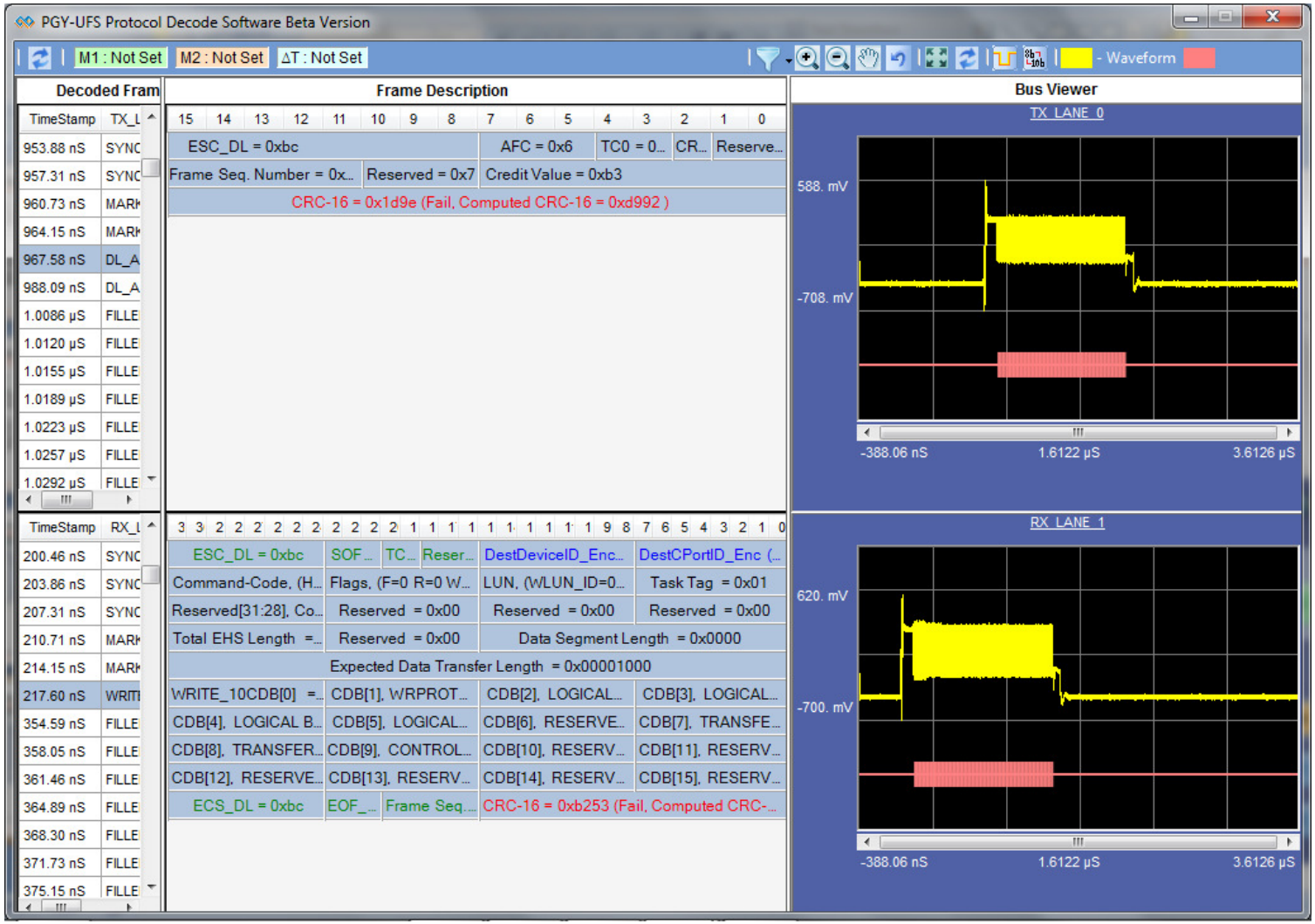
UniPRO-UFS Protocol –Write Command



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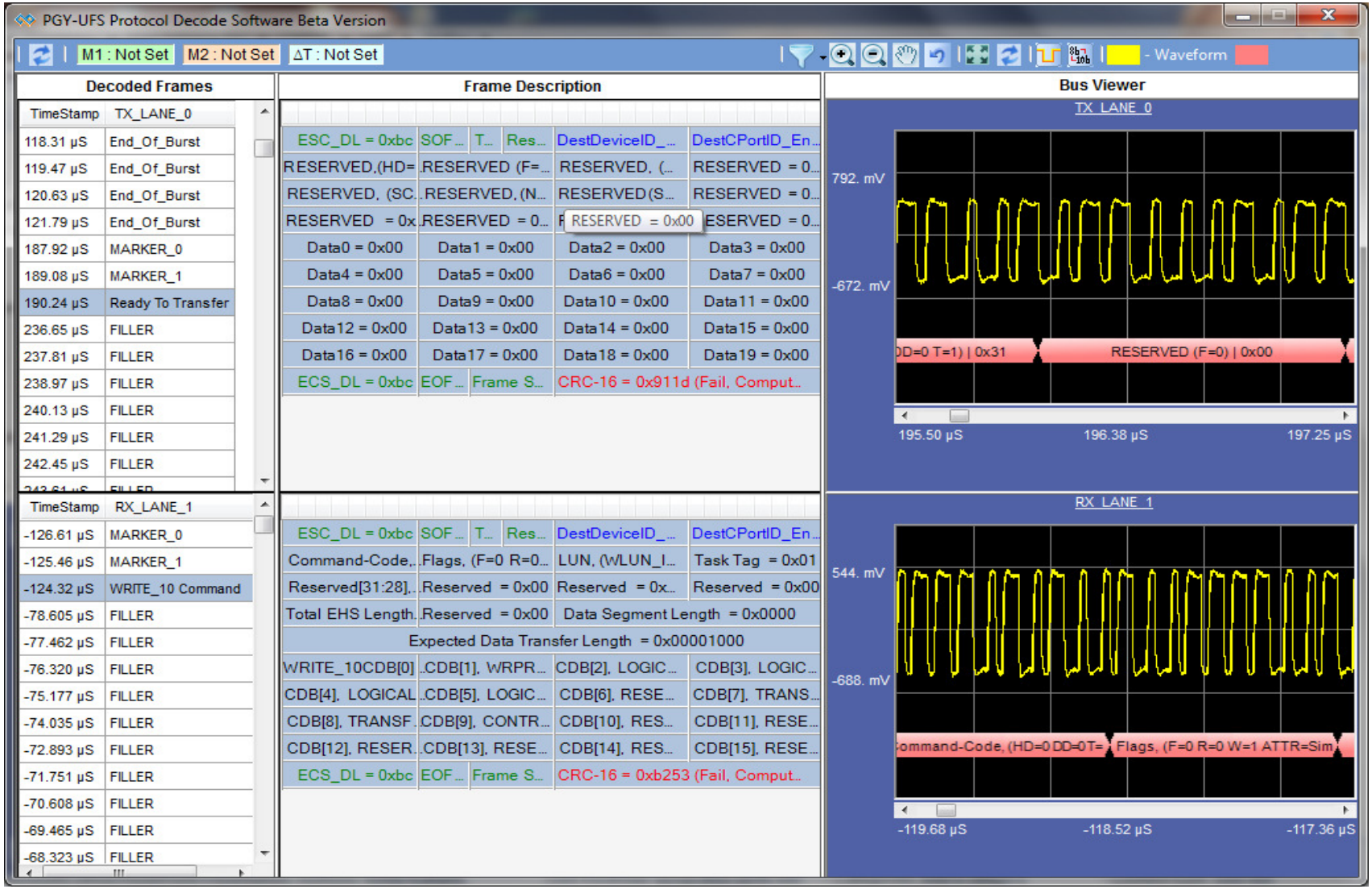
UniPRO-UFS Protocol Decode-Write command (PWM Signal)



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Thank You