



Mobile Storage Solution:
eMMC Electrical Validation and
Protocol Analysis S/W and UFS
Protocol Decode S/W



Agenda

- ▶ eMMC technology overview
- ▶ Electrical measurements V4.41, V4.51
- ▶ eMMC Protocol overview
- ▶ PGY-MMC Electrical Validation and Protocol Analysis Software
- ▶ UFS Technology Overview
- ▶ UFS Protocol Analysis
- ▶ PGY-UPRO/UFS Protocol Decode Software
- ▶ Demo
- ▶ Q&A



eMMC Technology Overview

- ▶ Multimedia card transfers data via configurable data bus signals
- ▶ Communication Signals
 - **CLK:** Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.
 - **CMD:** This signal is a bidirectional command channel used for card initialization and transfer of commands.
 - **DAT0-DAT7:** These are bidirectional data channels (1 bit/4 bit/8bit)

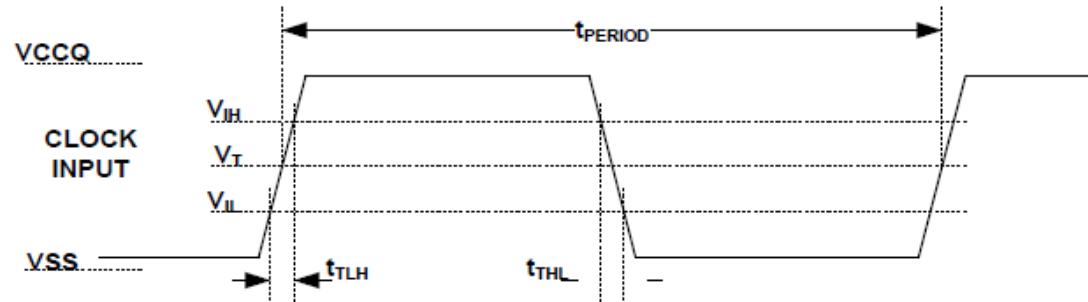
eMMC SDR Timing Data

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK⁽¹⁾					
Clock frequency Data Transfer Mode (PP) ⁽²⁾	f _{pp}	0	52 ⁽³⁾	MHz	CL ≤ 30 pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	f _{OD}	0	400	kHz	Tolerance: +20KHz
Clock high time	t _{WH}	6.5		ns	CL ≤ 30 pF
Clock low time	t _{WL}	6.5		ns	CL ≤ 30 pF
Clock rise time ⁽⁴⁾	t _{TLH}		3	ns	CL ≤ 30 pF
Clock fall time	t _{THL}		3	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t _{ISU}	3		ns	CL ≤ 30 pF
Input hold time	t _{IH}	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	t _{ODLY}		13.7	ns	CL ≤ 30 pF
Output hold time	t _{OH}	2.5		ns	CL ≤ 30 pF
Signal rise time ⁽⁵⁾	t _{RISE}		3	ns	CL ≤ 30 pF
Signal fall time	t _{FALL}		3	ns	CL ≤ 30 pF
<p>NOTE 1. CLK timing is measured at 50% of VDD.</p> <p>NOTE 2. A eMMC shall support the full frequency range from 0-26Mhz, or 0-52MHz</p> <p>NOTE 3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.</p> <p>NOTE 4. CLK rise and fall times are measured by min (VIH) and max (VIL).</p> <p>NOTE 5. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).</p>					

eMMC DDR timing Data

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK⁽¹⁾					
Clock frequency Data Transfer Mode (PP) ⁽²⁾	f _{pp}	0	52 ⁽³⁾	MHz	CL ≤ 30 pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	f _{OD}	0	400	kHz	Tolerance: +20KHz
Clock high time	t _{WH}	6.5		ns	CL ≤ 30 pF
Clock low time	t _{WL}	6.5		ns	CL ≤ 30 pF
Clock rise time ⁽⁴⁾	t _{TLH}		3	ns	CL ≤ 30 pF
Clock fall time	t _{THL}		3	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t _{ISU}	3		ns	CL ≤ 30 pF
Input hold time	t _{IH}	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	t _{ODLY}		13.7	ns	CL ≤ 30 pF
Output hold time	t _{OH}	2.5		ns	CL ≤ 30 pF
Signal rise time ⁽⁵⁾	t _{RISE}		3	ns	CL ≤ 30 pF
Signal fall time	t _{FALL}		3	ns	CL ≤ 30 pF
NOTE 1. CLK timing is measured at 50% of VDD.					
NOTE 2. A eMMC shall support the full frequency range from 0-26Mhz, or 0-52MHz					
NOTE 3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.					
NOTE 4. CLK rise and fall times are measured by min (VIH) and max (VIL).					
NOTE 5. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).					

eMMC v4.51 clock Timing Measurements

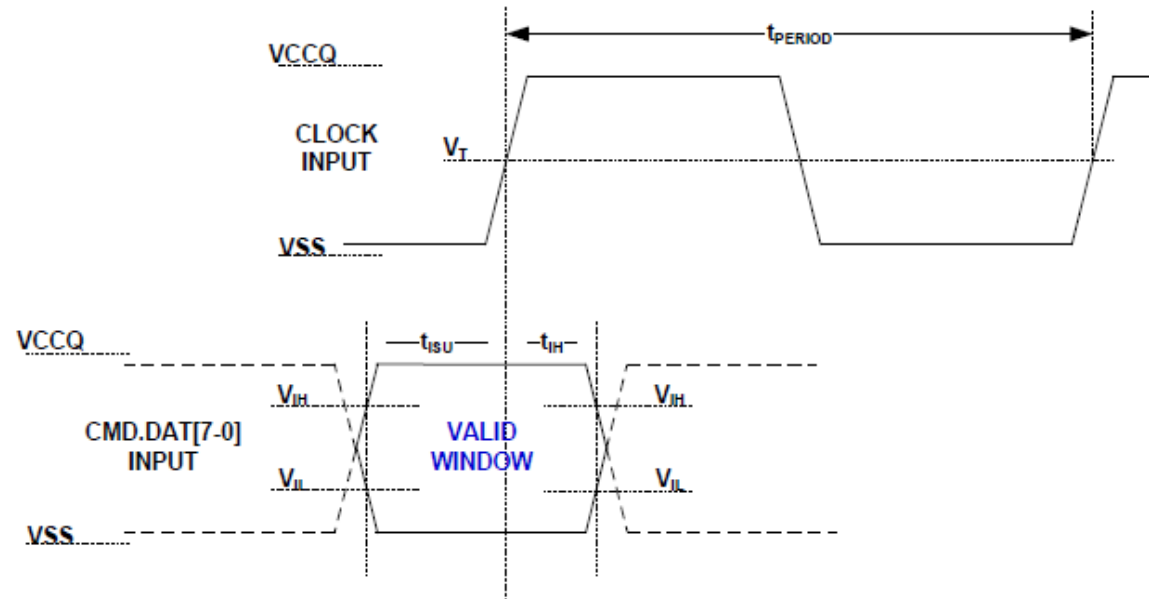


NOTE 1 V_{IH} denote $V_{IH(min.)}$ and V_{IL} denotes $V_{IL(max.)}$.

NOTE 2 $V_T=0.975V$ - Clock Threshold ($V_{CCQ} = 1.8V$) and $V_T=0.65V$ - Clock Threshold ($V_{CCQ} = 1.2V$) , indicates clock reference point for timing measurements.

Symbol	Min.	Max.	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	$0.2 \cdot t_{PERIOD}$	ns	$t_{TLH}, t_{THL} < 1ns$ (max.) at 200MHz, $C_{BGA}=12pF$, The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

eMMC4.51 timing Measurements

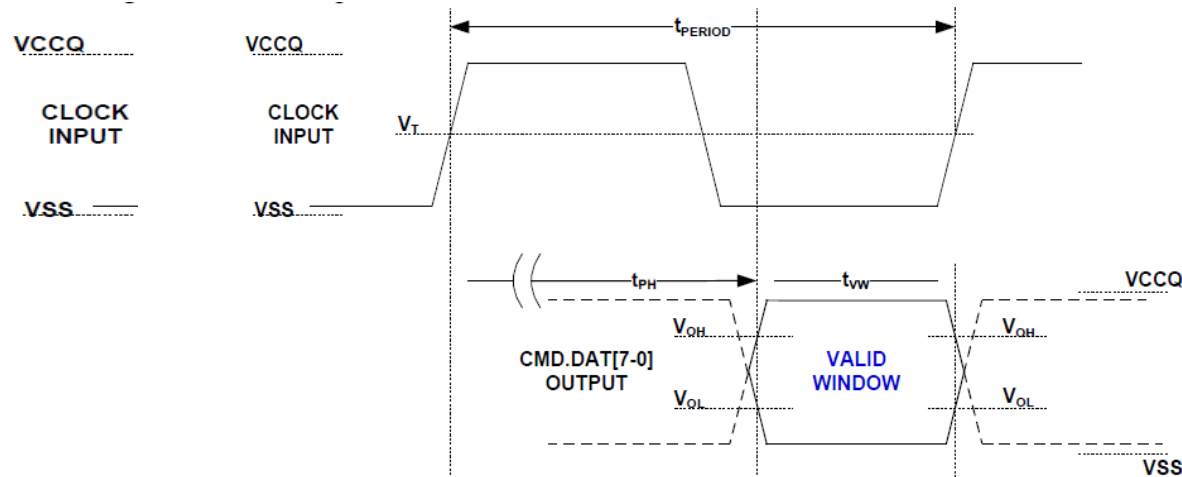


Note1: t_{ISU} and t_{IH} are measured at $V_{IL}(\max.)$ and $V_{IH}(\min.)$.

Note2: V_{IH} denote $V_{IH}(\min.)$ and V_{IL} denotes $V_{IL}(\max.)$.

Symbol	Min.	Max.	Unit	Remark
t_{ISU}	1.40	-	ns	$5\text{pF} \leq C_{BGA} \leq 12\text{pF}$
t_{IH}	0.8		ns	$5\text{pF} \leq C_{BGA} \leq 12\text{pF}$

eMMC 4.51 timing measurements

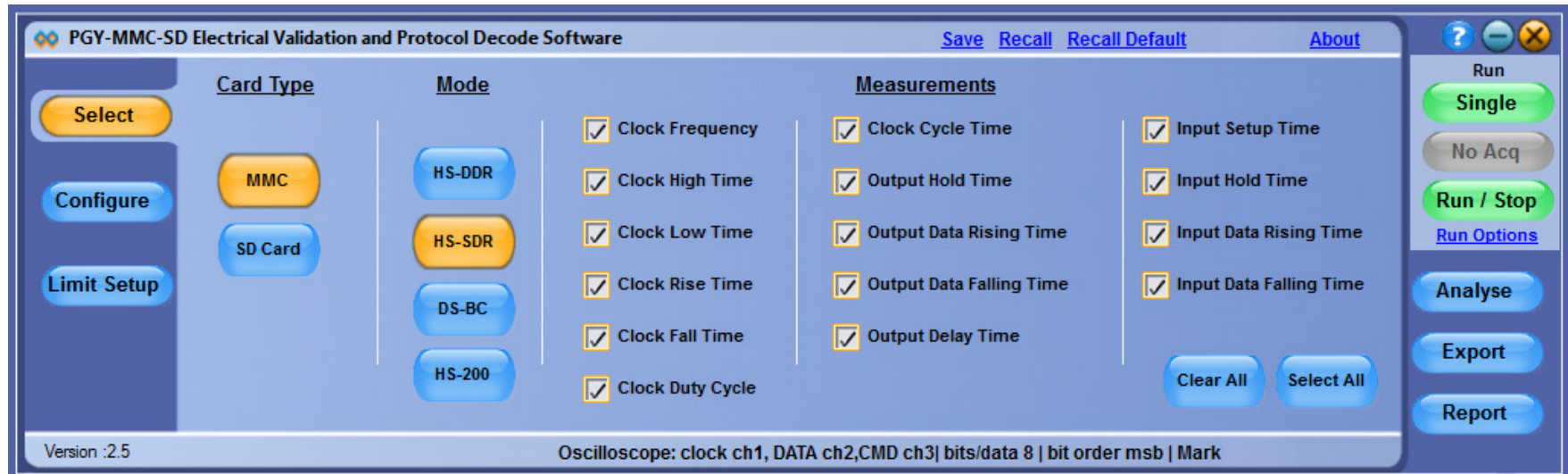


NOTE V_{OH} denotes $V_{OH(min.)}$ and V_{OL} denotes $V_{OL(max.)}$.

Table 1/2 — Output timing

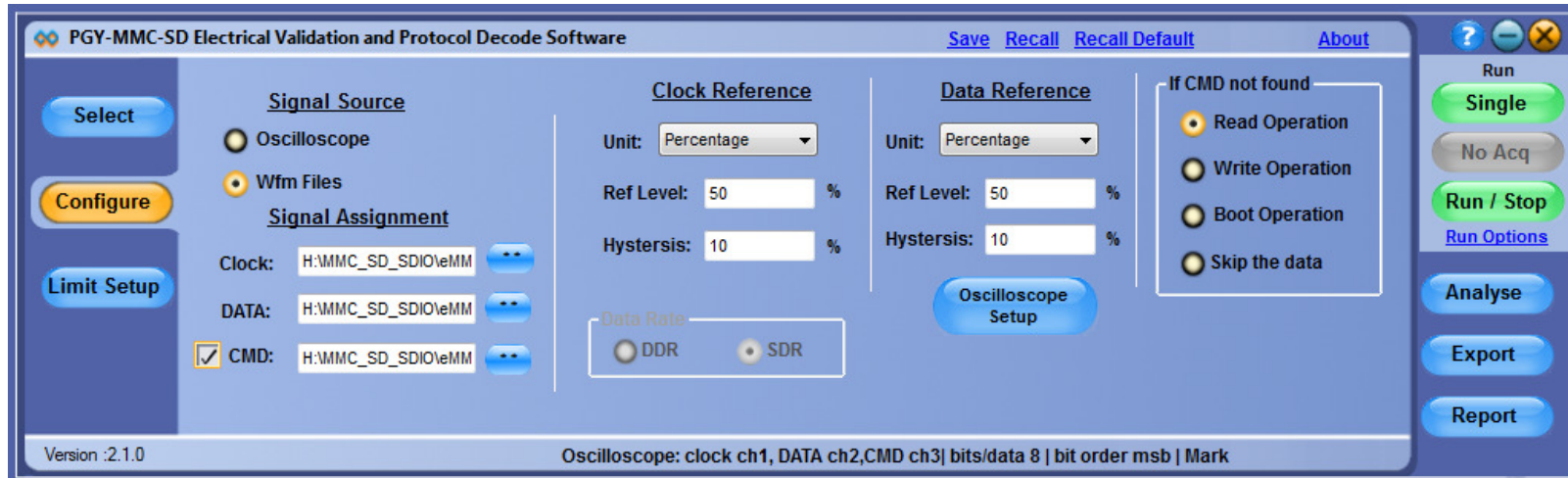
Symbol	Min.	Max.	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 ($\Delta T = -20$ deg.C)	+1550 ($\Delta T = 90$ deg.C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25 deg.C to 125 deg.C during operation.
t_{VW}	0.575	-	UI	$t_{VW} = 2.88ns$ at 200MHz Using test circuit in Figure 72 including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected T_{VW} at Host input is larger than 0.475UI.

PGY-eMMC/Sd Electrical Validation and Protocol Decode Software- Select



- ▶ User can select eMMC type and select data mode
- ▶ eMMC Electrical measurements as specified in I2C Standard document are listed
- ▶ User has flexibility select few measurements or all measurements
- ▶ Supports electrical measurement for eMMC4.41 and 4.51

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Configure



- ▶ Select the source of the signal from oscilloscope or saved files
- ▶ Use Clock and Data Reference by value. If signal is noisy set the hysteresis at least 15% to avoid any intermittent transition as logic state

PGY-eMMC-SD Electrical Validation and Protocol Decode Software- Limit Setup

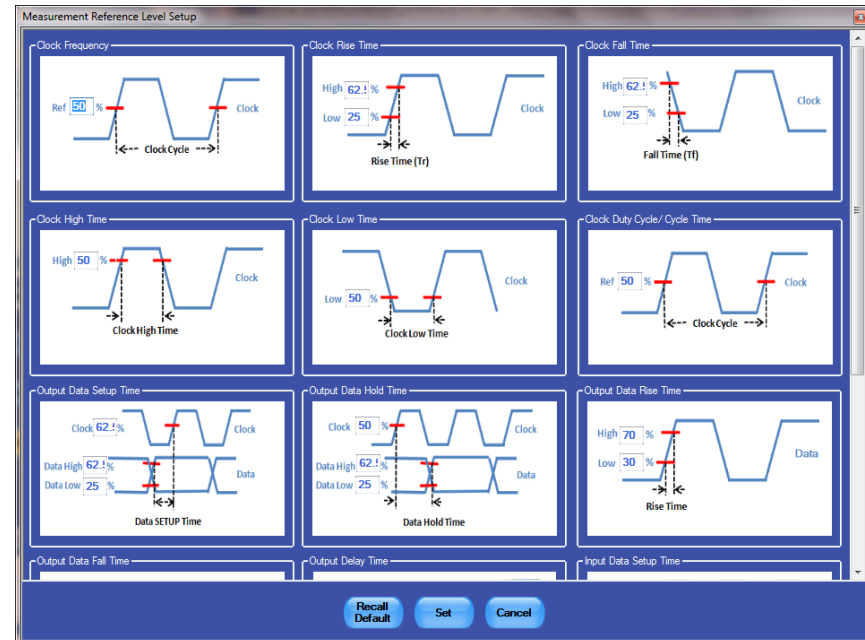
The screenshot shows the 'Limit Setup' window of the PGY-MMC-SD Electrical Validation and Protocol Decode Software. The window has a title bar with the software name and buttons for 'Save', 'Recall', 'Recall Default', and 'About'. On the left, there are three buttons: 'Select', 'Configure', and 'Limit Setup' (which is highlighted). The main area is titled 'Measurement Limits' and contains a grid of input fields for various timing parameters. Each field has a 'Low' and 'High' limit, a unit dropdown, and a 'NA' option. The parameters include Clock Frequency, Clock Cycle Time, Input Setup Time, Clock Rise Time, Output Hold Time, Input Hold Time, Clock Fall Time, Output Data Rise Time, Input Data Rise Time, Clock High Time, Output Data Fall Time, Input Data Fall Time, Clock Low Time, Output Delay Time, and Clock Duty Cycle. At the bottom left, the version is '2.1.0'. At the bottom right, there is an oscilloscope configuration string: 'Oscilloscope: clock ch1, DATA ch2,CMD ch3| bits/data 8 | bit order msb | Mark'. On the far right, there is a vertical toolbar with buttons: 'Run', 'Single', 'No Acq', 'Run / Stop', 'Run Options', 'Analyse', 'Export', and 'Report'.

Parameter	Low	High	Unit
Clock Frequency	0	52	MHz
Clock Cycle Time	1	5	nS
Input Setup Time	3	NA	nS
Clock Rise Time	NA	3	nS
Output Hold Time	2.5	NA	nS
Input Hold Time	3	NA	nS
Clock Fall Time	NA	3	nS
Output Data Rise Time	NA	3	nS
Input Data Rise Time	NA	3	nS
Clock High Time	6.5	NA	nS
Output Data Fall Time	NA	3	nS
Input Data Fall Time	NA	3	nS
Clock Low Time	6.5	NA	nS
Output Delay Time	8	20	nS
Clock Duty Cycle	NA	NA	%

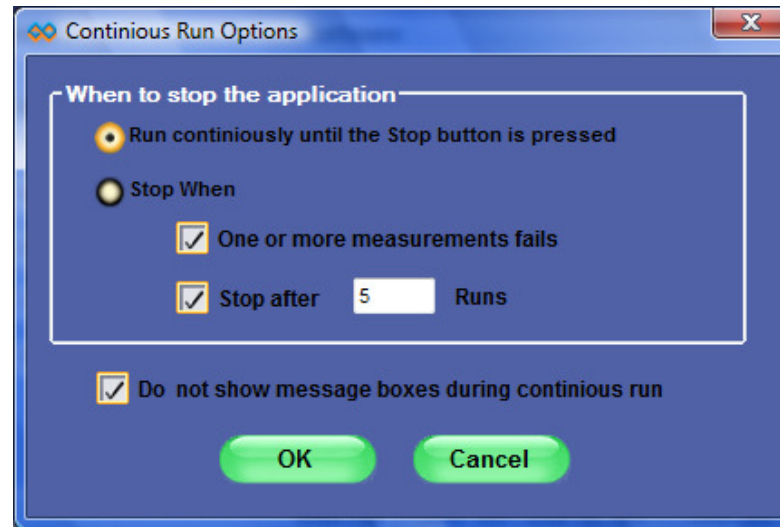
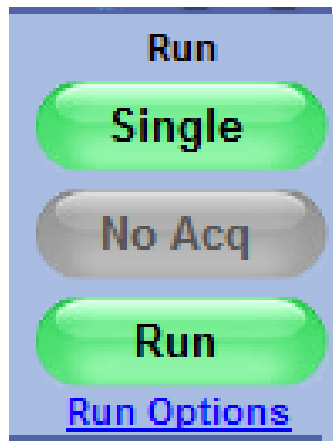
- ▶ Limits can be set to default limits as specified in standard document
- ▶ User defined Low and High Limits as per in-house specification
- ▶ Save and Recall the limits

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Reference Level Setup

- ▶ Graphical User Interface eases of reference level setup and avoid human errors
- ▶ User can view the default reference levels set for each of the electrical measurement
- ▶ Edit reference level setup for each of the measurements
- ▶ Save and recall of reference level setup



PGY-MMC-SD Electrical Validation and Protocol Decode Software- Run-Control



- ▶ Run Control captures the data and analyses it as per configure, limit values and reference level setup
- ▶ Analysis of signal using Single or Continuous acquisition
- ▶ Analysis of signals present in acquisition memory using **No Acq** mode
- ▶ Flexibility to stop the test if one or more measurement fails/ after running user defined number of tests

PGY-MMC-SD Electrical Validation and Protocol Decode Software-Analyze

Measurement	Minimum	Mean	Maximum	Low Limit	High Limit	Result
✓ Clock Frequency	389.84...	1.0558...	25.456...	0.0000Hz	52.000 MHz	Pass
✓ Clock Rise Time	1.3305 nS	1.8930 nS	3.5875 nS	NA	3.0000 nS	Pass★
✓ Clock Fall Time	1.3063 nS	1.9395 nS	3.9166 nS	NA	3.0000 nS	Pass★
✓ Clock High Time	19.742 nS	473.92 nS	1.2842 μS	6.5000 nS	NA	Pass
✓ Clock Low Time	18.460 nS	473.25 nS	1.2838 μS	6.5000 nS	NA	Pass
✗ Clock Duty C...	49.533 %	50.523 %	53.489 %	NA	NA	NA
✗ Clock Cycle ...	39.285 nS	947.16 nS	2.5652 μS	1.0000 nS	5.0000 nS	Fail
✓ Output Hold ...	19.239 nS	493.09 nS	1.2836 μS	2.5000 nS	NA	Pass
✓ Output Data ...	1.4091 nS	1.9213 nS	3.3658 nS	NA	3.0000 nS	Pass★

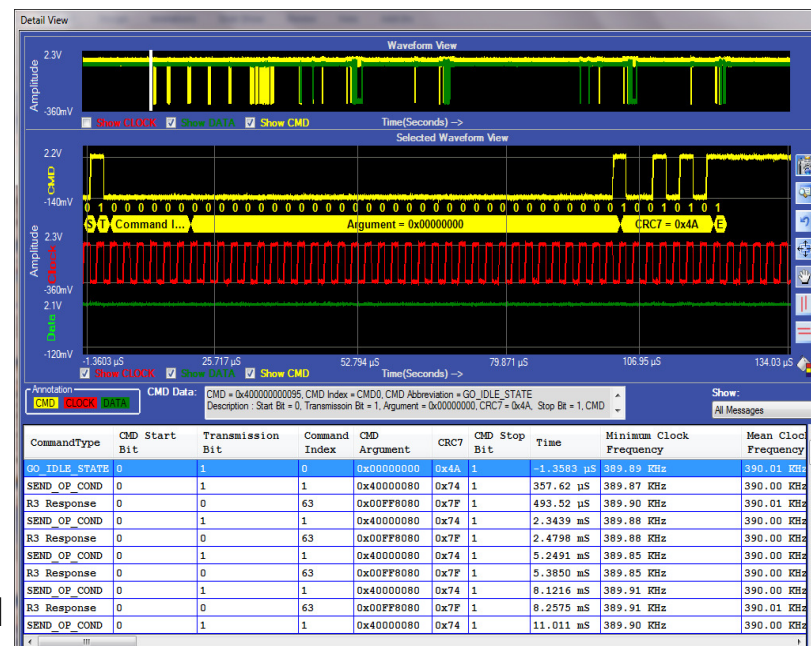
Version :2.1.0

Oscilloscope: clock ch1, DATA ch2,CMD ch3| bits/data 8 | bit order msb | Mark

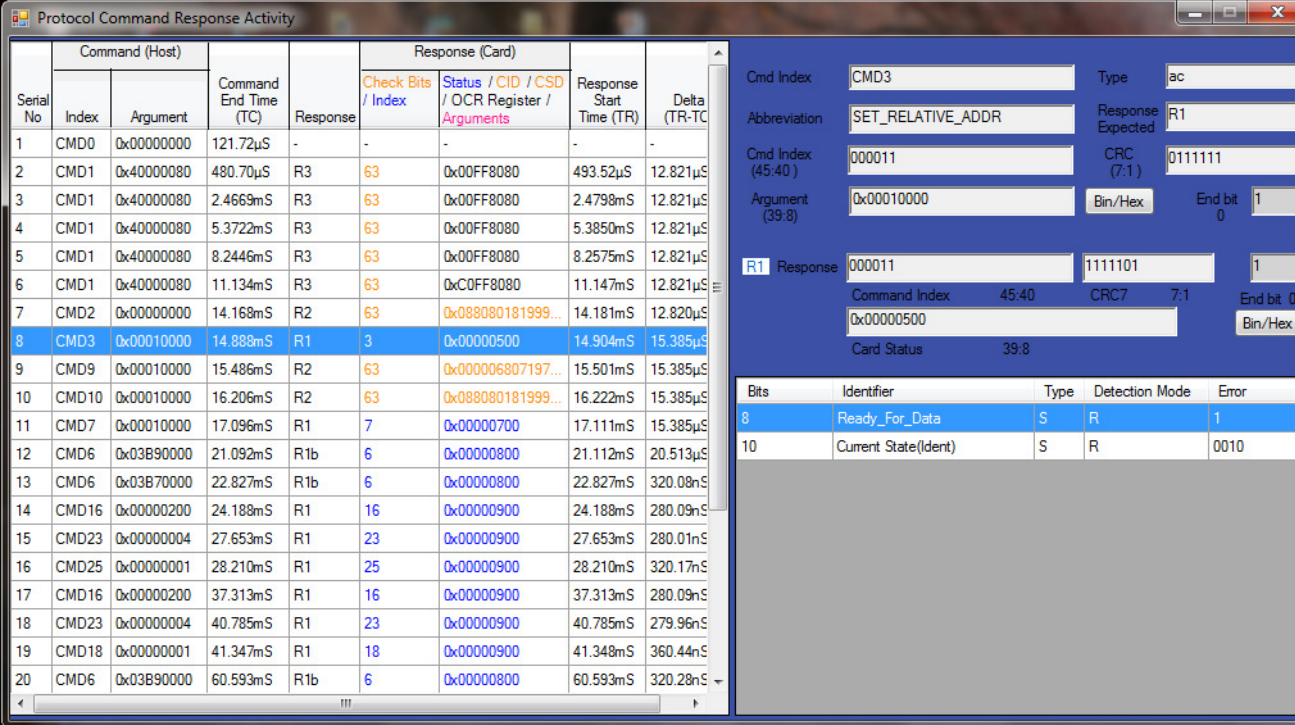
- ▶ Displays measurement limits and annotation to indicate pass or fail
- ▶ Provides min, max and mean measurement values
- ▶ Detail View provides debugging environment
- ▶ Protocol view provides details of protocol transaction

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Detail View

- ▶ Provides powerful debug environment co-relating physical layer waveform, protocol decode data and electrical measurements
- ▶ Selected protocol decode message waveform is plotted in selected waveform window
- ▶ Reference cursor will be placed in acquired waveform window to indicate the position of the waveform in Acquired data
- ▶ Failed Electrical measurements selected in red color
- ▶ Cursor measurements for manual analysis
- ▶ Markers to indicate reference level for measurement
- ▶ Take snapshot of selected waveform image from detail view for report
- ▶ Decode tables list the Commands and responses from card
- ▶ Utility features for zooming the waveform, pan, cursors, reference set markers and image capture for report



PGY-MMC-SD Electrical Validation and Protocol Decode Software- Protocol View



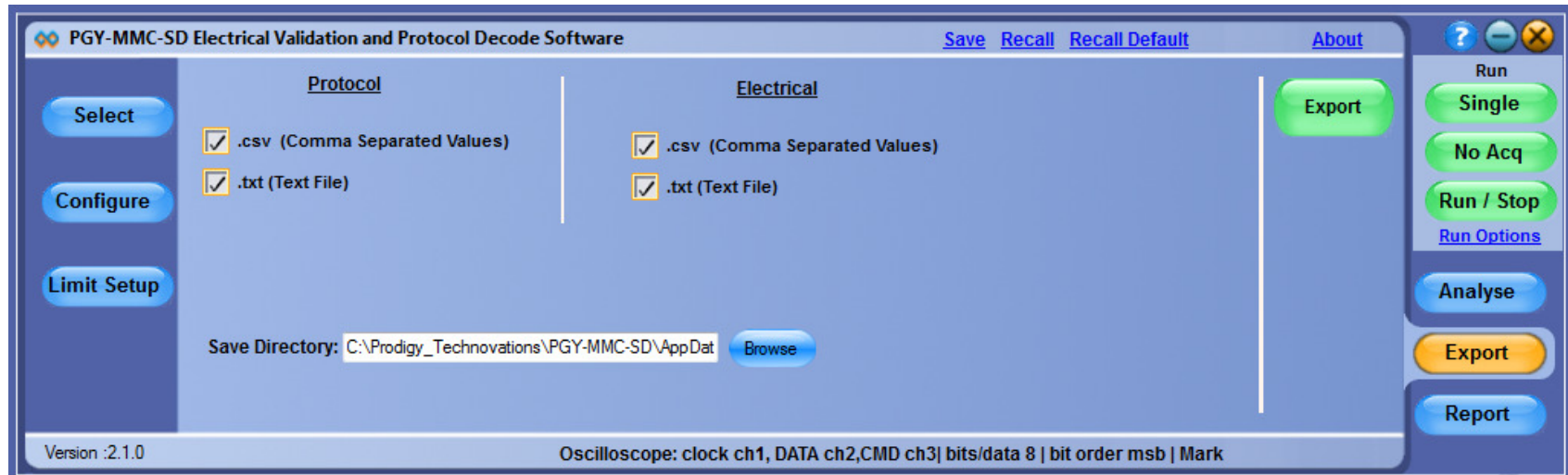
Serial No	Command (Host)		Command End Time (TC)	Response	Response (Card)		Response Start Time (TR)	Delta (TR-TC)
	Index	Argument			Check Bits / Index	Status / CID / CSD / OCR Register / Arguments		
1	CMD0	0x00000000	121.72µS	-	-	-	-	-
2	CMD1	0x40000080	480.70µS	R3	63	0x00FF8080	493.52µS	12.821µS
3	CMD1	0x40000080	2.4669mS	R3	63	0x00FF8080	2.4798mS	12.821µS
4	CMD1	0x40000080	5.3722mS	R3	63	0x00FF8080	5.3850mS	12.821µS
5	CMD1	0x40000080	8.2446mS	R3	63	0x00FF8080	8.2575mS	12.821µS
6	CMD1	0x40000080	11.134mS	R3	63	0xC0FF8080	11.147mS	12.821µS
7	CMD2	0x00000000	14.168mS	R2	63	0x088080181999...	14.181mS	12.820µS
8	CMD3	0x00010000	14.888mS	R1	3	0x00000500	14.904mS	15.385µS
9	CMD9	0x00010000	15.486mS	R2	63	0x000006807197...	15.501mS	15.385µS
10	CMD10	0x00010000	16.206mS	R2	63	0x088080181999...	16.222mS	15.385µS
11	CMD7	0x00010000	17.096mS	R1	7	0x00000700	17.111mS	15.385µS
12	CMD6	0x03B90000	21.092mS	R1b	6	0x00000800	21.112mS	20.513µS
13	CMD6	0x03B70000	22.827mS	R1b	6	0x00000800	22.827mS	320.08nS
14	CMD16	0x00000200	24.188mS	R1	16	0x00000900	24.188mS	280.09nS
15	CMD23	0x00000004	27.653mS	R1	23	0x00000900	27.653mS	280.01nS
16	CMD25	0x00000001	28.210mS	R1	25	0x00000900	28.210mS	320.17nS
17	CMD16	0x00000200	37.313mS	R1	16	0x00000900	37.313mS	280.09nS
18	CMD23	0x00000004	40.785mS	R1	23	0x00000900	40.785mS	279.96nS
19	CMD18	0x00000001	41.347mS	R1	18	0x00000900	41.348mS	360.44nS
20	CMD6	0x03B90000	60.593mS	R1b	6	0x00000800	60.593mS	320.28nS

Cmd Index	CMD3	Type	ac
Abbreviation	SET_RELATIVE_ADDR	Response Expected	R1
Cmd Index (45:40)	000011	CRC (7:1)	0111111
Argument (39:8)	0x00010000	Bin/Hex	End bit 0 1
R1 Response	000011	1111101	1
Command Index	45:40	CRC7	7:1
	0x00000500	Bin/Hex	End bit 0
Card Status	39:8		

Bits	Identifier	Type	Detection Mode	Error
8	Ready_For_Data	S	R	1
10	Current State(Ident)	S	R	0010

- ▶ List the command and respective response from card in same row
- ▶ Selected row's details of command and response are displayed at bottom the Protocol View table
- ▶ Time stamp at end of command frame and start of response
- ▶ Delta T column list the time lapsed between command and response

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Export



- ▶ Export of Electrical measurements and Protocol Decode data to CSV and TXT file format
- ▶ Browser allows to place the data in desired location

PGY-MMC-SD Electrical Validation and Protocol Decode Software- Report

Prodigy Technovations - PGY-I2C Electrical Validation and Protocol Decode Software

Content

☒ Configuration
☒ Electrical Parameters
☒ Saved Images
☒ Protocol Listing

Select Range

☐ Message Range ☒ All

Start Index: 0 End Index: 0

Report Header

Organisation Name: Prodigy Technovations
Project Name: <PROTOCOL ANALYSER> Test Name: <TEST NAME>
Description: DESCRIPTION
Remarks: REMARKS
Prepared by: <DESIGNER Name>
Report Location: C:\Prodigy_Technovations\PGY-I2C\AppData\Reports
☒ Use My Company Logo : Prodigy Technovations

Buttons: Select, Configure, Limit Setup, Review, Generate Report, Run, Single, No Acq, Run, Run Options, Analyze, Export, Report

Version 1.8.0 Wfm File | Clock: Ref Level 50, Hys 5 | Data: Ref Level 50, Hys 5 | Address 7/10 bit

- ▶ Supports customizable pdf format report generation
- ▶ Report can include electrical measurements, protocol decode, oscilloscope images, detail view images, and reference level setup
- ▶ Review of saved images allows the user to add title to image, description and delete the images

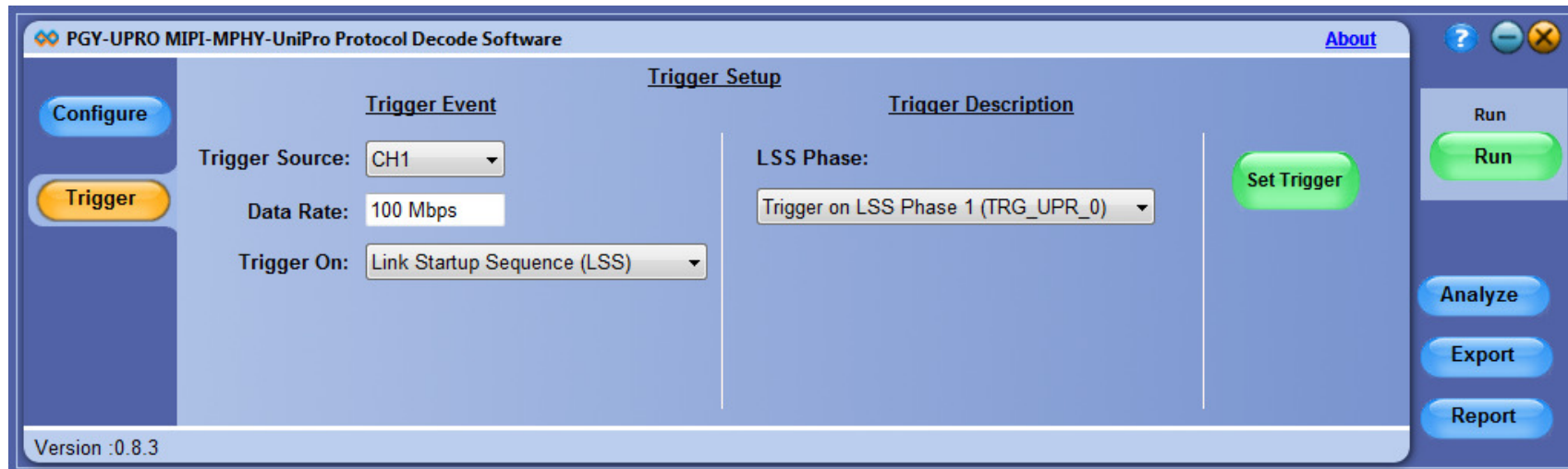
MPHY Protocol overview

OSI Layer

MIPI MPHY Protocols

Application (L7)	Application layer	UFS Protocol Layer	CSI-3/DSI-3 Layer	Application layer			
Presentation (L6)							
Session (L5)							
Transport (L4)	Transport					M-PCIe Protocol Layer	DigiRF Protocol
Network (L3)	Network (L3)						
Data Link (L2)	Data Link (L2)						
	PHY Adapter layer (L1.5)	UniPRO Protocol Layer	LLI Protocol	SSIC Protocol			
Physical layer (L1)	Physical layer (L1)						

Trigger setup for UniPro/LLI



- ▶ Applications make use of serial trigger available in scope to trigger UniPRO/LLI Protocol content
- ▶ Requires Option ST6G option in the oscilloscope
- ▶ Trigger source could be any oscilloscope live channels
- ▶ Supports triggering using Link startup sequence, PA layer packet content and datalink layer packet content

UniPro Trigger Features

Trigger Event	Trigger Content
Link Startup Sequence (LSS)	Trigger on LSS Phase 1 (TRG_UPR_0)
	Trigger on LSS Phase 2 (TRG_UPR_1)
	Trigger on LSS Phase 3 (TRG_UPR_2)
Phy Adapter layer Content	PACP_PWR_req
	PACP_PWR_cnf
	PACP_cap_ind
	PACP_EPR_ind
	PACP_TEST_MODE_req
	PACP_GET_req
	PACP_GET_cnf
	PACP_SET_req
	PACP_SET_cnf
Data Link layer Content	PACP_Test_Data
	Data_SOF
	Data_COF
	AFC (Acknowledgement)
	NAC (No Acknowledgement)

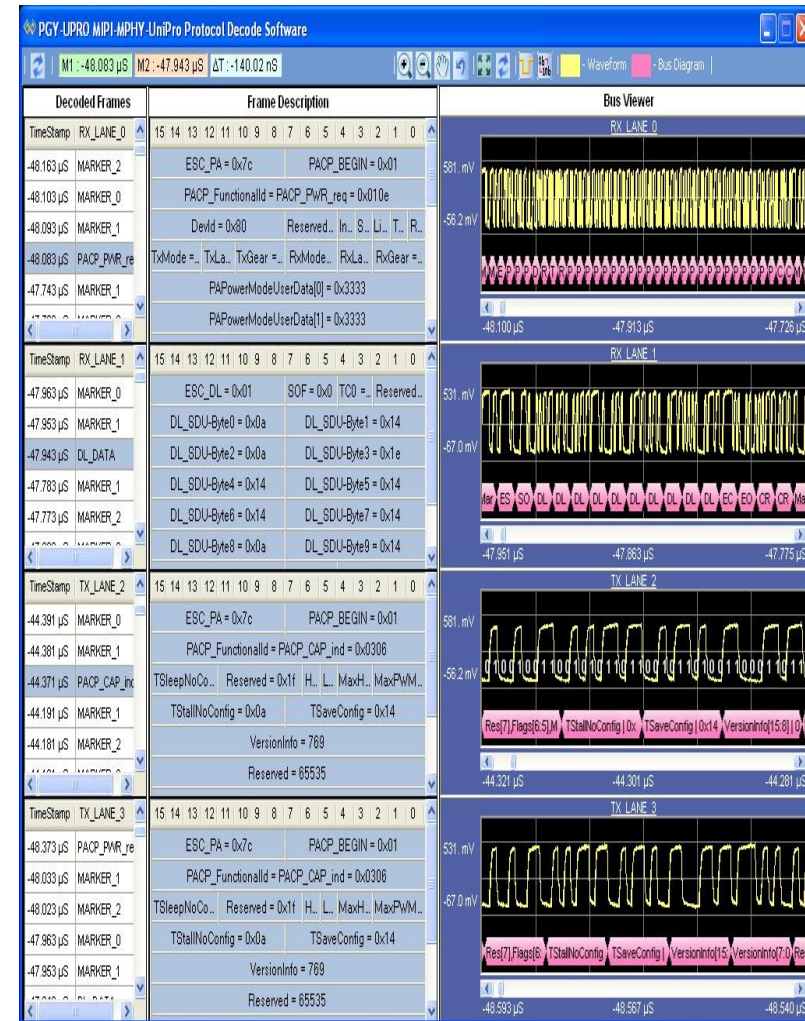
Seamless Integration of PGY-UniPro and Oscilloscope view

- ▶ Decoded data is displayed in bottom half of the scope display and scope waveform display on top
- ▶ Packet level info with flexibility to collapse the packet to view packet content
- ▶ Link the UniPro packet to oscilloscope waveform with cursors placement at start and end of the packet waveform



PGY-UniPro/LLI UniPro and LLI Protocol Decode S/W

- ▶ UniPro and LLI Protocol Decoder enables faster system level protocol debugging
- ▶ Conforms to UniPro Protocol Specification version 1.4 and LLI Protocol version 0.8
- ▶ Detail view provides a comprehensive protocol and physical layer data correlation
- ▶ Automated CRC computation to monitor CRC errors in protocol packet
- ▶ Trigger configuration leverages the Oscilloscope option ST6G serial trigger features and helps to trigger the UniPro and LLI specific events
- ▶ Generates comprehensive and customizable reports
- ▶ Ability to export the protocol and measurement details to txt and csv file formats





UFS Protocol Overview

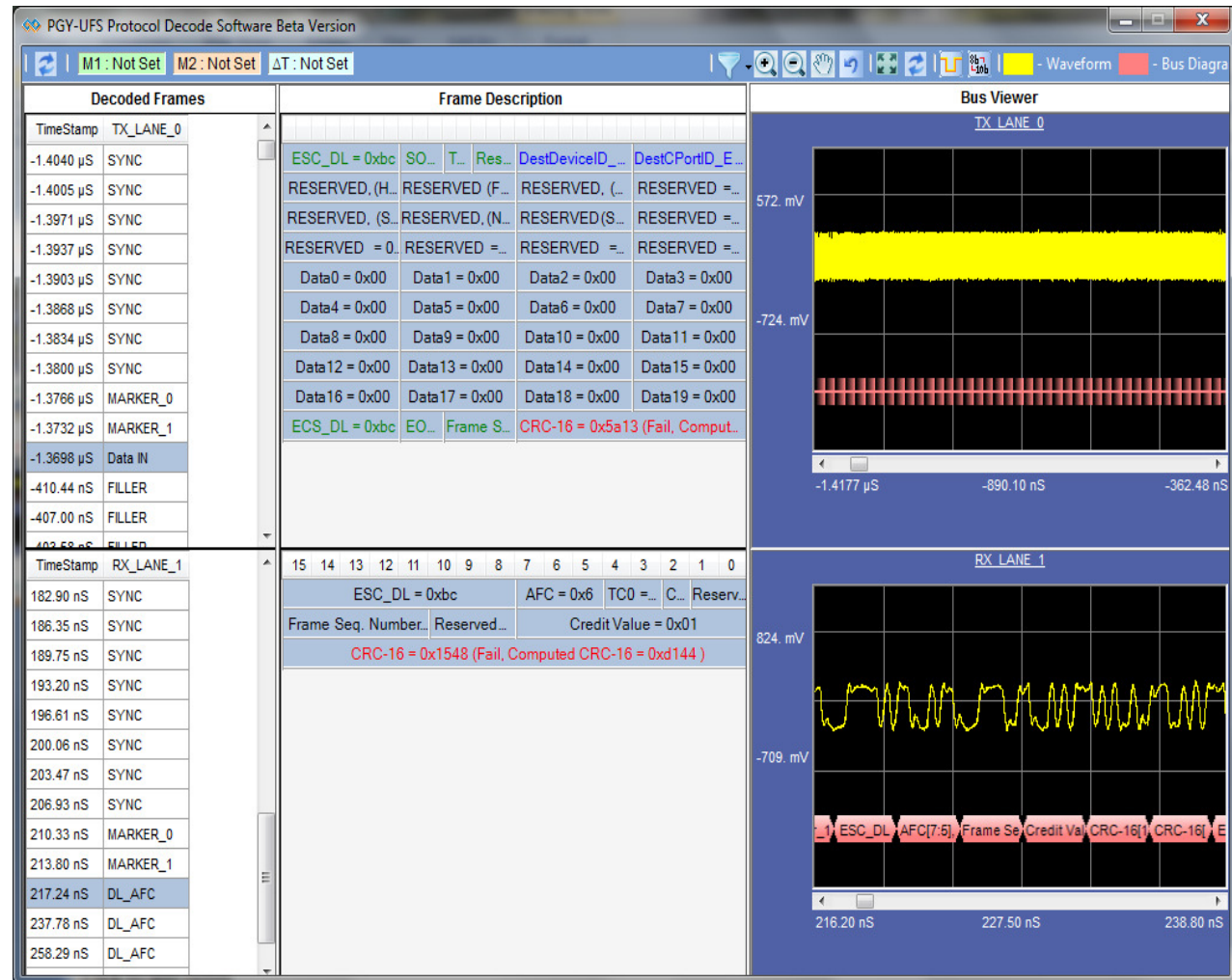
- ▶ UFS Protocol Information Units (UPIU) that travel between devices on the UniPRO bus
- ▶ All UFS UPIU's consist of a single basic header segment, possibly one or more extended header segments and zero or more data segments.
- ▶ A basic header segment has a fixed length of 12 bytes. The minimum UPIU size is 32 bytes which includes a basic header segment and transaction specific fields.

Details of UPIU

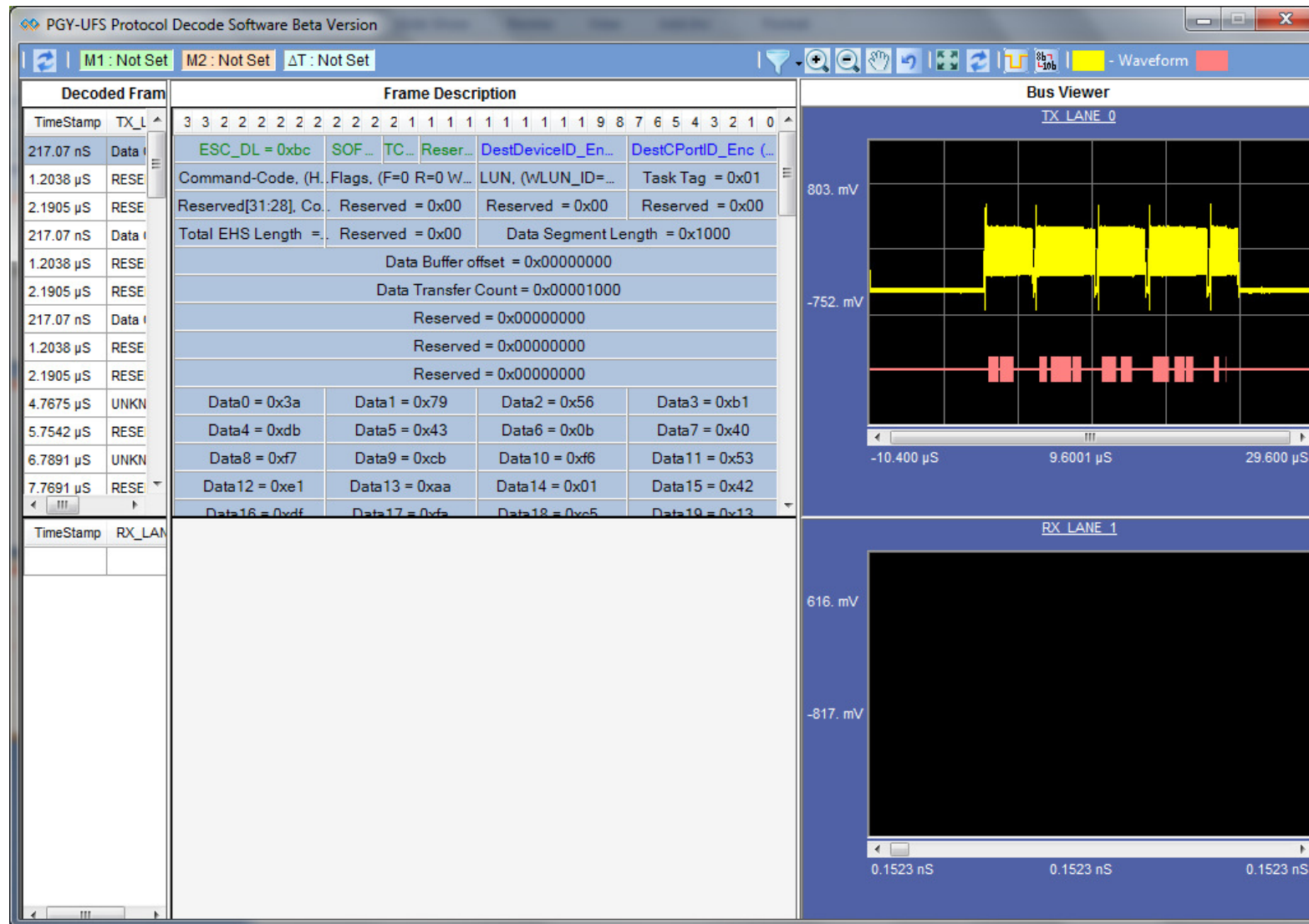
UPIU Data Structure	Description
NOP Out	The NOP Out transaction acts as a ping from an initiator to a target. It can be used to check for a connection path to a device and LUN.
NOP In	The NOP In transaction is a target response to an initiator when responding to a NOP In request.
Command	The Command transaction originates in the Initiator (host) and is sent to a logical unit within a Target device. A Command UPIU will contain a Command Descriptor Block as the command and the command parameters. When using the phase collapse feature the UPIU will also contain a data segment that would have been sent during the DATA OUT phase. This represents the COMMAND phase of the command.
Response	The Response transaction originates in the Target and is sent back to the Initiator (host). A Response UPIU will contain a command specific operation status and other response information. When using the phase collapse feature, the UPIU will also contain a data segment that would have been sent during the DATA IN phase. This represents the STATUS phase of the command.
Data Out	The Data Out transaction originates in the Initiator (host) and is used to send data from the Initiator to the Target (device). This represents the DATA OUT phase of a command.
Data In	The Data In transaction originates in the Target (device) and is used to send data from the Target to the Initiator (host). This represents the DATA IN phase of a command.
Task Management Request	This transaction type carries SCSI Architecture Model (SAM) task management function requests originating at the Initiator and terminating at the Target. The standard functions are defined by the SAM-5 specification. Addition functions might be defined by UFS.
Task Management Response	This transaction type carries SCSI Architecture Model (SAM) task management function responses originating in the Target and terminating at the Initiator.
Ready To Transfer	The Target device will send a Ready To Transfer transaction when it is ready to receive the next Data Out UPIU and has sufficient buffer space to receive the data. The Target can send multiple Ready To Transfer UPIU if it has buffer space to receive multiple Data Out UPIU packets. The maximum data buffer size is negotiated between the Initiator and Target during enumeration and configuration. The Ready To Transfer UPIU contains a DMA context and can be used to setup and trigger a DMA action within a host controller.
Query Request	This transaction originates in the Initiator and is used to request descriptor data from the Target. This transaction is defined outside of the Command and Task Management functions and is defined exclusively by UFS.
Query Response	This transaction originates in the Target and provides requested descriptor information to the Initiator in response of the Query Request transaction. This transaction is defined outside of the Command and Task Management functions and is defined exclusively by UFS.

Simultaneous view of UniPro and UFS Protocol

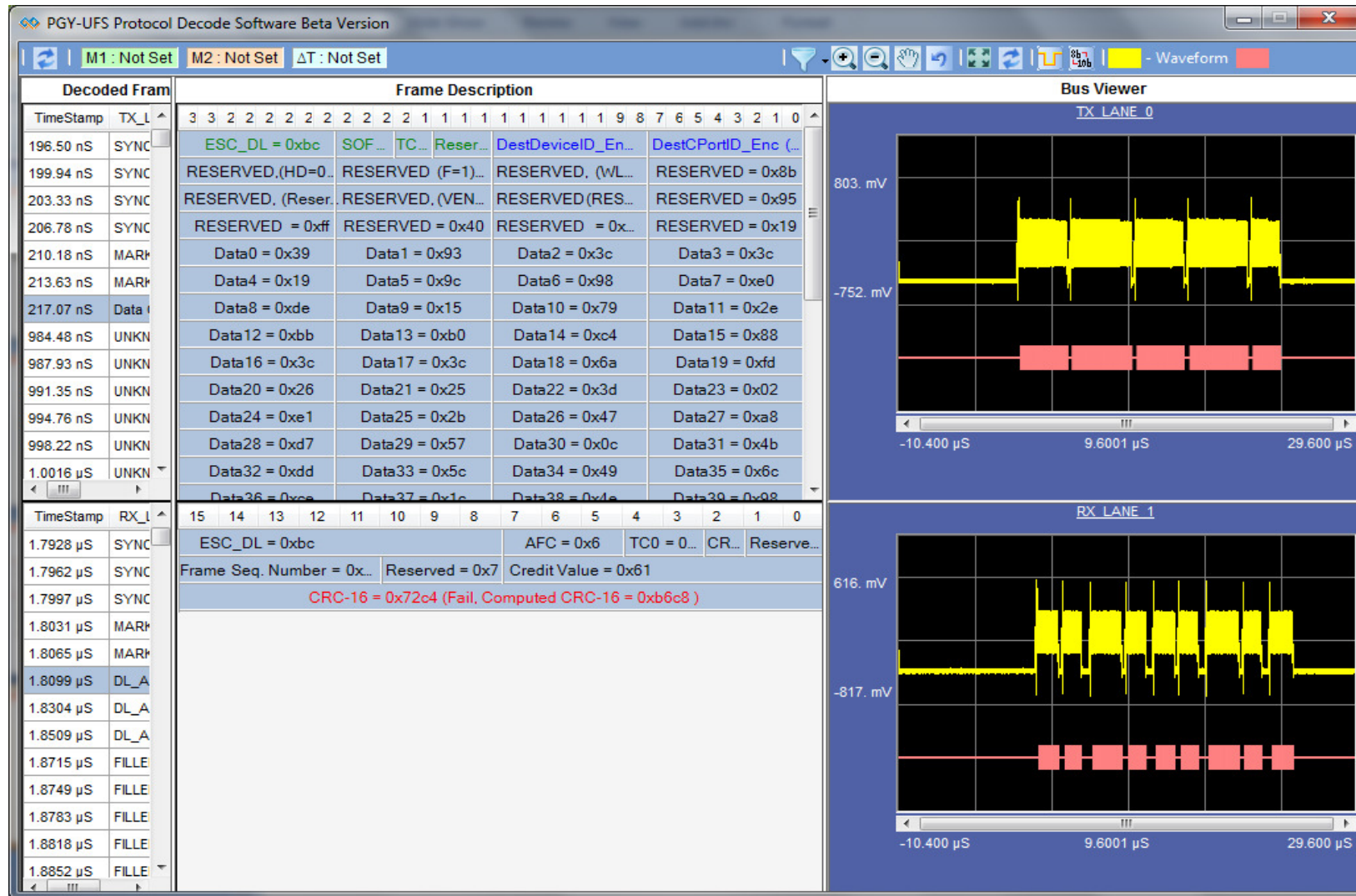
- ▶ Application supports simultaneous view of UniPRO and UFS Protocol
- ▶ In this screenshot you can UFS-Data-in packet info as well ACK packet using UniPRO-UFS View



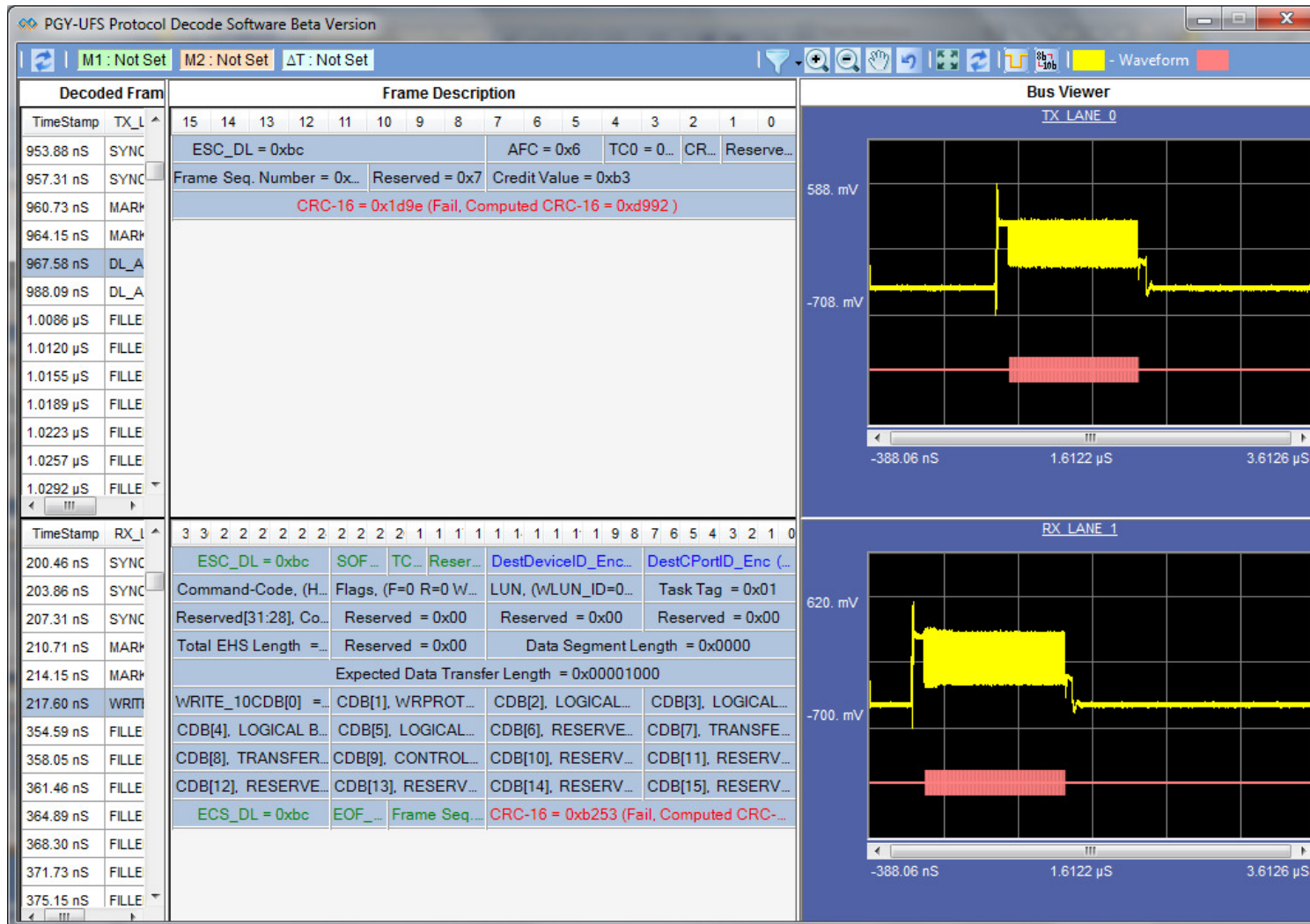
UFS Protocol view of data-out



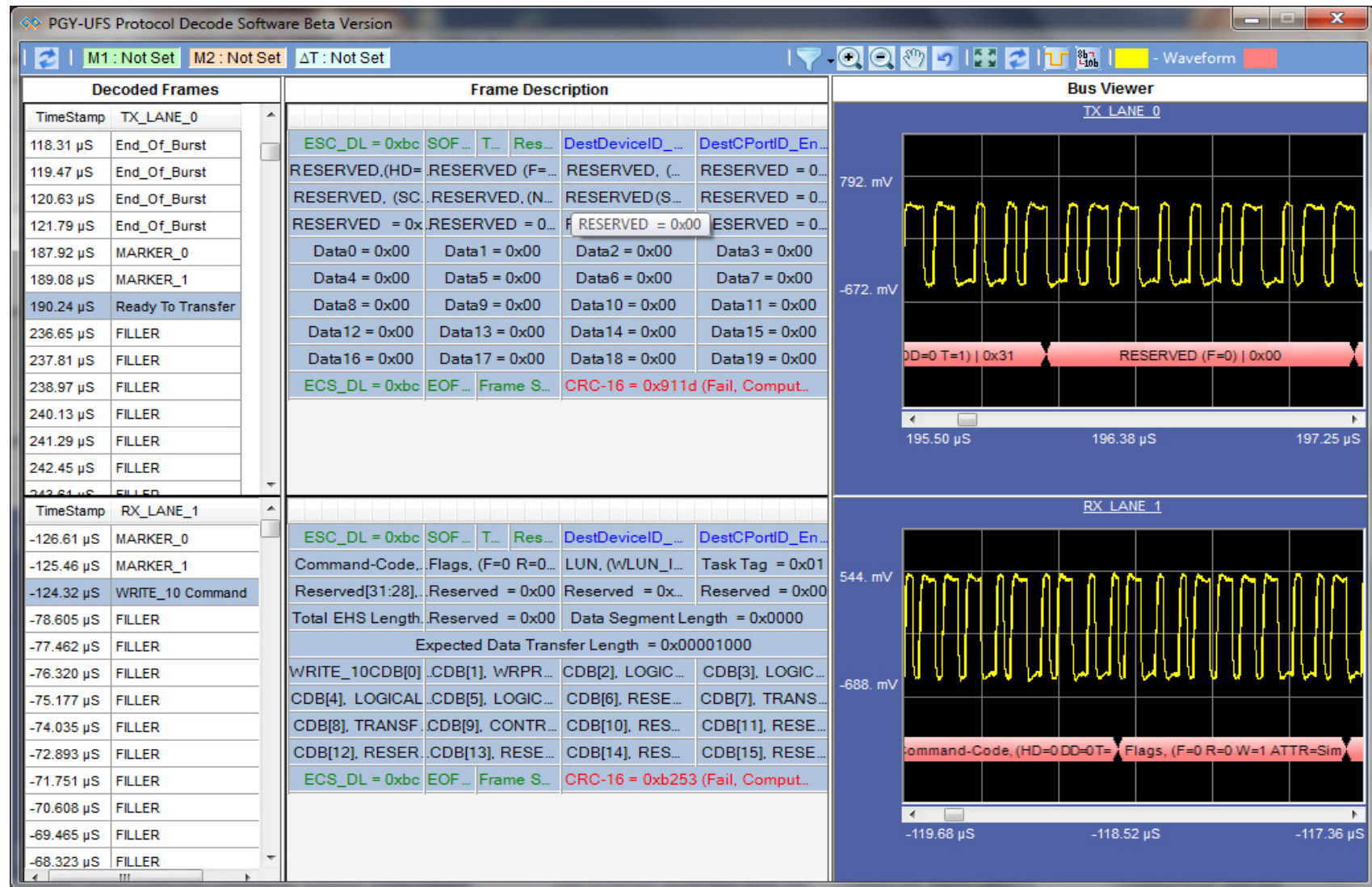
UniPRO-UFS Protocol View



UniPRO-UFS Protocol –Write Command



UniPRO-UFS Protocol Decode-Write command (PWM Signal)





Thank You