

Mobile Storage Solution: eMMC Electrical Validation and Protocol Analysis S/W and UFS Protocol Decode S/W

## Agenda

- eMMC technology overview
- Electrical measurements V4.41, V4.51
- eMMC Protocol overview
- PGY-MMC Electrical Validation and Protocol Analysis Software
- UFS Technology Overview
- UFS Protocol Analysis
- PGY-UPRO/UFS Protocol Decode Softwrae
- Demo
- ► Q&A



## eMMC Technology Overview

- Multimedia card transfers data via configurable data bus signals
- Communication Signals
  - CLK: Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.
  - CMD: This signal is a bidirectional command channel used for card initialization and transfer of commands.
  - DATO-DAT7: These are bidirectional data channels (1 bit/4 bit/8bit)





## eMMC SDR Timing Data

	- ·			U	
Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK <sup>(1)</sup>				A	2
Clock frequency Data Transfer Mode (PP) <sup>(2)</sup>	fpp	0	52 <sup>(3)</sup>	MHz	CL≤30 pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	fod	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	$CL \leq 30 \text{ pF}$
Clock low time	tWL	6.5		ns	$CL \le 30 \text{ pF}$
Clock rise time <sup>(4)</sup>	tTLH		3	ns	$CL \le 30 \text{ pF}$
Clock fall time	tTHL		3	ns	$CL \le 30 \text{ pF}$
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	$CL \leq 30 \text{ pF}$
Input hold time	tIH	3		ns	$CL \le 30 \text{ pF}$
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	$CL \leq 30 \text{ pF}$
Output hold time	tOH	2.5		ns	$CL \le 30 \text{ pF}$
Signal rise time <sup>(5)</sup>	tRISE		3	ns	$CL \le 30 \text{ pF}$
Signal fall time	tFALL		3	ns	$CL \le 30 \text{ pF}$
NOTE 1. CLK timing is measured at 50% of NOTE 2. A coMMC shall support the full for		from 0.2	() the or 0	52)/[U-	

NOTE 2. A e•MMC shall support the full frequency range from 0-26Mhz, or 0-52MHz

NOTE 3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.

NOTE 4. CLK rise and fall times are measured by min (VIH) and max (VIL).

NOTE 5. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD,

DAT rise and fall times are measured by min (VOH) and max (VOL).





## eMMC DDR timing Data

	~ ·			U	
Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK <sup>(1)</sup>	98.		× *	6	
Clock frequency Data Transfer Mode (PP) <sup>(2)</sup>	fpp	0	52 <sup>(3)</sup>	MHz	CL≤30 pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	fod	0	400	kHz	Tolerance: +20KHz
Clock high time	twn	6.5		ns	$CL \leq 30 \text{ pF}$
Clock low time	tWL	6.5		ns	$CL \le 30 \text{ pF}$
Clock rise time <sup>(4)</sup>	tTLH		3	ns	$CL \le 30 \text{ pF}$
Clock fall time	tTHL		3	ns	$CL \le 30 \text{ pF}$
Inputs CMD, DAT (referenced to CLK)	38				
Input set-up time	tISU	3		ns	$CL \le 30 \text{ pF}$
Input hold time	tIH	3		ns	$CL \le 30 \text{ pF}$
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	$CL \le 30 \text{ pF}$
Output hold time	tOH	2.5		ns	$CL \le 30 \text{ pF}$
Signal rise time <sup>(5)</sup>	tRISE		3	ns	$CL \le 30 \text{ pF}$
Signal fall time	tFALL		3	ns	$CL \le 30 \text{ pF}$

NOTE 1. CLK timing is measured at 50% of VDD.

NOTE 2. A e•MMC shall support the full frequency range from 0-26Mhz, or 0-52MHz

NOTE 3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.

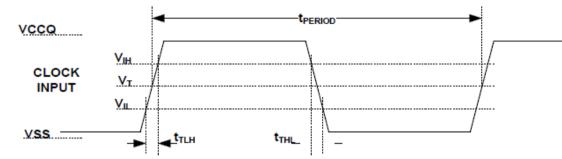
NOTE 4. CLK rise and fall times are measured by min (VIH) and max (VIL).

NOTE 5. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD,

DAT rise and fall times are measured by min (VOH) and max (VOL).



## eMMC v4.51 clock Timing Measurements



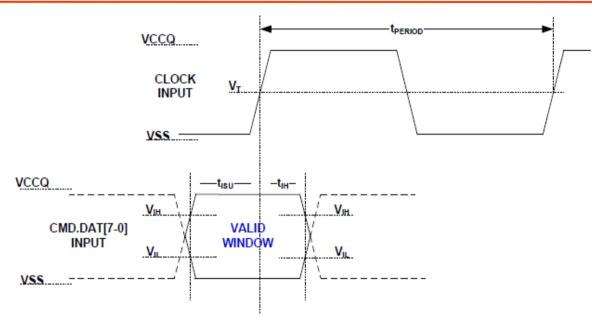
NOTE 1  $~V_{I\!H}$  denote  $V_{I\!H}(min.)$  and  $V_{I\!L}$  denotes  $V_{I\!L}(max.).$ 

NOTE 2  $V_T$ =0.975V - Clock Threshold ( $V_{CCQ}$  = 1.8V) and  $V_T$ =0.65V - Clock Threshold ( $V_{CCQ}$  = 1.2V) , indicates clock reference point for timing measurements.

Symbol	Min.	Max.	Unit	Remark
t <sub>PERIOD</sub>	5	-	ns	200MHz (Max.), between rising edges
t <sub>TLH</sub> , t <sub>THL</sub>	-	0.2 · t <sub>PERIOD</sub>	ns	tTLH, tTHL < 1ns (max.) at 200MHz, C <sub>BGA</sub> =12pF, The absolute maximum value of tTLH, tTHL is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	



## eMMC4.51 timing Measurements

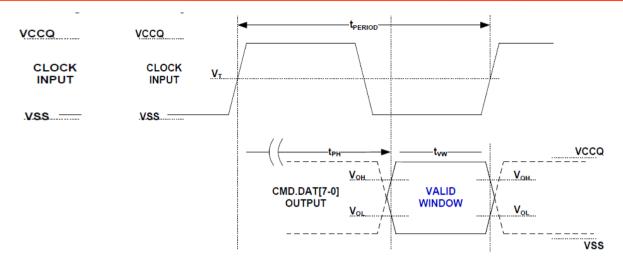


Note1:  $t_{ISU}$  and  $t_{IH}$  are measured at  $V_{IL}(max.)$  and  $V_{IH}(min.)$ . Note2:  $V_{IH}$  denote  $V_{IH}(min.)$  and  $V_{IL}$  denotes  $V_{IL}(max.)$ .

Symbol	Min.	Max.	Unit	Remark
t <sub>ISU</sub>	1.40	-	ns	$5pF \le C_{BGA} \le 12pF$
t <sub>IH</sub>	0.8		ns	$5pF \leq C_{BGA} \leq 12pF$



## eMMC 4.51 timing measurements



NOTE	V <sub>OH</sub> denote	NOTE	$V_{OH}$ denotes $V_{OH}$ (min.) and $V_{OL}$ denotes $V_{OL}$ (max.).

Symbol	Min.	Max.	Unit	Remark
t <sub>PH</sub>	0	2	UI	Device output momentary phase from CLK input to
				CMD or DAT lines output.
				Does not include a long term temperature drift.
$\Delta_{\text{TPH}}$	-350	+1550	ps	Delay variation due to temperature change after tuning.
	(ΔT= -20	(ΔT= 90		Total allowable shift of output valid window $(T_{VW})$
	deg.C)	deg.C)		from last system Tuning procedure
	_			$\Delta_{\text{TPH}}$ is 2600ps for $\Delta T$ from -25 deg.C to 125 deg.C
				during operation.
t <sub>vw</sub>	0.575	-	UI	t <sub>VW</sub> =2.88ns at 200MHz
				Using test circuit in Figure 72 including skew among
				CMD and DAT lines created by the Device.
				Host path may add Signal Integrity induced noise,
				skews, etc. Expected $T_{VW}$ at Host input is larger than
				0.475UI.





#### PGY-eMMC/Sd Electrical Validation and Protocol Decode Software-Select

🔯 PGY-MMC-SD	) Electrical Validation	and Protocol Decode	Software	<u>Save</u> <u>Recall</u> <u>Rec</u>	all Default About	
	Card Type	Mode		Measurements		Run Single
Select			Clock Frequency	Clock Cycle Time	🔽 Input Setup Time	No Acq
Configure	ммс	HS-DDR	Clock High Time	Vutput Hold Time	✓ Input Hold Time	Run / Stop
	SD Card	HS-SDR	Clock Low Time	🔽 Output Data Rising Time	🔽 Input Data Rising Time	Run Options
Limit Setup		DS-BC	🔽 Clock Rise Time	🔽 Output Data Falling Time	🔽 Input Data Falling Time	Analyse
			Clock Fall Time	🔽 Output Delay Time		Export
		HS-200	Clock Duty Cycle		Clear All Select All	
Version :2.5			Oscilloscope: clock ch1, DA	TA ch2,CMD ch3  bits/data 8   bit ord	er msb i Mark	Report
Volum 12.0			Cochioscope. Clock Ciri, DA	in charten of a bit and the of the of the		

- User can select eMMC type and select data mode
- eMMC Electrical measurements as specified in I2C Standard document are listed
- User has flexibility select few measurements or all measurements
- Supports electrical measurement for eMMC4.41 and 4.51



#### PGY-MMC-SD Electrical Validation and Protocol Decode Software-Configure

<b>PGY-MMC-SD Elect</b>	rical Validation and Protocol Decode S	oftware	<u>Save</u> <u>Recall</u> <u>Recall Default</u> <u>About</u>	
Configure Limit Setup	Signal Source Oscilloscope Wfm Files Signal Assignment Nock: H:VMMC_SD_SDIO\eMM ••• ATA: H:VMMC_SD_SDIO\eMM •••	Clock Reference Unit: Percentage Ref Level: 50 % Hystersis: 10 % Data Rate Data Rate DDR SDR	Data Reference         Unit:       Percentage         Ref Level:       50         50       %         Hystersis:       10         Oscilloscope Setup       Skip the data	Run Single No Acq Run / Stop Run Options Analyse Export Report
Version :2.1.0		Oscilloscope: clock ch1, DATA ch2,	CMD ch3  bits/data 8   bit order msb   Mark	

- Select the source of the signal from oscilloscope or saved files
- Use Clock and Data Reference by value. If signal is noisy set the hystersis at least 15% to avoid any intermittent transition as logic state



#### PGY-eMMC-SD Electrical Validation and Protocol Decode Software- Limit Setup

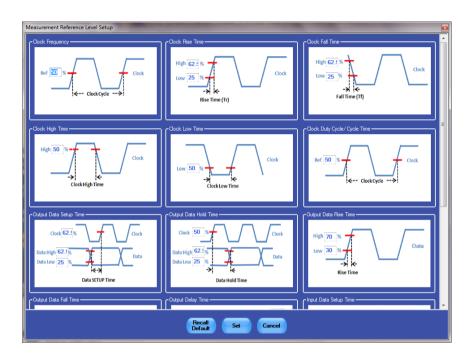
🔯 PGY-MMC-SI	D Electrical Validatio	n and	Protoco	ol Deco	ode	Software				Save Recall Recall De	efault		About	?
						Measurement L	imits.							Run
Select		Low	High			Lov	v High	1			Low	High		Single
	Clock Frequency:	0	52	MHz	•	Clock Cycle Time: 1	5	nS	•	Input Setup Time:	3	NA	nS 🔻	No Acq
Configure	Clock Rise Time:	NA	3	nS	•	Output Hold Time: 2.5	NA	nS	•	Input Hold Time:	3	NA	nS 🔻	Run / Stop
	Clock Fall Time:	NA	3	nS	•	Output Data Rise Time: NA	3	nS	•	Input Data Rise Time:	NA	3	nS 👻	Run Options
Limit Setup	Clock High Time:	6.5	NA	nS	•	Output Data Fall Time: NA	3	nS	•	Input Data Fall Time:	NA	3	nS 👻	Analyse
	Clock Low Time:	6.5	NA	nS	•	Output Delay Time: 8	20	nS	•	Reference	Recal		Update	Export
	Clock Duty Cycle:	NA	NA	%	•					Setup	Defau		Limits	Export
														Report
Version :2.1.0						Oscilloscope: clock ch1, D	ATA chi	2,CMD	ch3	bits/data 8   bit order m	sb   Ma	ark		

- Limits can be set to default limits as specified in standard document
- User defined Low and High Limits as per in-house specification
- Save and Recall the limits



PGY-MMC-SD Electrical Validation and Protocol Decode Software- <u>Reference</u> <u>Level Setup</u>

- Graphical User Interface eases of reference level setup and avoid human errors
- User can view the default reference levels set for each of the electrical measurement
- Edit reference level setup for each of the measurements
- Save and recall of reference level setup





#### PGY-MMC-SD Electrical Validation and Protocol Decode Software- <u>Run-</u> <u>Control</u>

	💸 Continious Run Options
Run	When to stop the application
Single No Acq	<ul> <li>Run continiously until the Stop button is pressed</li> <li>Stop When</li> <li>One or more measurements fails</li> </ul>
Run Run Options	✓ Stop after     5     Runs       ✓ Do not show message boxes during continious run       OK     Cancel

- Run Control captures the data and analyses it as per configure, limit values and reference level setup
- Analysis of signal using Single or Continuous acquisition
- Analysis of signals present in acquisition memory using No Acq mode
- Flexibility to stop the test if one or more measurement fails/ after running user defined number of tests



#### PGY-MMC-SD Electrical Validation and Protocol Decode Software-Analyze

	Measurement	Minimum	Mean	Maximum	Low Limit	High Limit	Result ^		Run
Select	🕑 Clock Frequency	389.84	1.0558	25.456	0.0000Hz	52.000 MHz	Pass	Detail View	Single
	🕜 Clock Rise Time	1.3305 nS	1.8930 nS	3.5875 nS	NA	3.0000 nS	Pass*		No Ac
onfiguro	🕗 Clock Fall Time	1.3063 nS	1.9395 nS	3.9166 nS	NA	3.0000 nS	Pass* ≡		Dun / S
onfigure	🕜 Clock High Time	19.742 nS	473.92 nS	1.2842 µS	6.5000 nS	NA	Pass	Protocol View	Run / St
	🕜 Clock Low Time	18.460 nS	473.25 nS	1.2838 µS	6.5000 nS	NA	Pass		Kun Opti
mit Setup	Clock Duty C	49.533 %	50.523 %	53.489 %	NA	NA	NA		Analyse
	🔀 Clock Cycle	39.285 nS	947.16 nS	2.5652 µS	1.0000 nS	5.0000 nS	Fail	-Acq Count-	
	🕗 Output Hold	19.239 nS	493.09 nS	1.2836 µS	2.5000 nS	NA	Pass	1	Export
	🕗 Output Data	1.4091 nS	1.9213 nS	3.3658 nS	NA	3.0000 nS	Pass*		Report

- Displays measurement limits and annotation to indicate pass or fail
- Provides min, max and mean measurement values
- Detail View provides debugging environment
- Protocol view provides details of protocol transaction





- Provides powerful debug environment co-relating physical layer waveform, protocol decode data and electrical measurements
- Selected protocol decode message waveform is plotted in selected waveform window
- Reference cursor will be placed in acquired waveform window to indicate the position of the waveform in Acquired data
- Failed Electrical measurements selected in red color
- Cursor measurements for manual analysis
- Markers to indicate reference level for measurement
- Take snapshot of selected waveform image from detail view for report
- Decode tables list the Commands and responses from card
- Utility features for zooming the waveform, pan, cursors, reference set markers and image capture for report

2.3V				Waveforr	n View				
Amplitude Amplitude									
C Sho	ow CLOCK 🔽 She	w DATA 🔽 Show C	MD	Time(Seco		orm View			
2.2V				Selecte	u wave	oun aiga			
8									
		0 0 0 0 0 0 0		0 0 0 0 0 0		0000	0 0 0 0 0 0		0 1
9 2.3V	Command I		A	u <mark>gument = 0x00</mark>	000000			¢RC7 = 0x4/	
Amplitude 2.3V -360mV									
2.1V						ng galianina ng katapata			
-120mV -1.3603		25.717 µS	52	794 uS		79.871 µS		106.95 µS	) S در 134.03 S
		DATA DOM O	- Internet						
Annotation CMD CLOCK D	w CLOCK 🗹 Sho CMD Data	CMD = 0x4000000000 Description : Start Bit =	MD 95, CMD Index •		viation = 0			Þ 🗘	Show: All Messages
- Annotation		CMD = 0x400000000	MD 95, CMD Index •	CMD0, CMD Abbre Bit = 1, Argument =	viation = 0			Minimum Clock Frequency	Show:
Annotation CMD CLOCK D	CMD Data CMD Start Bit	CMD = 0x400000000 Description : Start Bt = Transmission	MD 95, CMD Index 0, Transmissoin Command	CMD0, CMD Abbre Bit = 1, Argument = CMD	viation = C 0x000000	00, CRC7 = 0x4/ CMD Stop	A, Stop Bit = 1, CM	Minimum Clock Frequency	Show: Al Messages Mean Cloc
Annotation CMD CLOCK D	CMD Data CMD Start Bit	CMD = 0x400000000 Description : Start Bt = Transmission	MD 95, CMD Index + 0, Transmissoin Command Index	CMD0, CMD Abbre Bt = 1, Argument = CMD Argument	viation = 0 0x000000 CRC7	00, CRC7 = 0x4/ CMD Stop Bit	A, Stop Bit = 1, CM	Minimum Clock Frequency	Show: Al Messages Mean Cloc Frequency
Annotation CMD CLOCK D CommandType 30 IDLE STATE SEND_OP_COND	ATA CMD Data CMD Start Bit	CMD = 0x400000000 Description : Start Bit = Transmission Bit	SMD 95, CMD Index ( 0, Transmissoin Command Index 0	CMD0, CMD Abbre Bt = 1, Argument = CMD Argument 0x00000000	viation = 0 0x000000 CRC7 0x4A	CMD Stop Bit	A, Stop Bit = 1, CM Time -1.3583 μS	Minimum Clock Frequency 389.89 KHz	Show: All Messages Mean Cloc Frequency 390.01 KH:
Annotation CMD CLOCK D CommandType 30 IDLE STATE SEND_OP_COND 33 Response	CMD Data CMD Start Bit 0	CMD = 0x400000000 Description : Stat Bt = Transmission Bit 1	95, CMD Index 4 0, Transmissoin Command Index 0 1	CMDD, CMD Abbre Bt = 1, Argument = CMD Argument 0x00000000 0x40000080	cRC7 0x4A 0x74	CMD Stop Bit 1	A, Stop Bit = 1, CM Time -1.3583 μS 357.62 μS	Minimum Clock Frequency 389.89 KHz 389.87 KHz	Show: All Messages Mean Cloc Frequency 390.01 KH: 390.00 KH:
Annotation CMD CLOCK D CommandType 30 IDLE STATE SEND_OP_COND 33 Response SEND_OP_COND	CMD Data CMD Start Bit 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	CMD = 0x400000000 Description : Stat Bt = Transmission Bit 1 0	MD 95, CMD Index 0, Transmissoin Command Index 0 1 63	CMDD, CMD Abbre Bit = 1, Argument = CMD Argument 0x00000000 0x40000080 0x00FF8080	CRC7 0x4A 0x74 0x7F	CMD Stop Bit 1 1	A, Stop Bit = 1, CM Time -1.3583 μS 357.62 μS 493.52 μS	Minimum Clock Frequency 389.89 KHz 389.87 KHz 389.90 KHz	Show: Al Messages Frequency 390.01 KH 390.01 KH
Annotation CMD RECORD D CommandType 30 IDLE STATE SEND_OP_COND 33 Response SEND_OP_COND 33 Response	CMD Data CMD Start Bit 0 0 0 0	CMD = 0x400000000 Description : Start Bt = Transmission Bit 1 0 1	SMD 95, CMD Index 0, Transmission Command Index 0 1 63 1	CMD0, CMD Abbre Bt = 1, Argument = CMD Argument 0x0000000 0x4000080 0x00FF8080 0x4000080	viation = C 0x000000 CRC7 0x4A 0x74 0x77 0x77	CMD Stop Bit 1 1 1	A, Stop Bit = 1, CM Time -1.3583 μS 357.62 μS 493.52 μS 2.3439 mS	Minimum Clock Frequency 389.89 KHz 389.87 KHz 389.90 KHz 389.88 KHz	Show: Al Messages Bean Cloo Frequency 390.01 KH: 390.00 KH: 390.00 KH:
Arnolation CMD CLOCK 0 CommandType 30 IDLE STATE SEND OP COND 33 Response SEND OP COND 33 Response SEND OP COND	CMD Data CMD Start Bit 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	CMD = 0x400000000 Description : Start Bt = Transmission Bit 1 0 1 0	SMD 95, CMD Index 4 0, Transmission Command Index 0 1 63 1 63 1 63	CMD0, CMD Abbre Bt = 1, Argument = CMD Argument 0x40000000 0x40000080 0x00FF8080 0x4000080 0x00FF8080	viation = 0 (x000000 CRC7 0x4A 0x74 0x74 0x74 0x74 0x77	00.CRC7 = 0x44 CMD Stop Bit 1 1 1 1 1	A Stop Bt = 1.CM Time -1.3503 µS 357.62 µS 493.52 µS 2.3439 mS 2.4798 mS	Minimum Clock Frequency 389.89 KHz 389.87 KHz 389.90 KHz 389.88 KHz 389.88 KHz	Show: Al Messages Mean Cloc Frequency 390.01 KH: 390.00 KH: 390.01 KH: 390.01 KH:
Arnolation CMD EXCERNING CommandType CommandType CommandType CommandType CommandType SenD OP_COND R3 Response SEND OP_COND S3 Response SEND_OP_COND	CMD Data CMD Start Bit 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	CMD = 0x400000000 Description : Start Bt = Transmission Bit 1 0 1 0 1	MD 95, CMD Index 4 0. Transmission Command Index 0 1 63 1 63 1 1 63 1	CMD0, CMD Abbre Bt = 1, Argument = CMD Argument 0x00000000 0x40000080 0x40000080 0x40000080 0x40000080 0x40000080	viation = C CxC000000 CRC7 0x74 0x74 0x77 0x77 0x77 0x77	00, CRC7 = 0x44 CMD Stop Bit 1 1 1 1 1 1 1	A, Stop Bt = 1, CM Time -1.3583 µS 357.62 µS 493.52 µS 2.3439 mS 2.4798 mS 5.2491 mS	Minimum Clock Frequency 389.89 KHz 389.87 KHz 389.80 KHz 389.88 KHz 389.88 KHz 389.85 KHz	Show: Al Messages Mean Cloc Frequency 390.01 RH: 390.00 RH: 390.00 RH: 390.00 RH: 390.00 RH:
Amotation CMD CLOCK D CommandType 30 TDLE STATE SEND OP COND 33 Response SEND OP COND 33 Response SEND OP COND 33 Response	CMD Data CMD Start Bit 0 0 0 0 0 0 0 0 0 0 0	CMD - 0x400000000 Description : Start Bt = Transmission Bit 1 0 1 0 1 0 0	MD 95, CMD Index 4 0, Transmissoin Command Index 0 1 63 1 63 1 63 1 63	CMD0. CMD Abbre Bt = 1, Argument = CMD Argument 0x00000000 0x40000080 0x40000080 0x00FF8080 0x00FF8080 0x40000080 0x00FF8080	viation = 0 0x000000 0x74 0x74 0x77 0x74 0x77 0x74 0x77 0x74 0x77	00. CRC7 = 0x44 CMD Stop Bit 1 1 1 1 1 1 1 1 1	A Stop Bt = 1, CM Time -1.3583 µS 357.62 µS 493.52 µS 2.3439 mS 2.4798 mS 5.2491 mS 5.3850 mS	Minimum Clock Frequency 389.89 KHz 389.87 KHz 389.80 KHz 389.88 KHz 389.88 KHz 389.85 KHz 389.85 KHz	Show: Al Messages Mean Cloo Frequency 390.01 KH 390.00 KH 390.00 KH 390.00 KH 390.00 KH



#### PGY-MMC-SD Electrical Validation and Protocol Decode Software- Protocol View

	Com	mand (Host)			Res	ponse (Card)		•					
Serial No	Index	Argument	Command End Time (TC)	Response	Check Bits / Index	Status / CID / CSD / OCR Register / Arguments	Response Start Time (TR)	Delta (TR-TC	Cmd Index Abbreviation	CMD3 SET_RELATIVE_ADDR	_	Type ac Response R1 Expected	
1	CMD0	0x00000000	121.72µS	-	-	ō.	-	•	Cmd Index	000011		CRC 011	1111
2	CMD1	0x40000080	480.70µS	R3	63	0x00FF8080	493.52µS	12.821µS	(45:40)	000011	_	(7:1)	1111
3	CMD1	0x40000080	2.4669mS	R3	63	0x00FF8080	2.4798mS	12.821µS	Argument	0x00010000		Bin/Hex	End bit 1
4	CMD1	0x40000080	5.3722mS	R3	63	0x00FF8080	5.3850mS	12.821µS	(39:8)				0
5	CMD1	0x40000080	8.2446mS	R3	63	0x00FF8080	8.2575mS	12.821µS	R1 Response	000011		1111101	1
6	CMD1	0x40000080	11.134mS	R3	63	0xC0FF8080	11.147mS	12.821µS ≘	ПППоронас		5:40	CRC7 7:1	
7	CMD2	0x00000000	14.168mS	R2	63	0x088080181999	14.181mS	12.820µS		0x00000500	5.40	UNU7 7.1	End bi Bin/H
8	CMD3	0x00010000	14.888mS	R1	3	0x00000500	14.904mS	15.385µS			39:8		DITI/H
9	CMD9	0x00010000	15.486mS	R2	63	0x000006807197	15.501mS	15.385µS	-				
10	CMD10	0x00010000	16.206mS	R2	63	0x088080181999	16.222mS	15.385µS	Bits	Identifier	Туре	Detection Mode	Error
11	CMD7	0x00010000	17.096mS	R1	7	0x00000700	17.111mS	15.385µS	8	Ready_For_Data	S	R	1
12	CMD6	0x03B90000	21.092mS	R1b	6	0x00000800	21.112mS	20.513µS	10	Current State(Ident)	S	R	0010
13	CMD6	0x03B70000	22.827mS	R1b	6	0x00000800	22.827mS	320.08nS					
14	CMD16	0x00000200	24.188mS	R1	16	0x00000900	24.188mS	280.09nS					
15	CMD23	0x00000004	27.653mS	R1	23	0x00000900	27.653mS	280.01nS					
16	CMD25	0x00000001	28.210mS	R1	25	0x00000900	28.210mS	320.17nS					
17	CMD16	0x00000200	37.313mS	R1	16	0x00000900	37.313mS	280.09nS					
18	CMD23	0x00000004	40.785mS	R1	23	0x00000900	40.785mS	279.96nS					
19	CMD18	0x00000001	41.347mS	R1	18	0x00000900	41.348mS	360.44nS					
20	CMD6	0x03B90000	60.593mS	R1b	6	0x00000800	60.593mS	320.28nS +					

- List the command and respective response from card in same row
- Selected row's details of command and response are displayed at bottom the Protocol View table
- Time stamp at end of command frame and start of response
- Delta T column list the time lapsed between command and response



#### PGY-MMC-SD Electrical Validation and Protocol Decode Software-Export

🐼 PGY-MMC-SI	D Electrical Validation and Protocol Decode So	ftware	Save Recall Recall Default	About	2 🔿 😣
	Protocol	Electrical		Fund	Run Single
Select	✓ .csv (Comma Separated Values)	.csv (Comma Separated Values	;)	Export	No Acq
Configure	📝 .txt (Text File)	📝 .txt (Text File)			Run / Stop
					Run Options
Limit Setup					Analyse
	Save Directory: C:\Prodigy_Technovations\PC	GY-MMC-SD\AppDat Browse			Export
					Report
Version :2.1.0		Oscilloscope: clock ch1, DATA ch2,CMD ch3	3  bits/data 8   bit order msb   Ma	rk	

- Export of Electrical measurements and Protocol Decode data to CSV and TXT file format
- Browser allows to place the data in desired location



#### PGY-MMC-SD Electrical Validation and Protocol Decode Software-Report

ጰ Prodigy Tech	novations - PGY-I2C Electrical Validation	and Protocol Decode Software	About 🕜 🔿 😣
	Content Content	Report Header	Run
Select	Configuration	Organisation Name: Prodigy Technovations	Generate Single Single
	Electrical Parameters	Project Name: <protocol analyser=""> Test Name: <test name=""></test></protocol>	No Acq
Configure	Saved Images Review	Description: DESCRIPTION	Run
	Protocol Listing	Remarks : REMARKS	Run Options
Limit Setup	- Select Range	Prepared by: <designer name=""></designer>	Analyze
	OMessage Range 🧿 All	Report Location : C:\Prodigy_Technovations\PGY-I2C\AppData\Reports	r mai y 20
	Start IndexEnd Index00	Use My Company Logo: <u>Prodigy</u>	Export
Version 1.8.0		Wfm File   Clock: Ref Level 50, Hys 5   Data: Ref Level 50, Hys 5	

- Supports customizable pdf format report generation
- Report can include electrical measurements, protocol decode, oscilloscope images, detail view images, and reference level setup
- Review of saved images allows the user to add title to image, description and delete the images



## **MPHY Protocol overview**

### OSI Layer MIPI MPHY Protocols

Application (L7)							
Presentation (L6)		UFS Protocol	CSI- 3/DSI-3	Applicatio			
Session (L5)		Layer		n layer			
Transport (l4)	Transport						
Network (L3)	Network (L3)					M- PCle	
Data Link (L2)	Data Link (L2)					PCIe Protoc	DigiRF
	PHY Adapter layer	UniPRO	Protocol	LLI	Proto	ol	Protoco
	(L1.5)	Layer		Protocol	col	Layer	
Physical layer (L1)		Phy	ysical lay	er (L1)			



## Trigger setup for UniPro/LLI

ſ	🔅 PGY-UPRO M	IIPI-MPHY-UniPro Pro	otocol Decode Software			About	2 🔿 🛞
	Configure		Trigger Event	<u>Trigger</u>	Setup Trigger Description		Run
		Trigger Source:	CH1 -		LSS Phase:	Set Trigger	Run
	Trigger	Data Rate:	100 Mbps		Trigger on LSS Phase 1 (TRG_UPR_0) -	Jet Higger	
		Trigger On:	Link Startup Sequence (LS	SS) 👻			
							Analyze
							Export
							Report
	Version :0.8.3						

- Applications make use of serial trigger available in scope to trigger UniPRO/LLI Protocol content
- Requires Option ST6G option in the oscilloscope
- Trigger source could be any oscilloscope live channels
- Supports triggering using Link startup sequence, PA layer packet content and datalink layer packet content



Trigger Event	Trigger Content
	Trigger on LSS Phase 1 (TRG_UPR_0)
	Trigger on LSS Phase 2 (TRG_UPR_1)
Link Startup Sequence (LSS)	Trigger on LSS Phase 3 (TRG_UPR_2)
	PACP_PWR_req
	PACP_PWR_cnf
	PACP_cap_ind
	PACP_EPR_ind
	PACP_TEST_MODE_req
	PACP_GET_req
	PACP_GET_cnf
	PACP_SET_req
	PACP_SET_cnf
Phy Adapter layer Content	PACP_Test_Data
	Data_SOF
	Data_COF
	AFC (Acknowledgement)
Data Link layer Content	NAC (No Acknowledgement)



#### Seamless Integration of PGY-UniPro and Oscilloscope view

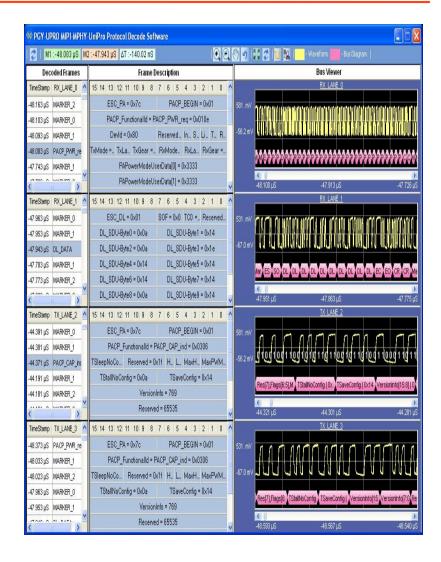
- Decoded data is displayed in bottom half of the scope display and scope waveform display on top
- Packet level info with flexibility to collapse the packet to view packet content
- Link the UniPro packet to oscilloscope waveform with cursors placement at start and end of the packet waveform





#### PGY-UniPro/LLI UniPro and LLI Protocol Decode S/W

- UniPro and LLI Protocol Decoder enables faster system level protocol debugging
- Conforms to UniPro Protocol Specification version 1.4 and LLI Protocol version 0.8
- Detail view provides a comprehensive protocol and physical layer data correlation
- Automated CRC computation to monitor CRC errors in protocol packet
- Trigger configuration leverages the Oscilloscope option ST6G serial trigger features and helps to trigger the UniPro and LLI specific events
- Generates comprehensive and customizable reports
- Ability to export the protocol and measurement details to txt and csv file formats





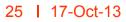
# UFS Protocol Overview

- UFS Protocol Information Units (UPIU) that travel between devices on the UniPRO bus
- All UFS UPIU's consist of a single basic header segment, possibly one or more extended header segments and zero or more data segments.
- A basic header segment has a fixed length of 12 bytes. The minimum UPIU size is 32 bytes which includes a basic header segment and transaction specific fields.





UPIU Data Structure	Description
	The NOP Out transaction acts as a ping from an initiator to a target. It can be used to check for a connection path to a device and
NOP Out	LUN.
NOP In	The NOP In transaction is a target response to an initiator when responding to a NOP In request.
	The Command transaction originates in the Initiator (host) and is sent to a logical unit within a Target device. A Command UPIU will contain a Command Descriptor Block as the command and the command parameters. When using the phase collapse feature the UPIU will also contain a data segment that would have been sent during the DATA OUT phase. This represents the COMMAND phase of the command.
Response	The Response transaction originates in the Target and is sent back to the Initiator (host). A Response UPIU will contain a command specific operation status and other response information. When using the phase collapse feature, the UPIU will also contain a data segment that would have been sent during the DATA IN phase. This represents the STATUS phase of the command.
Data Out	The Data Out transaction originates in the Initiator (host) and is used to send data from the Initiator to the Target (device). This represents the DATA OUT phase of a command.
Data In	The Data In transaction originates in the Target (device) and is used to send data from the Target to the Initiator (host). This represents the DATA IN phase of a command.
-	This transaction type carries SCSI Architecture Model (SAM) task management function requests originating at the Initiator and terminating at the Target. The standard functions are defined by the SAM-5 specification. Addition functions might be defined by UFS.
Task Management Response	This transaction type carries SCSI Architecture Model (SAM) task management function responses originating in the Target and terminating at the Initiator.
Ready To Transfer	The Target device will send a Ready To Transfer transaction when it is ready to receive the next Data Out UPIU and has sufficient buffer space to receive the data. The Target can send multiple Ready To Transfer UPIU if it has buffer space to receive multiple Data Out UPIU packets. The maximum data buffer size is negotiated between the Initiator and Target during enumeration and configuration. The Ready To Transfer UPIU contains a DMA context and can be used to setup and trigger a DMA action within a host controller.
Query Request	This transaction originates in the Initiator and is used to request descriptor data from the Target. This transaction is defined outside of the Command and Task Management functions and is defined exclusively by UFS.
Query Response	This transaction originates in the Target and provides requested descriptor information to the Initiator in response of the Query Request transaction. This transaction is defined outside of the Command and Task Management functions and is defined exclusively by UFS.





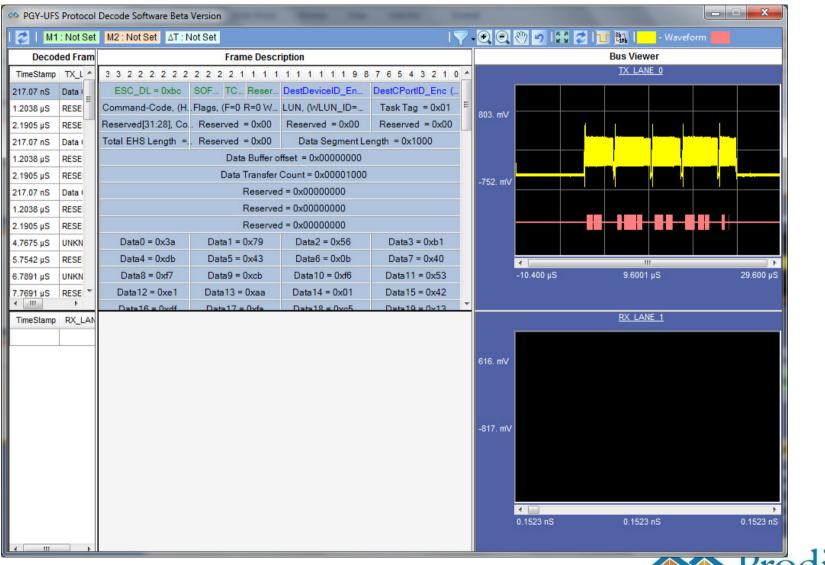
## Simultaneous view of UniPro and UFS Protocol

- Application supports simutaneous view of UniPRO and UFS Protocol
- In this screenshot you can UFS-Data-in packet info as well ACK packet using UniPRO-UFS View

🚸 PGY-UFS	Protocol Deco	ode Softwa	re B	leta Version	-	_	-			
🛃   M1	:NotSet M	2 : Not Set	Δ	T : Not Set		١Ţ	00	🖑 🤊 i 🖸 🎜 i 🖬 🐘	- Waveform	- Bus Diagra
D	ecoded Frame	es		Frame Des	cription			Bus Viev	ver	
TimeStamp	TX_LANE_0		^					<u>TX LAI</u>	<u>NE 0</u>	
-1.4040 µS	SYNC	L	_	ESC_DL = 0xbc SO T Res	DestDeviceID	DestCPortID_E				
-1.4005 µS	SYNC			RESERVED, (H RESERVED (F	RESERVED, (	RESERVED =	572. mV			
-1.3971 µS	SYNC			RESERVED, (S., RESERVED, (N.,	RESERVED(S	RESERVED =	372. IIIV			
-1.3937 µS	SYNC			RESERVED = 0 RESERVED =	RESERVED =	RESERVED =				
-1.3903 µS	SYNC			Data0 = 0x00 Data1 = 0x00	Data2 = 0x00	Data3 = 0x00				
-1.3868 µS	SYNC			Data4 = 0x00 Data5 = 0x00	Data6 = 0x00	Data7 = 0x00	-724. mV			
-1.3834 µS	SYNC			Data8 = 0x00 Data9 = 0x00	Data10 = 0x00	Data11 = 0x00	-124. 111			
-1.3800 µS	SYNC			Data12 = 0x00 Data13 = 0x00	Data14 = 0x00	Data15 = 0x00				
-1.3766 µS	MARKER_0			Data16 = 0x00 Data17 = 0x00	Data18 = 0x00	Data19 = 0x00				
-1.3732 µS	MARKER_1			ECS_DL = 0xbc EO Frame S	CRC-16 = 0x5a	13 (Fail, Comput				
-1.3698 µS	Data IN							Image: A state of the state		+
-410.44 nS	FILLER							-1.4177 µS -890.1	0 nS	-362.48 nS
-407.00 nS	FILLER									
402 50 -5	EILLED		Ŧ							
TimeStamp	RX_LANE_1		^	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0		<u>RX LAI</u>	<u>NE 1</u>	
182.90 nS	SYNC			ESC_DL = 0xbc	AFC = 0x6 TC	0 = C Reserv				
186.35 nS	SYNC			Frame Seq. Number Reserved	Credit Va	alue = 0x01	824. mV			
189.75 nS	SYNC			CRC-16 = 0x1548 (Fail,	Computed CRC-1	6 = 0xd144 )				
193.20 nS	SYNC							1 MAM AM M	M AAMAA A	MAAM
196.61 nS	SYNC							MMM	1211 1121	( VVV
200.06 nS	SYNC						-709. mV			
203.47 nS	SYNC									
206.93 nS	SYNC									اجمعه
210.33 nS	MARKER_0							1 ESC_DL AFC[7:5], Frame Se	Credit Val. CRC-16[	CRC-16[ E
213.80 nS	MARKER_1		=							
217.24 nS	DL_AFC							•		+
237.78 nS	DL_AFC							216.20 nS 227.50	) nS	238.80 nS
258.29 nS	DL_AFC									



# UFS Protocol view of data-out







## **UniPRO-UFS Protocol View**

🗱 PGY-UFS	PGY-UFS Protocol Decode Software Beta Version													
🌅   M1	: Not Set	M2:Not Set AT:N	Not Set		۱Ţ	- 🔍 🔍 🥙 💌 🔛 🔁 I 🖬 🔛	- Waveform							
Decod	led Fram		Frame Desci	ription	Bus Viewer									
TimeStamp	TX_L ^	3 3 2 2 2 2 2 2 2	2 2 2 2 1 1 1 1	1 1 1 1 1 1 9	8765432104	<u> </u>	X LANE 0							
196.50 nS	SYNC	ESC_DL = 0xbc	SOF TC Reser	DestDeviceID_En.	DestCPortID_Enc (									
199.94 nS	SYNC	RESERVED,(HD=0	RESERVED (F=1)	RESERVED, (WL.	RESERVED = 0x8b	803. mV								
203.33 nS	SYNC	RESERVED, (Reser.	RESERVED, (VEN	RESERVED (RES.	RESERVED = 0x95	505. mv								
206.78 nS	SYNC	RESERVED = 0xff	RESERVED = 0x40	RESERVED = 0x	RESERVED = 0x19		يرادا ومخذفا وتنصبا فبجه							
210.18 nS	MAR	Data0 = 0x39	Data1 = 0x93	Data2 = 0x3c	Data3 = 0x3c									
213.63 nS	MAR	Data4 = 0x19	Data5 = 0x9c	Data6 = 0x98	Data7 = 0xe0	-752. mV	المستقرية الكران الكور المراجع							
217.07 nS	Data (	Data8 = 0xde	Data9 = 0x15	Data10 = 0x79	Data11 = 0x2e									
984.48 nS	UNKN	Data12 = 0xbb	Data13 = 0xb0	Data14 = 0xc4	Data15 = 0x88		<u>کو جند جمع س</u>							
987.93 nS	UNKN	Data16 = 0x3c	Data17 = 0x3c	Data18 = 0x6a	Data19 = 0xfd									
991.35 nS	UNKN	Data20 = 0x26	Data21 = 0x25	Data22 = 0x3d	Data23 = 0x02									
994.76 nS	UNKN	Data24 = 0xe1	Data25 = 0x2b	Data26 = 0x47	Data27 = 0xa8		4							
998.22 nS	UNKN	Data28 = 0xd7	Data29 = 0x57	Data30 = 0x0c	Data31 = 0x4b	-10.400 µS	9.6001 µS 29.600 µS							
1.0016 µS	UNKN 🔻	Data32 = 0xdd	Data33 = 0x5c	Data34 = 0x49	Data35 = 0x6c									
< III	4	Data36 = Ovce	Data37 = 0x1c	Data38 = 0x/1e			X LANE 1							
TimeStamp	_		11 10 9 8	7 6 5	4 3 2 1 0									
1.7928 µS	SYNC	ESC_DL = 0xbc	- 0. D		TC0 = 0 CR Reserve									
1.7962 µS	SYNC	Frame Seq. Number =				616. mV								
1.7997 µS	SYNC		C-16 = 0x72c4 (Fail, C	computed CRC-10	- UXD0C6 )									
1.8031 µS	MAR													
1.8065 µS	MAR					و ای در سره میشد.								
1.8099 μS 1.8304 μS	DL_A DL_A					-817. mV								
1.8509 µS	DL_A													
1.8715 µS	FILLE													
1.8749 µS	FILLE						المستر بالمادي أعامتها والمت							
1.8783 µS	FILLE													
1.8818 µS	FILLE					<ul> <li>&lt;10.400 μS</li> </ul>	Ⅲ ► 9.6001 µS 29.600 µS							
	FILLE T					-10.400 µ3	23.000 µ3							
1.8852 µS ∢ III	N ILLE													



## UniPRO-UFS Protocol –Write Command

🌕 PGY-UFS	Protocol	Decode Sof	ftware Bet	ta Versie	on							-				
🛃   M1	: Not Set	M2 : Not s	Set <b>Δ</b> T	: Not Se	et									I	7	7 🗨 🔍 🥙 😰   🔀 🛃   🔟 🐘   🔜 - Waveform 🚃
Decod	led Fram				F	ram	e Descr	iption								Bus Viewer
TimeStamp	TX_L ^	15 14	13 12	2 11	10	) 9	8	7	6	5	4	3	2	1	0	<u>TX LANE 0</u>
953.88 nS	SYNC	ESC_DI	L = 0xbc					А	FC = 0	)x6	TC0	= 0	CR	Rese	rve	
957.31 nS	SYNC	Frame Seq	. Numbe	r = 0x	Re	eserv	ed = 0x	7 Cre	dit Val	lue =	0xb3					588. mV
960.73 nS	MAR		С	RC-16 -	= 0x	1d9e	e (Fail, C	ompu	ted CF	RC-16	6 = 0xo	992)				300. IIIV
964.15 nS	MAR															
967.58 nS	DL_A															
988.09 nS	DL_A															-708. mV
1.0086 µS	FILLE															
1.0120 µS	FILLE															
1.0155 µS	FILLE															
1.0189 µS	FILLE															
1.0223 µS	FILLE															
1.0257 µS	FILLE															-388.06 nS 1.6122 µS 3.6126 µS
1.0292 µS	FILLE *															
< <u> </u>	•															0 <u>RX LANE 1</u>
TimeStamp		3 3 2 2														
200.46 nS	SYNC		L = 0xbc				Reser.									
203.86 nS	SYNC	Command			-									g = 0x d = 0x		620. mV
207.31 nS	SYNC	Reserved[						Re	serve						00	
210.71 nS	MAR	Total EHS	Length							-		ength	= 0xt	0000		
214.15 nS	MAR	WRITE 10					ata Trans		-				101 1	0010	A 1	
217.60 nS	WRITI											-				-700. mV
354.59 nS	FILLE	CDB[4], L CDB[8], T							B[6], R			-				
358.05 nS	FILLE	CDB[8], 11 CDB[12], 1										-				
361.46 nS	FILLE		L = 0xbc									-				
364.89 nS	FILLE	ECS_D		EUF		rran	ne oeq		5-10 =	UXD2	200 (Fi	aii, Con	npute		<u> </u>	
368.30 nS	FILLE															
371.73 nS	FILLE															-388.06 nS 1.6122 μS 3.6126 μS
375.15 nS ∢ Ⅲ	FILLE *															



#### UniPRO-UFS Protocol Decode-Write command (PWM Signal)

PGY-UFS	Protocol Decode S	oftwa	re Beta Version	-						_ <b>_</b> x	
🤁   M1	: Not Set M2 : No	t Set	∆T : Not Set			. 🕹 ا	$\odot$	🖑 🤊 I 🔛 🍃 I 🔟	🐘   🔤 - Wavef	orm	
De	coded Frames		Fr	ame Desc	ription		Bus Viewer				
TimeStamp	TX_LANE_0	*						TX LANE 0			
118.31 µS	End_Of_Burst		ESC_DL = 0xbc SOF 7	T Res	DestDeviceID	DestCPortID_En					
119.47 µS	End_Of_Burst		RESERVED,(HD= RESER	VED (F=	RESERVED, (	RESERVED = 0	792. mV				
120.63 µS	End_Of_Burst		RESERVED, (SCRESER	VED, (N	RESERVED (S	RESERVED = 0	792.1119			00000	
121.79 µS	End_Of_Burst		RESERVED = 0x RESER	VED = 0	RESERVED = 0x0	ESERVED = 0				HIJE FETR	
187.92 µS	MARKER_0		Data0 = 0x00 Data1	= 0x00	Data2 = 0x00	Data3 = 0x00		eres: stat	الكاك كالكت	<b>             </b>	
189.08 µS	MARKER_1		Data4 = 0x00 Data5	5 = 0x00	Data6 = 0x00	Data7 = 0x00	-672. mV		א א א א א א א א א א א א א א א א א א א	ע עע עע	
190.24 µS	Ready To Transfer		Data8 = 0x00 Data9	) = 0x00	Data10 = 0x00	Data11 = 0x00	-072. 111				
236.65 µS	FILLER		Data12 = 0x00 Data13	3 = 0x00	Data14 = 0x00	Data15 = 0x00					
237.81 µS	FILLER		Data16 = 0x00 Data1	7 = 0x00	Data18 = 0x00	Data19 = 0x00		0D=0 T=1)   0x31	RESERVED (	F=0)   0x00	
238.97 µS	FILLER		ECS_DL = 0xbc EOF F	rame S	CRC-16 = 0x911d	l (Fail, Comput					
240.13 µS	FILLER							•		•	
241.29 µS	FILLER							195.50 µS	196.38 µS	197.25 µS	
242.45 µS	FILLER										
242 61	EILLED	*							RX LANE 1		
	RX_LANE_1	-							RA LANE I		
-126.61 µS	MARKER_0	-	ESC_DL = 0xbc SOF								
-125.46 µS	MARKER_1		Command-Code,Flags, (				544. mV	00000000	5 0 6 m 0 0 M	MAMONA	
	WRITE_10 Command		Reserved[31:28],Reserve								
-78.605 µS		_	Total EHS Length. Reserve			-					
-77.462 µS		_			sfer Length = 0x00						
-76.320 µS		_	WRITE_10CDB[0]CDB[1]			CDB[3], LOGIC	-688. mV				
-75.177 µS		_	CDB[4], LOGICALCDB[5],			CDB[7], TRANS					
-74.035 µS		_	CDB[8], TRANSF.CDB[9],			CDB[11], RESE					
-72.893 µS		_	CDB[12], RESERCDB[13			CDB[15], RESE		ommand-Code, (HD=01	DD=01=; Flags, (F=01	R=0 W=1 ATTR=Sim	
-71.751 µS		_	ECS_DL = 0xbc EOF F	rame S	CRC-16 = 0xb253	8 (Fail, Comput					
-70.608 µS		_						•		•	
-69.465 µS		_						-119.68 µS	-118.52 μS	-117.36 µS	
-68.323 µS	FILLER	-									





# Thank You