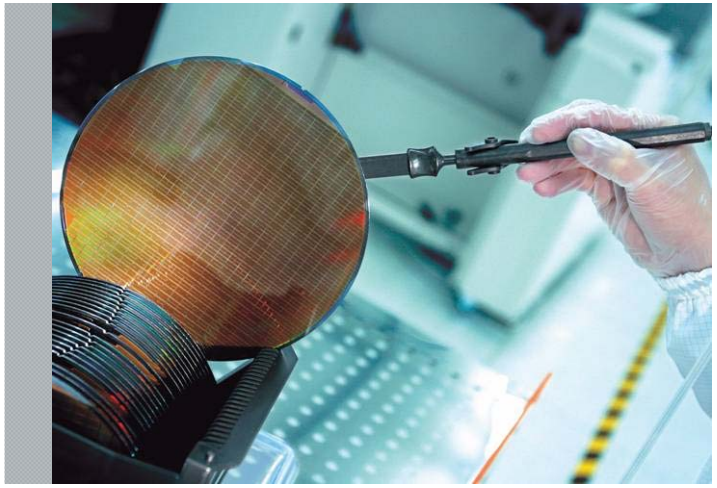
MIPI Physical Layer Test Solutions

D-PHY and M-PHY



Jong Bum, Kim
Application Engineer

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Agenda

- MIPI® Technologies
- MIPI D-PHY Test Solutions
  - D-PHY Tx
  - D-PHY Rx
- MIPI M-PHY Test Solutions
  - M-PHY Tx
  - M-PHY Rx
- Summary, Q&A

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What is MIPI and Why MIPI?

Drivers for Mobile Technologies

- **Feature set growing rapidly**
  - HD-Cameras, HD Displays, Touch screen, USB, etc
  - Mobile-TV, WiMax/ 3G, WLAN, GSM/ GPRS, GPS, FM, etc.
  - Numerous “new specialized parts” &suppliers
- **Bandwidths growing**
  - Need faster internal interconnect
- **Rising integration Time and Costs**
  - Need faster Time-To-Market
  - Need simplified system integration
  - Need “general-purpose” interfaces (like MIPI) to integrate diverse devices quickly

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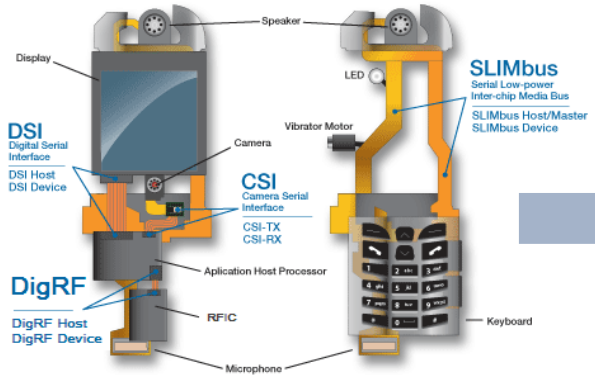
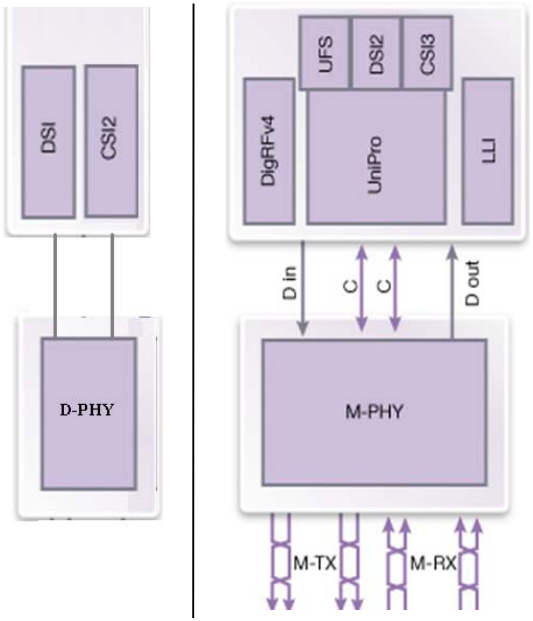
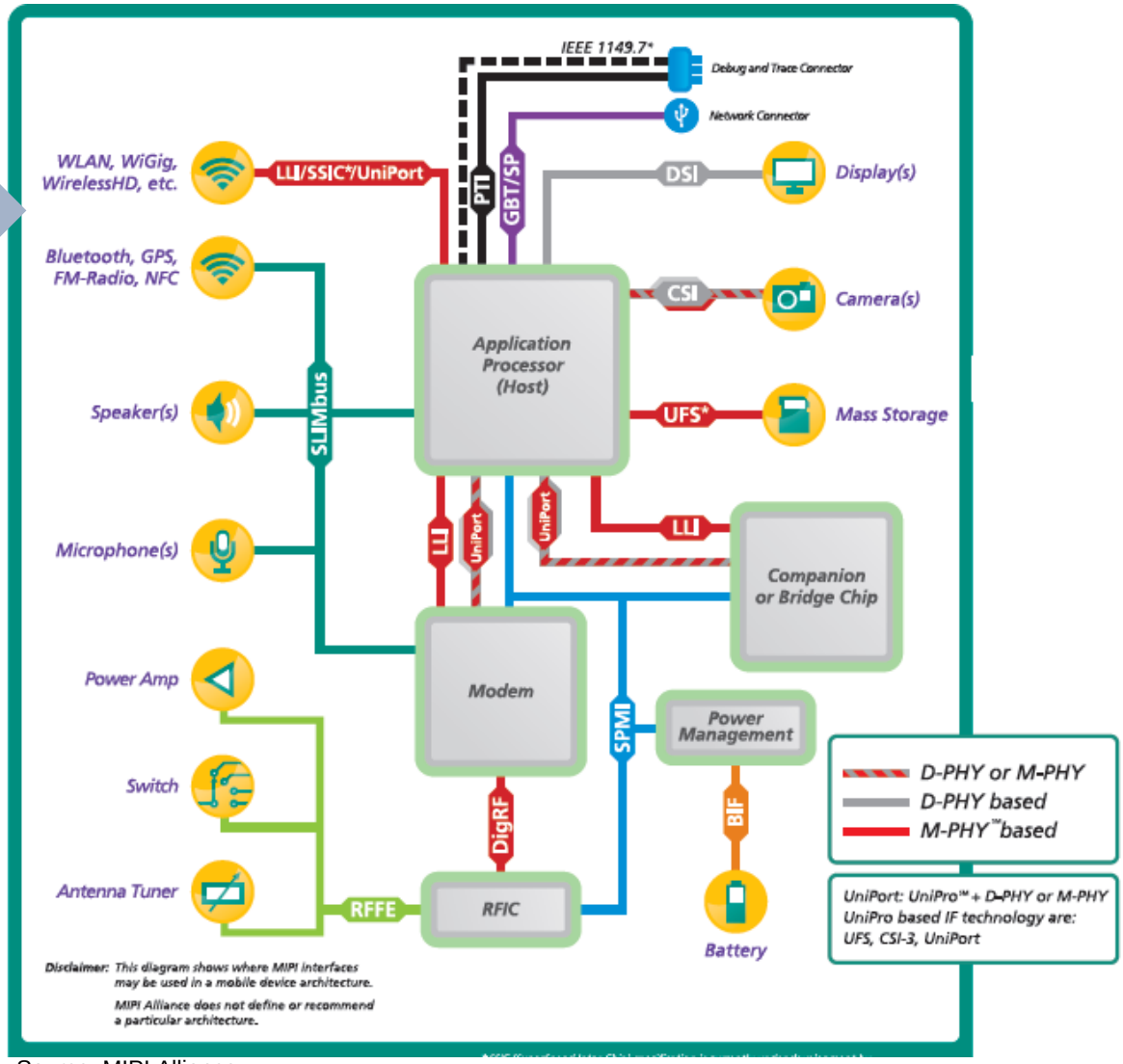
MIPI Technologies Overview







Source: MIPI Alliance

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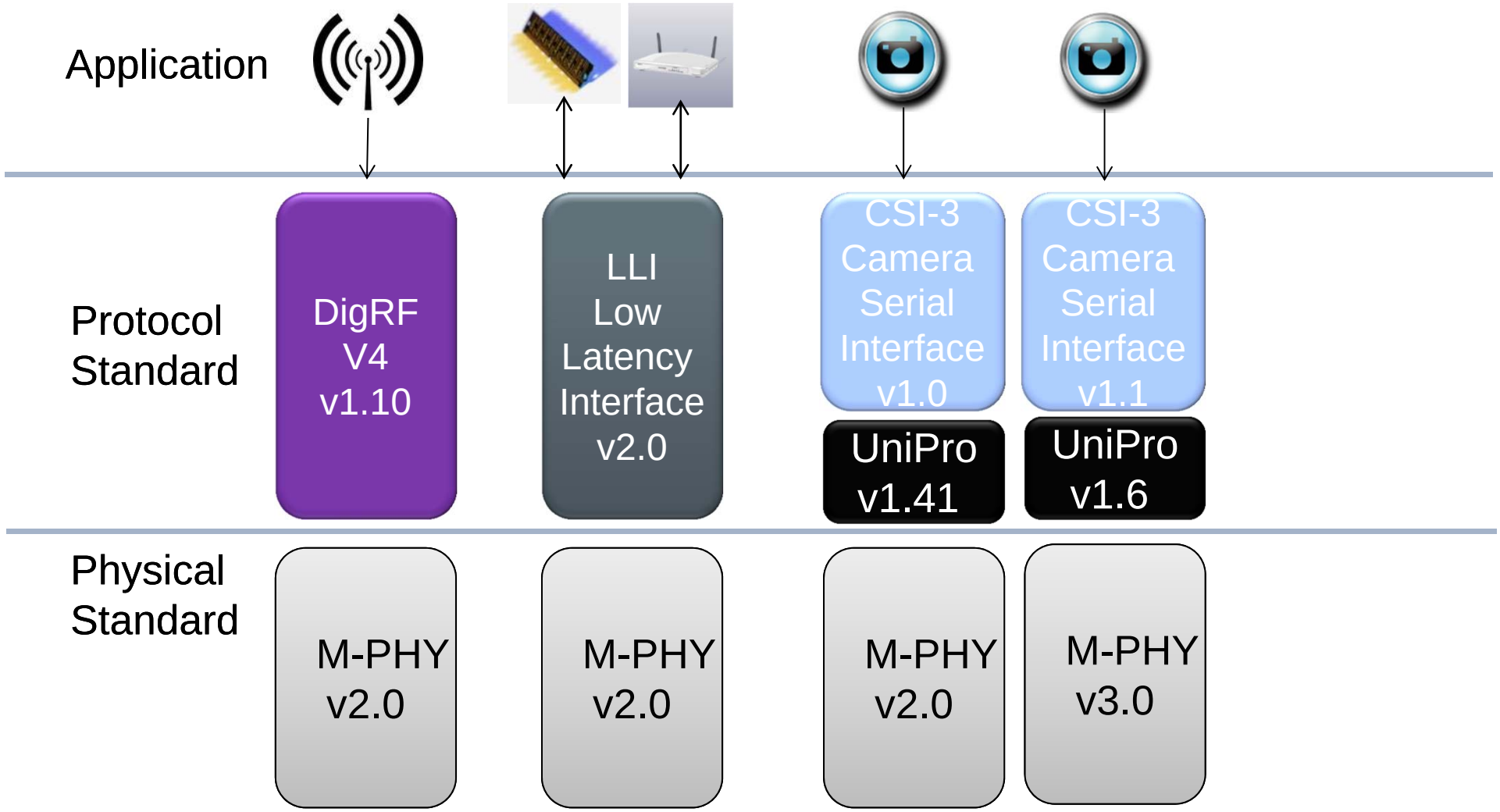
MIPI M-Phy, Protocol, Application Stackup



Neither UniPro v1.6 nor CSI-3 v1.1 have been officially released yet.

source: www.mipi.org

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MIPI M-Phy, Protocol, Application Stackup with Combined Standards

Application				
Protocol Standard	PCI-SIG M-PCIe M.2 Rev. 0.7a	USB-IF SSIC Rev. 1.01	JEDEC UFS V1.1 UniPro v1.41	JEDEC UFS V2.0 UniPro v1.6
Physical Standard	M-PHY v2.0	M-PHY v2.0	M-PHY v2.0	M-PHY v3.0

Neither UniPro v1.6 Nor UFS v2.0 have been officially released yet.

source: www.mipi.org

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Tek Strategic Involvement with MIPI Alliance &UNH-IOL

- Tektronix is a **Contributor Member** of the MIPI Alliance
- Tektronix is actively-participating in several MIPI Working Groups
- Tektronix has a close working relationship with UNH-IOL.
- Combined Tek Press-Release with UNH &MIPI Alliance in Sept-2010:
  - http://www2.tek.com/cmswpt/prdetails.lotr%3Fct%3DPR%26cs%3DNews%2BRelease%26ci%3D17639%26lc%3DEN&urlhash=HZu6

- "…….Tektronix is spurring the adoption of D-PHY and M-PHY specifications. Tektronix is aiding the adoption of the new M-PHY interface by giving designers the testing tools they need to ensure signal integrity and verify performance of increasingly complex designs."
  - ***Joel Huloux, Chairman of the MIPI Alliance.***
- "Tektronix has been supportive of UNH-IOL's collaborative efforts……,"
  - ***Andy Baldman, Senior technical staff, R&D, UNH-IOL.***

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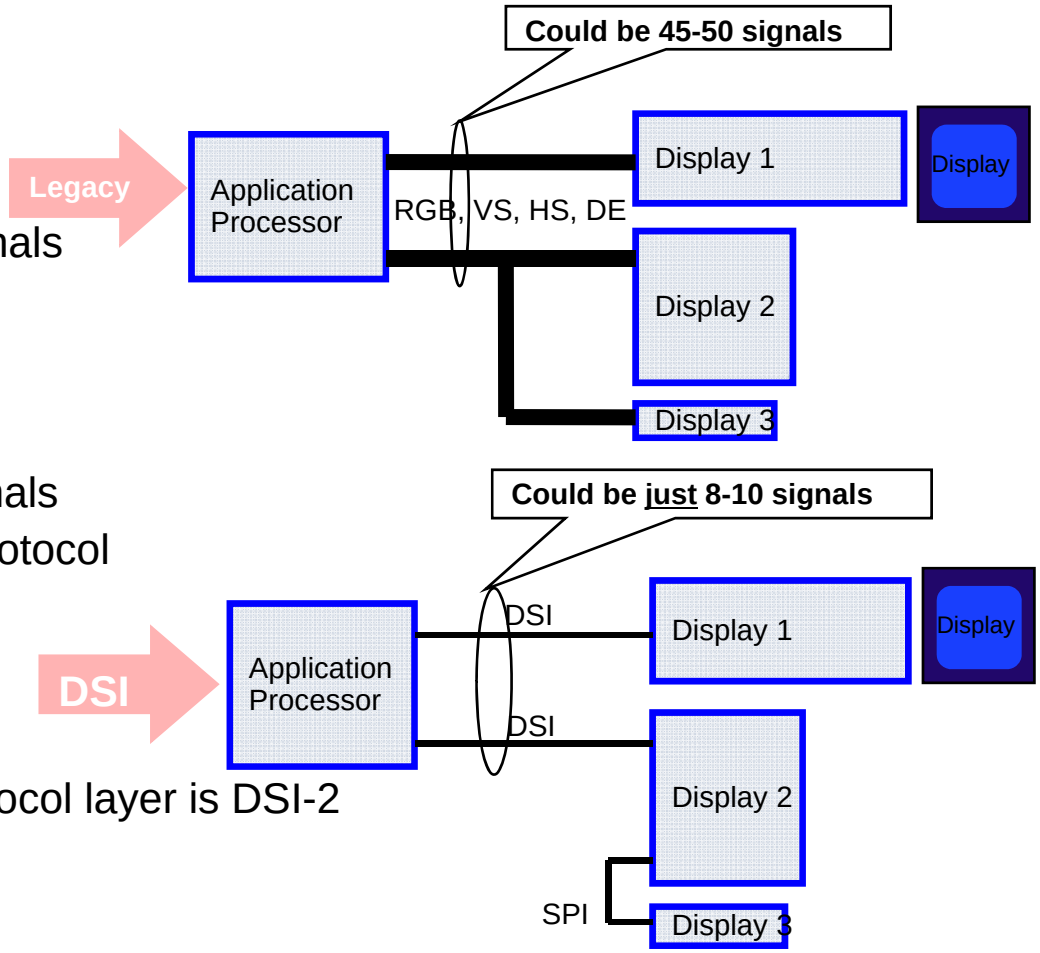
MIPI Display Serial Interface-DSI

- What is MIPI DSI?
  - DSI is the specification for Processor-to-Display interconnect

- Legacy Standards in a Mobile
  - Parallel busses with 45-50 signals

- MIPI DSI-1
  - A Serial bus with Just 8-10 signals
  - Physical layer is D-PHY and Protocol layer is DSI-1

- MIPI DSI-2
  - Physical layer is M-PHY & Protocol layer is DSI-2
  - Backward Compatible to DSI-1



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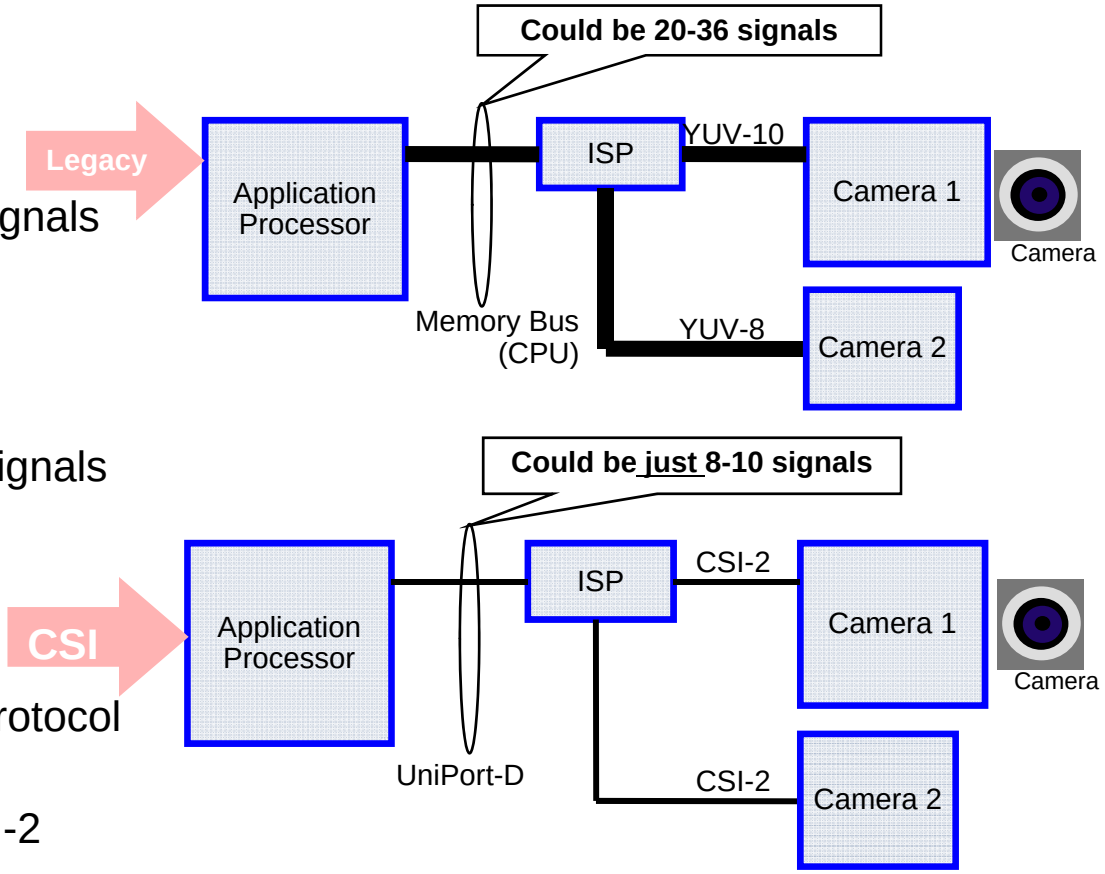
MIPI Camera Serial Interface CSI-2

- What is MIPI CSI?
  - CSI is the specification for Processor-to-Camera interconnect
- Legacy Standards in a Mobile
  - Parallel busses with 20-36 signals
- MIPI CSI-2
  - A Serial bus with Just 8-10 signals
  - Physical layer is D-PHY and Protocol layer is CSI-2
- MIPI CSI-3
  - Physical layer is M-PHY & Protocol layer is CSI-3
  - Backward Compatible to CSI-2



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MIPI D-PHY Functionality

- PHY standard for interfacing Camera (CSI) & Display (DSI)
- Synchronous connection between Master and Slave
- D-PHY Configuration
  - One clock signal
  - One or more data signals (Maximum 4-Lanes)
- Two modes of transmission

High-Speed (HS) mode	Low-Power (LP) mode
• Data Rate : 80 Mbps – 1.5 Gbps Typically at ~500 Mbps • Bus Termination : 50 ohms • Signal : 360mV (Max: V_{OHHS}) Differential • For fast-data traffic	• Data Rate : Up to 10 Mbps • Bus Termination : Hi-Z • Signal : 1.2V CMOS Level, Single ended • For control purposes

- Modes are mixed during the operation
  - Transitions from LP to HS and back to LP on the fly

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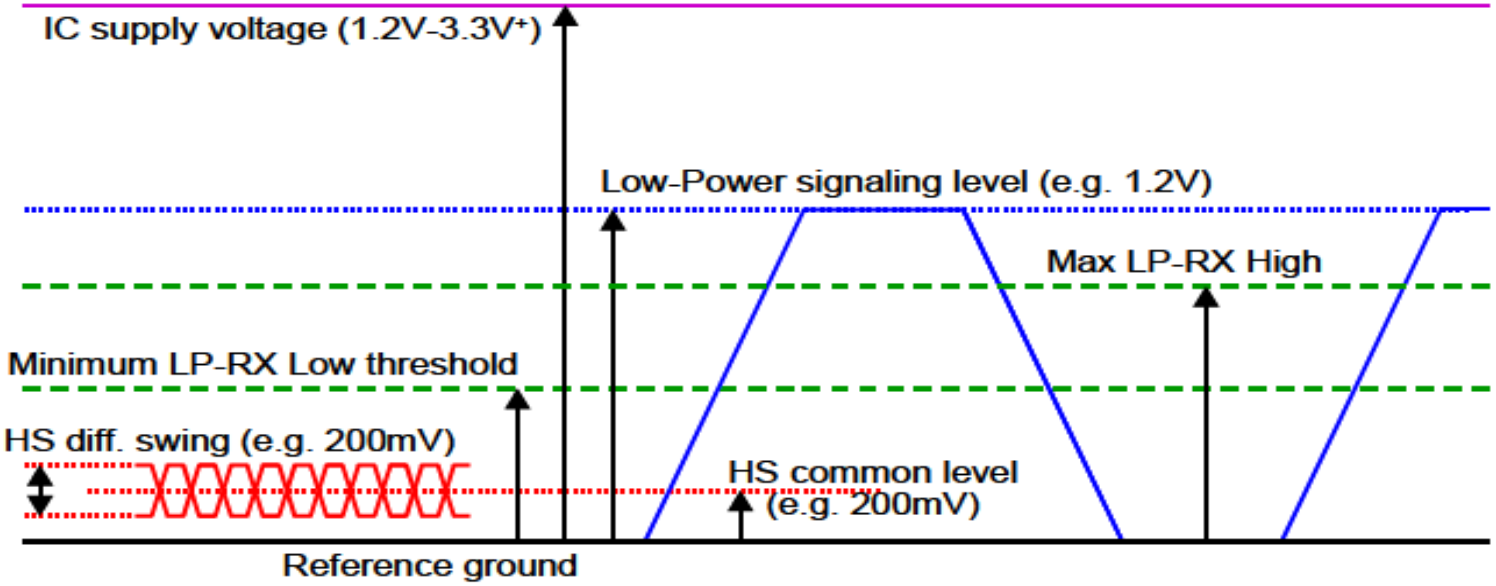
MIPI D-PHY Lane States and Line Levels

- Lane States
  - Low-Power Lane states : LP-00, LP-01, LP-10, LP-11
  - High Speed Lane states : HS-0, HS-1

- Line Levels (Typical)
  - LP High Level：0~1.2V
  - HS Common mode Voltage : 200mV
  - HS Differential Voltage 200mV



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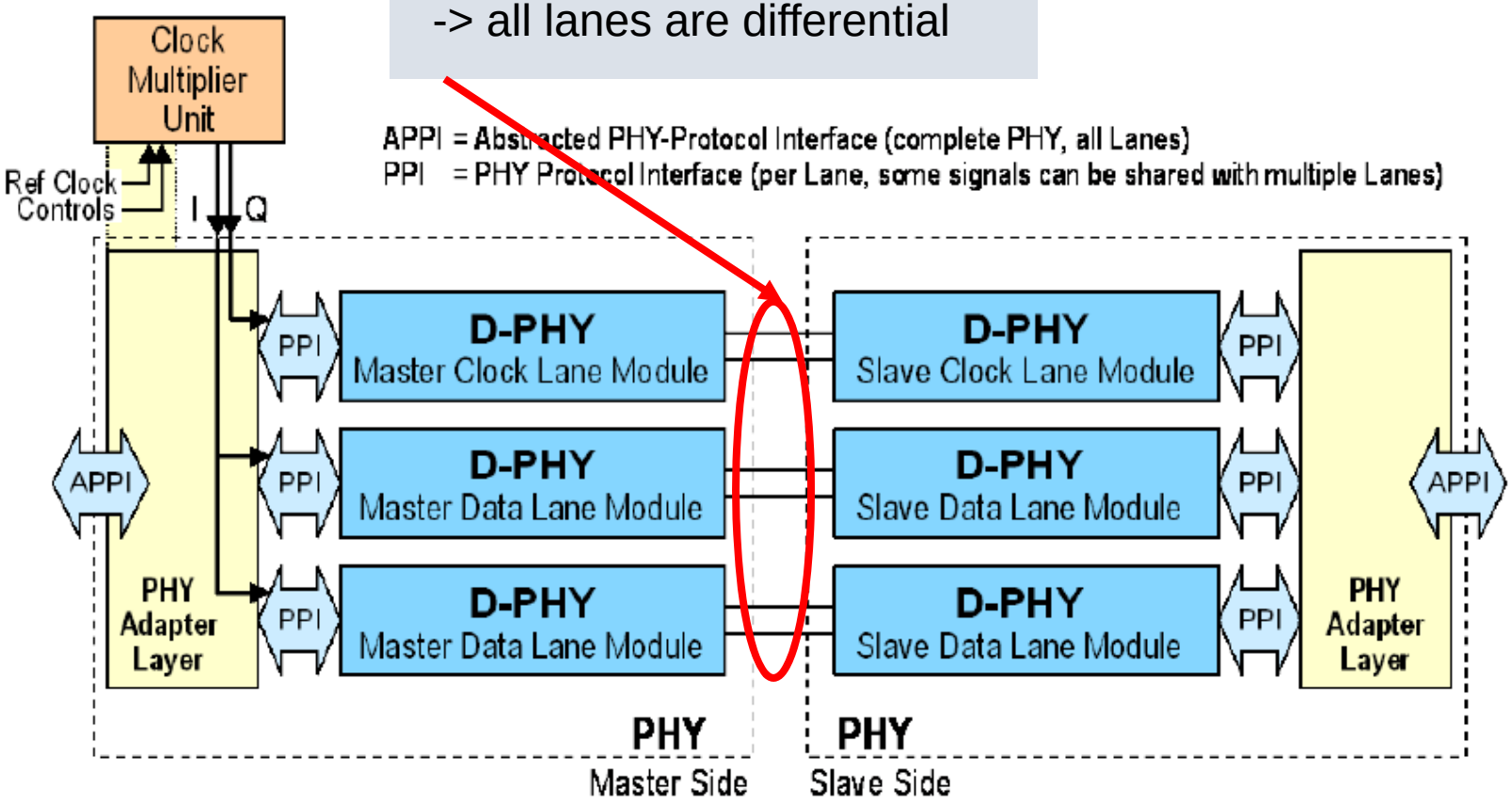
MIPI D-PHY Configuration

A MIPI D-PHY Link includes :
-. Clock lane : 1
-. Data lane : 1~4
-> all lanes are differential



Two-Data lanes MIPI D-PHY Link

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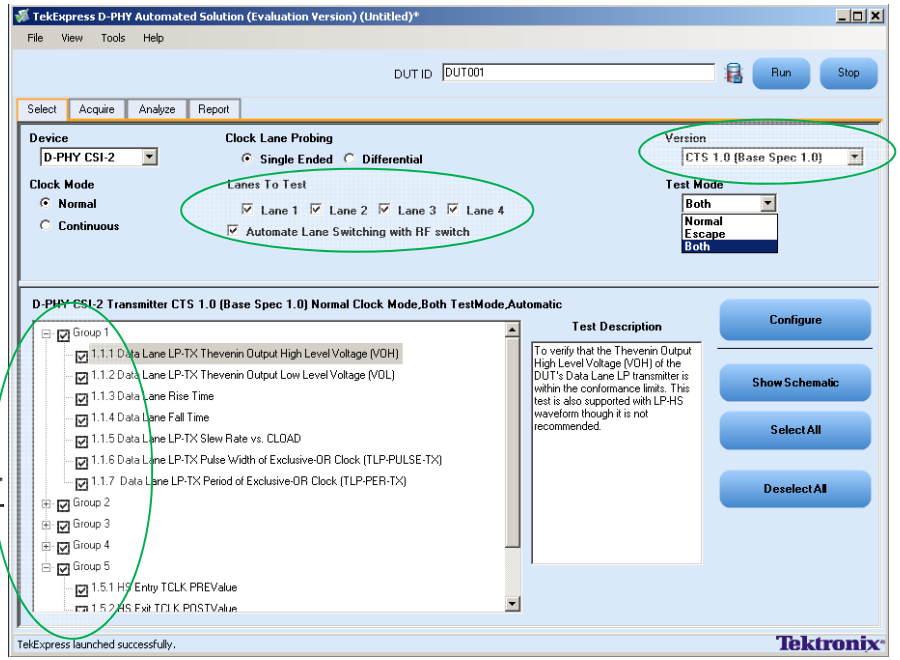
D-PHY Tx : Opt.D-PHYTX Conformance Test Solution

- Opt.D-PHYTX : D-PHY Automated Solution
  - TekExpress option for Fully-Automated testing
  - Provides Conformance and Characterization Testing
  - Based on Latest D-PHY Base Spec v1.1 and UNH's Conformance Test Suite v1.0.
  - Runs on 7K/C and 70K/B/C scopes
  - Opt.TEKEXP is Pre-Requisite
- Differentiation
  - **Un-parallel** Automation (Auto-Cursors)
  - **100%** Widest Test Coverage
  - Conformance to Latest CTS (v1.0)
  - Based on Latest Base spec (v1.1)
  - Fully-Automated for Multi-lane DUTs
  - Fully-Automated Temperature Chamber
- Value proposition
  - Custom-limits/ Limits-Editing
  - Test Reports with Pass/Fail summary, margins, & "Zoom-in" Waveform Captures
  - Tek 3.5GHz scope is the minimal configuration for accurate testing
  - D-PHY extension spec (1.5G) ready



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D-PHY Tx Test Items

Group 4	Clock Lane HS-TX Signaling
1.4.1	Clock Lane HS Entry: TLPX Value
1.4.2	Clock Lane HS Entry: TCLK-PREPARE Value
1.4.3	Clock Lane HS Entry: TCLK-PREPARE + TZERO Value
1.4.4	Clock Lane HS-TX Differential Voltages (VOD(0), VOD(1))
1.4.5	Clock Lane HS-TX Differential Voltage Mismatch (ΔVOD)
1.4.6	Clock Lane HS-TX Single Ended Output High Voltages (VOHHS(DP),VOHHS(DN))
1.4.7	Clock Lane HS-TX Common-Mode Voltages (VCMTX(1),VCMTX(0))
1.4.8	Clock Lane HS-TX Common-Mode Voltage Mismatch (ΔVCMTX(1,0))
1.4.9	Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450 MHz (ΔVCMTX(LF))
1.4.10	Clock Lane HS-TX Dynamic Common-Level Variations Above 450 MHz (ΔVCMTX(HF))
1.4.11	Clock Lane HS-TX 20%-80% Rise time (tR)
1.4.12	Clock Lane HS-TX 80%-20% Fall time (tR)
1.4.13	Clock Lane HS Exit: TCLK-TRAIL Value
1.4.14	Clock Lane HS Exit: 30%-80% Post-EoT Rise Time (TREOT) Value
1.4.15	Clock Lane HS Exit: TEOT Value
1.4.16	Clock Lane HS Exit: THS-EXIT Value
1.4.17	Clock Lane HS Clock Instantaneous (UIINST)

Group 5	HS-TX Clock-to-Data Lane Timing
1.5.1	HS Entry TCLK-PREValue
1.5.2	HS Exit TCLK-POST Value
1.5.3	HS Clock Rising Edge Alignment to First Payload Bit
1.5.4	Data-to-Clock Skew (TSKEW (TX))

Group 1	Data Lane LP-TX Signaling
1.1.1	Data Lane LP-TX Thevenin Output High Level Voltage (VOH)
1.1.2	Data Lane LP-TX Thevenin Output Low Level Voltage (VOL)
1.1.3	Data Lane Rise Time
1.1.4	Data Lane Fall Time
1.1.5	Data Lane LP-TX Slew Rate vs. CLOAD (δV/δtSR)
1.1.6	Data Lane LP-TX Pulse Width of Exclusive-OR Clock (TLP-PULSE-TX)
1.1.7	Data Lane LP-TX Period of Exclusive-OR Clock (TLP-PER-TX)
Group 2	Clock Lane LP-TX Signaling
1.2.1	Clock Lane LP-TX Thevenin Output High Level Voltage (VOH)
1.2.2	Clock Lane LP-TX Thevenin Output Low Level Voltage (VOL)
1.2.3	Clock Lane Rise Time
1.2.4	Clock Lane Fall Time
1.2.5	Clock Lane LP-TX Slew Rate vs. CLOAD (δV/δtSR)

Group 3	Data Lane HS-TX Signaling
1.3.1	Data Lane HS Entry: Data Lane TLPX Value
1.3.2	Data Lane HS Entry: THS-PREPARE Value
1.3.3	Data Lane HS Entry: THS-PREPARE + THS-ZERO Value
1.3.4	Data Lane HS-TX Differential Voltages (VOD(0), VOD(1))
1.3.5	Data Lane HS-TX Differential Voltage Mismatch (ΔVOD)
1.3.6	Data Lane HS-TX Single Ended Output High Voltages (VOHHS(DP),VOHHS(DN))
1.3.7	Data Lane HS-TX Common-Mode Voltages (VCMTX(1),VCMTX(0))
1.3.8	Data Lane HS-TX Common-Mode Voltage Mismatch (ΔVCMTX(1,0))
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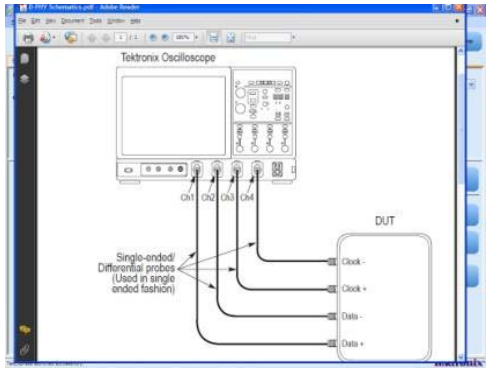
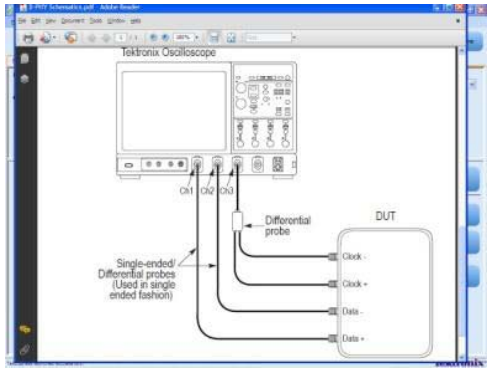
1.3.11	Data Lane HS-TX 20%-80% Rise time (tR)
1.3.12	Data Lane HS-TX 80%-20% Fall time (tR)
1.3.13	Data Lane HS Exit: THS-TRAIL Value
1.3.14	Data Lane HS Exit: 30%-80% Post-EoT Rise Time (TREOT) Value
1.3.15	Data Lane HS Exit: TEOT Value
1.3.16	Data Lane HS Exit: THS-EXIT Value
Group 6	
1.6.1	INIT: LP-TX Initialization Period (TINIT,MASTER)
1.6.2	ULPS Entry: Verification of Clock Lane LP-TX ULPS support
1.6.3	ULPS Exit: Transmitted TWAKEUP Interval
1.6.4	BTA: TX-Side TTA-GO Interval Value
1.6.5	BTA: RX-Side TTA-SURE Interval Value
1.6.6	BTA: RX-Side TTA-GET Interval Value





Probes connection for Data/CLK Lanes

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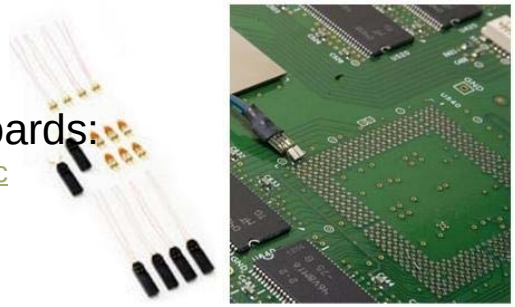
D-PHY Tx : Recommended Test Setup

www.tek.com/MIPI

- Scope
  - DPO7354 or DPO/DSA/MSO70404/B/C or higher for rise time accuracies
- Probes
  - For 7Ks: 4x TAPxx/ P6245/ P6249, or 4x TDP3500 (clock is non-continuous), or 3x TDP3500 (clock is continuous).
  - For 70Ks: 4xP7240, or 4xP73xx (clock is non-continuous), or 3xP73xx (clock is continuous).
- Scope Software
  - Opt.D-PHYTX on TEKEXP for Conformance Test
- Fixtures
  - As MIPI is a chip-to-chip interface, most DUT setups are LIVE with Master-Slave/ Receiver-end connected.
  - For live-setups: No Fixtures required.
  - For non-live setups:
    - No standard fixture is defined.
    - We recommend following UNH-IOL Termination boards: www.iol.unh.edu/services/testing/mipi/MIPI_Test_Fixture_Order_Form.doc



P7380 probe used with a probe-tip

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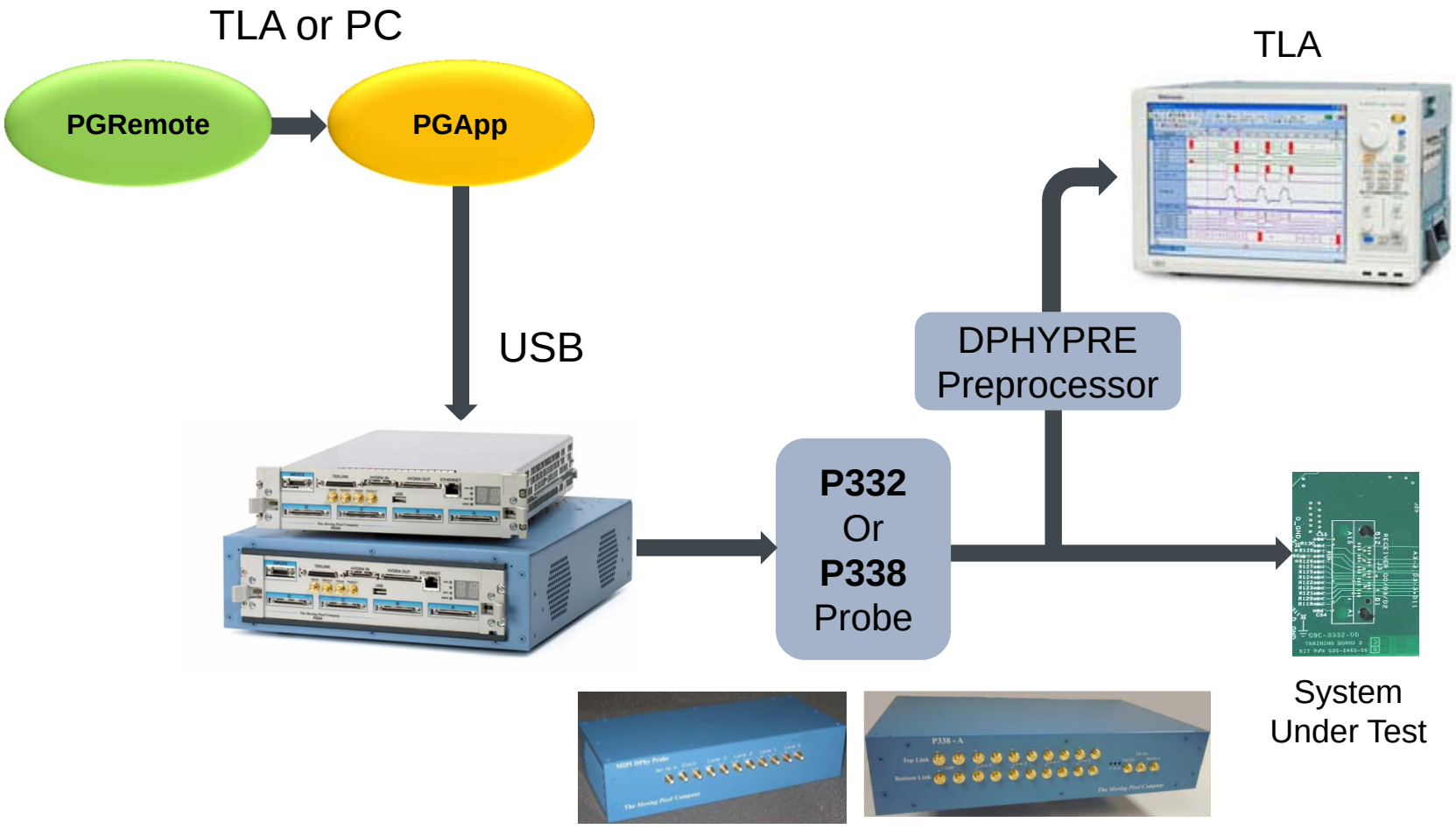
Stimulus Setup



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Stimulus

- **Protocol Testing** – Stimulating buses with known good data packets or packets with intentional errors tests the system's adherence to a specified protocol
- **Infrequent Events** - System bugs that only appear when infrequent events occur can be quickly reproduced with a pattern generator by repeatedly stimulating the system with the key external event
- **Automated Test** – Production line test setups can utilize the PG3A as a general purpose digital I/O source with a large number of channels

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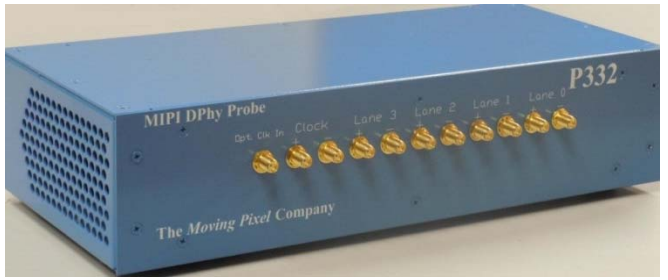
P332 MIPI D-PHY Probe for PG3A

Key Features

- MIPI D-PHY Probe for use with PG3AMOD and PG3ACAB
- Generate CSI2 and DSI data over D-PHY
- 4-Data Lanes and 1-Clock lane
- 1.5Gbps / Lane data rate
- SMA outputs for each lane
- LP and HS Voltage and Timing adjustable on a each lane separately

PG3A

P332



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D-PHY Rx : Test Solution Overview

100% Test Coverage

Group 1 LP - RX voltage and timing requirements			
Test	**Title**	**Page**	**Equipment**
2.1.1	LP - RX Logic 1 Input Voltage (V_{IH})	108	PG
2.1.2	LP - RX Logic 0 Input Voltage, non-ULP State (V_{IL})	110	PG
2.1.3	LP - RX Logic 0 Input Voltage, ULP State ($V_{IL-ULPS}$)	112	PG
2.1.4	LP - RX Minimum Pulse Width Response (T_{MIN-RX})	113	PG
2.1.5	LP - RX Input Hysteresis (T_{HYST})	114	PG
2.1.6	LP - RX Input Pulse Rejection (e_{SPIKE})	116	PG + AWG + DC Power Supply
2.1.7	LP - RX Interference Tolerance (V_{INT} and f_{INT})	120	PG + AWG
2.1.8	LP - CD Logic Contention Thresholds (V_{ILCD} and V_{IHCD})	122	PG + AWG

Group 2 LP - RX Behavioral Requirements			
Test	**Title**	**Page**	**Equip**
2.2.1	LP - RX Initialization Period (T_{INIT})	125	PG
2.2.2	ULPS Exit: LP - RX T_{WAKEUP} Timer Value	126	PG
2.2.3	Clock Lane LP - RX Invalid/Aborted ULPS Entry	127	PG
2.2.4	Data Lane LP - RX Invalid/Aborted Escape Mode Entry	128	PG
2.2.5	Data Lane LP - RX Invalid/Aborted Escape Mode Command	130	PG
2.2.6	Data Lane LP - RX Escape Mode Invalid Exit (Informative)	132	PG
2.2.7	Data Lane LP - RX Escape Mode, Ignoring Post Trigger-Command Extra Bits	134	PG
2.2.8	Data Lane LP - RX Escape Mode Unsupported/Unassigned Commands	136	PG

Group 3: HS - RX Voltage and Setup/Hold Requirements			
Test	**Title**	**Page**	**Equipment**
2.3.1	HS - RX Common Mode Voltage Tolerance ($V_{CMRX(DC)}$)	139	PG
2.3.2	HS-DX Differential Input High Threshold (V_{DTH})	141	PG
2.3.3	HS-DX Differential Input Low Threshold (V_{DTL})	143	PG
2.3.4	HS - RX Single-Ended Input High Voltage (V_{HSHI})	144	PG
2.3.5	HS - RX Single-Ended Input Low Voltage (V_{HSLO})	146	PG
2.3.6	HS - RX Common Mode Interference 50MHz - 450MHz (delta VCMRX(LF))	148	PG + AWG
2.3.7	HS - RX Common Mode Interference Beyond 450MHz (delta VCMRX(HF))	150	PG + AWG
2.3.8	HS - RX Setup/Hold and Jitter Tolerance	151	PG + AWG

Group 4: HS - RX Timer Requirements			
Test No.	**Title**	**Page**	**Equipment**
2.4.1	Data Lane HS - RX $T_{SETTLE(N)}$ Value	156	PG
2.4.2	Data Lane HS - RX $T_{SETTLE(PROTO)}$ + $T_{SETTLE(M)}$ Tolerance	158	PG
2.4.3	Data Lane HS - RX $T_{HS-SETTLE}$ Value	160	PG
2.4.4	Data Lane HS - RX $T_{HS-SETTLE}$ Tolerance	162	PG
2.4.5	Data Lane HS - RX $T_{HS-SKIP}$ Value	164	PG
2.4.6	Clock Lane HS - RX $T_{CLKSETTLE(N)}$ Value	166	PG
2.4.7	Clock Lane HS - RX $T_{CLKSETTLE(PROTO)}$ + $T_{CLKSETTLE(M)}$ Tolerance	167	PG
2.4.8	Clock Lane HS - RX $T_{CLKSETTLE}$ Value	169	PG
2.4.9	Clock Lane HS - RX $T_{CLKSETTLE}$ Tolerance	171	PG
2.4.10	Clock Lane HS - RX $T_{CLKMISS}$ Value	173	PG
2.4.11	Clock Lane HS - RX T_{CLKPRE} + $T_{CLKPOST}$ Tolerance	175	PG

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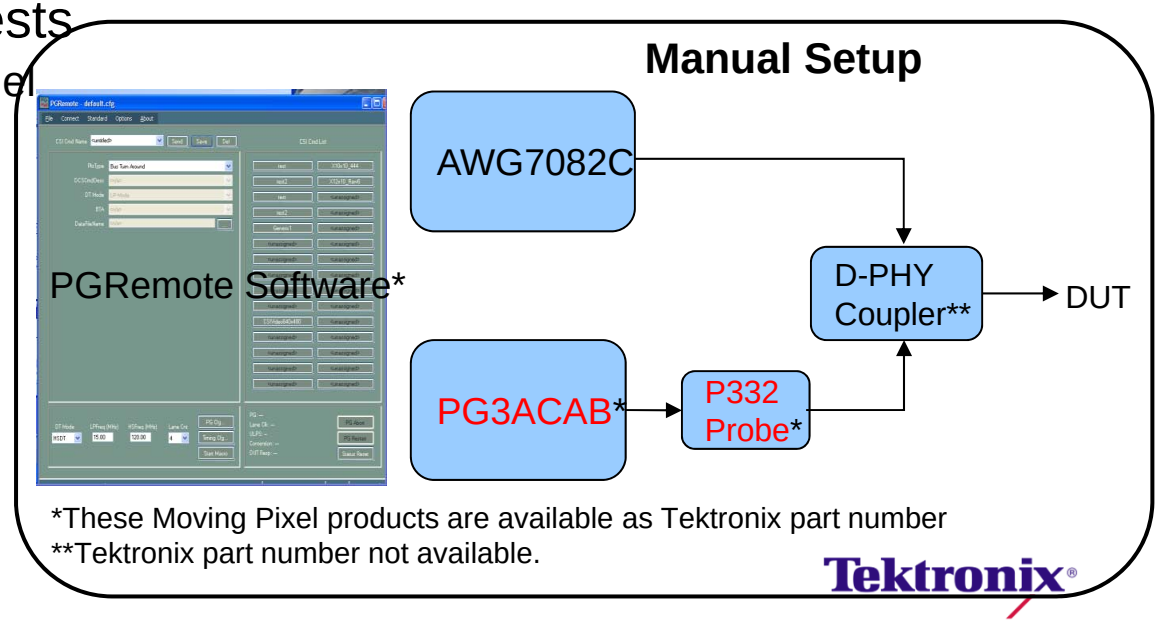
D-PHY Rx : Test Solution Overview

Manual/ Workaround Setup based on PG with PGRemote Software

Simple, Quick, Easy and Re-usable

- 100% Coverage to Rx CTS
  - Meets all the requirements in UNH-IOL CTS document (v1.0)
- Quick and Easy setup
  - No complex VXI system, just stand alone instruments, and a probe.
- Cost effective solution
  - 70% Lower list price vs Competition
- Re-usable for Protocol tests
  - PG3A is the Only 4 channel solution for CSI &DSI test
- PG3A Pattern Generator
  - Controls clock and signaling to establish link with DUT
  - Adjusts voltage levels, packet type, etc to stress test receiver
- AWG7082C with Coupler
  - Adds jitter and interference to the D-PHY signals
  - Needed only for 6 out of 35 total Rx tests.



PGRemote

- Push Button User interface to generate CSI2 or DSI vectors and probe control
- Adjust frequency, voltage and delay in HS and LP modes
- Adjust D-PHY state timing parameters
- Adjust frame timing and generate looping video
- Enter and exit Low power states
- Create custom commands, Macros and assign them to buttons
- Save restore a configuration
- Ability to use P332 as a generic high-speed serial probe
- The PG can be operated in several modes
  - Pushbutton Mode using the PGRemote software
  - Macro Mode using the PGRemote software
  - Scripting
  - Full remote control mode

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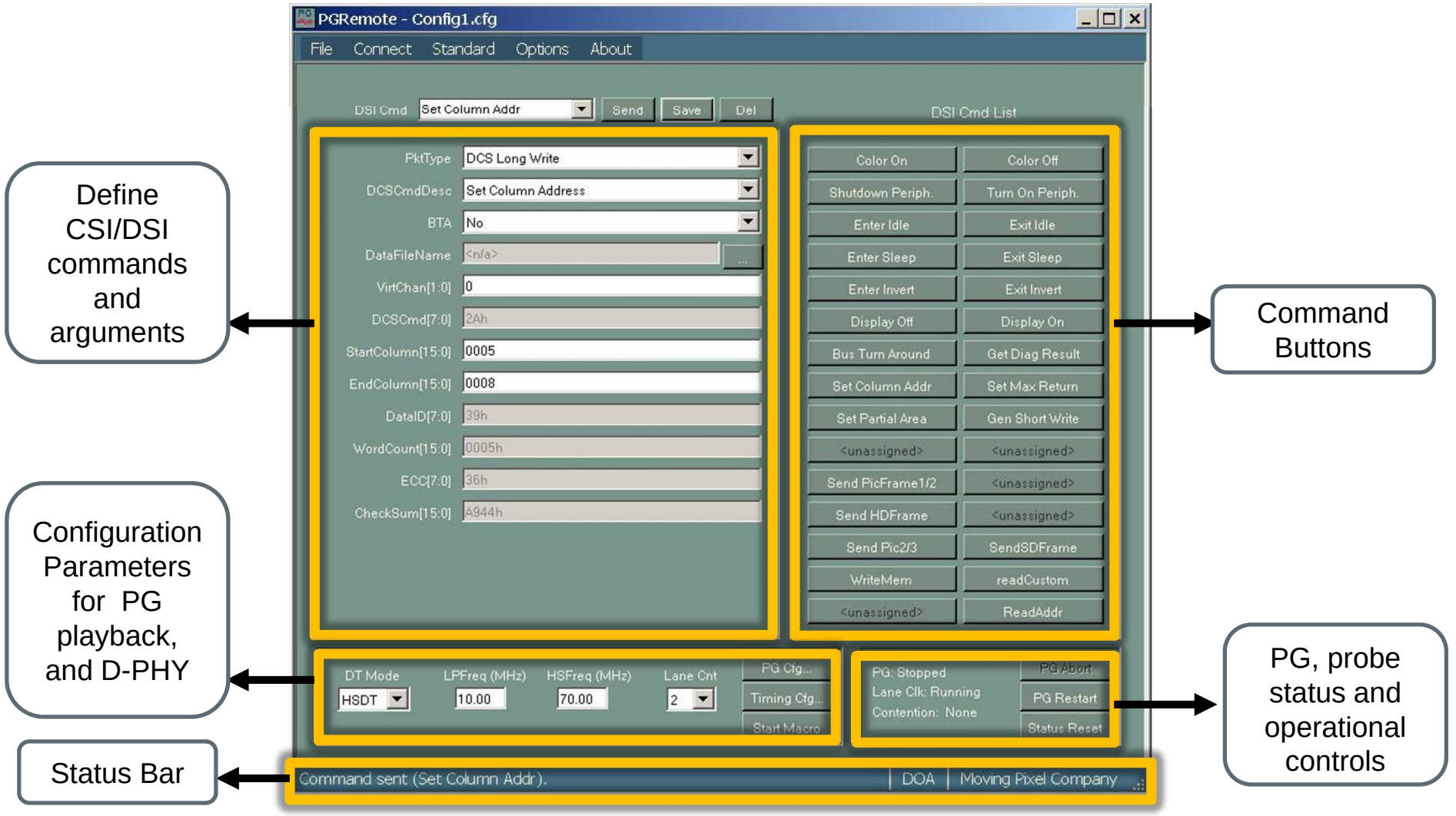
PGRemote

Push Button Interface to generate CSI2 / DSI Vectors



Define CSI/DSI commands and arguments

Configuration Parameters for PG playback, and D-PHY

Status Bar

Command Buttons

PG, probe status and operational controls

PGRemote Main Window

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CSI2/DSI Protocol validation

Solution Overview

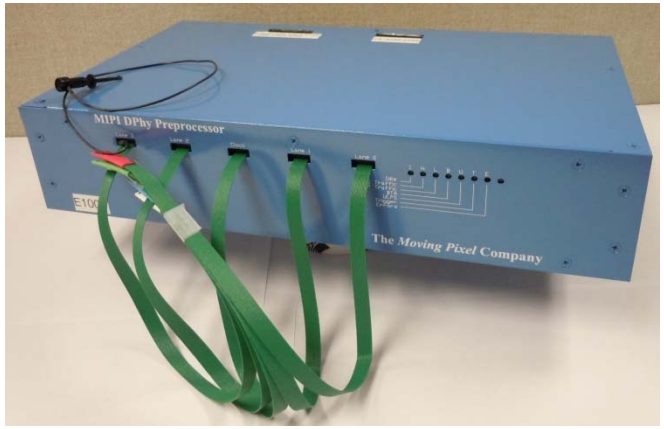
P6982 or
P6980 Probe

USB Cable
For Control

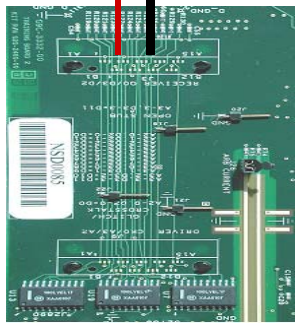
D-PHY
Preprocessor

Clk

Data
(up to 4 Lanes)



D-PHY Preprocessor



Tektronix®

D-PHY Preprocessor

- Support 1.5Gbps per lane
- Support for up to 4 Lanes of D-PHY data
- Color coded solder down probes for easy identification
- Support CSI2/DSI Protocols
- Advanced Packet Level Triggering
- Real Time Filtering
- Lane activity and Error Status
- Simultaneous Low Power and High Speed Data Acquisition
- 8x improvement in TLA Memory usage
- Image Export
- Compatible with both TLA6k and TLA7k

Preserve your investment with the ONLY 4 lane,
1.5Gbps protocol solution in the market.

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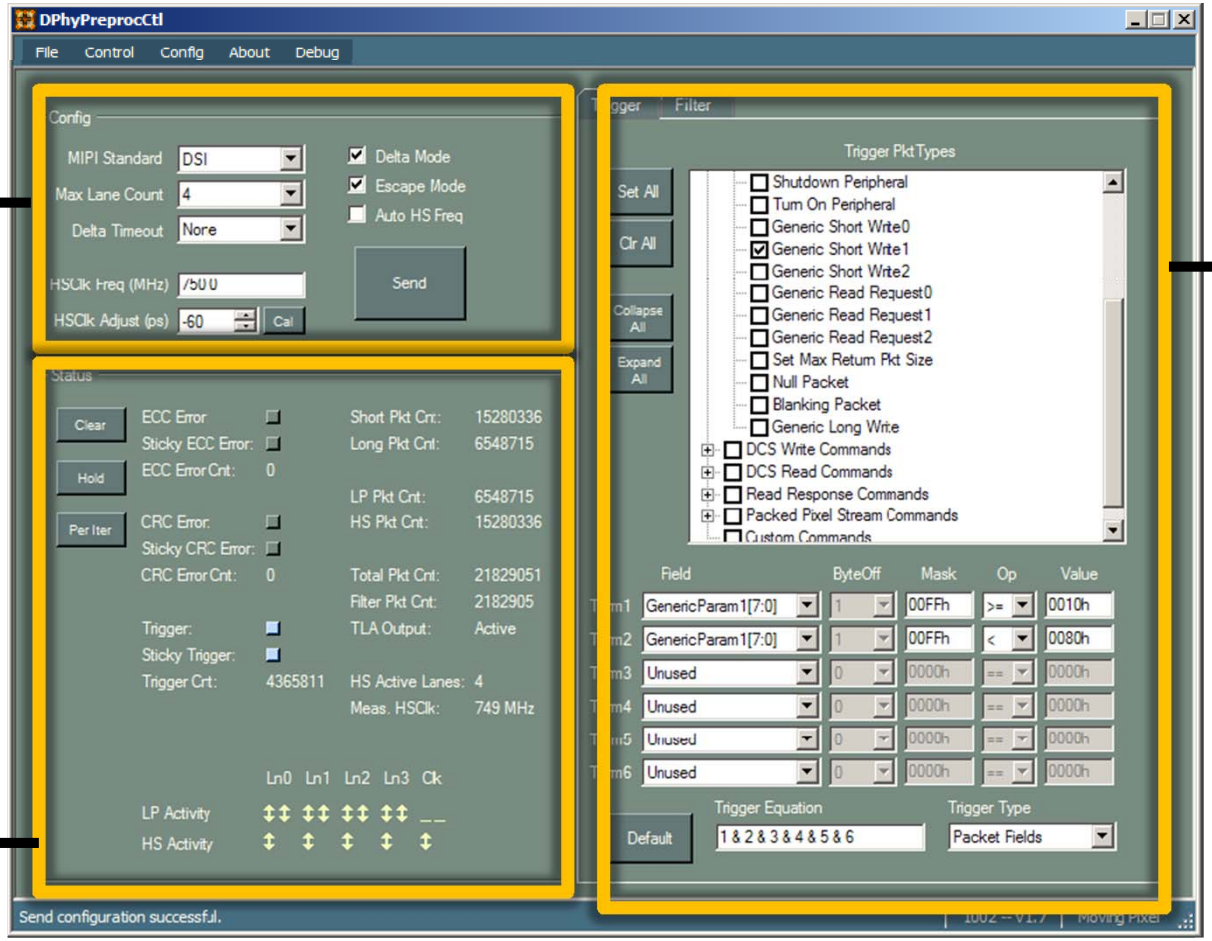
D-PHY Preprocessor control UI

Preprocessor Configuration



Trigger & Filter Definitions

Status Area
- Lane Activity
- Trigger Status
- Error Status

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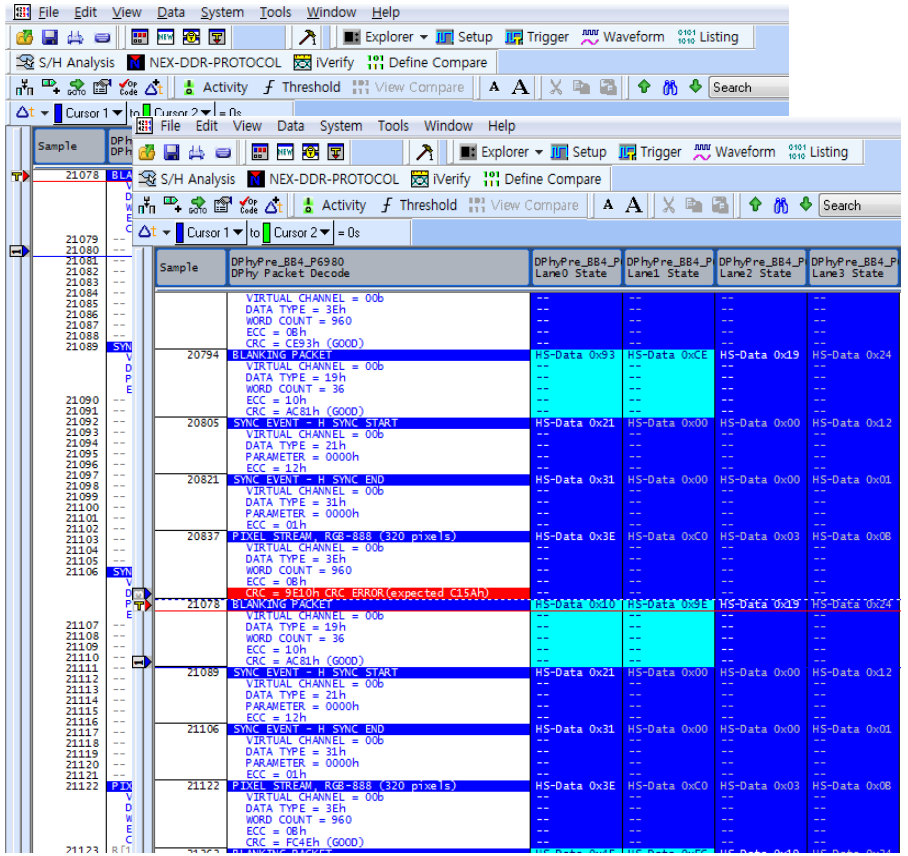
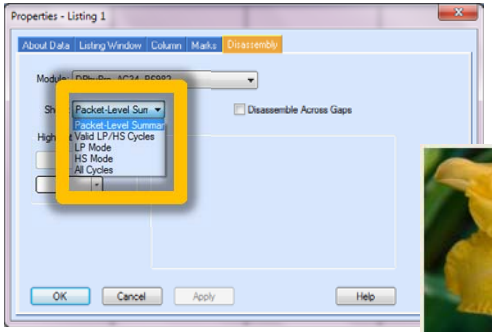
D-PHY Decode

- Supports from 1 to 4 lanes of D-PHY data
- Decode and Display
  - All LP and HS state transitions
  - LP commands and data
  - LP and HS Data in Byte Format
  - All types of Short and Long packets
  - DCS Command decode
- Supports different RGB and YUV Schemes
- Supports ECC and Checksum verification.
- selectively view the decoded information at different levels of hierarchy
- Packets extracted & stored for further analysis





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System Configuration

Protocol Decode

- Option - 1
  - DPHYPRE (1ea)
  - P6982 (2ea)
  - TLA6K or TLA7ACx (1ea)
  - TLA7012/TLA7016 (1ea)
    - For use with TLA7ACx
- Option - 2
  - DPHYPRE (1ea)
  - P6980 (1ea)
  - TLA7BBx (1ea)
  - TLA7012/TLA7016 (1ea)
    - For use with TLA7BBx

Stimulus

- Option - 1
  - PG3AMOD (1ea)
  - P332 (1ea)
  - PGRemoteSW (1ea)
  - TLA7012/TLA7016 (1ea)
    - For use with PG3AMOD
- Option - 2
  - PG3ACAB (1ea)
  - P332 (1ea)
  - PGRemoteSW (1ea)

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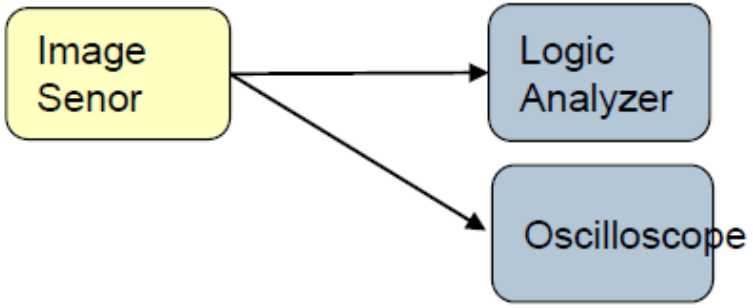
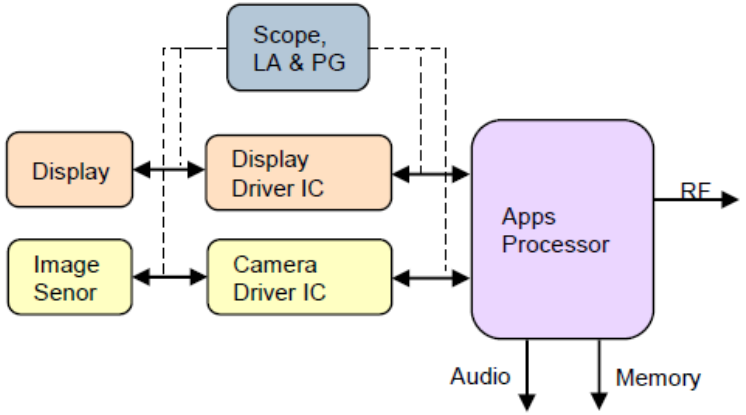
MIPI Solutions and Techniques

- Oscilloscope
  - Signal Integrity
  - D-PHY Physical Layer Test
- Logic Analyzer (LA)
  - Validation and debug of the MIPI Protocol
- Pattern Generator (PG)
  - MIPI Signal Generation
  - Stimulating Driver ICs, Devices and Processors
- Oscilloscope, Logic Analyzer and Pattern Generator
  - System level Validation & Debug
  - Testing fully integrated mobile handset platforms





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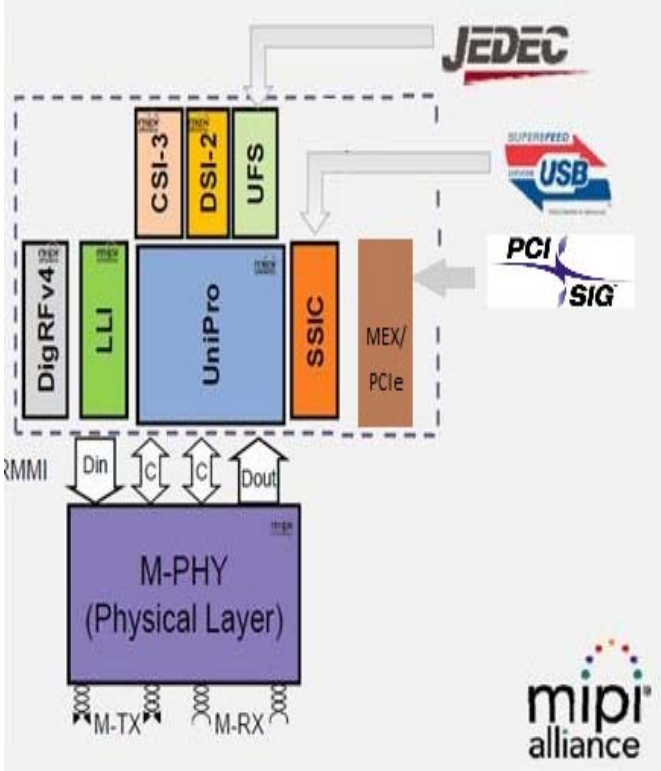
What is M-PHY ?

- M-PHY is a **Common** Electrical Spec for
  - **DigRFv4, UniPro, LLI, HSI, CSI-3 and DSI-2** protocols of the **MIPI Alliance.**
  - **SSIC** (Super Speed Inter Connect) protocol of **USB-IF**.
  - **UFS** (Universal Flash Storage) protocol of **JEDEC.**
  - MPCIe – PCIe protocol on M-PHY
  - Supports high data rates at Minimal power, Cost & I/O redesign
  - For High Definition Video capture/ transmission in a mobile phone, etc.



Application	Architecture
DigRF v4	DigRF
CSI-3	UNIPRO
DSI-2	UNIPRO
UFS Memory	UNIPRO
SuperSpeed USB	SSIC
DDR Memory	LLI
PCI Express	MPCIe

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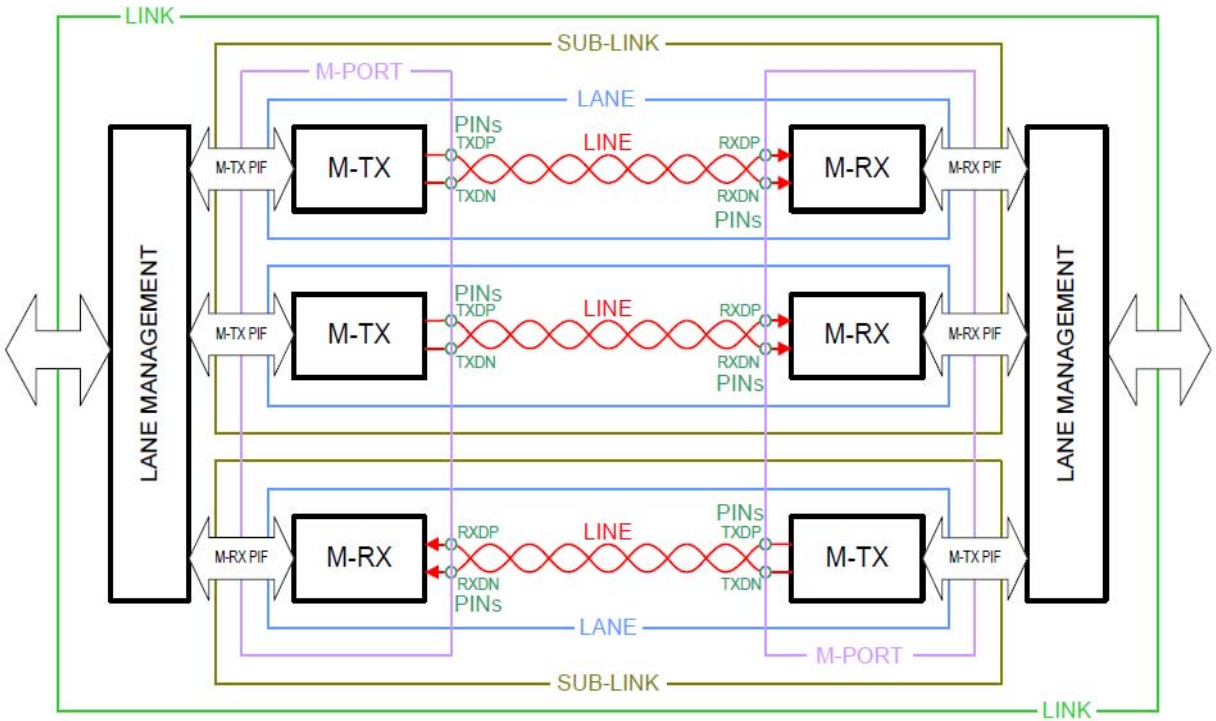
MIPI M-PHY Configuration

- M-PHY Operates as
  - Link : is made up of two SUBLINKs
  - Sub-link : Containing one or more LANEs
  - Lane : Consists of an M-PHY transmit MODULE (M-TX), an M-PHY receiver MODULE (M-RX), and a LINE
    : unidirectional point-to-point differential serial connection between PINs
  - Line : the point-to-point interconnect between the M-TX and M-RX



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M-PHY Signal Characteristics

M-PHY Signal Characteristics							
Signaling mode	**Data-rates**			**Amplitudes**		**Impedance**	
High Speed (HS)	Gears	A (Gbps)	B (Gbps)	Large	Small	Resistive Terminated	Non-Terminated
	G1	1.25	1.45	Terminated: 160-240mV, Non-Terminated: 320-480mV	Terminated: 100-130mV, Non-Terminated: 200-260mV	100 ohms	-
	G2	2.5	2.91				
	G3	5	5.83				
PWM (ie. TYPE-I)	Gears	Min (Mb/s)	Max (Mb/s)			100 ohms	10k ohms
	G0	0.01	3				
	G1	3	9				
	G2	6	18				
	G3	12	36				
	G4	24	72				
	G5	48	144				
	G6	96	288				
	G7	192	576				
SYS (ie. TYPE-II)			576 (Mb/s)			100 ohms	10k ohms

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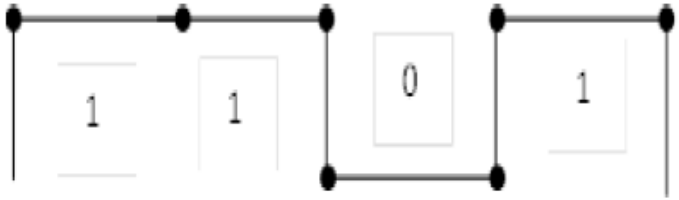
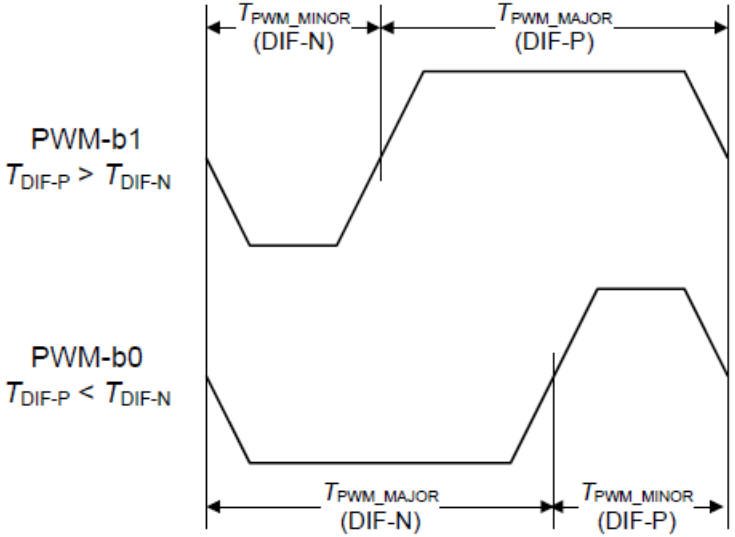
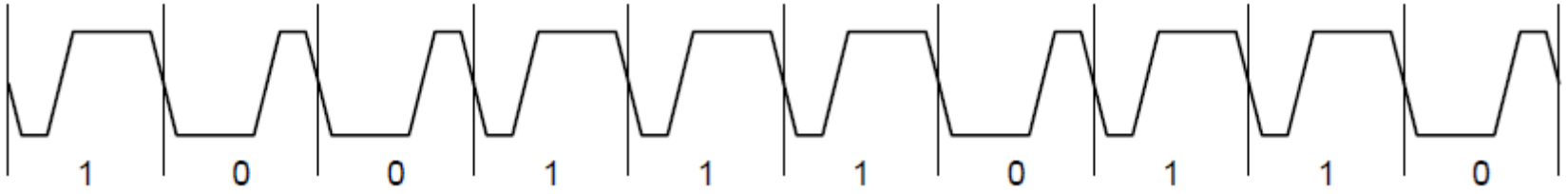
M-PHY Bit Signaling Schemes

- Two signaling Schemes
  - Non-Return-to-Zero (NRZ)
    - HS-Burst
    - SYS-Burst
  - Pulse-Width-Modulation (PWM) Signaling
    - Self-clocking
    - PWM-Burst







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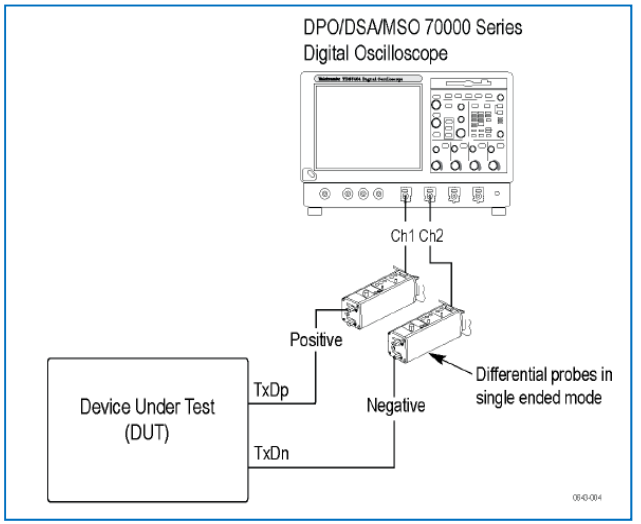
M-PHY Tx Testing

Transmitter Testing

Oscilloscope

HS Gear	Max Datarates	Oscilloscope Bandwidth
G1	1.45 Gb/s	5 GHz
G2	2.9 Gb/s	10 GHz
G3	5.83 Gb/s	20 GHz



Probing/Connectivity

- 2 ea. High-Impedance, Low-Capacitive-Load Differential Probes
- 1 ea. M-PHY 100Ohm Terminated-Mode Test Fixture
- 1 ea. M-PHY Unterminated-Mode Test Fixture

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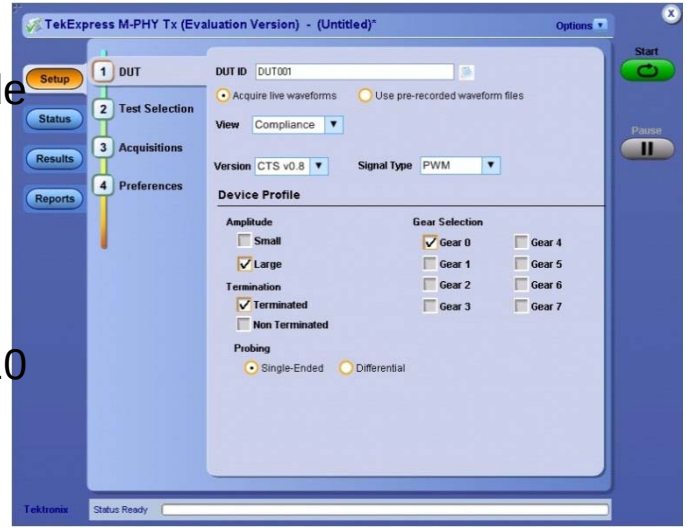
M-PHY Tx : Opt.M-PHYTX Automated Solution
Beyond Conformance Test, with Seamless-Debug

- Opt.M-PHYTX
  - **Single-button Fully-Automated** Transmitter Test Solution
  - Provides Conformance Test &Debug Analysis to Base Spec v1.0 &UNH's CTS.
  - Runs on a DPO/DSA70KB/C/D or MSO70K/C scope (6GHz and above)
  - Opt.DJA is pre-requisite. Opt.M-PHY not required. (Based on TekExpress 2.0.)
- Differentiation
  - **Seamless Debug** on Failures, &User-Defined mode
  - **Scope-based PSD** Power-Spectral Density tests
  - **Most Complete** Test coverage.
    - (95% HS all Gears, 74% PWM all Gears).
  - **Multi-lane** one-time Setup (Diff Acquisition mode)
  - Tek is **Industry 1st** in M-PHY Test, since Sept, 2010



- Value Proposition
  - For Gear2 M-PHY Tx testing, **Tek 8GHz oscilloscope is sufficient**. Where as, both competition requires a 12GHz or 13GHz oscilloscope setup.
  - For Gear3 M-PHY Tx testing, **Tek 20G oscilloscope is sufficient**. Where as, both competition requires a 25GHz oscilloscope setup.

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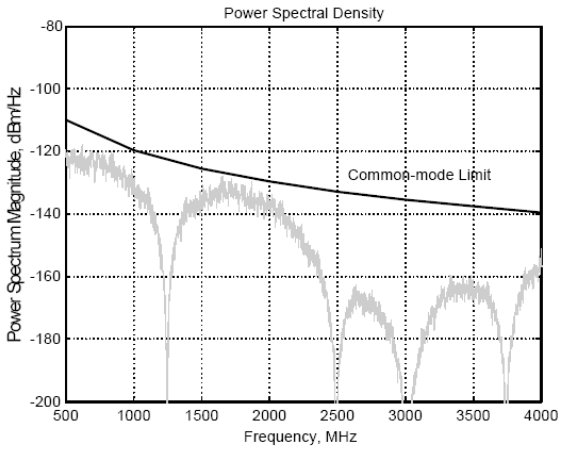
M-PHY Tx: Opt.M-PHYTX Automation Features

Oscilloscope based Power Spectral Density(PSD), Eye Diagram

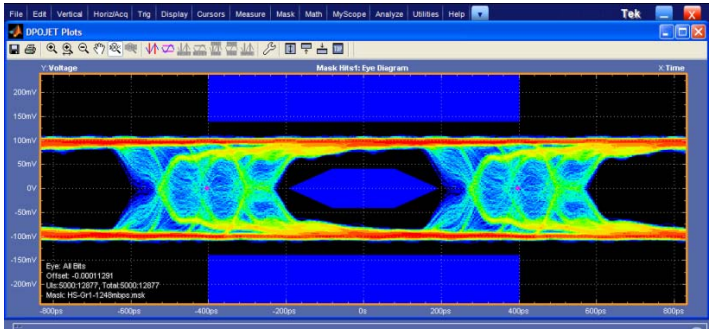


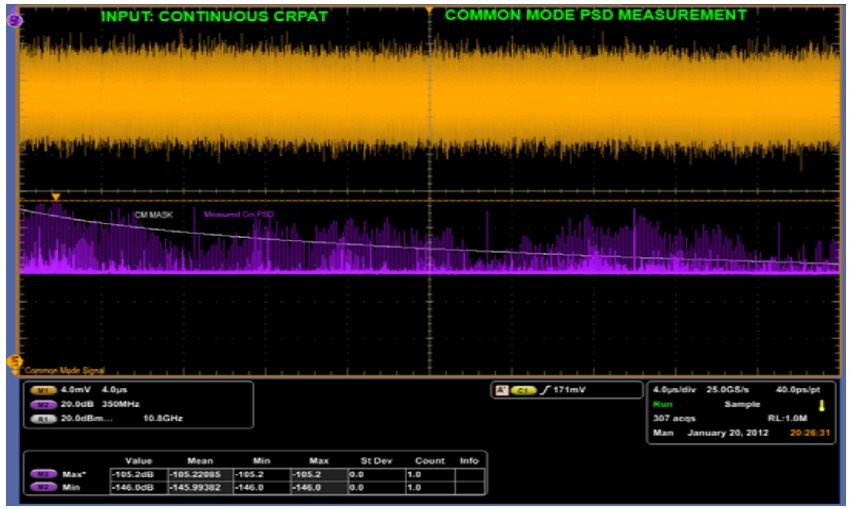
Common-Mode Limit

F, MHz	Limit, dBm/Hz
500	-109.9
1000	-119.8
1500	-125.6
2000	-129.7
2500	-132.9
3000	-135.5
3500	-137.7
≥4000	-139.6

Figure 34 Common-mode Power Spectral Magnitude Limit

Eye Diagram





PSD Spectrum using Scope Math

M-PHYTX performs both Time & Frequency Domain Tx Tests.

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M-PHY Tx : Opt.M-PHYTX Automation Features
Beyond Conformance Test, with Seamless-Debug

Key Feature	Benefit
Single-button Fully-Automated	• Automates **~1000 tests** in regression, in different combinations of Gears, Sub-Gears, Terminations, Amplitudes, etc • Significantly reduces testing time, and enables you to test devices faster
Seamless Debug	• User-Defined mode allows Pause on a Test while in Automation, and Switch to DPOJET Analysis Tool for Detailed Debug of failures
Highly Optimized Setup	• Performs Power Spectral Density (PSD) Tests using Oscilloscope-integrated Algorithms Uniquely, • Does not require an External Spectral Analyzer or Extra Hardware to Perform PSD Measurements
Most Complete Tests coverage	• Automates 95% of High Speed, and 75% of PWM tests • All HS Gears including Gear3, and all PWM Gears, and sub-Gears • Configure for Large/Small Amplitudes, Termination/Un-termination, etc
Multi-lane one-time Setup	• Connect upto 4-lanes of DUT to 4-channels on an oscilloscope, using differential mode of acquisition.
Single-Printable Test reports	• Provides Single Printable Report, across Different Combinations • Provides Pass/Fail Summary Table, along with Margin Details, Optional Waveform Captures, and Eye Diagrams

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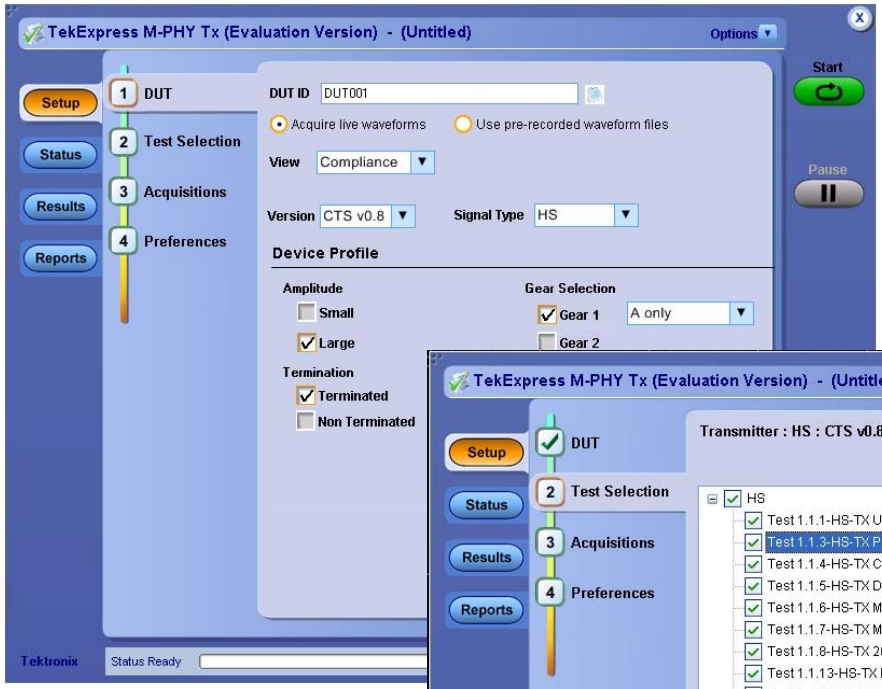
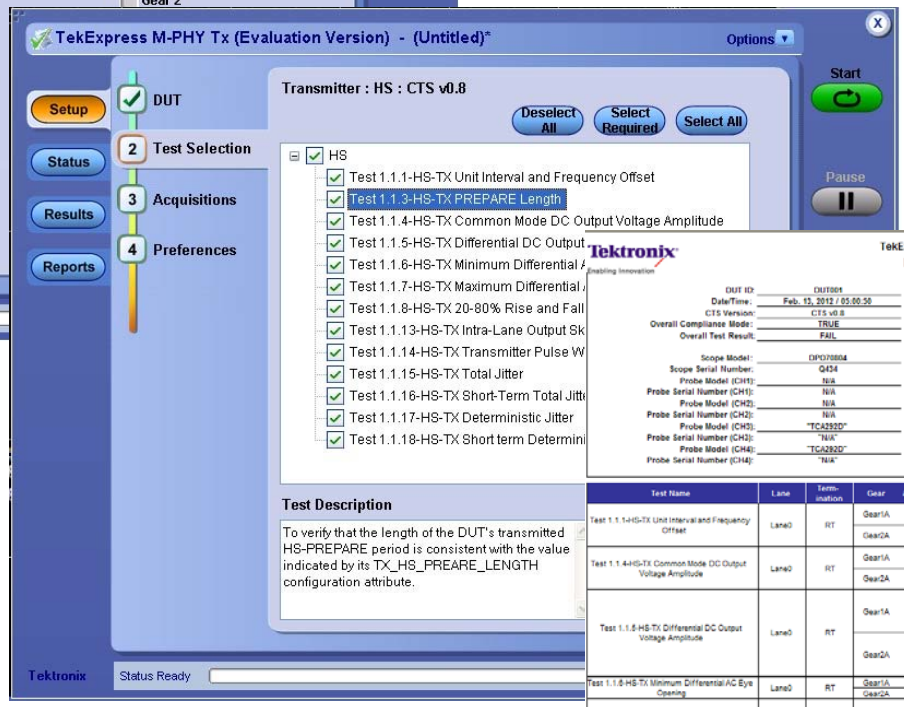
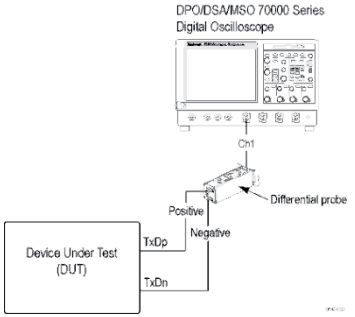
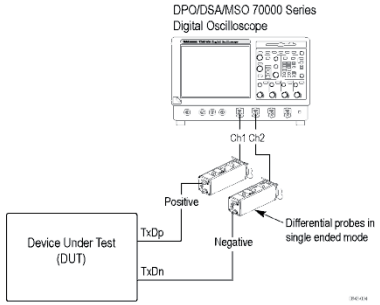
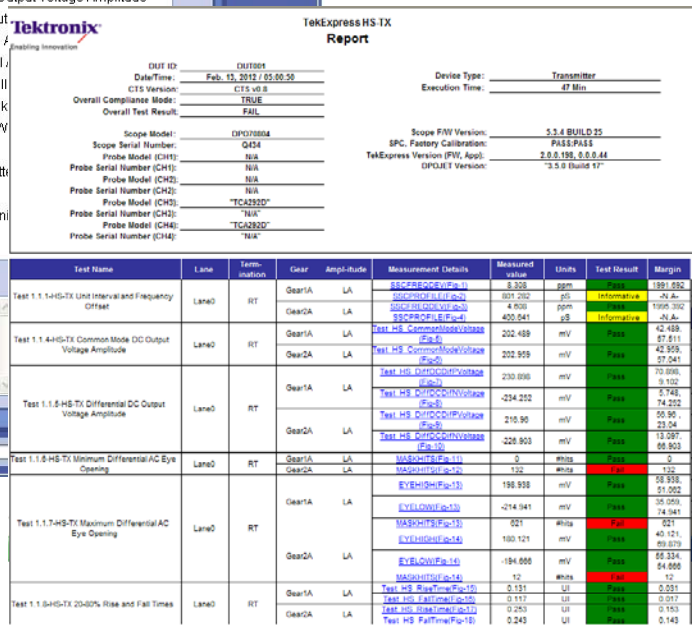
M-PHY Tx : Opt.M-PHYTX Automation Features











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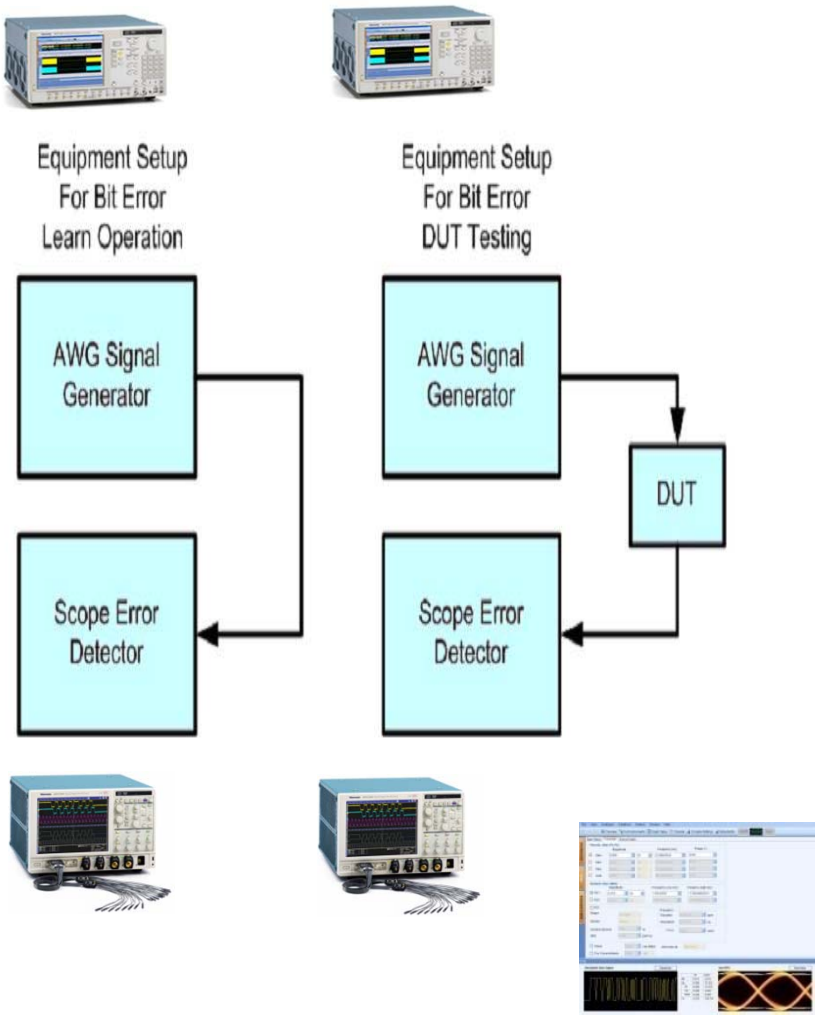
M-PHY Rx Test Automation



- Oscilloscope-based M-PHY BER with AWG as Pattern Source
- HS Gear 8b/10b Error Detect & Pat Gen:
  - Hardware Serial trigger: 1.25 Gb/s -6.25 Gb/s
  - BER covers PRBS 312Mbs+ data rates
- Testing Guidance in published Methods of Implementation

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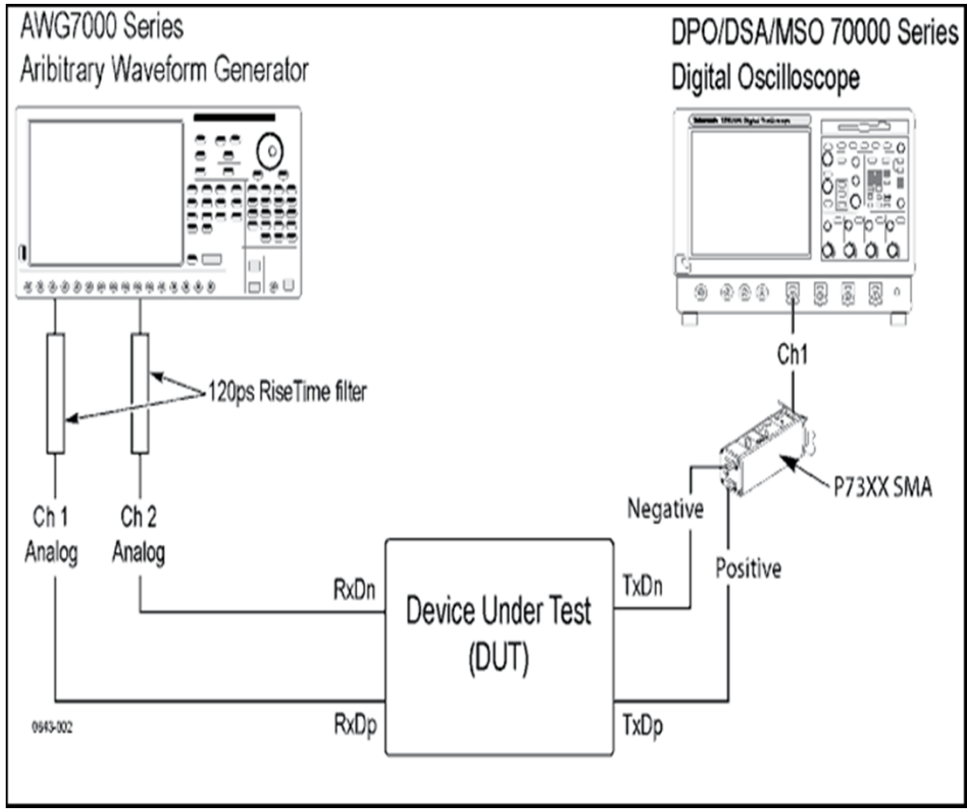
M-PHY Rx Testing

- Generation of M-PHY test pattern
- Signal input through ISI Compliance Channel
- Calibration
- Error Analysis



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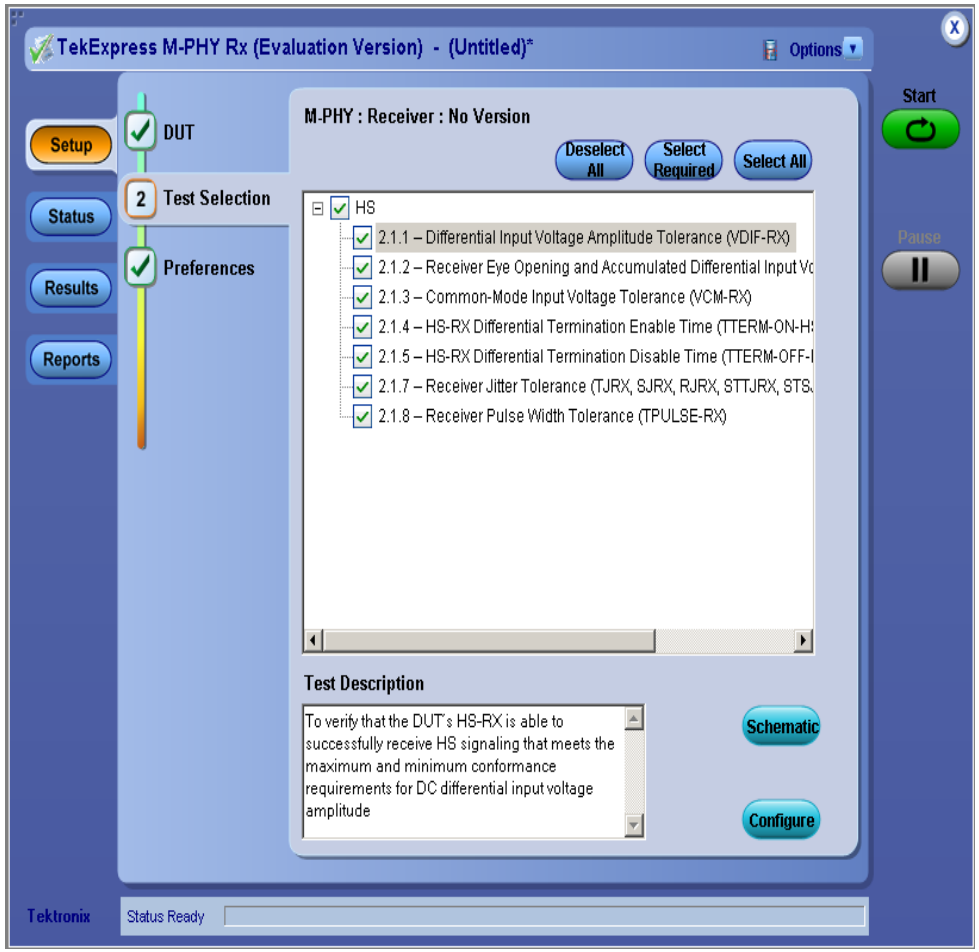
M-PHY Rx: Opt.M-PHYRX Automated Solution

- Opt.M-PHYRX
  - **Automated** Receiver Conformance test
  - Runs on a DPO/DSA70KB/C or MSO70K/C scope
- Differentiation
  - **Simply 2-box** setup.
  - **Scope ErrorDetector** ERRDT based
  - Wide HS Rx Tests coverage
- Value proposition
  - Test Reports with Pass/Fail summary, with Bit-Error counts



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M-PHY Rx: Opt.M-PHYRX Automation Features

Feature	Benefit
Automated Testing	• Reduces the complexity of executing receiver tests • Reduces testing time • Enables you to test devices faster
Tests coverage	• Automated test setup has comprehensive coverage of high speed Rx tests, with Pre-created patterns.
Simple setup	• Simple Scope+AWG setup for a complete Receiver as well as Transmitter testing of M-PHY. • Enables easy and quick setup, saves resource time and costs. • No other instrument is needed.
Integrated BER	• Leverages Bit-Error-Rate or Error-Counting using Scope-Integrated ERRDT. •Scope ERRDT testing supports PRBS 312Mbps &above for all Gears. • No external/ extra hardware is required to perform BER testing
Signal Validation	• Check the acquired signal for correct Data rate/ Unit-Interval, MARKER0 (both positive and negative disparity), or one complete CRPAT (LLI specific),
Test reports	• Provides a Pass/Fail summary for all tests. •-Provides additional details -Signal type, Bit Error, Execution time, etc

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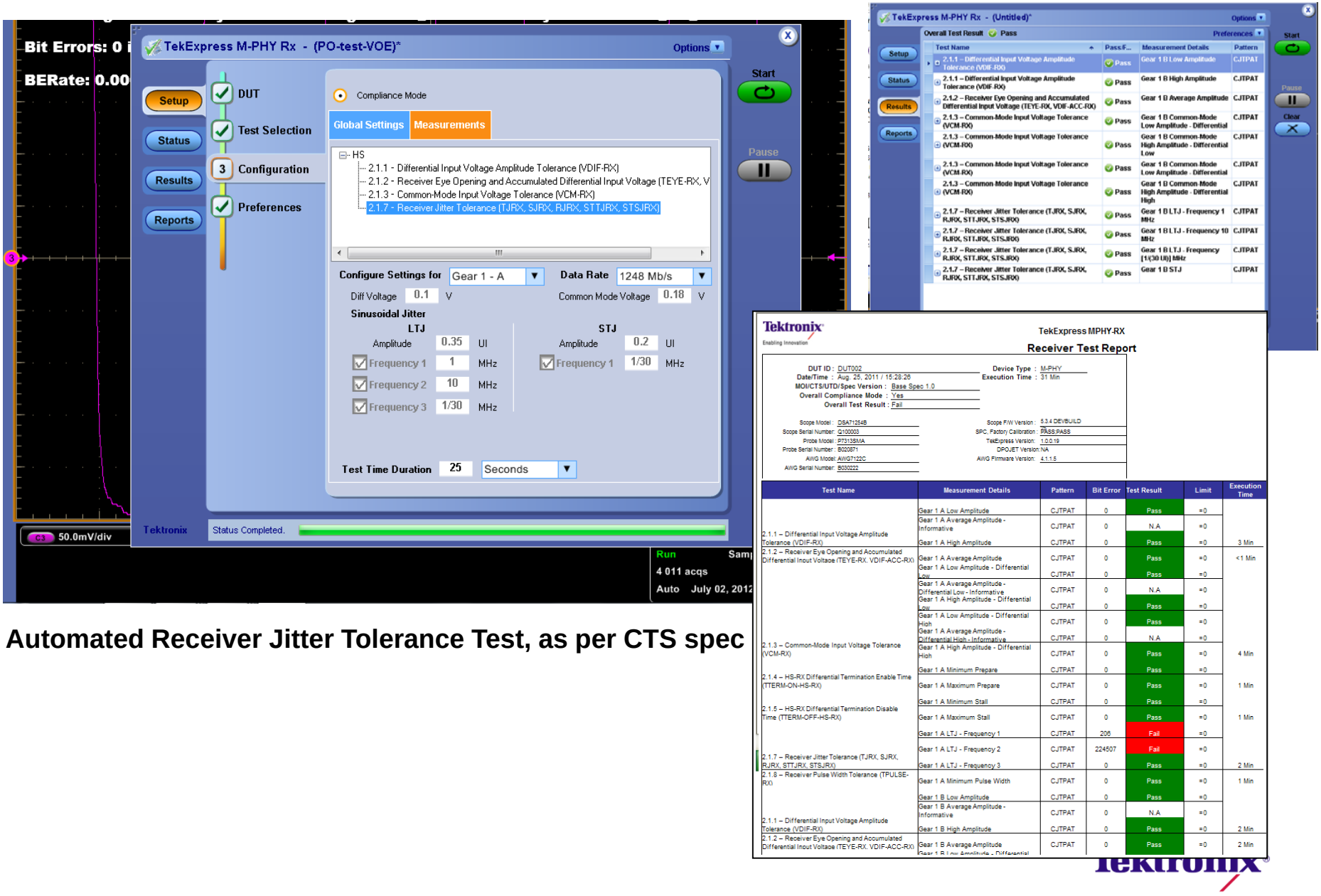
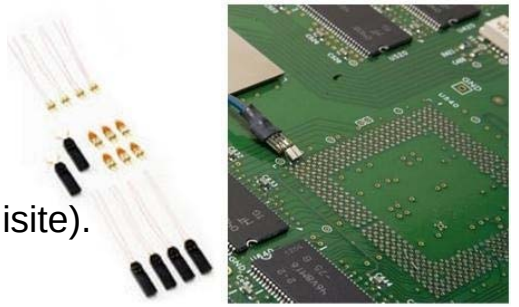
M-PHY Rx : Opt.M-PHYRX Automation Features



Automated Receiver Jitter Tolerance Test, as per CTS spec

M-PHY Tx &Rx Recommended Test Setup (www.Tek.com/MIPI)

- Oscilloscope
  - DPO70604/B/C or above, for HS-Gear1 Only (Tx &Rx).
  - DPO70804/B/C or above, for HS-Gear1&2 Only (Tx &Rx)
  - DPO71254/B/C or above, for All HS-Gears (Tx & Rx)
  - DPO72004/B/C or above, for All HS-Gears (Tx &Rx).
- Probes
  - 2x P75xx with P75LRST for Tx HS All Gears, or 2x P73xxSMA/P73xx for Tx HS up to Gears2.
  - 2x P73xxSMA/P73xx for Tx PWM All Gears.
  - 1x P73xxSMA for Rx.
- Signal Generator for Rx
  - AWG7082C, AWG7102 or above, for HS-Gear1 Only.
  - AWG7122C without Interleave, for HS-Gear1&2 Only.
  - AWG7122C with Interleave (option 06), for All HS-Gears.
- Software
  - Opt.M-PHYTX Transmitter Automated Solution (Opt.DJA is pre-requisite).
  - Opt.M-PHYRX Receiver Automation (Opt.ERRDT is pre-requisite).
  - PGY-UPRO Protocol Decode (Opt.ST6G optionally required).
  - PGY-LLI Protocol Decode (Opt.ST6G optionally required).
  - MPHYVIEW, for DigRFv4 Protocol Decode
  - Opt.SR-810B, for 8b-10b Decode
  - Optional: Opt.M-PHY Essentials for Customization (Opt.DJA is pre-required).
  - Optional: SerialXpress for custom-patterns using AWG



P7380 probe used with a probe-tip

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M-PHY Rx Recommended Test Setup – Continued

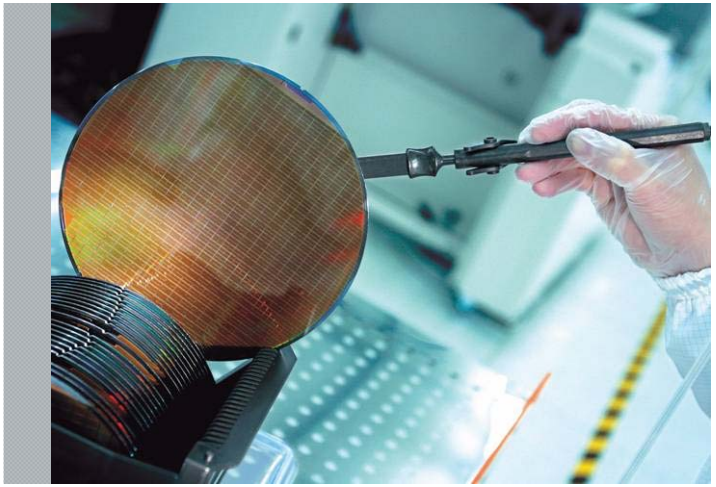
- Recommended Accessories, for opt.M-PHYRX Receiver Automation setup
  - 2x Matched pair of SMA cables
  - 1x GPIB Cable
  - 2x Rise Time Filter – 120 ps (part number 5915-121-120PS from Picosecond) with barrel connectors
- Optional: Accessories for Rx “custom-pattern generation” using SerialXpress, in manual setup
  - 2x Matched pair of SMA cables, , for AWG custom patterns creation
  - 2x Rise Time Filter – 120 ps (part number 5915-121-120PS from Picosecond) with barrel connectors
  - 2x BiasTee (part number 5542 from Pico Second), for AWG Interleave Option (for HS-Gear3)
  - 2x TCA-SMA Connectors, for AWG custom patterns creation
  - Option 01 –Memory expansion to 64 M enabled on AWG
  - Option 08 – Fast Sequence Switching enabled on AWG
  - Option 09 – Subsequence and Dynamic Jump enabled on AWG.

MODEL 5542
BIAS TEE

Picosecond
Pulse Labs

Tektronix®

Thank you



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