MIPI Physical Layer Test Solutions
D-PHY and M-PHY

Jong Bum, Kim
Application Engineer
Agenda

- MIPI® Technologies
- MIPI D-PHY Test Solutions
  - D-PHY Tx
  - D-PHY Rx
- MIPI M-PHY Test Solutions
  - M-PHY Tx
  - M-PHY Rx
- Summary, Q&A
What is MIPI and Why MIPI?
Drivers for Mobile Technologies

- **Feature set growing rapidly**
  - HD-Cameras, HD Displays, Touch screen, USB, etc.
  - Mobile-TV, WiMax/3G, WLAN, GSM/GPRS, GPS, FM, etc.
  - Numerous “new specialized parts” & suppliers

- **Bandwidths growing**
  - Need faster internal interconnect

- **Rising integration Time and Costs**
  - Need faster Time-To-Market
  - Need simplified system integration
  - Need “general-purpose” interfaces (like MIPI) to integrate diverse devices quickly
Neither UniPro v1.6 nor CSI-3 v1.1 have been officially released yet.

source: www.mipi.org
MIPI M-Phy, Protocol, Application Stackup with Combined Standards

Application

Protocol Standard

- PCI-SIG M-PCIe M.2 Rev. 0.7a
- USB-IF SSIC Rev. 1.01
- JEDEC UFS V1.1
- JEDEC UFS V2.0

Physical Standard

- M-PHY v2.0
- M-PHY v2.0
- M-PHY v2.0
- M-PHY v3.0

Neither UniPro v1.6 Nor UFS v2.0 have been officially released yet.

source: www.mipi.org
Tek Strategic Involvement with MIPI Alliance & UNH-IOL

- Tektronix is a **Contributor Member** of the MIPI Alliance
- Tektronix is actively-participating in several MIPI Working Groups
- Tektronix has a close working relationship with UNH-IOL.
- Combined Tek Press-Release with UNH & MIPI Alliance in Sept-2010:
  - [http://www2.tek.com/cmswpt/prdetails.lotr%3Fct%3DPR%26cs%3DNews%2BRelease%26ci%3D17639%26lc%3DEN&urlhash=HZu6](http://www2.tek.com/cmswpt/prdetails.lotr%3Fct%3DPR%26cs%3DNews%2BRelease%26ci%3D17639%26lc%3DEN&urlhash=HZu6)

- “.......Tektronix is spurring the adoption of D-PHY and M-PHY specifications. Tektronix is aiding the adoption of the new M-PHY interface by giving designers the testing tools they need to ensure signal integrity and verify performance of increasingly complex designs.”
  - **Joel Huloux, Chairman of the MIPI Alliance.**

- “Tektronix has been supportive of UNH-IOL's collaborative efforts……..,”
  - **Andy Baldman, Senior technical staff, R&D, UNH-IOL.**
MIPI Display Serial Interface-DSI

- **What is MIPI DSI?**
  - DSI is the specification for Processor-to-Display interconnect

- **Legacy Standards in a Mobile**
  - Parallel busses with 45-50 signals

- **MIPI DSI-1**
  - A Serial bus with Just 8-10 signals
  - Physical layer is D-PHY and Protocol layer is DSI-1

- **MIPI DSI-2**
  - Physical layer is M-PHY & Protocol layer is DSI-2
  - Backward Compatible to DSI-1
MIPI Camera Serial Interface CSI-2

- What is MIPI CSI?
  - CSI is the specification for Processor-to-Camera interconnect

- Legacy Standards in a Mobile
  - Parallel busses with 20-36 signals

- MIPI CSI-2
  - A Serial bus with Just 8-10 signals
  - Physical layer is D-PHY and Protocol layer is CSI-2

- MIPI CSI-3
  - Physical layer is M-PHY & Protocol layer is CSI-3
  - Backward Compatible to CSI-2
MIPI D-PHY Functionality

- PHY standard for interfacing Camera (CSI) & Display (DSI)
- Synchronous connection between Master and Slave
- D-PHY Configuration
  - One clock signal
  - One or more data signals (Maximum 4-Lanes)
- Two modes of transmission

<table>
<thead>
<tr>
<th>High-Speed (HS) mode</th>
<th>Low-Power (LP) mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Data Rate : 80 Mbps – 1.5 Gbps</td>
<td>• Data Rate : Up to 10 Mbps</td>
</tr>
<tr>
<td>Typically at ~500 Mbps</td>
<td>• Bus Termination : Hi-Z</td>
</tr>
<tr>
<td>• Bus Termination : 50 ohms</td>
<td>• Signal : 1.2V CMOS Level,</td>
</tr>
<tr>
<td>• Signal : 360mV (Max: $V_{OHHS}$)</td>
<td>Single ended</td>
</tr>
<tr>
<td>Differential</td>
<td>• For control purposes</td>
</tr>
<tr>
<td>• For fast-data traffic</td>
<td></td>
</tr>
</tbody>
</table>

- Modes are mixed during the operation
  - Transitions from LP to HS and back to LP on the fly
MIPI D-PHY Lane States and Line Levels

- **Lane States**
  - Low-Power Lane states: LP-00, LP-01, LP-10, LP-11
  - High Speed Lane states: HS-0, HS-1

- **Line Levels (Typical)**
  - LP High Level: 0~1.2V
  - HS Common mode Voltage: 200mV
  - HS Differential Voltage: 200mV
MIPI D-PHY Configuration

A MIPI D-PHY Link includes:
- Clock lane: 1
- Data lane: 1~4

-> all lanes are differential

Two-Data lanes MIPI D-PHY Link
D-PHY Tx : Opt.D-PHYTX Conformance Test Solution

  - TekExpress option for Fully-Automated testing
  - Provides Conformance and Characterization Testing
  - Based on Latest D-PHY Base Spec v1.1 and UNH’s Conformance Test Suite v1.0.
  - Runs on 7K/C and 70K/B/C scopes
  - Opt.TEKEXP is Pre-Requisite

- Differentiation
  - Un-parallel Automation (Auto-Cursors)
  - 100% Widest Test Coverage
  - Conformance to Latest CTS (v1.0)
  - Based on Latest Base spec (v1.1)
  - Fully-Automated for Multi-lane DUTs
  - Fully-Automated Temperature Chamber

- Value proposition
  - Custom-limits/ Limits-Editing
  - Test Reports with Pass/Fail summary, margins, & "Zoom-in" Waveform Captures
  - Tek 3.5GHz scope is the minimal configuration for accurate testing
  - D-PHY extension spec (1.5G) ready
## D-PHY Tx Test Items

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<th>Group 4</th>
<th>Clock Lane HS-TX Signaling</th>
</tr>
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<td>Clock Lane HS Entry: TLPX Value</td>
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<td>1.4.2</td>
<td>Clock Lane HS Entry: TCLK-PREPA Value</td>
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<td>1.4.3</td>
<td>Clock Lane HS Entry: TCLK-PREPA + TZERO Value</td>
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<tr>
<td>1.4.4</td>
<td>Clock Lane HS TX Differential Voltages: VOD(0), VOD(1)</td>
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<td>1.4.5</td>
<td>Clock Lane HS-TX Differential Voltage Mismatch</td>
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<td>1.4.6</td>
<td>Clock Lane HS-TX Single Ended Output High Voltages: VDI(0), VDI(1), VDI(2), VDI(3)</td>
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<td>1.4.7</td>
<td>Clock Lane HS-TX Common-Mode Voltages: VCMTX(0), VCMTX(1)</td>
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<td>1.4.8</td>
<td>Clock Lane HS-TX Common-Mode Voltage Mismatch: VCMTX(1)</td>
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<td>1.4.9</td>
<td>Clock Lane HS-TX Dynamic Common-Level Variations Between 50-50 MHz: VCMTX(0), VCMTX(1)</td>
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<td>1.4.10</td>
<td>Clock Lane HS-TX Dynamic Common-Level Variations Above 25 MHz: VCMTX(0)</td>
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<td>1.4.11</td>
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<td>1.4.12</td>
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<td>1.4.14</td>
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<td>1.4.15</td>
<td>Clock Lane HS Exit: TST-EOT Value</td>
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<td>1.4.16</td>
<td>Clock Lane HS Exit: TBL-EOT Value</td>
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<td>1.4.17</td>
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<th>HS-TX Clock-to-Data Lane Timing</th>
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<td>1.5.3</td>
<td>HS Clock Rising Edge Alignment to First Payload Bit</td>
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<td>1.5.4</td>
<td>Data-to-Clock Skew (TSKEW (TX))</td>
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</table>

<table>
<thead>
<tr>
<th>Group 6</th>
<th>Data Lane HS-TX Signaling</th>
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</thead>
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<tr>
<td>1.6.1</td>
<td>Data Lane HS Entry: Data Lane TLPX Value</td>
</tr>
<tr>
<td>1.6.2</td>
<td>Data Lane HS Entry: TCLK-PREPA Value</td>
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<td>1.6.3</td>
<td>Data Lane HS Entry: TCLK-PREPA + TZERO Value</td>
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<tr>
<td>1.6.4</td>
<td>Data Lane HS-TX Differential Voltages: VOD(0), VOD(1)</td>
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<tr>
<td>1.6.5</td>
<td>Data Lane HS-TX Dynamic Common-Level Variations Between 50-50 MHz: VCMTX(0), VCMTX(1)</td>
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<tr>
<td>1.6.6</td>
<td>Data Lane HS-TX Dynamic Common-Level Variations Above 25 MHz: VCMTX(0)</td>
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<tr>
<td>1.6.7</td>
<td>Clock Lane HS-TX 20%-80% Rise Time (RI)</td>
</tr>
<tr>
<td>1.6.8</td>
<td>Clock Lane HS-TX 20%-80% Fall Time (RF)</td>
</tr>
<tr>
<td>1.6.9</td>
<td>Clock Lane HS Exit: TST-TRAIL Value</td>
</tr>
<tr>
<td>1.6.10</td>
<td>Clock Lane HS Exit: TST-EOT Value</td>
</tr>
</tbody>
</table>

### Probes connection for Data/CLK Lanes

![Diagram of Probes connection for Data/CLK Lanes](attachment:image.png)
D-PHY Tx : Recommended Test Setup

www.tek.com/MIPI

- **Scope**
  - DPO7354 or DPO/DSA/MSO70404/B/C or higher for rise time accuracies
- **Probes**
  - For 7Ks: 4x TAPxx/ P6245/ P6249, or 4x TDP3500 (clock is non-continuous), or 3x TDP3500 (clock is continuous).
  - For 70Ks: 4xP7240, or 4xP73xx (clock is non-continuous), or 3xP73xx (clock is continuous).
- **Scope Software**
  - Opt. D-PHYTX on TEKEXP for Conformance Test
- **Fixtures**
  - As MIPI is a chip-to-chip interface, most DUT setups are LIVE with Master-Slave/Receiver-end connected.
  - For live-setups: No Fixtures required.
  - For non-live setups:
    - No standard fixture is defined.
    - We recommend following UNH-IOL Termination boards: [www.iol.unh.edu/services/testing/mipi/MIPI_Test_Fixture_Order_Form.doc](http://www.iol.unh.edu/services/testing/mipi/MIPI_Test_Fixture_Order_Form.doc)
Stimulus Setup

- TLA or PC
  - PGRemote
  - PGApp
  - USB

- P332
- Or
- P338
- Probe

- DHPYPRE Preprocessor

- TLA

- System Under Test
Stimulus

- **Protocol Testing** – Stimulating buses with known good data packets or packets with intentional errors tests the system's adherence to a specified protocol.

- **Infrequent Events** - System bugs that only appear when infrequent events occur can be quickly reproduced with a pattern generator by repeatedly stimulating the system with the key external event.

- **Automated Test** – Production line test setups can utilize the PG3A as a general purpose digital I/O source with a large number of channels.
P332 MIPI D-PHY Probe for PG3A

Key Features

- MIPI D-PHY Probe for use with PG3AMOD and PG3ACAB
- Generate CSI2 and DSI data over D-PHY
- 4-Data Lanes and 1-Clock lane
- 1.5Gbps / Lane data rate
- SMA outputs for each lane
- LP and HS Voltage and Timing adjustable on a each lane separately
# D-PHY Rx : Test Solution Overview

## 100% Test Coverage

### Group 1 LP - RX voltage and timing requirements

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<th>Title</th>
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<th>Equipment</th>
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<td>2.1.1</td>
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<td>2.1.3</td>
<td>LP - RX Logic 0 Input Voltage, ULP State ($V_{in}$)</td>
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<td>2.1.5</td>
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### Group 2 LP - RX Behavioral Requirements

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<td>2.2.2</td>
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<td>2.2.4</td>
<td>Data Lane LP - RX Invalid Aborted Escape Mode Entry</td>
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<td>2.2.5</td>
<td>Data Lane LP - RX Invalid Aborted Escape Mode Command</td>
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<td>2.2.7</td>
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<td>Data Lane LP - RX Escape Mode Unsupported Unassigned Commands</td>
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### Group 3 HS - RX Voltage and Setup/Hold Requirements

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<th>Equipment</th>
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<tbody>
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<td>2.3.1</td>
<td>HS - RX Common Mode Voltage Tolerance ($V_{nom}$)</td>
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<tr>
<td>2.3.2</td>
<td>HS-CX Differential Input High Threshold ($V_{hi}$)</td>
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<td>PG</td>
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<td>2.3.3</td>
<td>HS-CX Differential Input Low Threshold ($V_{lo}$)</td>
<td>143</td>
<td>PG</td>
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<td>2.3.4</td>
<td>HS - RX Single-Ended Input High Voltage ($V_{nom}$)</td>
<td>144</td>
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<tr>
<td>2.3.5</td>
<td>HS - RX Single-Ended Input Low Voltage ($V_{nom}$)</td>
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<tr>
<td>2.3.6</td>
<td>HS - RX Common Mode Interface 50MHz - 460MHz (data VCMRX(LF))</td>
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<td>2.3.7</td>
<td>HS - RX Common Mode Interface Beyond 460MHz (data VCMRX(HF))</td>
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<td>HS - RX Setup-Hold and Jitter Tolerance</td>
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</table>

### Group 4 HS - RX Timer Requirements

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</thead>
<tbody>
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<td>Data Lane HS - RX $T_{nom}$ Value</td>
<td>156</td>
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<td>2.4.2</td>
<td>Data Lane HS - RX $T_{nom}$ $T_{tol}$ Tolerance</td>
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<td>2.4.5</td>
<td>Data Lane HS - RX $T_{nom}$ Value</td>
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<td>2.4.7</td>
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<tr>
<td>2.4.8</td>
<td>Clock Line HS - RX $T_{nom}$ $T_{tol}$ Tolerance</td>
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<td>2.4.9</td>
<td>Clock Line HS - RX $T_{nom}$ Value</td>
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<td>PG</td>
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<td>2.4.10</td>
<td>Clock Line HS - RX $T_{nom}$ $T_{tol}$ Tolerance</td>
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<td>PG</td>
</tr>
</tbody>
</table>

[tektronix logo]
D-PHY Rx : Test Solution Overview

Manual/ Workaround Setup based on PG with PGRemote Software

Simple, Quick, Easy and Re-usable

- **100% Coverage to Rx CTS**
  - Meets all the requirements in UNH-IOL CTS document (v1.0)

- **Quick and Easy setup**
  - No complex VXI system, just stand alone instruments, and a probe.

- **Cost effective solution**
  - 70% Lower list price vs Competition

- **Re-usable for Protocol tests**
  - PG3A is the Only 4 channel solution for CSI &DSI test

- **PG3A Pattern Generator**
  - Controls clock and signaling to establish link with DUT
  - Adjusts voltage levels, packet type, etc to stress test receiver

- **AWG7082C with Coupler**
  - Adds jitter and interference to the D-PHY signals
  - Needed only for 6 out of 35 total Rx tests.

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**Manual Setup**

![Diagram of manual setup with components: PG3ACAB, AWG7082C, D-PHY Coupler, P332 Probe, PGRemote Software, DUT.]

*These Moving Pixel products are available as Tektronix part number
**Tektronix part number not available.
PGRemote

- **Push Button User interface** to generate CSI2 or DSI vectors and probe control
- Adjust **frequency, voltage** and **delay** in HS and LP modes
- Adjust D-PHY state timing parameters
- Adjust **frame timing** and generate **looping video**
- Enter and exit Low power states
- Create **custom commands, Macros** and assign them to buttons
- Save restore a configuration
- Ability to use P332 as a generic high-speed serial probe
- The PG can be operated in several modes
  - Pushbutton Mode using the PGRemote software
  - Macro Mode using the PGRemote software
  - Scripting
  - Full remote control mode
PGRemote
Push Button Interface to generate CSI2 / DSI Vectors

PGRemote Main Window

Define CSI/DSI commands and arguments

Configuration Parameters for PG playback, and D-PHY

Status Bar

Command Buttons

PG, probe status and operational controls
CSI2/DSI Protocol validation

Solution Overview

D-PHY Preprocessor

P6982 or P6980 Probe

USB Cable For Control

D-PHY Preprocessor

Clk

Data (up to 4 Lanes)
D-PHY Preprocessor

- Support **1.5Gbps** per lane
- Support for **up to 4 Lanes** of D-PHY data
- Color coded solder down probes for easy identification
- Support **CSI2/DSI Protocols**
- Advanced Packet Level **Triggering**
- **Real Time Filtering**
- Lane activity and Error Status
- Simultaneous Low Power and High Speed Data Acquisition
- **8x improvement** in TLA Memory usage
- **Image Export**
- Compatible with both TLA6k and TLA7k

Preserve your investment with the ONLY 4 lane, 1.5Gbps protocol solution in the market.
D-PHY Preprocessor control UI

- Preprocessor Configuration
  - MIPI Standard
  - Max Lane Count
  - Delta Timeout
  - SLK freq (MHz)
  - HCLK Adjust (ps)

- Trigger & Filter Definitions
  - Trigger PickTypes
  - Set All
  - Clear All
  - Check All

- Status Area
  - Lane Activity
  - Trigger Status
  - Error Status
D-PHY Decode

- Supports from 1 to 4 lanes of D-PHY data
- Decode and Display
  - All LP and HS state transitions
  - LP commands and data
  - LP and HS Data in Byte Format
  - All types of Short and Long packets
  - DCS Command decode
- Supports different RGB and YUV Schemes
- Supports ECC and Checksum verification.
- selectively view the decoded information at different levels of hierarchy
- Packets extracted & stored for further analysis
# System Configuration

## Protocol Decode

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<th>Option - 2</th>
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<td>DPHYPRE (1ea)</td>
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<tr>
<td>P6982 (2ea)</td>
<td>P6980 (1ea)</td>
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<td>TLA6K or TLA7ACx (1ea)</td>
<td>TLA7BBx (1ea)</td>
</tr>
<tr>
<td>TLA7012/TLA7016 (1ea)</td>
<td>TLA7012/TLA7016 (1ea)</td>
</tr>
<tr>
<td>For use with TLA7ACx</td>
<td>For use with TLA7BBx</td>
</tr>
</tbody>
</table>

## Stimulus

<table>
<thead>
<tr>
<th>Option - 1</th>
<th>Option - 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG3AMOD (1ea)</td>
<td>PG3ACAB (1ea)</td>
</tr>
<tr>
<td>P332 (1ea)</td>
<td>P332 (1ea)</td>
</tr>
<tr>
<td>PGRremoteSW (1ea)</td>
<td>PGRremoteSW (1ea)</td>
</tr>
<tr>
<td>TLA7012/TLA7016 (1ea)</td>
<td>TLA7012/TLA7016 (1ea)</td>
</tr>
<tr>
<td>For use with PG3AMOD</td>
<td>For use with PG3AMOD</td>
</tr>
</tbody>
</table>
MIPI Solutions and Techniques

- Oscilloscope
  - Signal Integrity
  - D-PHY Physical Layer Test

- Logic Analyzer (LA)
  - Validation and debug of the MIPI Protocol

- Pattern Generator (PG)
  - MIPI Signal Generation
  - Stimulating Driver ICs, Devices and Processors

- Oscilloscope, Logic Analyzer and Pattern Generator
  - System level Validation & Debug
  - Testing fully integrated mobile handset platforms
What is M-PHY?

- M-PHY is a **Common** Electrical Spec for
  - DigRFv4, UniPro, LLI, HSI, CSI-3 and DSI-2 protocols of the **MIPI Alliance**.
  - SSIC (Super Speed Inter Connect) protocol of **USB-IF**.
  - UFS (Universal Flash Storage) protocol of **JEDEC**.
  - MPCIe – PCIe protocol on M-PHY
- Supports high data rates at Minimal power, Cost & I/O redesign
- For High Definition Video capture/ transmission in a mobile phone, etc.
MIPI M-PHY Configuration

- M-PHY Operates as
  - Link: is made up of two SUBLINKs
  - Sub-link: Containing one or more LANES
  - Lane: Consists of an M-PHY transmit MODULE (M-TX), an M-PHY receiver MODULE (M-RX), and a LINE
    - unidirectional point-to-point differential serial connection between PINs
  - Line: the point-to-point interconnect between the M-TX and M-RX
M-PHY Signal Characteristics

<table>
<thead>
<tr>
<th>Signaling Mode</th>
<th>Data-rates</th>
<th>Amplitudes</th>
<th>Impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Gears</td>
<td>A (Gbps)</td>
<td>B (Gbps)</td>
</tr>
<tr>
<td>High Speed (HS)</td>
<td>G1</td>
<td>1.25</td>
<td>1.45</td>
</tr>
<tr>
<td></td>
<td>G2</td>
<td>2.5</td>
<td>2.91</td>
</tr>
<tr>
<td></td>
<td>G3</td>
<td>5</td>
<td>5.83</td>
</tr>
<tr>
<td>PWM (ie. TYPE-I)</td>
<td>G0</td>
<td>0.01</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>G1</td>
<td>3</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>G2</td>
<td>6</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td>G3</td>
<td>12</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>G4</td>
<td>24</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>G5</td>
<td>48</td>
<td>144</td>
</tr>
<tr>
<td></td>
<td>G6</td>
<td>96</td>
<td>288</td>
</tr>
<tr>
<td></td>
<td>G7</td>
<td>192</td>
<td>576</td>
</tr>
</tbody>
</table>

Terminated: 160-240mV, Non-Terminated: 320-480mV
M-PHY Bit Signaling Schemes

- Two signaling Schemes
  - Non-Return-to-Zero (NRZ)
    - HS-Burst
    - SYS-Burst
  - Pulse-Width-Modulation (PWM) Signaling
    - Self-clocking
    - PWM-Burst
M-PHY Tx Testing

Transmitter Testing
Oscilloscope

<table>
<thead>
<tr>
<th>HS Gear</th>
<th>Max Datarates</th>
<th>Oscilloscope Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>G1</td>
<td>1.45 Gb/s</td>
<td>5 GHz</td>
</tr>
<tr>
<td>G2</td>
<td>2.9 Gb/s</td>
<td>10 GHz</td>
</tr>
<tr>
<td>G3</td>
<td>5.83 Gb/s</td>
<td>20 GHz</td>
</tr>
</tbody>
</table>

Probing/Connectivity
- 2 ea. High-Impedance, Low-Capacitive-Load Differential Probes
- 1 ea. M-PHY 100Ohm Terminated-Mode Test Fixture
- 1 ea. M-PHY Unterminated-Mode Test Fixture
M-PHY Tx : Opt.M-PHYTX Automated Solution
Beyond Conformance Test, with Seamless-Debug

- **Opt.M-PHYTX**
  - **Single-button Fully-Automated** Transmitter Test Solution
  - Provides Conformance Test & Debug Analysis to Base Spec v1.0 & UNH's CTS.
  - Runs on a DPO/DSA70KB/C/D or MSO70K/C scope (6GHz and above)
  - Opt.DJA is pre-requisite. Opt.M-PHY not required. (Based on TekExpress 2.0.)

- **Differentiation**
  - **Seamless Debug** on Failures, & User-Defined mode
  - **Scope-based PSD** Power-Spectral Density tests
  - **Most Complete** Test coverage.
    - (95% HS all Gears, 74% PWM all Gears).
  - **Multi-lane** one-time Setup (Diff Acquisition mode)
  - Tek is **Industry 1st** in M-PHY Test, since Sept, 2010

- **Value Proposition**
  - For Gear2 M-PHY Tx testing, **Tek 8GHz oscilloscope is sufficient**. Where as, both competition requires a 12GHz or 13GHz oscilloscope setup.
  - For Gear3 M-PHY Tx testing, **Tek 20G oscilloscope is sufficient**. Where as, both competition requires a 25GHz oscilloscope setup.
M-PHY Tx: Opt.M-PHYTX Automation Features

Oscilloscope based Power Spectral Density (PSD), Eye Diagram

**Power Spectral Density**

<table>
<thead>
<tr>
<th>Frequency, MHz</th>
<th>Limit, dBm/Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>500</td>
<td>-109.9</td>
</tr>
<tr>
<td>1000</td>
<td>-119.9</td>
</tr>
<tr>
<td>1500</td>
<td>-125.6</td>
</tr>
<tr>
<td>2000</td>
<td>-129.7</td>
</tr>
<tr>
<td>2500</td>
<td>-133.9</td>
</tr>
<tr>
<td>3000</td>
<td>-135.6</td>
</tr>
<tr>
<td>3500</td>
<td>-137.7</td>
</tr>
<tr>
<td>4000</td>
<td>-139.6</td>
</tr>
</tbody>
</table>

**Common-mode Power Spectral Magnitude Limit**

**Eye Diagram**

**PSD Spectrum using Scope Math**

M-PHYTX performs both Time & Frequency Domain Tx Tests.
# M-PHY Tx : Opt.M-PHYTX Automation Features Beyond Conformance Test, with Seamless-Debug

<table>
<thead>
<tr>
<th>Key Feature</th>
<th>Benefit</th>
</tr>
</thead>
</table>
| Single-button Fully-Automated      | • Automates ~1000 tests in regression, in different combinations of Gears, Sub-Gears, Terminations, Amplitudes, etc  
• Significantly reduces testing time, and enables you to test devices faster |
| Seamless Debug                     | • User-Defined mode allows Pause on a Test while in Automation, and Switch to DPOJET Analysis Tool for Detailed Debug of failures |
| Highly Optimized Setup             | • Performs Power Spectral Density (PSD) Tests using Oscilloscope-integrated Algorithms Uniquely,  
• Does not require an External Spectral Analyzer or Extra Hardware to Perform PSD Measurements |
| Most Complete Tests coverage       | • Automates 95% of High Speed, and 75% of PWM tests  
• All HS Gears including Gear3, and all PWM Gears, and sub-Gears  
• Configure for Large/Small Amplitudes, Termination/Un-termination, etc |
| Multi-lane one-time Setup          | • Connect upto 4-lanes of DUT to 4-channels on an oscilloscope, using differential mode of acquisition. |
| Single-Printable Test reports      | • Provides Single Printable Report, across Different Combinations  
• Provides Pass/Fail Summary Table, along with Margin Details, Optional Waveform Captures, and Eye Diagrams |
M-PHY Tx : Opt.M-PHYTX Automation Features
M-PHY Rx Test Automation

- Oscilloscope-based M-PHY BER with AWG as Pattern Source
- HS Gear 8b/10b Error Detect & Pat Gen:
  - Hardware Serial trigger: 1.25 Gb/s -6.25 Gb/s
  - BER covers PRBS 312Mbs+ data rates
- Testing Guidance in published Methods of Implementation
M-PHY Rx Testing

- Generation of M-PHY test pattern
- Signal input through ISI Compliance Channel
- Calibration
- Error Analysis
M-PHY Rx: Opt.M-PHYRX Automated Solution

- **Opt.M-PHYRX**
  - **Automated** Receiver Conformance test
  - Runs on a DPO/DSA70KB/C or MSO70K/C scope

- **Differentiation**
  - **Simply 2-box** setup.
  - **Scope ErrorDetector** ERRDT based
  - Wide HS Rx Tests coverage

- **Value proposition**
  - Test Reports with Pass/Fail summary, with Bit-Error counts
# M-PHY Rx: Opt.M-PHYRX Automation Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefit</th>
</tr>
</thead>
</table>
| Automated Testing     | • Reduces the complexity of executing receiver tests  
                       • Reduces testing time  
                       • Enables you to test devices faster                                                                 |
| Tests coverage        | • Automated test setup has comprehensive coverage of high speed Rx tests, with Pre-created patterns.        |
| Simple setup          | • Simple Scope+AWG setup for a complete Receiver as well as Transmitter testing of M-PHY.  
                       • Enables easy and quick setup, saves resource time and costs.  
                       • No other instrument is needed.                                                                 |
| Integrated BER        | • Leverages Bit-Error-Rate or Error-Counting using Scope-Integrated ERRDT.  
                       • Scope ERRDT testing supports PRBS 312Mbps &above for all Gears.  
                       • No external/ extra hardware is required to perform BER testing |
| Signal Validation     | • Check the acquired signal for correct Data rate/ Unit-Interval, MARKER0 (both positive and negative disparity), or one complete CRPAT (LLI specific), |
| Test reports          | • Provides a Pass/Fail summary for all tests.  
                       • Provides additional details -Signal type, Bit Error, Execution time, etc                        |
M-PHY Rx : Opt.M-PHYRX Automation Features

Automated Receiver Jitter Tolerance Test, as per CTS spec
M-PHY Tx & Rx Recommended Test Setup (www.Tek.com/MIPI)

- Oscilloscope
  - DPO70604/B/C or above, for HS-Gear1 Only (Tx & Rx).
  - DPO70804/B/C or above, for HS-Gear1&2 Only (Tx & Rx)
  - DPO71254/B/C or above, for All HS-Gears (Tx & Rx)
  - DPO72004/B/C or above, for All HS-Gears (Tx & Rx).

- Probes
  - 2x P75xx with P75LRST for Tx HS All Gears, or 2x P73xxSMA/P73xx for Tx HS up to Gears2.
  - 2x P73xxSMA/P73xx for Tx PWM All Gears.
  - 1x P73xxSMA for Rx.

- Signal Generator for Rx
  - AWG7082C, AWG7102 or above, for HS-Gear1 Only.
  - AWG7122C without Interleave, for HS-Gear1&2 Only.
  - AWG7122C with Interleave (option 06), for All HS-Gears.

- Software
  - MPHYVIEW, for DigRFv4 Protocol Decode
  - Opt.SR-810B, for 8b-10b Decode
  - Optional: SerialXpress for custom-patterns using AWG
M-PHY Rx Recommended Test Setup  – Continued

- **Recommended Accessories, for opt.M-PHYRX Receiver Automation setup**
  - 2x Matched pair of SMA cables
  - 1x GPIB Cable
  - 2x Rise Time Filter – 120 ps (part number 5915-121-120PS from Picosecond) with barrel connectors

- **Optional: Accessories for Rx “custom-pattern generation” using SerialXpress, in manual setup**
  - 2x Matched pair of SMA cables, for AWG custom patterns creation
  - 2x Rise Time Filter – 120 ps (part number 5915-121-120PS from Picosecond) with barrel connectors
  - 2x BiasTee (part number 5542 from Pico Second), for AWG Interleave Option (for HS-Gear3)
  - 2x TCA-SMA Connectors, for AWG custom patterns creation
  - Option 01 – Memory expansion to 64 M enabled on AWG
  - Option 08 – Fast Sequence Switching enabled on AWG
  - Option 09 – Subsequence and Dynamic Jump enabled on AWG.
Thank you