TDR Techniques for Characterization and Modeling of Electronic Packaging

TDR Measurements

Time Domain Reflectometry (TDR) has traditionally been used as the key measurement technology for electrical characterization of electronic packages. Theory of TDR measurement can be found in [1], a number of papers and application materials on electrical characterization of packages has been published (for example, [2], [3]), and guidelines for use of TDR for package lumped parameter extraction have been standardized by the Joint Electron Device Engineering Council (JEDEC) in [4] as early as 1994. A typical TDR measurement setup is shown in Figure 1.
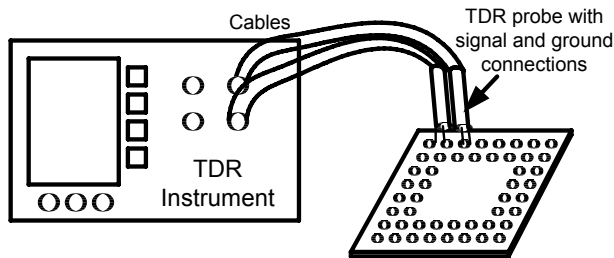

Figure 1. Typical package characterization setup

TDR is a very visual and intuitive modeling methodology; it is easier understood and accepted by digital designers. The intuitiveness of TDR has resulted in its wide acceptance for interconnect measurements and modeling work in general, and specifically for electrical modeling of packages. Package modeling techniques using TDR can be easily extended for characterization of other electrically short structures, such as connectors, sockets and multichip modules (MCMs).

Some of the advantages of TDR-based modeling over the frequency domain methodologies is that TDR allows the designer to obtain both lumped as well as distributed SPICE and IBIS models for the package interconnect that will closely correlate to the physical layout of the package (Figure 2).

Frequency domain modeling is more focused on obtaining single-value lumped L and C, or on obtaining S-parameters, which can be difficult, if at all possible, to use with a SPICE or IBIS simulator. These S-parameter data then need to be converted
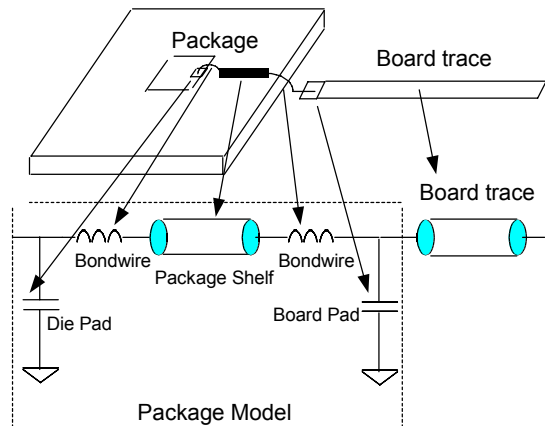

Figure 2. The intuitive and easy to use TDR modeling methodology allows the designer to extract a package model that correlates well with the physical layout of the package under test

into a SPICE or IBIS model, which normally results in a behavioral model. The behavioral model normally does not correlate to the physical layout of the package, and therefore cannot be used to determine what part of the package performs the worst electrically and causes the most signal integrity problems.

It should be noted, however, that S-parameter data can be computed from TDR measurements [5], as well as TDR data can be computed from S-parameter measurements. In this paper, we will treat TDR-capable network analyzers the same as TDR oscilloscopes.

Multiple Reflections and the True Impedance Profile

TDR is a reflection measurement technology, and can measure characteristic impedance at a single discontinuity very accurately. In order to determine impedance of a structure with multiple impedance discontinuities, one needs to deconvolve the multiple reflections from the TDR waveform, and compute the true impedance profile for the Device

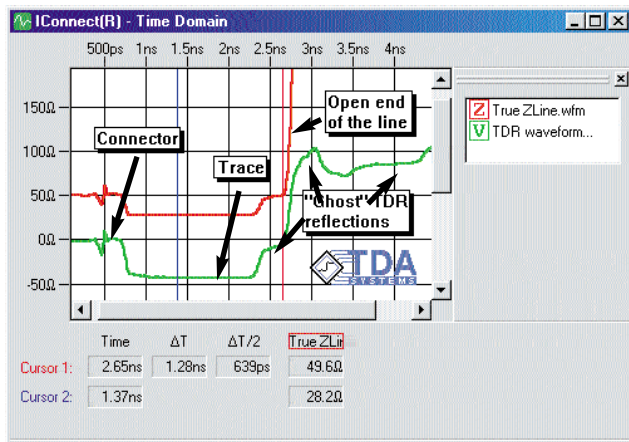Under Test (DUT), [6], [7]. Multiple reflection effects are evident in the following example, Figure 3.

Figure 3. TDR waveform vs. the true impedance profile. True impedance profile provides accurate impedance readouts

The TDR waveform may be confusing for the designer and will not provide accurate impedance readings for all but the first couple of impedance sections. The true impedance profile, in turn, computes accurate impedance values and provides an easy path for computing the values of the distributed model. Qualitatively, a straight-line impedance profile section is a transmission line, a peak is an inductance and a dip is a capacitance. The appropriate transmission line impedance values can be directly read from the impedance profile display, and the appropriate capacitance and inductance values can be computed as:

$$C_{total} = \frac{1}{2} \cdot \int_{t_1}^{t_2} \frac{1}{Z(t)} dt \qquad L_{self} = \frac{1}{2} \cdot \int_{t_1}^{t_2} Z(t) dt \qquad (1)$$

where t_1 and t_2 are the boundaries of the lumped segment "dip" or "peak," Figure 4.
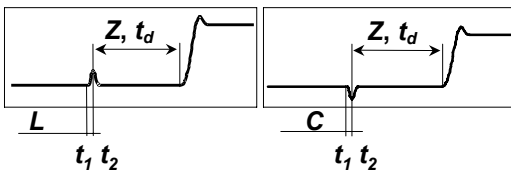

Figure 4. Peaks in package impedance profile correspond to inductive segments, dips to capacitive segments, and straight sections to transmission lines

C_{total} is the sum of the self-capacitance of the lead and its mutual capacitance to other leads. This is the diagonal term in the capacitance matrix as it is computed by 3D field solvers for a segment of a package trace[1].

[1] However, when a 3D field solver writes a netlist for lumped coupled circuit to be used for circuit simulations, it typically writes a self capacitance value, not the total capacitance.

Impedance deconvolution algorithm discussed above is implemented in TDA Systems IConnect® TDR software. Additionally, IConnect uses the true impedance profile, which it computes beforehand, to automatically compute and save the appropriate Z, t_d, L and C values.

Choosing Model Type and Model Validity Range

When a designer is tasked with extracting an equivalent circuit model for a package, he or she needs to answer two key questions:

1. Is a simple RLC, or lumped model for the package acceptable, or is a distributed model required?
2. What is the desired frequency range of validity for the package model?

A lumped model for the package is sufficient if the package trace in question is electrically small compared to the rise time of devices for which the package was designed. Ideally, the length of the package trace should be less than 1/10 of the device rise time, but a more moderate factor of 1/5 or 1/6 is sufficient in most practical applications. Therefore, one can say that a lumped model for the package trace can be used if:

$$t_{package} < t_{rise}/6 \qquad (2)$$

TDR also provides the designer with an easy way to measure the electrical length of the package trace. Keep in mind, however, that TDR provides the round trip delay through the interconnect, which needs to be divided in half in order to obtain the actual propagation delay. Alternatively, if the package inductance L and capacitance C have been found, the propagation delay through the package interconnect can be estimated as:

$$t_{package} = \sqrt{LC} \qquad (3)$$

If a lumped model cannot be used, a more complex distributed model must be extracted. For even faster rise times and higher frequencies, the level of detail in the distributed model increases, and sometimes even high-frequency loss mechanisms must be taken into account. To avoid the unnecessary high complexity of the model, the designer should keep in mind the specific application and rise time for which the package was designed, and limit the range of validity for his or her package model to that rise time. The equivalent 3 dB frequency range of validity for such model can then be estimated from the application rise time as:

$$f_{3dB} < 0.35/t_{rise} \qquad (4)$$

TDR Resolution

Sometimes it is believed that TDR is not capable of resolving small features in the package under test. Generally speaking, it is true that a TDR user can not separate two discontinuities, the electrical distance between which is less than half the TDR rise time. Since a typical rise time in currently available TDR oscilloscopes is on the order of 30-40 ps, that means that a typical TDR oscilloscope can not separate two discontinuities that are less than 15-20 ps apart – that is, less than about 3-4 mm for a typical package. This number can be somewhat better if the true impedance profile is used.

In fact, this analysis holds true if one really wanted to resolve the two distinct discontinuities. However, when a package is that small, for a vast majority of high-speed digital applications, a simple single-element lumped model extracted using one of the techniques described below will be sufficient as long as the lumped element assumption discussed below is met. Additionally, since these techniques rely on comparing two TDR waveforms – the DUT and the reference – capacitance and inductance of a package with a trace much shorter than 3-4 mm can be obtained, and the resolution limitation discussed above can not be applied. Inductance and capacitance for the package traces as short as 1 mm, with inductance of less than 1 nH and capacitance as small as 200 fF can be computed with a sufficient level of accuracy.

Minimizing Measurement Complexity

Modern electronic packages have become very complex structures, with pincounts in the hundreds and layouts utilizing multiple layers on the package substrate. It is simply impractical to measure every single lead in the package under test in order to obtain a package model, unless the measurement can be completely automated. Such automation can be very costly, in particularly in terms of package fixturing required to accommodate automated measurements.

We can take advantage, however, of the package symmetry, thereby minimizing the amount of measurement effort required. For example, we can choose a corner pin and a pin in the middle of the package, which should provide us with a sufficient range of inductance and capacitance values for the package under test.

For example, for a BGA package sample shown on Figure 5 below, one can choose to characterize the longest leads in the outside row as the leads with the largest parasitics, the shortest leads in the outside row as the medium parasitics, and the shortest

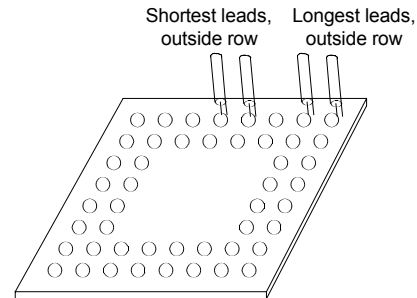leads in the inside row as the leads with the smallest parasitics.

Figure 5. Choosing strategic locations for the package characterization. The data for these strategic locations should represent the range of package parasitics accurately, both self and mutual

Additionally, a number of high-quality electromagnetic field solvers exist that allow the designer to extract the parasitic values for the package under test. If a package layout is complex and does not lend itself easily to identifying "smallest" and "largest" leads, an alternative approach that a designer might take it as follows. First, the designer provides the package layout data to the field solver software, and computes the parasitics for the package leads. Then, the leads with smallest, medium and largest parasitics can be identified, and their parasitic values can be validated with a TDR measurement using one of the techniques discussed below.

Validating the Model

Once the model is extracted, whether from TDR measurements or from an electromagnetic field solver, the designer must simulate the model for the package under test and ensure the correlation between simulation and measurement. When running a validation simulation, the designer should also keep in mind the desired frequency range of validity and rise time for the model. Running a validation simulation with a rise time much faster than required by the designer's application will result in unnecessarily complex models and excessive amount of effort required to obtain such models. It is recommended that the simulated and measured data be filtered down to the application-specific rise time when comparison between simulation and measurement is performed, using either the oscilloscope filter, or the IConnect software rise time filter.

IConnect TDR software from TDA Systems significantly simplifies comparing results of simulations with TDR measurements by providing a link to simulators and TDR instruments and quickly combining the measured and simulated data in one waveform viewer. To further facilitate the validation of the package models, IConnect provides a quick way to

model the TDR source in order to ensure that the source in the simulation and measurement are the same, and any discrepancy between the model simulation and the measurement come from the model only.

The designer obtains immediate feedback in IConnect on accuracy of the model by comparing the simulation and measurement. As a result, fine-tuning of the model, if the correlation between simulation and the measurement is not perfect, is extremely simple and quick.

Package Fixturing and Probing

A fixture or probe for package TDR measurement must provide a 50-Ohm environment to the package under test in order to obtain meaningful TDR results. It also must ensure that the fixture itself does not add to the computation of inductance or capacitance of the package, or that it is de-embedded during the measurement process.

In addition, the fixture should resemble the application environment in which the package will be used. For example, for a package with a thermal plug that does not serve as a ground plane, the plug must not be connected to the fixture ground plane. If there are current-carrying planes in the package, such planes must be connected to the fixture or probe ground plane. The ground plane of the fixture, its distance from the package and its dielectric constant should resemble those for the environment in which the package will be used, if this information about the application ground plane is available. If it is known which pins in the package serve as ground and power pins, connecting these pins to the fixture ground will further facilitate accurate application-specific characterization of the package.

A wide variety of different techniques can be used to provide a ground contact for the package under test. A ground plane for a leaded package can be easily provided by placing conductive material under the package, and isolating the package leads from this ground plane as required by the measurement. A chuck of a microwave probe station, or even a metal plate of sufficient thickness (at least thicker than the skin depth at the frequency range of interest) can serve as good ground planes. For an area array package or a chip-scale package, developing a simple PCB or metal characterization fixture, which allows either easy contact by a microwave probe, or connection by a coax probe or an SMA cable, can create a high-quality ground plane, Figure 6.
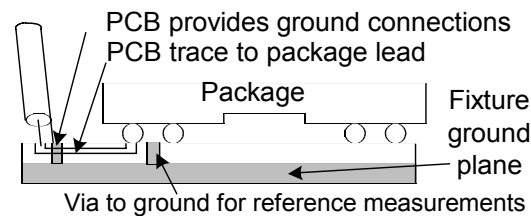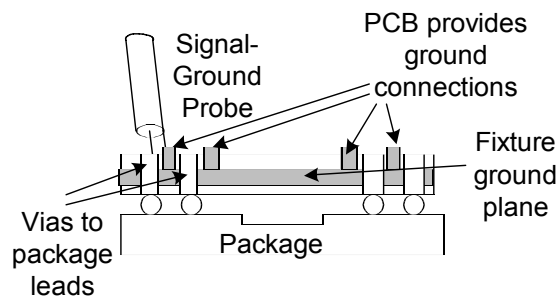

Figure 6. BGA characterization fixture examples. These examples show PCB-based fixtures, which allow for an easy connection to the package with a microwave probe. These fixtures do not contribute to the parasitics of the package, since the measurement reference plane can be easily established at the tip of the measurement probe, and the parasitics of the fixture can be de-embedded

A fixture with traces on a low-loss PCB leading into SMA or similar connectors can be convenient because of the ease of making the connection from the fixture to the TDR instrument. However, such fixture must be carefully de-embedded from the measurement. A simple method of putting conductive epoxy or paste over the package leads, providing a ground connection and leaving only several leads for testing, can be extremely effective in providing a package characterization test setup. The fixture or probe can be de-embedded from the measurement by windowing if the impedance profile technique is used, or by performing a reference measurement with a bare fixture, and using the lumped element extraction method below.

Additional thought should also be given to the interaction of the package leads under test with the adjacent leads, in particular in case of area array (BGA and LGA) packages. For example, for the self-capacitance measurement, the adjacent leads must be shorted to ground on the side where the signal is injected to minimize the effect of mutual capacitance of those leads. For the self-inductance measurement they must be open-ended, to minimize the effect of mutual inductance [8]. Additionally, the true impedance profile method discussed later may not provide correct results if there is large amount of coupling into those adjacent leads, and the differential techniques may need to be applied.

4

Single-ended TDR Techniques

Single-ended TDR allows the designer to obtain a package model by sending a single TDR signal into the package lead. A distributed model, necessary for multilayer packages with traces that are electrically long, such as PGA and some large complex area array packages (BGA and LGA), can be extracted using the impedance profile approach. A lumped L-C model, more appropriate for electrically short packages, such as small area arrays, TSOP, chip-scale packages (CSP), or packages operating at relatively low frequencies, can be extracted from a single-ended lumped element extraction method. Mutual inductance and capacitance can also be found based on near end crosstalk measurement.

Single-ended TDR measurement provides accurate results only in case of weak coupling to the adjacent leads in the package. If the coupling is strong, differential measurement will provide more accurate results.

Impedance Profile Analysis

Impedance profile analysis is useful for packages and multichip modules (MCMs) with complex layouts (large LGA and BGA), or for packages with traces that are long electrically (PGA), for which the lumped model criterion defined by equation (2) does not hold. For MCMs and area array packages, the package layout may have many lines that cross over each other and have potential for coupling, and little symmetry is observed in the package. Overall, such layout becomes so complex that it resembles more a PCB layout rather than a package layout. The impedance profile analysis allows the designer to obtain a distributed model for such complex or electrically long packages.

The value of this approach is that it allows the designer to obtain distributed models for the package under test. The disadvantage of this method is that the coupling to trace segments adjacent to the trace under test is not considered during the trace modeling, which can lead to some inaccuracies in the model. The designer may ensure the accuracy of the model by using a transmission (TDT) measurement in addition to the TDR measurement for model validation.

It should be noted that a package layout with high level of complexity presents not only characterization problems, but also has great potential for presenting signal integrity problems as well. Simplifying the layout as much as possible will not only simplify the package characterization, but also will allow easier package simulation as part of the system design simulations and, most likely, better signal

integrity in the package.

As an example, we extracted a model for a PGA package. The package impedance profile is shown in Figure 7.
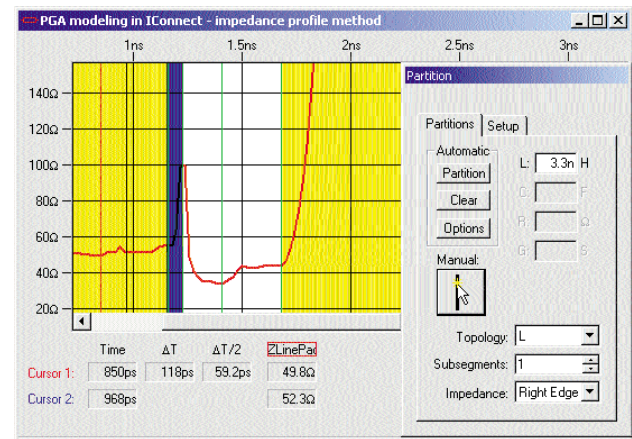

Figure 7. Modeling the package using the true impedance profile analysis. The package true impedance profile shows several distinct segments in the package. IConnect software computes inductance, capacitance and impedance and delay for each of segment

The package true impedance profile shows three distinct segments – one inductive segment in the beginning, due to the inductance of the package pin, and two transmission line segments on the substrate layers inside the package, with no termination (open-ended) inside the package. The corresponding model computed by IConnect TDR software consists of a 3.3 nH inductor and two transmission lines, 34 and 44 Ohms, each about 100 ps long. Once the model is extracted, the correlation between the simulation and measurement are shown in Figure 8.
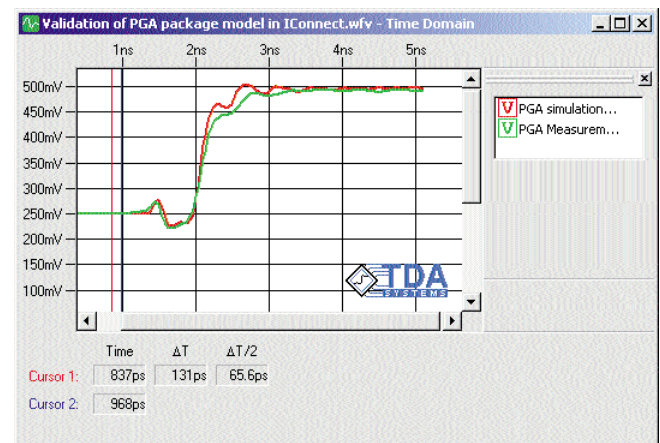

Figure 8. Validation of the PGA package model in IConnect software. The simulated and measured waveforms have been filtered to 150 ps. A good level of model accuracy is achieved

5

Lumped Element Model Extraction (JEDEC Guideline Method)

The purpose of this method is to extract C_{self} and L_{self} for the package lead under test, as well as C_{mutual} and L_{mutual} for the given pair for the package leads, if required. This technique is the preferred method when a lumped model is required. However, fixturing requirements may make the adjacent-opposite technique discussed below an easier one for inductance computation.

This lumped element model extraction relies on relative measurement, comparing the reference (short or open) waveform to the reflected or induced waveform. Any difference between the reference and DUT waveform is caused by the self or mutual inductance or capacitance of the DUT. It is very useful for practically any type of package without an internal current carrying ground plane, particularly if a simple single-element model is required, and the condition of an electrically short package trace (2) is met. This technique can also provide excellent results when inductance of the ground lead needs to be obtained for characterization of the package ground bounce (delta I noise).

The fixturing in this method for capacitance measurement is very straightforward - the leads on the inside of the package are left open-ended, whereas on the outside of the package they should be shorted to ground, except for the leads under test.
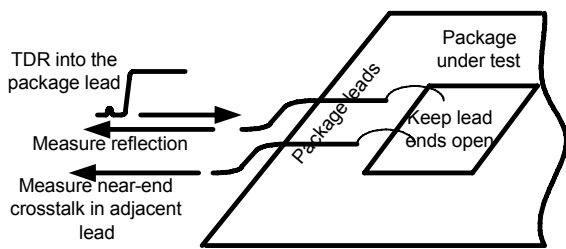

Figure 9. Capacitance measurement setup. The leads on the inside of the package are left open-ended, whereas on the outside of the package they should be shorted to ground, except for the leads under test

For self-capacitance C_{self}, a reference open waveform is required, which is obtained by disconnecting the measurement probe from the package lead, and capturing a TDR waveform while the probe is in the air. The difference between the TDR waveform of the package trace and the reference open TDR waveform gives the sum of lead capacitance and mutual capacitances to other leads C_{total}:

$$C_{total} = \frac{1}{2 \cdot Z_0 \cdot V} \cdot \int_0^\infty (W_{open} - W_{TDR})dt \qquad (5)$$

where V is the TDR voltage incident at the lead under test, normally half the TDR source amplitude, and Z_0 equals the characteristic impedance of the measurement system, 50 Ω for currently available TDR instruments.

For practical purposes, it is not necessary to integrate to infinity, but only until the difference between the W_{open} and W_{TDR} is negligibly small.
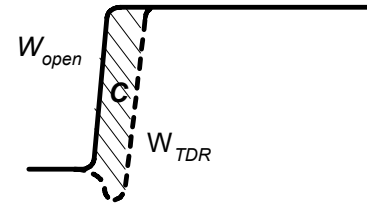

Figure 10. Self-capacitance measurement

For mutual capacitance C_{mutual}, the measurement setup is the same, but the near-end crosstalk waveform on the victim lead under test is acquired instead, while the TDR signal is sent on the offender line. Additionally, it is recommended to acquire a background noise waveform, acquired with no TDR stimulus on either of the lines, which allows us to correct for possible DC offset in TDR oscilloscope, as well as take into account any additional external sources inducing a signal on the victim line. The mutual capacitance can then be computed as:

$$C_{mutual} = \frac{1}{2 \cdot Z_0 \cdot V} \cdot \int_0^\infty (W_{induced} - W_{background})dt \qquad (6)$$

where $W_{background}$ is the background noise waveform. One all the mutual capacitances for the given lead are found, its self capacitance can be found by subtracting all the mutual capacitances from the total capacitance value.

For inductance measurements, the outside leads of the package are also shorted to ground or terminated to 50 Ohms, except for the leads under test and several adjacent leads which share mutual inductance with the lead under test. On the inside of the package, however, for inductance measurement the leads must be shorted to ground. At the very least, for inductance measurement the leads must be shorted together on the inside of the package to provide a low inductance exit path for the current.

For self inductance L_{self}, a reference short waveform is now required, which is obtained by shorting the measurement probe signal lead to ground on a piece of conductive material, such as copper. The difference between the TDR waveform of the package trace and the reference short TDR waveform
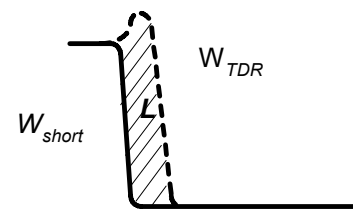

Figure 11. Self-inductance measurement

will now give us the lead inductance:

$$L_{self} = \frac{Z_0}{2 \cdot V} \cdot \int_0^\infty (W_{TDR} - W_{short}) dt \qquad (7)$$

Mutual inductance can be computed as:

$$L_{mutual} = \frac{Z_0}{2 \cdot V} \cdot \int_0^\infty (W_{induced} - W_{background}) dt \qquad (8)$$

In both cases, the fixturing requirements limit the usability of this method of inductance measurements to packages that are easily accessible on the inside. This may be a preferred method for small packages such as TSOP, SOIC, CSP; however, if the number of leads used for a current return path to ground is small, the inductance of the return path is extracted in addition to the lead inductance. This method can also be used for larger packages, such PGA and QFP, as long as the lumped model approximation (2) for the package lead holds.

The advantage of this method is that the technique is simple, well understood and standardized. The fixturing disadvantages for package inductance measurement are obvious. There is also great possibility of not taking into account coupling of energy into leads adjacent to the lead under test.

For example, consider the following package lead measurement on 6-lead TSSOP package.
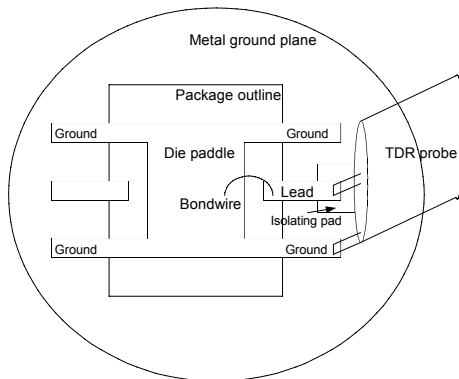

Figure 12. TSSOP package measurement setup. The package was placed on a probe station metal chuck, which provided a good ground plane for the measurement. The package lead to which the test probe was connected was isolated from the probe station chuck

The lead on the inside of the package was shorted to the die paddle with a bondwire, and four ground leads were connected to the die paddle directly, with a low-inductance connection. As a result, using IConnect C and L computational procedures that implement equations (5) and (7), we obtain capacitance and inductance for the package lead of 200 fF and 1.0 nH (for inductance example, see Figure 13).
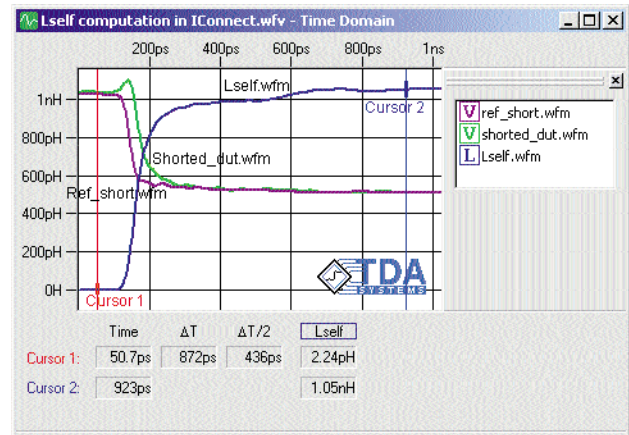

Figure 13. Computation of self-inductance in IConnect. The inductance waveform is computed using equation (7), and the difference between the two cursors at the beginning and end of inductance waveform provide the inductance value of 1.0nH

The inductance for the tested lead includes inductance of the lead itself, inductance of the bondwire, and the combined inductance of the four leads that are connected to the ground and through which the current, injected into the lead under test, exits the package and returns to ground. Therefore, this additional inductive value of the four leads in parallel (L_{ground} / 4) should be taken into account. However, in this particular case it was believed that the overall inductance was dominated by the bondwire inductance, and therefore the inductance of the ground leads was ignored.

The capacitance computed is just the capacitance of the package lead and all its mutual capacitances. Keep in mind that if the die is placed inside the package when the characterization is performed, the total capacitance measured will be a combination of the capacitance of the package lead and the input capacitance of the die. If a designer needs to resolve the package lead capacitance separately from the die capacitance when the die is inside the package, a single-ended or differential impedance profile technique (either the single-ended technique above or the differential technique discussed below) must be used.

Since this modeling technique relies on a relative measurement, it is easy to note that any fixture that can provide such relative measurement will allow the designer to obtain the package and die parasitics, as discussed in a corresponding IBIS specification [9]. For example, for the following measurement of the input capacitance of the die combined with the capacitance of the package lead, the fixture constituted a test board with a socket to hold the QFP type of package. To acquire the reference waveform, we sent a TDR signal into an

empty socket. To acquire a package lead waveform, we put the packaged part into the socket and sent the signal into the same path. The difference between the two waveforms, computed using equation (5), constituted the input capacitance of the die combined with capacitance of the package lead (see Figure 14).
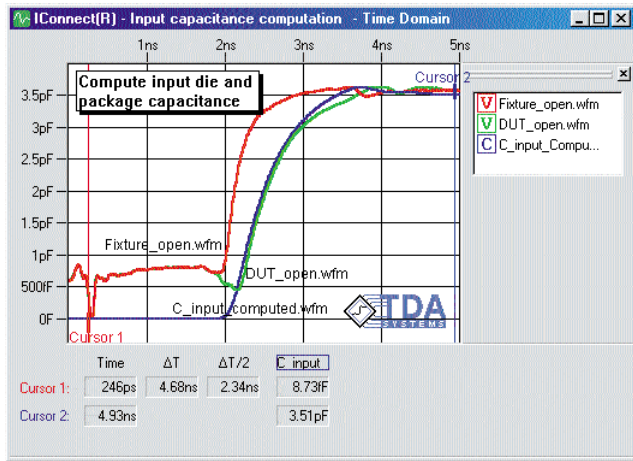

Figure 14. Computation of a die capacitance combined with the package lead capacitance

Differential TDR Techniques

Single-ended TDR allows the designer to obtain a lumped or distributed model for the package lead; differential TDR, on the other hand, allows the designer to obtain a coupled lumped or distributed model for the DUT. As the name implies, differential TDR relies on sending two simultaneous steps, of the same amplitude and opposite polarity, to the two package leads under test. Most modern TDR oscilloscopes have differential capability built in, and as many as 4 to 8 or even more ports can be measured simultaneously.

The differential stimulus creates a virtual ground plane effect, which significantly simplifies complete characterization of the package. For example, with a differential measurement setup, lead inductance can be extracted using the even and odd impedance profile analysis described below without additional fixturing on the inside of the package, whereas the adjacent-opposite technique allows the designer to extract the self and mutual inductance of a package lead essentially without providing a ground connection for the measurement probe. Furthermore, the virtual ground plane created between the two leads results in that the electromagnetic field interaction is mainly limited to the two leads under test, and minimum energy coupling occurs into any other leads, Figure 15. In case of a single-ended TDR measurement, on the other hand, unless all the leads around the lead under test are grounded on the outside of the package for capaci-

tance measurements, energy coupling into those leads can result in incorrect measurement results.
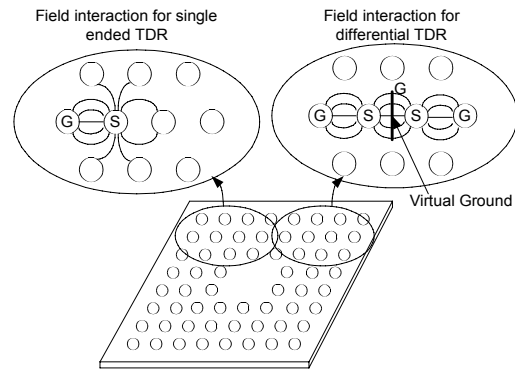

Figure 15. In case of a differential TDR, the virtual ground plane is the closest ground plane to the leads under test, and practically no interaction with the adjacent leads occurs. For a single-ended TDR measurement, energy can be coupled into the adjacent leads, resulting in measurement error

A key assumption when performing differential TDR is that the two leads under test must be reasonably symmetric. Therefore, the usability of this method is limited to most packages and leads, except for the more complex large-pincount ones with a complex interleaving layout. For the complex large pincount package category, the impedance profile technique in conjunction with a field solver analysis must be used.

Another assumption when performing a differential measurement is that the two steps of opposite polarity in the differential stimulus arrive at the device under test at the same time. This is easily achieved, because modern TDR oscilloscopes have capabilities to adjust the relative delay of the TDR sources within the sampling module and between different modules up to several hundred picoseconds. To adjust the position of the two TDR sources, disconnect the probes that will be used in the differential measurement from the DUT, and connect them to ground. The difference between the two TDR responses observed on the TDR oscilloscopes will be the round trip delay difference between the two sources; adjusting the relative source position by half that delay will ensure that the sources arrive to the DUT at the same time. After that, use the acquisition delay adjustment to correct for the signal path back to the scope and ensure that the two signals are observed at the same time position on the oscilloscope.

Alternatively, to adjust the relative source position, you can TDR into a short symmetric test device, such as a power combiner, with TDR sources being in differential mode, and observe the difference in the wave shape between the two TDR channels.

Since the device is absolutely symmetric, no differential discontinuities should be observed, and the two TDR responses should look absolutely identical in shape. You can adjust the source delay until such identical waveshape is observed.

Even and Odd Impedance Analysis

The even and odd impedance profile analysis is useful when a coupled line model is necessary for packages and modules with complex layout, or for packages with traces that are long electrically (PGA). It has the advantages of the single-ended impedance profile analysis, but also takes into account coupling between leads under test. The even and odd impedance profile analysis allows the designer to obtain a distributed model for these complex or electrically long packages, using a methodology for differential line characterization discussed in [10], or to compute a complete LC matrix for a short package lead pair. However, this approach can be used only if the package lead pair in question exhibits a reasonable level of symmetry – otherwise the basic differential modeling assumption does not hold.

One advantage that this approach gives the designer is that many times one can get away with a much simpler fixturing setup than otherwise required by single-ended modeling techniques. For example, no shorting of the package leads on the inside of the package is required; however, good grounding on the side of the package where the stimulus is applied is still necessary for a good common mode measurement.

An additional important advantage of this method compared to a single-ended method is in the more controlled field interaction in the case of area array packages, and, therefore, better measurement accuracy. For a differential measurement, a virtual ground plane created between the two leads, pads, or balls under test results in a very controlled field interaction just between these two leads, pads or balls. In case of a single-ended measurement, however, unless the leads, pads or balls are adjacent to the test leads are grounded, the interaction to these leads can change the computed inductance / capacitance values (see Figure 15).

This approach, however, may not be quite as accurate as the lumped element method or adjacent-opposite method if a single value lumped model must be extracted, and the extracted model must always be validated with a simulation from IConnect software.

Additionally, compared to the adjacent-opposite method discussed in the following section, even-odd

impedance profile analysis still requires a good ground contact for the probe for the common mode measurement.

To perform the measurement, the designer must TDR into the two leads under test with a differential and common mode stimulus, and acquire channel 1 only on the TDR oscilloscope in both cases (no waveform math is required), Figure 16.
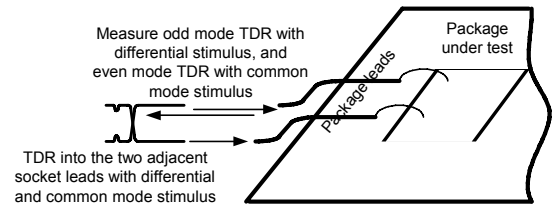

Figure 16. Differential and common mode measurements for even and odd impedance profile computations

Then a reference short or open waveform is acquired, and the even (common mode channel 1) and odd (differential mode channel 1) impedance profiles are computed. A differential model can be extracted by partitioning the two impedance profiles in the IConnect symmetric-coupled line modeling window. Alternatively, L and C self and mutual values can be extracted using the following equations:

$$L_{self} = \frac{1}{2}\left(Z_{even}t_{even} + Z_{odd}t_{odd}\right) \qquad (9)$$

$$L_{mutual} = \frac{1}{2}\left(Z_{even}t_{even} - Z_{odd}t_{odd}\right) \qquad (10)$$

$$C_{total} = \frac{1}{2}\left(\frac{t_{odd}}{Z_{odd}} + \frac{t_{even}}{Z_{even}}\right) \qquad (11)$$

$$C_{mutual} = \frac{1}{2}\left(\frac{t_{odd}}{Z_{odd}} - \frac{t_{even}}{Z_{even}}\right) \qquad (12)$$

where $C_{total} = C_{self} + C_{mutual}$, and Z_{odd}, t_{odd}, Z_{even}, t_{even} are the odd and even impedances and delays, correspondingly. The reason for using C_{total} rather than C_{self} is that most field solver analysis will produce a value equivalent to C_{total}. To achieve good characterization accuracy, the board traces leading to the package leads under test must be symmetric also.

Consider the following example of an LGA package. The conductive epoxy covering most of the package contacts was used as a ground plane. The die placement area was planar with the top side of the package, and it was easy to short all the leads on the die side of the package to ground by turning the package upside down and placing it on a probe station chuck. The differential and common mode TDR

measurements are performed on two package leads, and the even and odd mode impedances are computed, Figure 17.
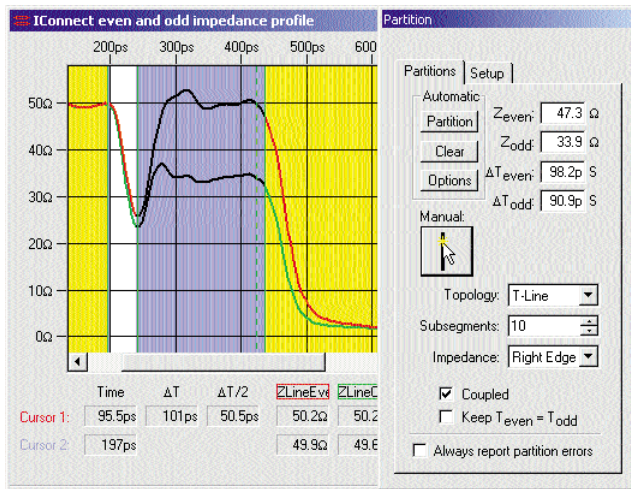

Figure 17. Even and odd impedance profile analysis for an LGA package. The selected section can be modeled as a coupled transmission line section of about 90 ps, or as a lumped coupled segment for slower rise time

The fast TDR rise time resolves two sections. The first section is lumped, mainly capacitive and not coupled, as seen from the fact that the even and odd mode impedances for this first segment are the same. Computed capacitance of the segment is 730 fF. The other section is a distributed one; it can be modeled separately as a symmetric-coupled model discussed in [10], with 98 ps even mode delay and 92 ps odd mode delay. For slower rise time of 500 ps, it can be treated as a lumped element with the following parameters: L_{self}=3.9 nH, L_{mutual}=0.7 nH, C_{self}=2.2 pF, C_{mutual}=0.4 pF. The correlation between simulation and measurement for this model is shown in Figure 18. Filtering the
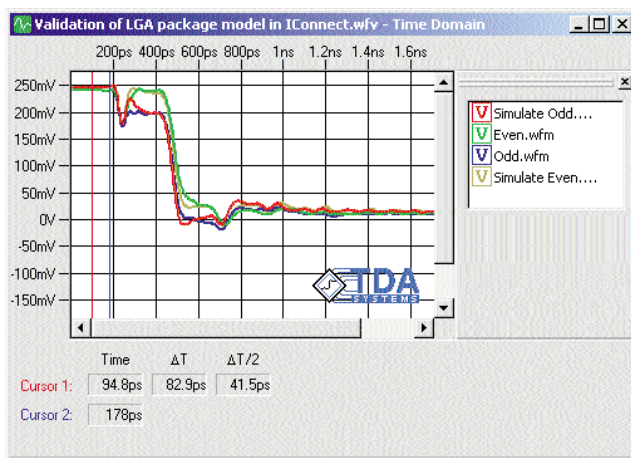

Figure 18. Validation of even and odd mode analysis model for an LGA package. Filtering the waveforms down to a slower rise time will further improve the correlation

waveforms down to an application-specific rise time will further improve the correlation. The combined value of the package lead self-inductance is 4.4 nH and mutual inductance remains 0.7 nH.

It is worth noting the single-line impedance profile analysis for one lead in this package provides values of L_{self} =3.9 nH and C_{self} =2.3 pF. These values are sufficiently close to those for L_{self} and C_{self} computed using even and odd impedance profile.

Adjacent-Opposite Analysis

The technique described here was originally reported in [11]. The purpose of this approach is only to compute L_{self} and L_{mutual}. It is the preferred method for package characterization when a lumped model for the package inductance is required. This method is useful for smaller BGA packages, SOICs and other packages that do not provide easy connection from the package cavity to a ground plane. The advantage of this approach is in its better accuracy compared to single-ended measurement, due to the presence of the virtual ground plane between the two differential signals. However, you still have to connect the leads under test together (but not to ground) on the inside of the package, and only the inductances can be computed using this method.

To perform the measurement, you first do a differential measurement on the two package leads under test. The inductance is measured based on these two waveforms using the self-inductance measurement procedure in IConnect and equation (7). The measured inductance, however, is not just an inductance of one lead, but also a difference of self and mutual inductance between the leads:

$$L_{total\ adjacent} = L_{self} - L_{mutual} \qquad (13)$$

Then a differential measurement is performed, but on leads on the opposite or orthogonal sides of the package, the leads that do not share any mutual inductance between each other, Figure 19.
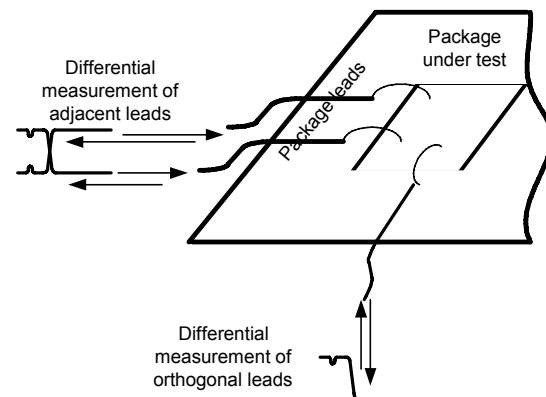

Figure 19. Adjacent-opposite inductance modeling

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The inductance is again computed using IConnect self-inductance computation or equation (7), but the resulting inductance in that case is just L_{self} for each pin. For better accuracy, one can subtract the positive going waveform and the negative going waveform and divide it by two before computing the inductance of the pin, thereby taking the average between the two measurements. Then, the mutual inductance between the two pins can be computed as:

$$L_{mutual} = L_{total\ opposite} - L_{total\ adjacent} \qquad (14)$$

For the same LGA package used in the even and odd impedance profile analysis, the computed value of $L_{total\ adjacent}$ is computed to be 3.5 nH and $L_{total\ separate}$ = 4.3 nH, which gives the values of L_{self} of 4.3 nH and L_{mutual} = 0.8 nH, sufficiently close to those obtained using the even and odd mode analysis (4.3 nH for self and 0.7 nH for mutual).

Selecting the Package Modeling Method

The following table provides suggestions on how to select an appropriate TDR modeling method for the given package type.

Table 1. Recommendations for selecting a TDR modeling method for different packages

	Model required	*Primary modeling method*	*Secondary modeling method*
SOIC	C	Lumped	Lumped
	L	Adjacent-opposite	
TSOP	C	Lumped	Lumped
	L	Adjacent-opposite	
PGA	Distributed, coupled	Impedance profile	Even-odd impedance
QFP	Distributed-coupled	Even-odd impedance	Lumped, adjacent-opp.
Small BGA, LGA	Distributed-coupled	Even-odd impedance	Lumped, adjacent-opp.
Large BGA, LGA	Distributed-coupled	Impedance profile	Even-odd impedance
MCM	Distributed-coupled	Impedance profile	Even-odd impedance
CSP	C	Lumped	Lumped
	L	Adjacent-opposite	

Small packages, such as SOIC or TSOP, are typically electrically short and a lumped element model for those packages is sufficient. Small CSP can be modeled using the same lumped modeling approaches. Larger packages typically require a

distributed model, although sometimes a lumped model can be used if short interconnect condition (2) is met. The amount of coupling in a PGA package varies, and sometimes an uncoupled model for this package type is sufficient; however, a coupled model is normally preferred. Larger and complex BGA, LGA and MCM packaging solutions sometimes can be characterized using the even and odd impedance profile analysis. However, many times a more complex model, which takes into account the complexity of the package, may be necessary.

Appendix A. Derivations

Lumped Model Circuit Description

A lumped model describing a package is typically defined by its inductance and capacitance matrices:

$$C = \begin{bmatrix} C_{total1} & -C_{mutual21} & \cdots & -C_{mutual\,n1} \\ -C_{mutual12} & C_{total2} & \cdots & -C_{mutual\,n2} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{mutual\,1n} & -C_{mutual\,2n} & \cdots & C_{total\,n} \end{bmatrix} \quad (A1)$$

$$L = \begin{bmatrix} L_{self11} & L_{mutual21} & \cdots & L_{mutual\,n1} \\ L_{mutual12} & L_{self2} & \cdots & L_{mutual\,n2} \\ \vdots & \vdots & \ddots & \vdots \\ L_{mutual\,1n} & L_{mutual\,2n} & \cdots & L_{self\,n} \end{bmatrix} \quad (A2)$$

where n is the number of leads in the package. These matrices are diagonal symmetric, that is:

$$\begin{aligned} C_{mutual\,mn} &= C_{mutual\,nm} \\ L_{mutual\,mn} &= L_{mutual\,nm} \end{aligned} \quad (A3)$$

These matrices are also normally sparse, because the elements that are far from the diagonal represent package pins that are far away from each other, and therefore have little or no coupling.

When performing circuit simulation, the following equivalent circuit for a pin pair, represented by 2x2 L and C matrices, is used in simulators (Figure A1).
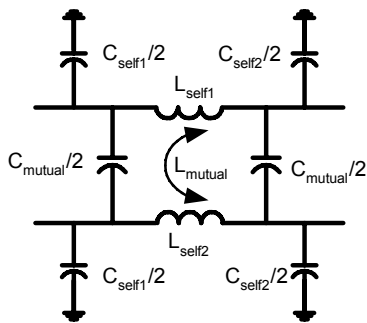

Figure A1. Equivalent circuit for a pin pair, represented by a 2x2 L and C matrices

Note that the coupled line matrix notation uses the C_{total} term, whereas a circuit simulator uses C_{self} for netlist syntax.

Capacitance and Inductance of an Impedance Segment (equation 1)

First, consider the inductance of an impedance segment. Inductance can be determined from inductance per unit length as:

$$L_{self} = \int_{x_1}^{x_2} L_{self}(x)dx \quad (A4)$$

Length dx can be found from velocity of propagation through this impedance segment, and time required to propagate through the segment:

$$L_{self} = \frac{1}{2}\int_{t_1}^{t_2} L_{self}(t)V_{prop}(t) \cdot dt \quad (A5)$$

The factor of ½ comes from the fact that TDR gives us the round trip delay value, and we need to take half of that delay in order to get an accurate delay computation. Converting equation (3) to obtain the velocity of propagation, we obtain:

$$V_{prop}(t) = \frac{1}{\sqrt{L_{self}(t) \cdot C_{total}(t)}} \quad (A6)$$

Using this equation, we obtain:

$$\begin{aligned} L_{self} &= \frac{1}{2}\int_{t_1}^{t_2} L_{self}(t)\frac{1}{\sqrt{L_{self}(t) \cdot C_{total}(t)}} \cdot dt \\ &= \frac{1}{2}\int_{t_1}^{t_2}\sqrt{\frac{L_{self}(t)}{C_{total}(t)}} \cdot dt = \frac{1}{2}\int_{t_1}^{t_2} Z(t)dt \end{aligned} \quad (A7)$$

Similar reasoning gives us:

$$C_{total} = \frac{1}{2} \cdot \int_{t_1}^{t_2}\frac{1}{Z(t)}dt \quad (A8)$$

Self and Mutual Capacitance and Inductance from Lumped Element Extraction Method (5)-(8)

The equations (5)-(8) are derived here for a case of a lumped interconnect.

Lumped Self-Capacitance

Lumped self-capacitance measurement is performed with the far end of the line open ended. The equivalent circuit for such measurement is shown in Figure A2.
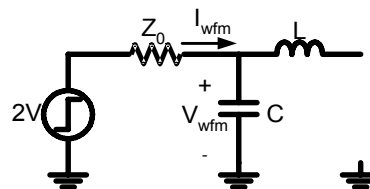

Figure A2. Equivalent circuit for a lumped self capacitance measurement

2V is the amplitude of the TDR source, and Z_0 the equivalent resistance of the source. For the lumped structure shown in the figure above, no current flows through the inductor. Using:

$$I_{wfm} = C\frac{dV}{dt} \tag{A9}$$

we obtain:

$$C\int_0^\infty dv = \int_0^\infty I_{wfm}\,dt \tag{A10}$$

$$V(\infty) - V(0) = \frac{1}{C}\int_0^\infty I_{wfm}\,dt \tag{A11}$$

Since $V(0) = 0$ and $V(\infty) = 2V,$ we obtain:

$$2V = \frac{1}{C}\int_0^\infty I_{wfm}\,dt \tag{A12}$$

Since:

$$I_{wfm} = \frac{2V - V_{wfm}}{Z_0} \tag{A13}$$

$$C = \frac{1}{2 \cdot V \cdot Z_0}\int_0^\infty (2V - V_{wfm})\,dt \tag{A14}$$

In practice, we have not only the output resistance Z_0, but also a cable, a fixture or a probe. This is why a reference waveform is required to allow us to remove the capacitance of the cable, fixture or probe. Subtracting the capacitance obtained using a reference waveform, we obtain equation (5).

In the presence of mutual capacitance, however, the measurement setup for capacitance measurement is determined by Figure A3. As one can readily observe, the mutual capacitance to adjacent lines C_{mutual} is in parallel with the capacitance C_2 of the line under test. Therefore, the derivation above
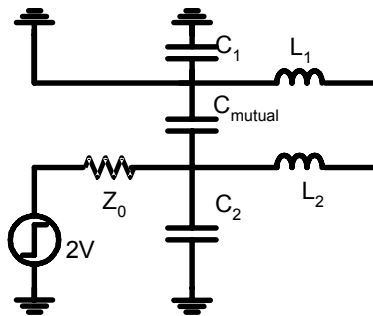

Figure A3. Equivalent circuit for a lumped self capacitance measurement in presence of mutual capacitance

describes the sum of self-capacitance and mutual capacitance to adjacent leads, or total capacitance of the lead C_{total}.

Lumped Self-Inductance

Lumped self inductance measurement is performed with the far end of the line shorted to ground. The equivalent circuit for such a measurement is shown in Figure A4.
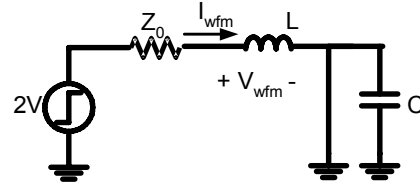

Figure A4. Equivalent circuit for a lumped self inductance measurement

For the lumped structure shown in figure A4, above, no current flows through the capacitor. Using:

$$V_{wfm} = L\frac{dI_{wfm}}{dt} \tag{A15}$$

we obtain:

$$L\int_0^\infty di = \int_0^\infty V_{wfm}\,dt \tag{A16}$$

$$i(\infty) - i(0) = \frac{1}{L}\int_0^\infty V_{wfm}\,dt \tag{A17}$$

Since $i(0) = 0$ and $i(\infty) = 2V / Z_0$, we obtain:

$$\frac{2 \cdot V}{Z_0} = \frac{1}{L}\int_0^\infty V\,dt \tag{A18}$$

$$L = \frac{Z_0}{2 \cdot V}\int_0^\infty V_{wfm}\,dt \tag{A19}$$

In practice, we have not only the output resistance Z_0, but also a cable, a fixture or a probe. This is why a reference waveform is required to allow us to remove the inductance of the cable, fixture or probe. Subtracting the inductance obtained using a reference waveform, we obtain equation (7). This equation is correct for the self inductance (L_{self}) of the lead.

Lumped Mutual Capacitance

Mutual capacitance measurement is performed with the far end of the victim line open ended. The equivalent circuit for such a measurement is shown in Figure A5 on the following page.
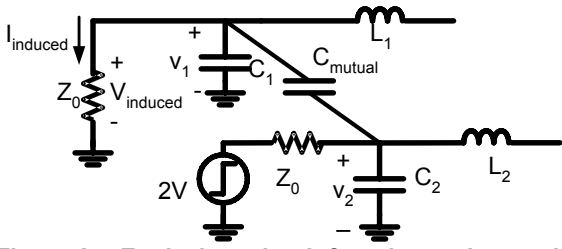
Figure A5. Equivalent circuit for a lumped mutual capacitance measurement

Induced current can be determined as:

$$I_{induced} = C_{mutual} \frac{d(v_2 - v_1)}{dt} - C_1 \frac{dv_1}{dt} \qquad (A20)$$

which gives us:

$$\int_0^\infty I_{induced}dt = C_{mutual}\left[\int_0^\infty dv_2 - \int_0^\infty dv_1\right] - C_1\int_0^\infty dv_1 \qquad (A21)$$

$$C_{mutual}\left[v_2(\infty) - v_2(0) - v_1(\infty) + v_1(0)\right] + \\ - C_1\left[v_1(\infty) - v_1(0)\right] = \int_0^\infty I_{induced}dt \qquad (A22)$$

Since $v_1(\infty) = 0$, $v_1(0) = 0$, $v_2(0) = 0$, and $v_2(\infty) = 2V$, we obtain:

$$C_{mutual} 2V = \int_0^\infty I_{induced}dt \qquad (A23)$$

Then using:

$$I_{induced} = V_{induced}/Z_0 \qquad (A24)$$

we obtain:

$$C_{mutual} = \frac{1}{2 \cdot V \cdot Z_0}\int_0^\infty V_{induced}dt \qquad (A25)$$

In order to remove background noise and possible DC offset in the TDR oscilloscope, we need to subtract the background noise waveform from the induced waveform, which gives us equation (6).

Lumped Mutual Inductance

Mutual inductance measurement is performed with the far end of the victim line shorted to ground. The equivalent circuit for such measurement is shown in Figure A6.
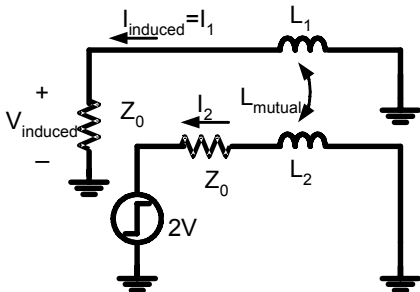

Figure A6. Equivalent circuit for a lumped mutual inductance measurement

Induced voltage can be determined as:

$$V_{induced} = L_{mutual} \frac{di_2}{dt} + L_1 \frac{di_1}{dt} \qquad (A26)$$

which gives us:

$$\int_0^\infty V_{induced}dt = L_{mutual}\int_0^\infty di_2 + L_1\int_0^\infty di_1 \qquad (A27)$$

$$L_{mutual}\left[i_2(\infty) - i_2(0)\right] + L_1\left[i_1(\infty) - i_1(0)\right] = \int_0^\infty V_{induced}dt \qquad (A28)$$

Since $i_1(\infty) = 0$, $i_1(0) = 0$, $i_2(0) = 0$, and $i_2(\infty) = 2V/Z_0$, we obtain:

$$L_{mutual} = \frac{Z_0}{2V}\int_0^\infty V_{induced}dt \qquad (A29)$$

In order to remove background noise and possible DC offset in the TDR oscilloscope, we need to subtract the background noise waveform from the induced waveform, which gives us equation (8).

Self and Mutual Capacitance and Inductance from Even and Odd Impedance Analysis (9)-(12)

Even and odd mode impedance and delays can be shown to be:

$$Z_{odd} = \sqrt{\frac{L_{self} - L_{mutual}}{C_{total} + C_{mutual}}} \qquad (A30)$$

$$Z_{even} = \sqrt{\frac{L_{self} + L_{mutual}}{C_{total} - C_{mutual}}} \qquad (A31)$$

$$t_{odd} = \sqrt{\left(L_{self} - L_{mutual}\right)\left(C_{total} + C_{mutual}\right)} \qquad (A32)$$

$$t_{even} = \sqrt{\left(L_{self} + L_{mutual}\right)\left(C_{total} - C_{mutual}\right)} \qquad (A33)$$

From this, equations (9)-(12) easily follow.

Self and Mutual Inductance from Adjacent-Opposite Analysis (13), (14)

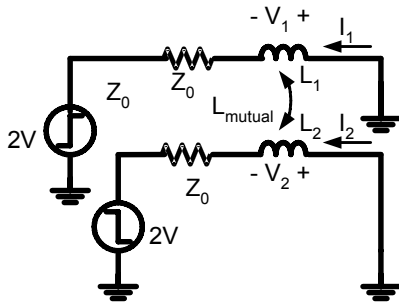The following figure shows the measurement setup for the adjacent-opposite measurement.

Figure A7. Equivalent circuit for an adjacent-opposite self and mutual inductance measurement

We can see that:

$$V_1 = L_1 \frac{di_1}{dt} + L_{mutual} \frac{di_2}{dt}$$
$$V_2 = L_{mutual} \frac{di_1}{dt} + L_2 \frac{di_2}{dt} \qquad \text{(A34)}$$

Since $V_1 = -V_2$, $i_1 = -i_2$, and $L_1 = L_2 = L_{self}$, we obtain:

$$V = (L_{self} - L_{mutual}) \frac{di}{dt} \qquad \text{(A35)}$$

This equation, following the derivation for the self inductance of the package lead, gives us:

$$(L_{self} - L_{mutual}) = \frac{Z_0}{2 \cdot V} \int_0^\infty V_{wfm} dt \qquad \text{(A36)}$$

which leads to equation (13). Equation (14) follows easily.

Appendix B. Abbreviations

CSP – Chip Scale Package
LGA – Land Grid Array
BGA – Ball Grid Array
MCM – Multichip Module
PGA – Pin Grid Array
QFP – Quad Flat Pack
SOIC – Small Outline Integrated Circuit
TSOP – Tape Small Outline Package

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