Instruction Manual

Tektronix

92DM35A
88100 Microprocessor Support

070-8311-00

This document supports software release 2, version 1.50 and above.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

Please check for change information at the rear of this manual.

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Preface: A GUIDE TO DAS 9200 DOCUMENTATION

The Digital Analysis System (DAS) 9200 documentation package provides the information necessary to install, operate, maintain, and service the DAS 9200. The DAS 9200 documentation consists of the following:

- a series of microprocessor-specific **microprocessor support instructions** that describe the various microprocessor support packages
- a **system user's manual** that includes a beginning user's orientation, a discussion of DAS 9200 system-level operation, and reference information such as installation procedures, specifications, error messages, and a complete system glossary
- a series of **module user's manuals** that describe each of the DAS 9200 acquisition, pattern generation, and optional I/O modules
- an **on-line documentation** package that includes "context-sensitive" technical notes
- a **programmatic command language user's manual** that describes the set of programmatic commands available for remotely controlling the DAS 9200
- a series of **application software user's manuals** that describe the various application software packages
- a **technician's reference manual** that helps a qualified technician isolate DAS 9200 problems to the individual module level and determine corrective action (including on-site removal and replacement of modules)
- a **verification and adjustment procedures manual** that allows a qualified technician to make necessary adjustments and verify specifications of the mainframe and modules
- a series of **workbooks** that teach concepts about DAS 9200 acquisition modules and pattern generation modules

GENERAL SAFETY SUMMARY

The general safety information in this summary is for operating and servicing personnel. Specific warnings and cautions can be found throughout the manual where they apply, and may not appear in this summary.

TERMS IN THIS MANUAL

CAUTION

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION indicates a hazard to property, including the equipment itself, and could cause minor personal injury.

WARNING indicates solely a personal injury hazard not immediately accessible as you read the marking.

DANGER indicates a personal injury hazard immediately accessible as you read the marking.

SYMBOLS AS MARKED ON EQUIPMENT

DANGER—High voltage.

Protective ground (earth) terminal.

ATTENTION—REFER TO MANUAL.

GROUNDING THE PRODUCT

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground.

WARNING: This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation. (I.E.C. Safety Class I)

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

POWER DISCONNECT

The main power disconnect is by means of the power cord or, if provided, an ac power switch.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product. Use only a power cord that is in good condition. CSA Certification includes the equipment and power cords appropriate for use on the North America power network. All other power cords supplied are approved for the country of use.

USE THE PROPER FUSE

To avoid fire hazard use only a fuse of the correct type, voltage rating, and current rating.

USE THE PROPER VOLTAGE SETTING

Make sure the line selector is in the proper position for the power source being used.

REMOVE LOOSE OBJECTS

During disassembly or installation procedures, screws or other small objects may fall to the bottom of the mainframe. To avoid shorting out the power supply, do not power-up the instrument until such objects have been removed.

DO NOT OPERATE WITHOUT COVERS

To avoid personal injury or damage to the product, do not operate this product with covers or panels removed.

USE CARE WITH COVERS REMOVED

To avoid personal injury, remove jewelry such as rings, watches, and other metallic objects before removing the cover. Do not touch exposed connections and components within the product while the power cord is connected.

REMOVE FROM OPERATION

If you have reason to believe that the instrument has suffered a component failure, do not operate the instrument until the cause of the failure has been determined and corrected.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Section 1: OVERVIEW

The 92DM35A Microprocessor Support product disassembles data from systems based on the Motorola 88100 microprocessor. The 92DM35A product runs on a DAS 9200 equipped with one of the following data acquisition module combinations:

- one 92A90 Data Acquisition Module to acquire data from one bus of an 88100 system running at or below 20 MHz
- two 92A90 Data Acquisition Modules to acquire data both buses of an 88100 system running at or below 20 MHz
- two 92A90 Data Acquisition Modules with one High-Speed Microprocessor Interface to acquire data from one bus of an 88100 system running above 20 MHz
- four 92A90 Data Acquisition Modules with two High-Speed Microprocessor Interfaces to acquire data from both buses of an 88100 system running above 20 MHz
- one 92A96 Data Acquisition Module with one 90-Channel Microprocessor Interfaces at any clock frequency to acquire data from one bus
- two 92A96 Data Acquisition Modules with two 90-Channel Microprocessor Interface at any clock frequency to acquire data from both buses

This product consists of software on a floppy disk, a probe adapter, this manual, and can optionally include 90-Channel Microprocessor Interfaces. The High-Speed Microprocessor Interface is a separate product. The software includes both setup files and a disassembler program.

Also included in the software files is a demonstration reference memory. This file (called 88100_Demo) shows disassembled data; it is automatically installed on the DAS 9200 when you install the disassembler software. All figures in Section 4 that show acquired data are taken from this demonstration reference memory. Directions for viewing the 88100_Demo file are in Section 3.

BASIC INFORMATION

To use this product, you need to have the following:

- this manual
- other DAS 9200 mainframe and data acquisition module user's manuals
- knowledge of your specific DAS 9200 configuration and its operation
- the *MC88100 RISC Microprocessor's User's Manual* (Motorola Inc., 1990)
- knowledge of your 88100 system

DAS 9200 System Software Compatibility

The 88100 Microprocessor Support is compatible with DAS 9200 System Software Release 2, Version 1.5 or greater. It is not compatible with previous system software versions.

About This Manual

The organization of this manual is based on the sequence of steps necessary to use the disassembler. If you are an experienced DAS 9200 user familiar with loading software and connecting microprocessor support probe adapters to a system under test, you can use the *Quick Start* section. The *Quick Start* section gives brief instructions on how to install the 92DM35A software, connect the DAS 9200 to your 88100 system, configure the probe adapter, and acquire data. You can then proceed to Section 4 to use disassembly.

If you are using DAS 9200 microprocessor support for the first time, you should read some sections sequentially. Read Sections 1, 3, and 4 if you are going to acquire and view disassembled data. Read Sections 1, 3, and 5 if you are going to acquire and view timing or state data for hardware analysis. Figure 1-1 shows how to proceed through this manual.

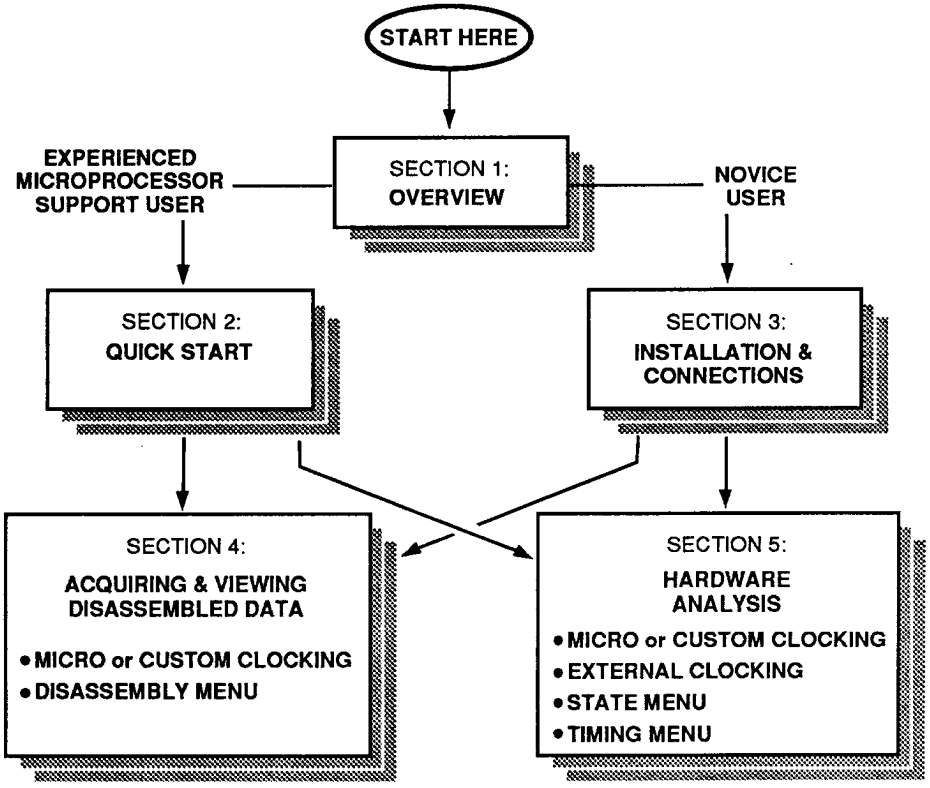

Figure 1-1. How to proceed through this manual.

In this manual, the following conventions are used:

- the terms disassembler and disassembler software are used interchangeably in reference to the 92DM35A software that disassembles the bus cycles into instruction mnemonics and cycle types
- the terms system under test and SUT are used interchangeably in reference to the microprocessor system under test
- references to the 92A90 and 92A96 Data Acquisition Modules include all versions of those module unless otherwise noted
- references to the 90-Channel Microprocessor Interface are abbreviated to 90-channel interface
- references to the 92A60/90 Retargetable Buffer Probe are abbreviated to buffer probe
- references to the High-Speed Microprocessor Interface are abbreviated to HSMI
- a signal that is active low has a tilde (~) following its name

Other Necessary Manuals

Before using these instructions, you should be familiar with the operation of a DAS 9200 with the data acquisition module you are using. For general instructions on the use of the DAS 9200 and a data acquisition module, refer to both the *DAS 9200 System User's Manual* and the data acquisition module user manual.

Refer to Motorola's *MC88100 RISC Microprocessor User's Manual* (1990) for information about the 88100 microprocessor.

DAS 9200 Configuration

To use the 88100 Microprocessor Support, your DAS 9200 must be equipped with one of the following module combinations:

- one or two 92A90 Modules to acquire data from an 88100 system operating at or below 20 MHz
- two or four 92A90 Modules to acquire data from an 88100 system operating above 20 MHz
- one or two 92A96 Modules operating at any clock rate

When you are acquiring data with 92A90 Modules, buffer probes are used. When you are acquiring data with 92A96 Modules, 90-channel interfaces are used. One module acquires code bus information and the other module acquires data bus information. You can use one module to acquire information from only one of the two buses, code or data.

To acquire information from both the code and data buses of an 88100 system, you must use at least two 92A90 Modules or two 92A96 Modules. You must also use at least two 92A90 Modules to acquire information from just one bus of an 88100 system operating at clock speeds above 20 MHz. And, when using two or four 92A90 Modules, you will also need to use one HSMI per bus.

Figure 1-2 shows an overview of the DAS 9200 connected to an 88100 system under test. This view is for a DAS 9200 configured with 92A90 Modules.

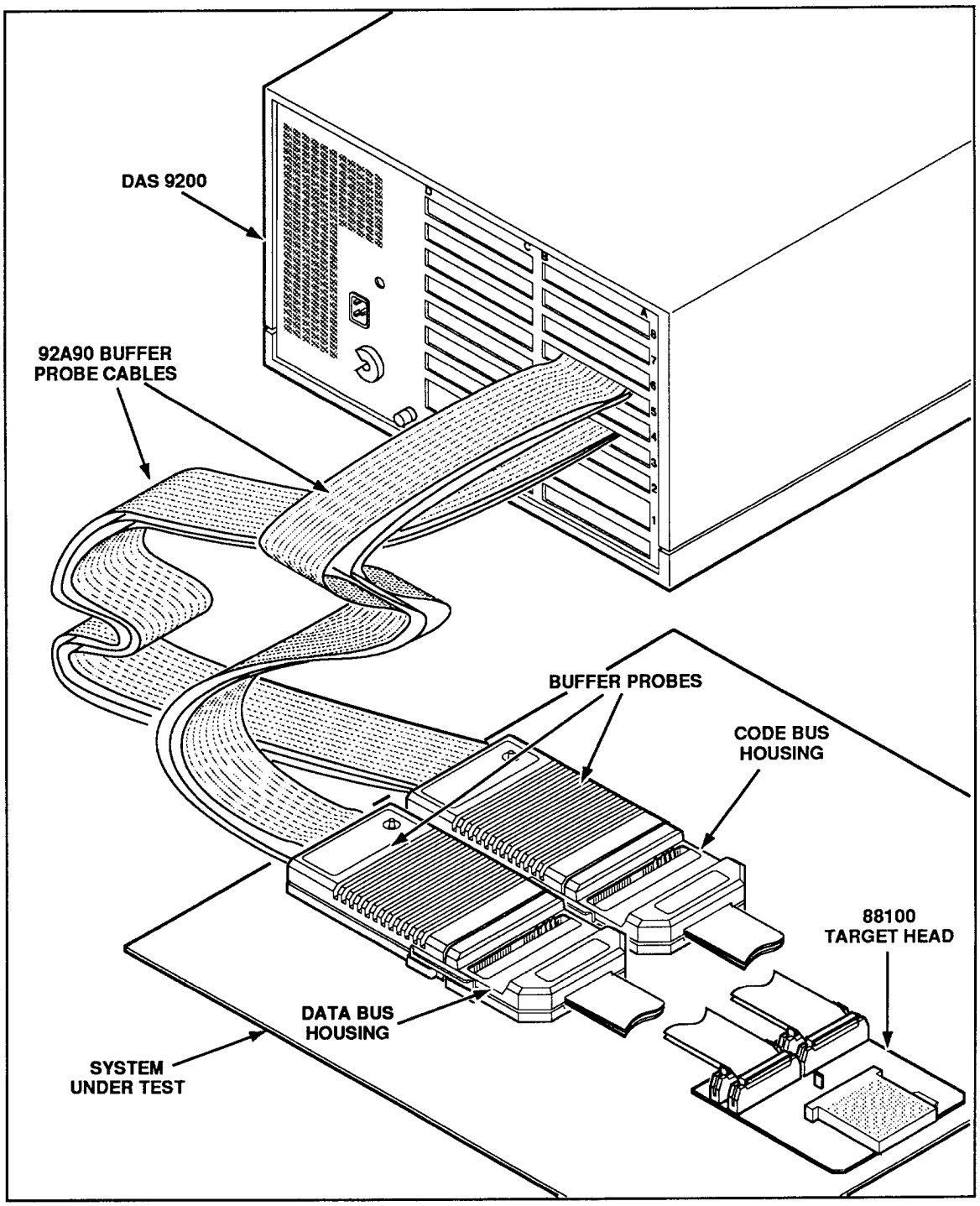

Figure 1-2. Overview of a DAS 9200 with 92A90 Modules connected to an 88100 system.

Figure 1-3 shows another overview of the DAS 9200 connected to an 88100 system under test. This view is for a DAS 9200 configured with two 92A96 Modules.

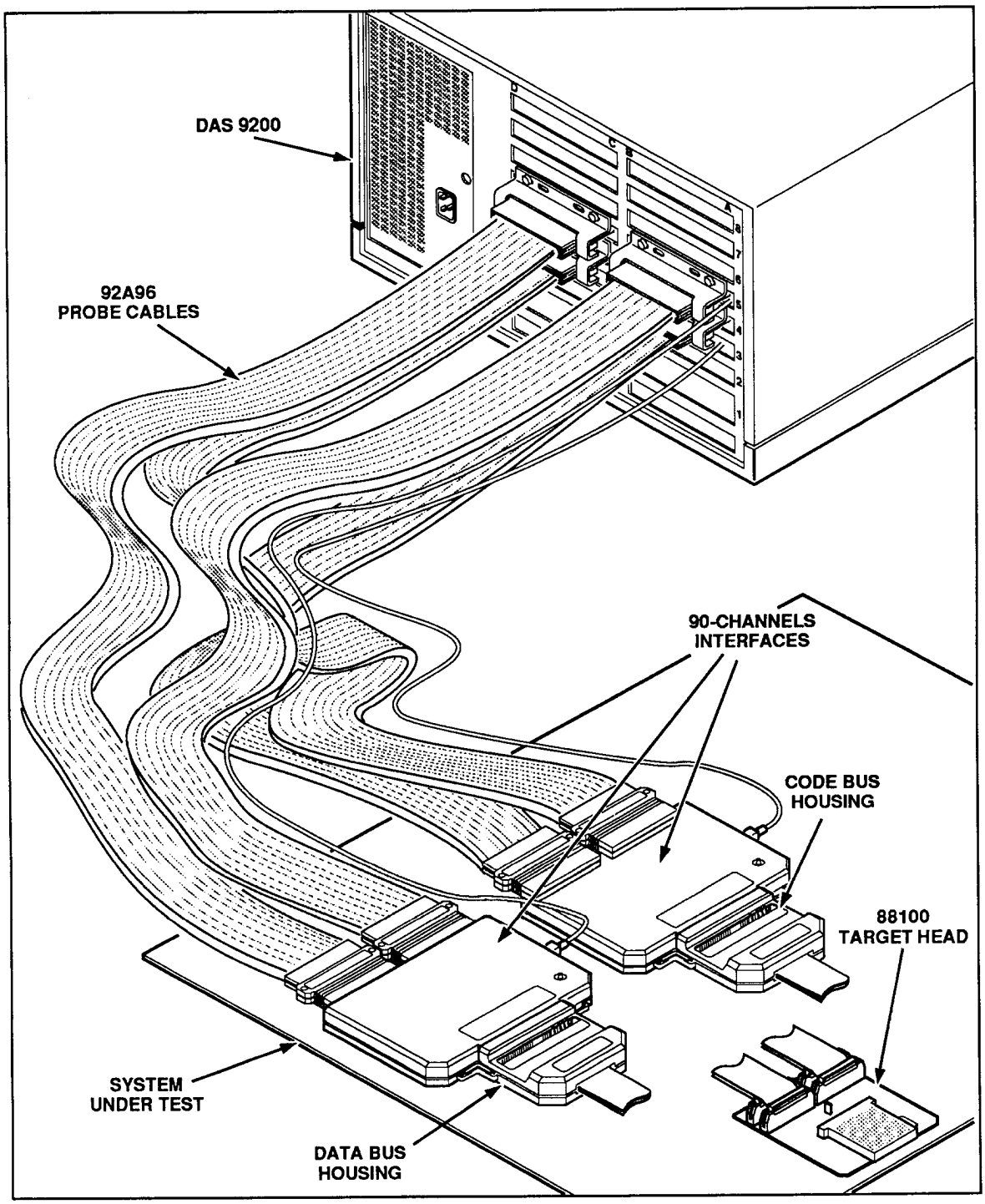

Figure 1-3. Overview of a DAS 9200 with 92A96 Modules connected to an 88100 system.

DIFFERENCES BETWEEN THE 92A96 AND 92A90 MODULES

If you have used a DAS 9200 with a 92A90 Module but haven't used a 92A96 Module, there are some key differences you should note. Table 1-1 lists the key differences.

Table 1-1
Differences Between 92A96 and 92A90 Data Acquisition Modules

Characteristic	92A96 Module	92A90 Module
Maximum synchronous data sampling rates	100 MHz	20 MHz
Memory depth	92A96 has 8K 92A96D has 32K	92A90 has 32K 92A90D has 128K
Physical connections to the probe adapter	4 probe cables connecting to 1 90-channel interface	3 cables connecting to 1 buffer probe
Clock channels	Not stored as data	Stored as data
Clock Menu selections	Custom, Internal, External	Micro, Internal, External, Demux
Flags	1 flag	2 flags
Counter/timers	2 counter/timers	3 counter/timers
Counter/timer width	32-bit counter/timer	24-bit counter/timer
Word/range recognizers	8 word and 0 range or 6 word and 1 range or 4 word and 2 range	16 word and 2 range

88100 SYSTEM REQUIREMENTS AND RESTRICTIONS

You should consider certain system requirements and restrictions of the 88100 microprocessor before operating the disassembler. You should also consider all electrical, environmental, and mechanical specifications in Appendix C as they pertain to your system under test. The remainder of this section describes other 88100 constraints.

System Clock Rate. The microprocessor support package supports the 88100 microprocessor running up to 33.3 MHz[1] for the 92A96 Modules and 20 MHz for the 92A90 Modules without HSMI or 33.3 MHz for the 92A90 Modules with HSMI.

[1] Specification at time of printing. Contact your DAS 9200 sales representative for current information on the fastest devices supported.

Probe Adapter Clearance. Your 88100 system must have a minimum amount of clear space surrounding the 88100 microprocessor to accommodate the probe adapter. Figure C-1 in *Appendix C: Service Information* gives these dimensions.

Probe Adapter Loading. Any electrical connection to your system adds an additional ac and dc load. The probe adapter was carefully designed to add the minimum possible load to your system. However, this additional load may affect the operation of the 88100 system in systems with extremely tight timing margins. Appendix C contains complete specifications on how the 92DM35A probe adapter affects your system.

Deskewing 92A90 Modules. If you are acquiring data from an 88100 system operating above 25 MHz, you must deskew the channels on the 92A90 Modules because of the extremely tight timing margins on the 88100 microprocessor. If you are acquiring data from an 88100 system operating at or below 25 MHz, you do not need to deskew the channels.

You do not need to deskew 92A96 Modules.

Section 2: QUICK START

If you are an experienced user of 92A90 or 92A96 Data Acquisition Modules, you can use this section to quickly set up your 88100 system and use it. Before setting up your system, read the discussion on *88100 System Requirements and Restrictions* in Section 1.

Symbol tables are presented at the end of this section for you to remove or photocopy. This provides you with an easy reference when setting up the Trigger menu using symbols. All of the symbol tables are duplicated in Section 3 in case they are lost or damaged after being removed.

CONFIGURING THE DAS 9200

You must make sure that the data acquisition modules are positioned correctly in the DAS 9200 in order for disassembly to be correct. When using the supplied cluster setups, the module in the lower-numbered slot acquires data from the code bus and is called the CodeBus module. The module in the higher-numbered slot acquires data from the data bus and is called the DataBus module.

Using 92A96 Modules. When using high-speed signals with 92A96 Modules, they must be positioned next to each other in the DAS 9200. Probe cables should be connected to the modules after you position the modules in the DAS 9200. Directions for connecting the probe cables and positioning the modules are in the module user's manual. Also, in a multimodule system, it is easier to identify which modules are connected to the probe adapter if slot number labels are applied to the module and DAS 9200. Applying slot number labels is shown in Figure 2-1.

Using 92A90 Modules. When using 92A90 Modules, you should connect the buffer probes at the same time that you position the modules in the DAS 9200. When using four 92A90 Modules to acquire data from an 88100 system operating above 20 MHz, the two DataBus modules must be in the same mainframe and the two CodeBus modules must be in the same mainframe, but the two DataBus modules can be in a separate mainframe from the two CodeBus modules.

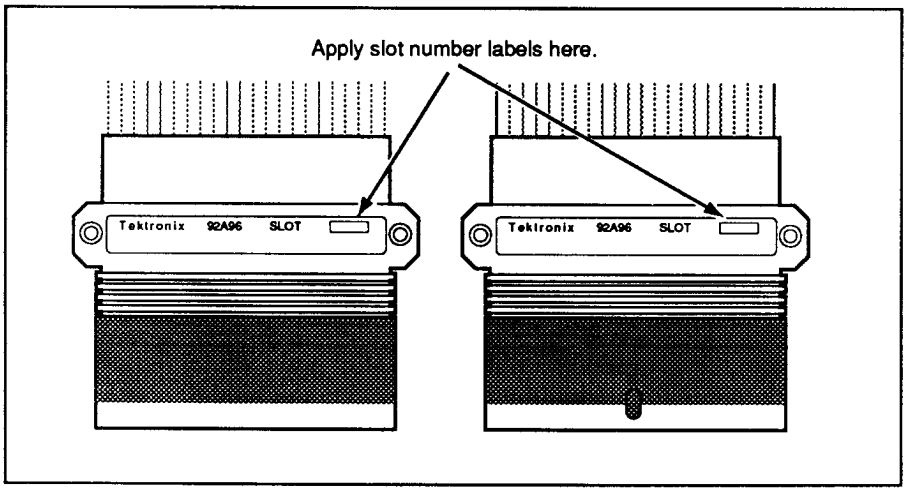

Figure 2-1. Applying slot number labels (92A96 only).

INSTALLING SOFTWARE

The DAS 9200 will not allow you to install 92DM35A software if 92DM35 software is already installed on the system. The DAS 9200 will not overwrite 92DM35 files with 92DM35A files. Therefore, you will have to remove 92DM35 software prior to installing 92DM35A software.

However, the DAS 9200 will overwrite 92DM35A files if you reinstall 92DM35 software. Be aware of this if you need to reinstall 92DM35 on a system that already has 92DM35A software installed on it.

To install the 88100 support software, follow these steps:

1. Power on the DAS 9200 and select the Disk Services menu.
2. Select Install Application and press F8: EXECUTE OPERATION.
3. Follow the on-screen prompts.

You may need to remove applications or files from the hard disk if there is not enough available disk free space to accommodate the microprocessor support files.

CONFIGURING THE PROBE ADAPTER

The 88100 microprocessor lets you select either Big- or Little-Endian byte ordering for data reads and writes. This allows the probe to correctly synthesize the low-order address bits (DA1, DA0). A jumper on the probe adapter, J1380, must be set to match the byte-ordering used in your 88100 system. Set J1380 in the BIG position to acquire data having Big-Endian byte ordering and in the LITTLE position to acquire data having Little-Endian byte ordering.

If your 88100 system changes the byte order dynamically, then you can also position the jumper so it does not synthesize DA0 and DA1 in either Big- or Little-Endian byte order. To do this, position J1380 on the center pin with one receptacle of the jumper remaining open. Using this jumper position means that the two lower-order address bits (DA0 and DA1) will always be acquired as 0. Be aware of this when specifying address values in your trigger program.

Figure 2-2 shows the location of J1380 on the probe adapter.

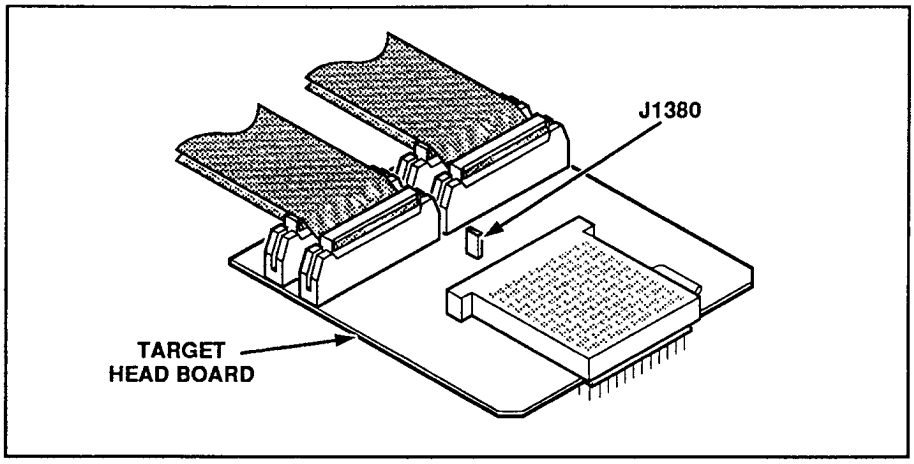

Figure 2-2. Location of J1380 on the probe adapter.

CONNECTING THE DAS 9200 TO THE 88100 SYSTEM

After the modules and buffer probes or probe cables are properly labeled and installed in the DAS 9200, you can complete the module-to-probe adapter connections.

You can move the byte-order jumper whenever you want but you should configure the probe adapter before placing it in the 88100 system. There may be inadequate space in which to change the position of the jumper after the probe adapter is in the system.

Placing the Probe Adapter in the 88100 System

To place the probe adapter in the system under test, refer to Figure 2-3 and follow this procedure:

1. Power down the DAS 9200 and your 88100 system.

CAUTION

Static-discharge can damage the 88100 microprocessor, probe adapter, or the 92A90 and 92A96 Modules. To prevent static damage, observe the following precautions while following all the connection procedure.

Handle the microprocessor only in a static-free environment.

Always wear a grounding wrist strap, or similar device, while handling the microprocessor and probe adapter.

2. Carefully remove the microprocessor. Be sure to follow standard static precautions while handling either the microprocessor or the probe adapter.
3. Carefully plug the probe adapter into the 88100 socket. Align pin A1 on the probe adapter to pin A1 on the 88100 system socket.
4. Open the ZIF socket by pulling the lever up and away from the socket.

CAUTION

You can damage the 88100 microprocessor if you do not orient it correctly. A1 is printed on the target head circuit board and an arrow indicates pin A1 on the ZIF socket. Figure 2-3 shows the proper alignment of pin A1 on the 88100 microprocessor, the ZIF socket, and the 88100 system socket.

5. Carefully plug the 88100 microprocessor into the ZIF socket. Align pin A1 on the 88100 to pin A1 of the socket.

6. Push the ZIF socket's lever down to lock the ZIF socket.

NOTE

If there is not enough vertical clearance in the 88100 system to accommodate the ZIF socket, you can remove it. If you remove the ZIF socket, be careful when inserting the 88100 directly on to the probe adapter circuit board.

7. Power on the DAS 9200.
8. Power on the 88100 system.

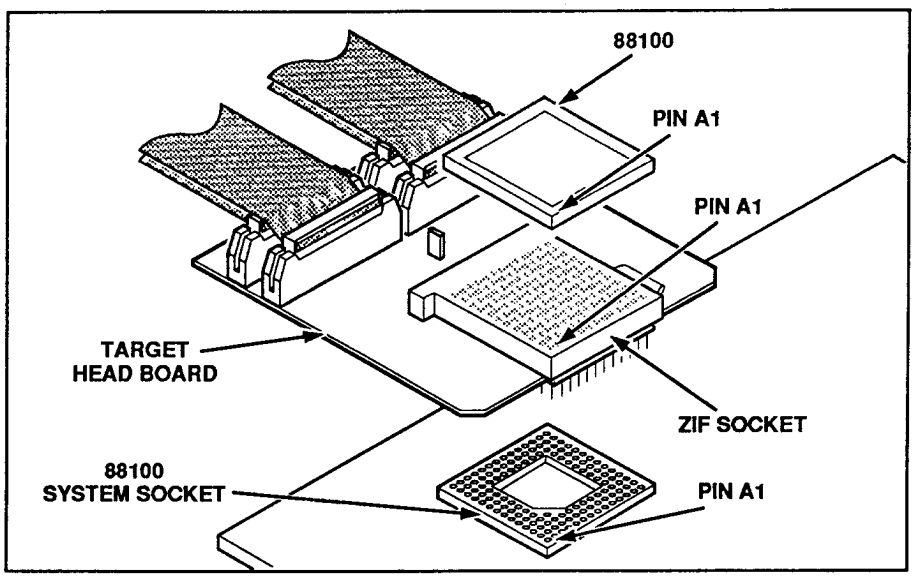

Figure 2-3. Placing the probe adapter in the 88100 system.

92A90 Module Connections

After you position the 92A90 Modules in the appropriate slots and connect the buffer probes, you can connect the buffer probes to the probe adapter. Be sure to set the byte-order jumper on the probe adapter and place the probe adapter in the 88100 system before you complete the connections.

To acquire data from an 88100 system operating above 25 MHz, you must deskew each module and save the values in deskew values files, or restore previously saved deskew values files before connecting the buffer probes to the probe adapter. You do not have to deskew the modules if you are acquiring data from an 88100 system operating at or below 25 MHz. If you are not familiar with deskewing 92A90 Modules, refer to the discussion on *Deskewing 92A90 Modules* in Section 3.

If you are using two or four 92A90 Modules to acquire data from an 88100 system operating above 20 MHz, you will also have to connect one or two HSMIs.

You can also connect the auxiliary channels on the probe adapter to acquire data from other signals in your 88100 system. For directions on how to connect 88100 signals to these channels, refer to *Auxiliary Channel Connections* later in this section .

Buffer Probe Connections

To connect the buffer probes to the probe adapter housings, refer to Figure 2-4 and follow this procedure:

1. Align the connector from the buffer probe connected to the CodeBus module (lower-numbered slot) with the connector on the target head labeled CODE BUS and connect them.
2. Align the connector from the buffer probe connected to the DataBus module (higher-numbered slot) with the connector on the target head labeled DATA BUS and connect them.
3. Press the Probe ID button on each buffer probe to confirm that the connections are correct. A message appears such as **Module:DataBus Pod:6A Pod 1D pressed**, where Module is the module name and Pod:6A is the slot number.
4. Attach the probe adapter retention clips to secure the connections between the buffer probes and probe adapter.

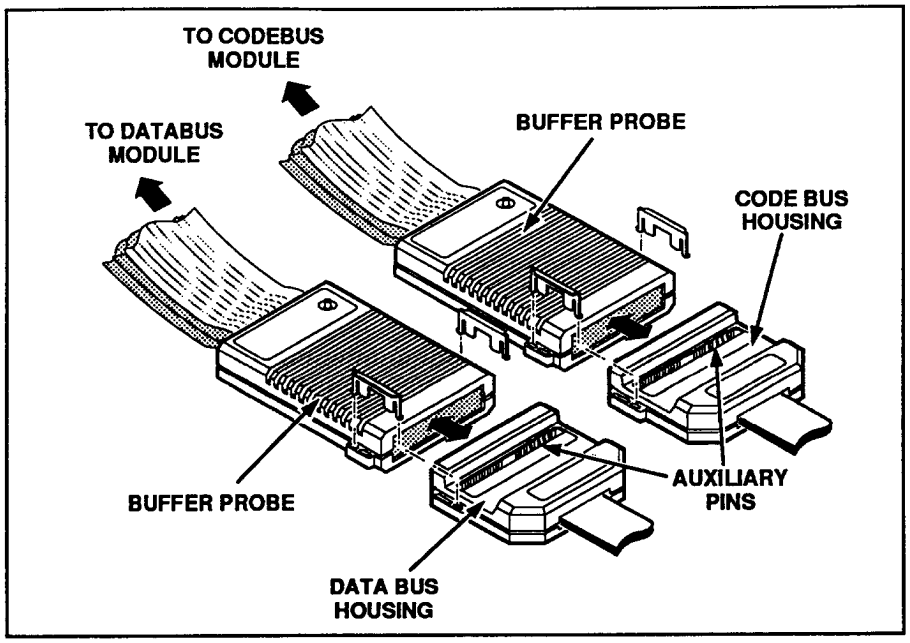

Figure 2-4. Buffer probes connections. These connections are used with 92A90 Modules.

HSMI Connections

If you are using a setup that uses an HSMI, refer to Figure 2-5 and follow these steps:

1. Connect the probe adapter cable connector for the desired 88100 bus to the single male connector on the HSMI.
2. Connect the two buffer probes from the assigned 92A90 Module to the two female connectors on the HSMI. The buffer probes can connect to either HSMI connector.

NOTE

If you are using an HSMI, make sure that the two 92A90 Modules designated as either the DataBus or the CodeBus module reside in the same DAS 9200 mainframe. However, if you are using four 92A90 Modules with two HSMIs, the two DataBus modules do not have to be in the same DAS 9200 mainframe as the two CodeBus modules.

3. Repeat steps 2 and 3 for the other 88100 bus if you are acquiring data from both buses.

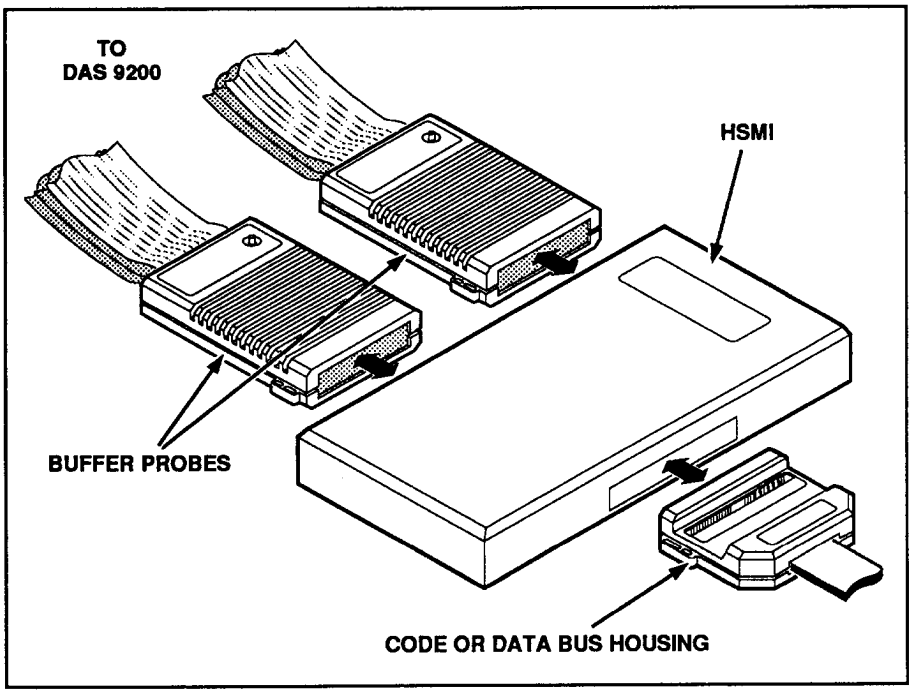

Figure 2-5. HSMI connections.

92A96 Module Connections

After the 92A96 Modules, probe cables, and the probe adapter are in place, you can connect the 90-channel interfaces. All four probe cables from one 92A96 Module connect to one 90-channel interface.

You do not have to deskew the 92A96 Modules.

To connect the probe cables to the 90-channel interfaces, refer to Figures 2-6 and 2-7, and follow this procedure:

NOTE

It is important to connect the probe cables to the 90-channel interface in a specific color sequence to avoid miskeying them. The sequence is orange, blue, green, and gray.

1. Match the orange label on the loose end of a 92A96 probe cable to the orange label on one of the 90-channel interface housings.
2. Line up the key and key slot and connect them.
3. Repeat steps 1 and 2 for each of the other three probe cables on that module. Connect the blue cable to the blue slot, the green cable to the green slot, and the gray cable to the gray slot. Make these connections in the color-keyed sequence exactly as described.
4. Connect the probe ID/power cord from the 92A96 Module to the corresponding 90-channel interface. Figure 2-6 shows the keying of the probe ID/power cord connectors on the 90-channel interface and the 92A96 Module.

NOTE

Be careful to match the keying on each end of the probe ID/power cord to the keying of the corresponding connector on the 90-channel interface and 92A96 Module.

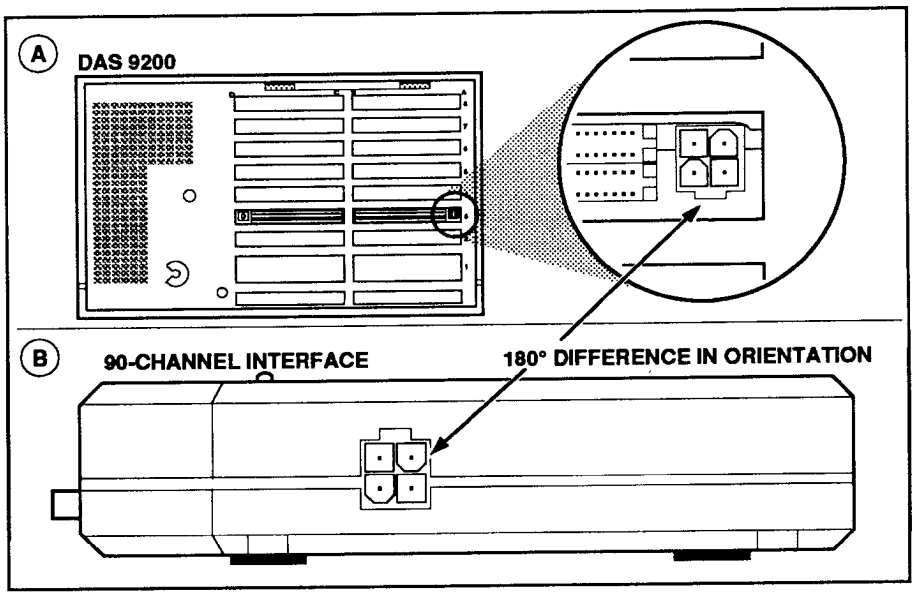

Figure 2-6. Keying of the connectors for the probe ID/power cord. The orientation between the two jacks is different because the 92A96 Module is positioned upside down in the mainframe.

5. Repeat steps 1 through 4 for the probe cables from the other 92A96 Module to the other 90-channel interface.

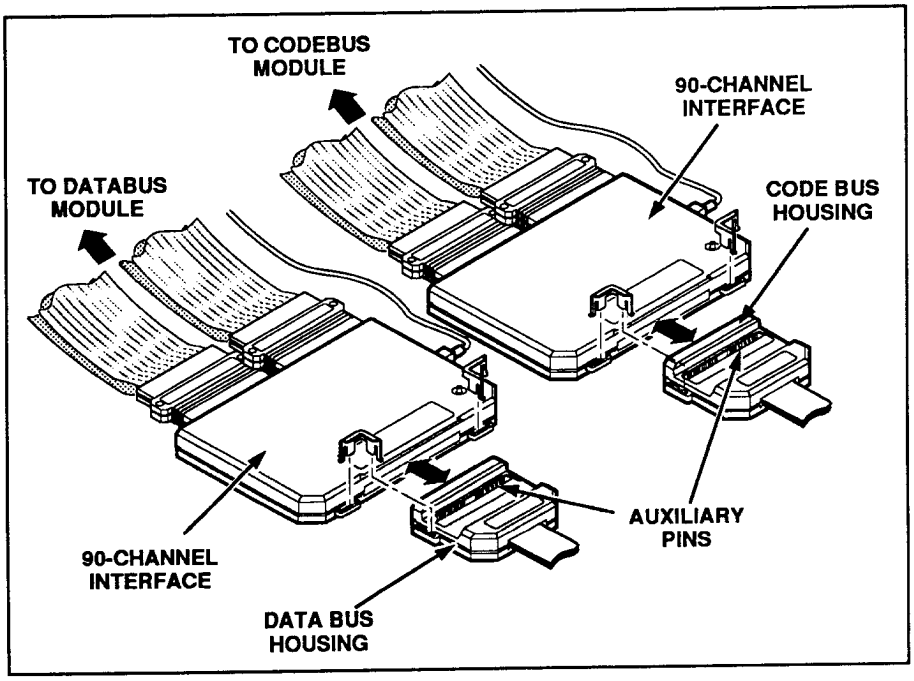

Figure 2-7. 90-channel interface connections. These connections are used with 92A96 Modules only.

To connect the 90-channel interfaces to the probe adapter, refer to Figure 2-7 and follow this procedure:

1. Align the connector from the 90-channel interface connected to the CodeBus module (lower-numbered slot) with the connector on the target head labeled CODE BUS and connect them.
2. Press the Probe ID button on the 90-channel interface to confirm that the connections are correct. A message appears such as **Module:DataBus Pod:6D Pod 1D pressed**, where Module is the module name and Pod:6D is the slot number.
3. Repeat steps 1 and 2 for the DataBus module, the target head connector labeled DATA BUS, and the other 90-channel interface.
4. Attach probe adapter retention clips to secure the connections between the 90-channel interfaces and probe adapter housings.

Auxiliary Channel Connections

To acquire data on the auxiliary channels, connect a 10-inch leadset (Tektronix part number 012-0747-00) to the row of pins on the probe adapter labeled either Aux1 or Aux0. Connect the other end of the leadset to other signals in your 88100 system. Figure 2-4 shows the location of the auxiliary pins on the probe adapter.

Make sure that the black wire of the leadset connects to channel 0. If you are not connecting to square pins in your system, you may need to attach grabber tips (Tektronix part number 020-1386-01) in order to make the connections. Be sure to connect at least one of the two wires connected to the auxiliary pins marked ground to the ground of the 88100 system.

When removing the 10-inch leadset from the probe adapter, do not pull on the wires. Instead, grasp and pull on the leadset's connector.

SETTING UP THE DISASSEMBLER

To set up the disassembler, perform the following steps:

1. Restore one of the five cluster setups provided with the disassembler software. Select the Save/Restore menu and select Restore Setup in the Operation field. Move the cursor to select the file to restore. Your choices are the 88100_CD90, 88100_CC, 88100_DD, 88100_CCDD, or 88100_CD96 setup files. The 88100_CC, 88100_DD, and 88100_CCDD files are for use with 92A90 Modules to acquire data from an 88100 system operating above 20 MHz with HSMIs.

   Press F8: EXECUTE OPERATION. When you do this, the Channel, Clock, and Trigger menus for both the CodeBus and DataBus modules will be set up for microprocessor support.

   When restoring the 88100_CC, 88100_DD, or 88100_CCDD cluster setup files, the existing deskew values are overwritten with default values. If you are operating above 25 MHz, you must deskew the 92A90 Modules or restore the deskew values from the deskew values files after restoring the 88100_CC, 88100_DD, or 88100_CCDD setup. Refer to *Restoring Deskew Values from a File* in Section 3 for directions on how to do this.

   If you are using one module, access the Configuration menu and select 88100C Support or 88100D Support in the Software Support field. When you do this, the Channel, Clock, and Trigger menus for the CodeBus or DataBus module will be set up for microprocessor support.

   Two or three 92A96 Modules in adjacent slots are automatically formed into a multicard module by the system software at power up. If you need to use one 92A96 Module from a multicard module, you must reconfigure the DAS 9200 accordingly prior to selecting software support in the 92A96 Configuration menu. If you restore a supplied cluster setup, the reconfiguration is done for you. Refer to the discussion of the System Configuration menu in the *DAS 9200 System User's Manual* for details on how to reconfigure multicard modules.

   NOTE

   Remember to read the discussion 88100 System Requirements and Restrictions *in Section 1 prior to setting up the 92A90 and 92A96 Modules for disassembly.*

NOTE

Do not disturb the C_Addr, C_Data, or C_Ctrl, groups for the CodeBus module (in the Channel menu) or the D_Addr, D_Data, D_Size, or D_Ctrl groups for the DataBus module (in the Channel menu), or the channel assignments within them while using the disassembler. Changing these groups causes invalid instruction mnemonics disassembly. You can find the channel group definitions and channel assignments in Appendix C.

2. If you want to acquire all cycles, you must change the clocking Cycles Included option in the Clock menu. The default clocking is to acquire valid cycles only. Refer to Appendix B for a description of how cycles are sampled. When using HSMIs, the clocking selection must match on both CodeBus modules or on both DataBus modules for disassembly to function properly.

   If you are using 92A90 Modules, you must make another selection for the 88100 Probe Adapter option: Without HSMI (≤20 MHz) or With HSMI (any clock rate). The option must match the actual hardware configuration for the acquisition to be valid. The default is Without HSMI.

3. Select the Trigger menu if you want to change the trigger program. The default trigger program will trigger on the first address sample acquired after pressing F1: START.

   When using HSMIs, the trigger program must be the same on both CodeBus and on both DataBus modules.

Tables 2-1 and 2-2 are symbol tables intended for you to remove or photocopy and use while performing disassembly.

ACQUIRING AND DISPLAYING DATA

After completing the DAS 9200 and probe adapter setups, you can acquire and display data. To acquire and view instruction mnemonics, perform the following steps:

1. Press F1: START on the DAS 9200 from any setup or display menu.
2. Power on and start running the 88100 system. (You can also power on the 88100 system before pressing F1: START on the DAS 9200.)

After satisfying the trigger program and filling acquisition memory, the DAS 9200 will display data in the default State menu. You may need to press F1: STOP if the stop conditions are not met.

3. Select the Disasm menu from the Menu Selection overlay to view instruction mnemonics.

The Disassembly menu displays the disassembled data in different formats:

- Hardware format shows instruction mnemonics on instruction Fetch cycles and cycle-type information for all other acquired cycles.
- Software format shows only instruction fetches; all other cycle types are suppressed such as data reads, data writes and flushed instruction cycles.
- Control Flow format shows only instructions that change the control flow such as branches, jumps, returns, and traps.
- Subroutine format shows only subroutine calls such as BSR, JSR, RTE, and traps.

Refer to *Appendix A: Error Messages and Disassembly Problems* if there are problems acquiring instruction mnemonics.

This is the end of the *Quick Start* section.

Table 2-1
C_Ctrl Group Symbol Table for the Code Bus (88100C_CTL))

Symbol*	C_Ctrl Group Value CS/U~ CFETCH INT	RST~ ERR CR1 CR0	Meaning
SUPR_FETCH	1 1 X	1 X 1 0	Supervisor fetch cycle
USER_FETCH	0 1 X	1 X 1 0	User fetch cycle
FETCH	X 1 X	1 X 1 0	Any fetch cycle
FAULT	X 1 X	1 X 1 1	Fault reply
WAIT	X 1 X	1 X 0 1	Wait reply
RESERVED	X 1 X	1 X 0 0	Reserved reply
SUCCESS	X 1 X	1 X 1 0	Success reply
SUPR	1 1 X	1 X X X	Supervisor mode (any reply)
USER	0 1 X	1 X X X	User mode (any reply)
NULL	X 0 X	1 X X X	Null cycle, no instruction fetch, no reply
RESET	X X X	0 X X X	CPU reset input
INT	X X 1	X X X X	CPU interrupt input
ERR	X X X	X 1 X X	Master/Checker error

*The Symbol Editor shows symbols with colons; these are combinations of the symbols in this table.

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Table 2-2
D_Ctrl Group Symbol Table for the Data Bus (88100D_CTL)

Symbol*	D_Ctrl Group Value DS/U~ DLOCK~ DR/W~	DNULL~ ERR_LATE RST~	ERR DR1 DR0	Meaning
SUPR_LOCK_RD	1 0 1	1 X 1	X 1 0	Supervisor locked read cycle (success)
SUPR_LOCK_WR	1 0 0	1 X 1	X 1 0	Supervisor locked write cycle (success)
USER_LOCK_RD	0 0 1	1 X 1	X 1 0	User locked read cycle (success)
USER_LOCK_WR	0 0 0	1 X 1	X 1 0	User locked write cycle (success)
LOCK_RD	X 0 1	1 X 1	X 1 0	Any locked read cycle (success)
LOCK_WR	X 0 0	1 X 1	X 1 0	Any locked write cycle (success)
SUPR_RD	1 X 1	1 X 1	X 1 0	Supervisor read cycle (success)
SUPR_WR	1 X 0	1 X 1	X 1 0	Supervisor write cycle (success)
USER_RD	0 X 1	1 X 1	X 1 0	User read cycle (success)
USER_WR	0 X 0	1 X 1	X 1 0	User write cycle (success)
RD	X X 1	1 X 1	X 1 0	Any read cycle (success)
WR	X X 0	1 X 1	X 1 0	Any write cycle (success)
FAULT	X X X	1 X 1	X 1 1	Fault reply
WAIT	X X X	1 X 1	X 0 1	Wait reply
RESERVED	X X X	1 X 1	X 0 0	Reserved reply
SUCCESS	X X X	1 X 1	X 1 0	Success reply
SUPR_LOCK	1 0 X	1 X 1	X X X	Supervisor locked bus cycle
USER_LOCK	0 0 X	1 X 1	X X X	User locked bus cycle
LOCK	X 0 X	1 X 1	X X X	Any locked bus cycle
SUPR	1 X X	1 X 1	X X X	Supervisor address mode
USER	0 X X	1 X 1	X X X	User address mode
NULL	X X X	0 X 1	X X X	Null cycle; no read/write; no reply
RESET	X X X	X X 0	X X X	CPU Reset Input
WDE	X X 0	1 1 1	X X X	Write Data Error
ERR	X X X	X X X	1 X X	Master/Checker Error

*The Symbol Editor shows symbols with colons; these are combinations of the symbols in this table.

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Section 3: INSTALLATION AND CONNECTIONS

This section contains detailed descriptions of how to do the following:

- configure the DAS 9200
- position the modules in the DAS 9200
- install the disassembler software
- view the demonstration reference memory
- set up the disassembler software
- configure the probe adapter
- connect the DAS 9200 to the 88100 system

You can install the software either before or after installing the modules or connecting the probe adapter to the 88100 system. The byte-order jumper on the probe adapter should be configured before placing the probe adapter in your 88100 system.

CONFIGURING THE MODULES

Included with the microprocessor support software are five multimodule setups that simplify preparation when you are acquiring data from more than one bus. You can also create your own setups and save them for later use. This discussion describes the multimodule setups provided with the disassembler, the requirements for using these setups, and creating your own setups.

You must make sure that the data acquisition modules are positioned correctly in the DAS 9200 in order for disassembly to be correct. When using high-speed signals with 92A96 Modules, the modules must be positioned next to each other in the DAS 9200. When using four 92A90 Modules to acquire data from an 88100 system operating above 20 MHz, the two DataBus modules must be in the same mainframe and the two CodeBus modules must be in the same mainframe, but the DataBus modules and the CodeBus modules can be in separate mainframes.

When using the supplied cluster setups, the module in the lower-numbered slot acquires data from the code bus and is called the CodeBus module. The module in the higher-numbered slot acquires data from the data bus and is called the DataBus module.

INSTALLING SOFTWARE

The disassembler software sets up the DAS 9200 to acquire, disassemble, and display data from an 88100 system. To install the software, the application files on the 5 1/4-inch floppy disk must be copied to the DAS 9200 hard disk. You cannot execute the disassembler from the floppy disk.

The DAS 9200 will not allow you to install 92DM35A software if 92DM35 software is already installed on the system. The DAS 9200 will not overwrite 92DM35 files with 92DM35A files. Therefore, you will have to remove 92DM35 software prior to installing 92DM35A software.

However, the DAS 9200 will overwrite 92DM35A files if you reinstall 92DM35 software. Be aware of this if you need to reinstall 92DM35 on a system that already has 92DM35A software installed on it.

To install the software, follow these steps:

1. Power on the DAS 9200 and press the Select Menu key.
2. Select the Disk Services menu in the Utilities column.
3. Press the Return key.
4. Select Install Applications in the Operation field.
5. Press F8: EXECUTE OPERATION and follow the on-screen prompts.

If there is inadequate disk free space available on the hard disk, you must use the Remove Application or Delete File function of the Disk Services menu to free up enough disk space to install the software. The approximate space required to install the software is listed on the label of the 92DM35A floppy disk.

After the DAS 9200 successfully copies the application files from the floppy disk to the hard disk, the message **Application installation complete with no errors** appears on your screen. Remove the floppy disk and store it in a safe place in case you need to reinstall the software.

If you would like to see an example of 88100 bus activity with mnemonic disassembly, read the next discussion and procedure.

Viewing the Refmem File

A reference memory file is provided so you can become familiar with the way the disassembler displays 88100 cycle types and instruction mnemonics. You can select the reference memory file to see how 88100 mnemonics are displayed without making any of the DAS 9200 connections to the system under test.

The 88100_Demo reference memory file is automatically installed when the disassembler software is installed on the hard disk. A symbol table file for the C_Addr group (called 88100_Demo) is also automatically installed and is valid only for the 88100_Demo reference memory file. All of the figures in Section 4 showing acquired data are from these files. The data you acquire from your 88100 system will be different.

To view the 88100_Demo Refmem, use the following procedure:

1. Press the Select Menu key to return to the Menu Selection overlay.
2. Move the cursor to the Refmem column and select the 88100_Demo file.
3. Move the cursor to the Display column and select Disasm.
4. Press the Return key to view the reference memory.

You can change the format of disassembled data from the Disassembly Format Definition overlay, which you can access through the Disassembly menu. Hardware disassembly is the default format in the Disassembly menu. Examples of the disassembly formats are found under *Display Formats* in Section 4.

If there is not enough free space left on the hard disk, you can delete the 88100_Demo files. They are presented strictly for viewing and are not necessary to the operation of the disassembler.

Setting Up Disassembler Software

The microprocessor support package supplies the disassembler software and setup files for the data acquisition module to use to acquire and display instruction mnemonics. Predefined cluster setup files supply setups for the Configuration, Channel, Clock, and Trigger menus for the various combinations of data acquisition modules. Symbol table files are supplied for displaying data in the State menu and to use in the Trigger menu as word recognizer values.

Before selecting and setting up the disassembler, read the descriptions of *88100 System Requirements and Restrictions* in Section 1.

You can select the disassembler and its associated setup files by restoring one of the supplied cluster setup files. Refer to the procedure in *Restoring and Using a Multimodule Setup* later in this section.

When there are two or three 92A96 Modules in adjacent slots they are automatically formed into a multicard module by the system software at power up. If you need to use one 92A96 Module from a multicard module, you must reconfigure the DAS 9200 accordingly prior to selecting software support in the 92A96 Configuration menu. If you restore a supplied cluster setup, the reconfiguration is done for you. Refer to the discussion of the System Configuration menu in the *DAS 9200 System User's Manual* for details on how to reconfigure multicard modules.

Single Module Setup

If you are using one module, access the Configuration menu and select 88100C Support or 88100D Support in the Software Support field. When you do this, the Channel, Clock, and Trigger menus for the CodeBus or DataBus module will be set up for microprocessor support.

Multimodule Setup

When you select a multimodule setup the DAS 9200 automatically will do the following:

- cluster and correlate 92A90 Modules or 92A96 Modules
- designate the module in the lower-numbered slot as the CodeBus module and the module in the higher-numbered slot as the DataBus module
- select the appropriate software support for each module
- define two communication signals for use in the trigger programs of the modules called C-to-D and D-to-C
- define triggering for each module using one of the two communication signals, C-to-D or D-to-C

The clustered module setup files provided with the disassembler software are called 88100_CD90, 88100_CC, 88100_DD, 88100_CCDD, and 88100_CD96. These setups configure the DAS 9200 to acquire data using at least two modules from either the code bus, the data bus, or both buses of the 88100.

If both modules are not the same memory depth, the deeper module should be used as the CodeBus module and the shallower module should be used as the DataBus module.

88100_CD90. The 88100_CD90 setup configures the DAS 9200 to acquire data from both the code and data buses of an 88100 system operating at or below 20 MHz using two 92A90 Modules with no HSMIs.

88100_CC. The 88100_CC setup configures the DAS 9200 to acquire data from the code bus of an 88100 system operating above 20 MHz using two 92A90 Modules with an HSMI.

88100_DD. The 88100_DD setup configures the DAS 9200 to acquire data from the data bus of an 88100 system operating above 20 MHz using two 92A90 Modules with an HSMI.

88100_CCDD. The 88100_CCDD setup configures the DAS 9200 to acquire data from both the code and data buses of an 88100 system operating above 20 MHz using four 92A90 Modules with two HSMIs. The two DataBus modules must be in the same mainframe and the two CodeBus modules must be in the same mainframe but the two DataBus modules can be in a separate mainframe from the two CodeBus modules.

88100_CD96. The 88100_CD96 setup configures the DAS 9200 to acquire data from both the code and data buses of an 88100 system at any clock rate using two 92A96 Modules. When using high-speed signals with 92A96 Modules, the modules must be positioned next to each other in the DAS 9200.

Restoring and Using a Multimodule Setup

To restore and use a multimodule setup, refer to Figure 3-1 and follow these steps:

1. Select the Save/Restore menu.
2. Press the Return key.
3. Select Restore Setup in the Operation field.
4. Select the desired setup in the File field. Five cluster setup files are supplied with the disassembler software. They are the 88100_CD90, 88100_CC, 88100_DD, 88100_CCDD, and 88100_CD96 files.
5. Press F8: EXECUTE OPERATION.

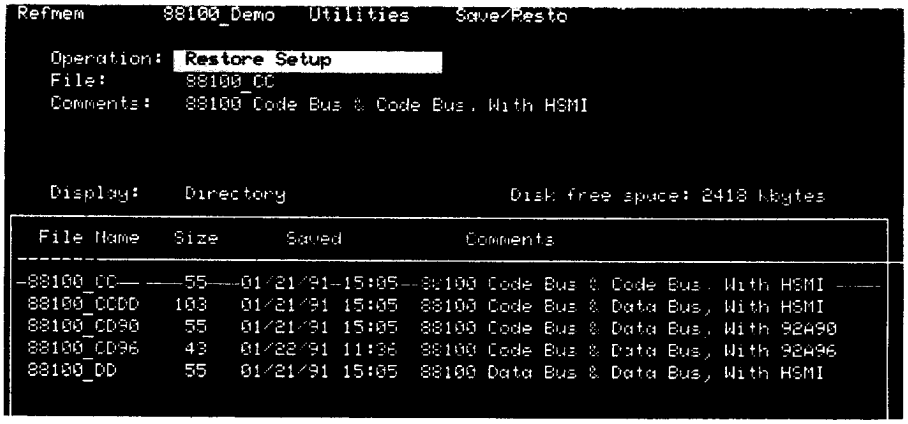


Figure 3-1. Save/Restore menu. The setups listed in the directory are included with the disassembler software.

The DAS 9200 automatically configures itself for multimodule operation. If the current placement of the data acquisition modules does not match that of the setup selected, the Restore Formation overlay appears. Press the F4: PLACE MODULES key or use the overlay to assign the module setups to the current placement of the data acquisition modules. This applies to all versions of any data acquisition module.

When restoring the 88100_CC, 88100_DD, or 88100_CCDD cluster setup files, the existing 92A90 deskew values are overwritten with default values. You must restore the deskew values from the deskew values files after restoring the 88100_CC, 88100_DD, or 88100_CCDD setup to override the default values. Refer to *Restoring Deskew Values from a File* in this section for directions on how to do this.

If you are using 92A90D modules when you restore a setup, the 92A90D's default memory depth is set to 32K. If you are using 92A96D modules when you restore a setup, the 92A96D's default memory depth is set to 8K. To use a greater memory depth, select a higher value in the Acquisition Memory Size field of the Configuration menu for each deep module.

Creating Multimodule Setups

You can create setups that meet the needs of your specific application. For example, you can create a setup that provides additional inter-module communication signals for use in more complex trigger programs, or a setup to acquire data from multiple 88100 microprocessors.

To create a new setup using the 88100 disassembler, you must first install the software and its associated files on your DAS 9200. Refer to the discussion on *Installing Software* in this section for directions on how to do this. After installing the software, you should select the pre-defined multimodule setup that most closely applies to your DAS 9200 setup. If need be, you can change the setup, name the modified setup, and save it.

If you create a new cluster, certain naming conventions must be followed when naming the modules. You must use the names the disassembler assigned to the modules (CodeBus and DataBus) but you can add a suffix. The same suffix must be used for each module for each 88100 being disassembled; for example, CodeBusNew and DataBusNew.

When operating above 20 MHz with the 92A90 Module and an HSMI, the names the disassembler assigns to the modules are CodeBus2 and DataBus2. When operating without an HSMI for multiple 88100s, do not use 2 in the suffix. Keep this in mind if you are creating a cluster setup without basing it on a supplied cluster setup.

You must also correlate the data between two modules. To correlate data from the two modules, refer to Figure 3-2 and use the following procedure:

1. Select the Cluster Setup menu from the Menu Selection overlay.
2. Press F4: DEFINE CORRELATN to access the Correlation Definition overlay.
3. Open the Correlate field, select the CodeBus module, and close the field.
4. Press F7: ADD CORR. A second field appears under the first.
5. Open the second field, select the DataBus module, and close the field.
6. Press F8: EXIT & SAVE and return to the Menu Selection overlay by pressing the Select Menu key.

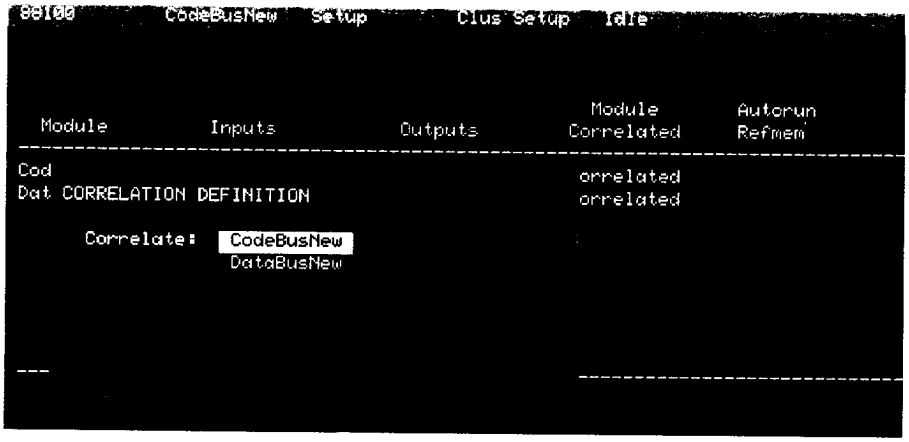


Figure 3-2. Correlation Definition overlay.

You must also define signals to use between two modules. To define signals for the two modules, refer to Figure 3-3 and use the following procedure:

1. Select the Cluster Setup menu from the Menu Selection overlay.
2. Press F2: DEFINE SIGNAL to access the Signal Definition overlay.
3. Press F7: ADD SIGNAL. A signal name field appears.
4. Enter the name of the signal and press Return.
5. Define the signals as either input or output in the Direction field and press Return.
6. Do not change the selection for the Type field.

   For information on any of these fields, refer to the *DAS 9200 System User's Manual.*
7. Press F8: EXIT & SAVE and return to the Menu Selection overlay to reconfigure the system with signals defined for correlated CodeBus and DataBus modules.

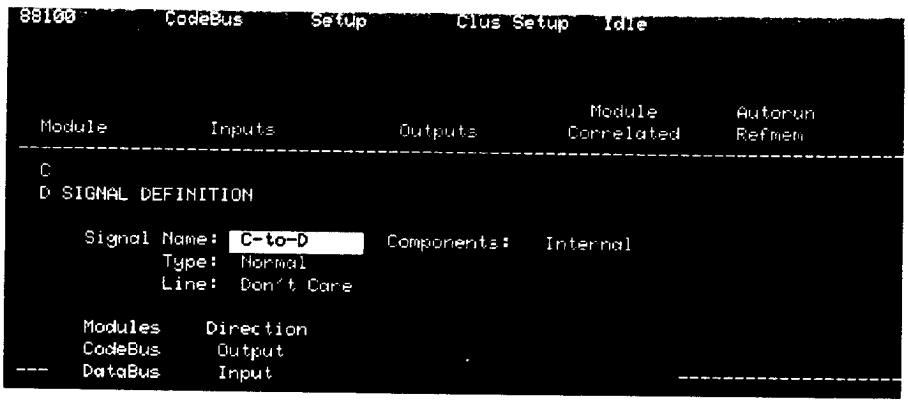


Figure 3-3. Signal Definition overlay.

To complete the setup, you must select 88100C Support for each of the CodeBus modules and 88100D Support for each of the DataBus modules in the Configuration menu.

When two or three 92A96 Modules are in adjacent slots they are automatically formed into a multicard module by the system software at power up. If you need to use two 92A96 Modules from a multicard module, you must reconfigure the DAS 9200 accordingly prior to selecting software support in the 92A96 Configuration menu. Refer to the discussion of the System Configuration menu in the *DAS 9200 System User's Manual* for details on how to reconfigure multicard modules.

Use the Save Cluster Setup operation of the Save/Restore menu to save the setup for later use.

To save deskew values for 92A90 Modules, refer to the discussion on *Deskewing Modules and Saving the Values to a File*, later in this section.

What You Can Change During Setup

You can change part of the module setup without affecting disassembly. You can change the trigger program in the Trigger menu and the display radix for any channel group in the Channel menu. Any change to the radix of the D_Data group will only affect the Trigger and State menus, not the Disassembly menu. You can change the clocking selection for the Cycles Included option field to Valid Cycles Only or All Cycles without affecting the disassembler.

If you are using 92A90 Modules, you must make another selection for the 88100 Probe Adapter option: Without HSMI (≤20 MHz) or With HSMI (any clock rate). The option must match the actual hardware configuration for the acquisition to be valid. The default is Without HSMI.

You can change the channel grouping and name of the C_Misc, C_Aux1, C_Aux0, D_Misc, D_Aux1, and D_Aux0 groups and not affect disassembly. You can also delete any of these groups.

You cannot change the channel grouping or the name of the C_Addr, C_Data, C_Ctrl, D_Addr, D_Data, D_Size, and D_Ctrl groups, the threshold voltage, polarity, or clocking selection (Micro or Custom), and expect the disassembler to function properly.

Channel Groups and Assignments

The disassembler relies on the presence of the signals and channel groups defined by the support software for the C_Addr, C_Data, and C_Ctrl groups of the CodeBus module and on the D_Addr, D_Data, D_Size, and D_Ctrl groups of the DataBus module. The channel assignment table used in 88100 setups is located in Appendix C.

Symbol Tables

You can use symbol tables to display channel group information symbolically in the State menu and to control triggering.

The microprocessor support software contains symbol table files for the C_Ctrl and D_Ctrl channel groups. The file names are 88100C_CTL and 88100D_CTL. These symbol tables assign symbolic names to combinations of signal values within the C_Ctrl and D_Ctrl channel groups. Refer to *Displaying the C_Addr or D_Addr Group Symbolically* in Section 4 for a description of how to display the Address group symbolically.

Table 3-1 shows the name, bit pattern, and meaning for the symbols in the file 88100C_CTL, the C_Ctrl group symbol table for the CodeBus module.

Table 3-1
C_Ctrl Group Symbol Table for the Code Bus (88100C_CTL))

Symbol*	C_Ctrl Group Value CS/U~ CFETCH INT	RST~ ERR CR1 CR0	Meaning
SUPR_FETCH	1 1 X	1 X 1 0	Supervisor fetch cycle
USER_FETCH	0 1 X	1 X 1 0	User fetch cycle
FETCH	X 1 X	1 X 1 0	Any fetch cycle
FAULT	X 1 X	1 X 1 1	Fault reply
WAIT	X 1 X	1 X 0 1	Wait reply
RESERVED	X 1 X	1 X 0 0	Reserved reply
SUCCESS	X 1 X	1 X 1 0	Success reply
SUPR	1 1 X	1 X X X	Supervisor mode (any reply)
USER	0 1 X	1 X X X	User mode (any reply)
NULL	X 0 X	1 X X X	Null cycle, no instruction fetch, no reply
RESET	X X X	0 X X X	CPU reset input
INT	X X 1	X X X X	CPU interrupt input
ERR	X X X	X 1 X X	Master/Checker error

*The Symbol Editor shows symbols with colons; these are combinations of the symbols in this table.

Table 3-2 shows the name, bit pattern, and meaning for the symbols in the file 88100D_CTL, the D_Ctrl group symbol table for the DataBus module.

Table 3-2
D_Ctrl Group Symbol Table for the Data Bus (88100D_CTL))

Symbol*	D_Ctrl Group Value DS/U~ DNULL~ ERR DLOCK~ ERR_LATE DR1 DR/W~ RST~ DR0	Meaning
SUPR_LOCK_RD	1 0 1 1 X 1 X 1 0	Supervisor locked read cycle (success)
SUPR_LOCK_WR	1 0 0 1 X 1 X 1 0	Supervisor locked write cycle (success)
USER_LOCK_RD	0 0 1 1 X 1 X 1 0	User locked read cycle (success)
USER_LOCK_WR	0 0 0 1 X 1 X 1 0	User locked write cycle (success)
LOCK_RD	X 0 1 1 X 1 X 1 0	Any locked read cycle (success)
LOCK_WR	X 0 0 1 X 1 X 1 0	Any locked write cycle (success)
SUPR_RD	1 X 1 1 X 1 X 1 0	Supervisor read cycle (success)
SUPR_WR	1 X 0 1 X 1 X 1 0	Supervisor write cycle (success)
USER_RD	0 X 1 1 X 1 X 1 0	User read cycle (success)
USER_WR	0 X 0 1 X 1 X 1 0	User write cycle (success)
RD	X X 1 1 X 1 X 1 0	Any read cycle (success)
WR	X X 0 1 X 1 X 1 0	Any write cycle (success)
FAULT	X X X 1 X 1 X 1 1	Fault reply
WAIT	X X X 1 X 1 X 0 1	Wait reply
RESERVED	X X X 1 X 1 X 0 0	Reserved reply
SUCCESS	X X X 1 X 1 X 1 0	Success reply
SUPR_LOCK	1 0 X 1 X 1 X X X	Supervisor locked bus cycle
USER_LOCK	0 0 X 1 X 1 X X X	User locked bus cycle
LOCK	X 0 X 1 X 1 X X X	Any locked bus cycle
SUPR	1 X X 1 X 1 X X X	Supervisor address mode
USER	0 X X 1 X 1 X X X	User address mode
NULL	X X X 0 X 1 X X X	Null cycle; no read/write; no reply
RESET	X X X X X 0 X X X	CPU Reset Input
WDE	X X 0 1 1 1 X X X	Write Data Error
ERR	X X X X X X 1 X X	Master/Checker Error

*The Symbol Editor shows symbols with colons; these are combinations of the symbols in this table.

Copying and Editing Predefined Symbol Tables

You cannot directly edit any symbol tables supplied by microprocessor support. But you can copy a predefined symbol table and then edit the copy for your specific use.

To create a new symbol table, follow these steps:

1. Select the Symbol Editor menu.
2. Press F2: FILE FUNCTIONS.
3. Select Open File in the Function field.
4. Select New File in the Edit Status field.
5. Enter a new symbol table file name in the New File Name field.
6. Select Pattern in the Table Type field to match the symbol table you are copying.
7. Press F5: EXECUTE FUNCTION.
8. Select Merge Files in the Function field.
9. Select the file to base your new symbol table on, such as the 88100C_CTL file, in the File Name to Merge In field.
10. Press F5: EXECUTE FUNCTION.
11. Press F8: EXIT & SAVE.
12. Edit the file as desired. Refer to your *DAS 9200 System User's Manual* for information on editing the symbol table.
13. Press the Select Menu key to return to the Menu Selection overlay.
14. Select the Channel menu.
15. Change the file name of the symbol table for the C_Ctrl group (or whichever group's symbol table you are replacing) to the one that you specified in step 5.

92A96 LABELS

When using 92A96 Modules, you should apply slot number labels to various parts of the modules and DAS 9200 as shown in Figure 3-4. These slot numbers will help you identify which modules are connected to the probe adapter in a multimodule system.

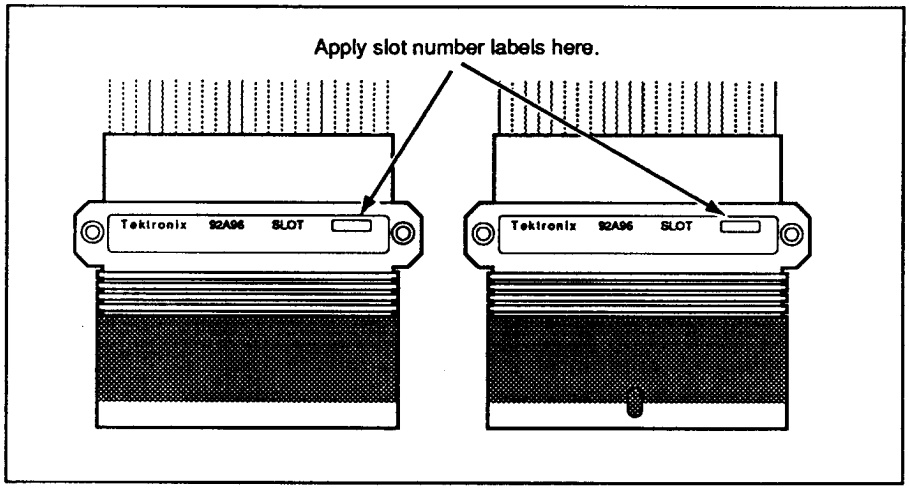


Figure 3-4. Applying slot number labels (92A96 only).

The probe connectors and cables for the 92A96 Module have color-coded labels. Table 3-3 shows the color of the probe connector and cable labels, as well as the module section and clock assignments.

Table 3-3
92A96 Label Information

Label Color	Sections	Clock
Orange	A0, A1, C0	Ck 0
Green	A2, A3, C1	Ck 1
Blue	D0, D1, C2	Ck 2
Gray	D2, D3, C3	Ck 3

CONFIGURING THE PROBE ADAPTER

There is one jumper that you need to configure on the probe adapter. It controls the synthesis of DA0 and DA1 according to the byte order of acquired data.

You can move the jumper whenever you want but you should configure the probe adapter before placing it in the 88100 system. There may be inadequate space in which to change the position of the byte-order jumper if you place the probe adapter in the 88100 system before configuring it.

The 88100 microprocessor supports either Big- or Little-Endian byte ordering for data reads and writes. A jumper on the probe adapter, J1380, can be set to match the byte-ordering used in your 88100 system. Set J1380 in the BIG position to acquire data having Big-Endian byte ordering and in the LITTLE position to acquire data having Little-Endian byte ordering.

If your 88100 system changes the byte order dynamically, then you can also position the jumper so it does not synthesize DA0 and DA1 in either Big- or Little-Endian byte order. To do this, position J1380 on the center pin with one receptacle of the jumper remaining open. Using this jumper position means that the two lower-order address bits (DA0 and DA1) will always be acquired as 0. Be aware of this when specifying address values in your trigger program.

Figure 3-5 shows the location of J1380 on the probe adapter.

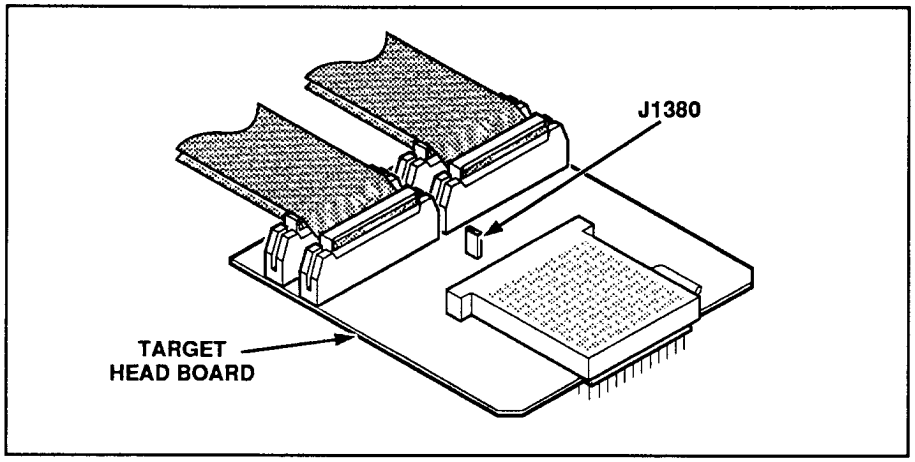


Figure 3-5. Location of J1380 on the probe adapter.

CONNECTING THE DAS 9200 TO THE 88100 SYSTEM

Before acquiring data you must connect the probe adapter to both the SUT, and to the buffer probes for the 92A90 Modules being used at or below 20 MHz, to the buffer probes and HSMIs for 92A90 Modules being used above 20 MHz, or to the 90-channel interfaces for the 92A96 Modules. Your 88100 system must have a minimum amount of clear space surrounding the 88100 microprocessor to accommodate the probe adapter. *Appendix C: Service Information* gives these dimensions.

CAUTION

Static-discharge can damage the 88100 microprocessor, probe adapter, or the 92A90 and 92A96 Modules. To prevent static damage, observe the following precautions while following all the connection procedures.

Handle the microprocessor only in a static-free environment.

Always wear a grounding wrist strap, or similar device, while handling the microprocessor and probe adapter.

This discussion describes how to do the following:

- configure and place the probe adapter in your SUT
- restore saved deskew values from a file or deskew 92A90 Modules when operating above 25 MHz
- connect the buffer probes to the 92A90 Modules and to the probe adapter, or connect the 90-channel interfaces to the 92A96 Modules and to the probe adapter
- connect the HSMI to the buffer probe for 92A90 Modules operating above 20 MHz
- connect the auxiliary channels on the probe adapter

Placing the Probe Adapter in the SUT

After the modules, buffer probes, and 90-channel interfaces are in place, and the probe adapter is configured, you can install the probe adapter in your 88100 system. To place the probe adapter in the SUT, refer to Figure 3-6 and follow this procedure:

1. Turn off the power to the SUT.
2. Carefully remove the microprocessor from your system.
3. Open the ZIF socket on the probe adapter by pulling the lever up and away from the socket.
4. Carefully plug the 88100 microprocessor into the ZIF socket, so that pin A1 of the microprocessor is inserted into pin A1 of the ZIF socket.

CAUTION

You can damage the 88100 microprocessor if you do not orient it correctly. A1 is printed on the target head circuit board and an arrow indicates pin A1 on the ZIF socket. Figure 3-6 shows the proper alignment of pin A1 on the 88100 microprocessor, the ZIF socket, and the 88100 system socket.

5. Push the ZIF socket's lever down to lock the ZIF socket in the closed position.
6. Carefully plug the probe adapter into the 88100 socket of the SUT. Be sure to align pin A1 of the probe adapter to pin A1 of the system socket.

NOTE

If there is not enough vertical clearance in the 88100 system to accommodate the ZIF socket, you can remove it. If you remove the ZIF socket, be careful when inserting the 88100 directly on to the probe adapter circuit board.

7. Power on the DAS 9200.
8. Power on the 88100 system.

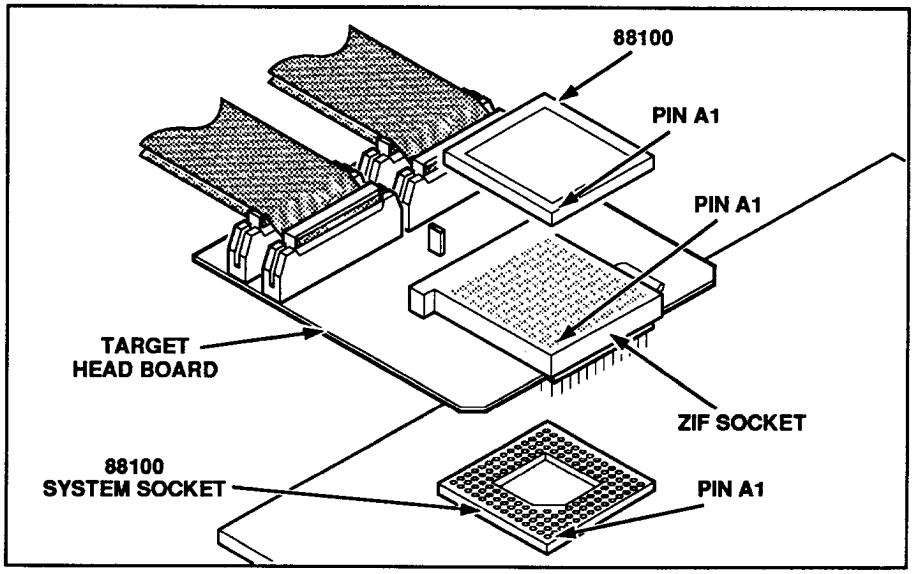


Figure 3-6. Placing the probe adapter in the 88100 system.

Deskewing 92A90 Modules

The 92A90 Modules must be deskewed for valid data to be acquired from an 88100 system operating above 25 MHz. Deskewing is not necessary to acquire data from an 88100 system operating at or below 25 MHz. There are two ways to deskew the modules:

- perform the deskew procedure and save the values to a deskew values file
- restore existing deskew values files

You must perform the deskew procedure if the modules have never been deskewed or if one or both modules has moved to another slot from where it was previously deskewed. After deskewing a module, you should save the values in a deskew values file. There will be one deskew values file per module.

You can restore deskew values files only if the modules are in the same slot they were in when the deskew values were saved.

Deskewing Modules and Saving the Values to a File

To deskew 92A90 modules and save these values to a file, perform the following steps:

1. Select the Configuration menu for the CodeBus module from the Menu Selection overlay.
2. Press F4: MOVE TO SETUP.
3. Press F8: DESKEW.
4. Connect the end of the deskew cable with the BNC to the deskew adapter and the other end of the cable to the CodeBus module.
5. Plug the deskew adapter into the buffer probe connected to the CodeBus module.
6. Follow the on-screen procedures. Set the switch on the deskew adapter to TEST and perform the TEST procedure first to ensure that all the channels are good before deskewing them.
7. After verifying that all the channels are good, set the switch on the deskew adapter to DESKEW and deskew the channels on the CodeBus module.
8. Press F6: ADD FILE.
9. Enter a name for the new deskew values file and press Close. The filename can not exceed 10 characters.
10. Press F3: SAVE DESKEW.

11. Press F8: EXIT & SAVE.
12. Perform steps 1 through 11 for the DataBus module.

After deskewing the modules and saving the deskew values files, you can connect the buffer probes to the probe adapter or HSMI.

Restoring Deskew Values from a File

To restore previously saved deskew values files, perform the following steps:

1. Select the Configuration menu for the CodeBus module from the Menu Selection overlay.
2. Press F4: MOVE TO SETUP.
3. Press F8: DESKEW.
4. Open the Deskew Values File field and select the deskew file for the CodeBus module.
5. Close the field and press F4: RESTORE DESKEW.
6. Press F8: EXIT & SAVE.
7. Perform steps 1 through 6 for the DataBus module.

After restoring deskew values, you can connect the buffer probes to the probe adapter or HSMI. If the buffer probes are already connected, you do not need to disconnect them to restore deskew values.

92A90 Module Connections

After the modules, buffer probes (optionally deskewed), and probe adapter are in place, you can complete the buffer probe connections.

If you are using two or four 92A90 Modules to acquire data from an 88100 system operating above 20 MHz, you will also have to connect one or two HSMIs. You can also connect the auxiliary channels of the probe adapter to acquire data from other signals in your 88100 system.

Buffer Probe Connections

To connect the buffer probes to the probe adapter, refer to Figure 3-7 and follow this procedure:

1. Align the connector from the buffer probe connected to the CodeBus module (lower-numbered slot) with the connector on the target head labeled CODE BUS and connect them.
2. Align the connector from the buffer probe connected to the DataBus module (higher-numbered slot) with the connector on the target head labeled DATA BUS and connect them.
3. Press the Probe ID button on each buffer probe to confirm that the connections are correct. A message appears such as **Module:DataBus Pod:6A Pod 1D pressed**, where Module is the module name and Pod:6A is the slot number.
4. Attach the probe adapter retention clips to secure the connections between the buffer probes and probe adapter housings.

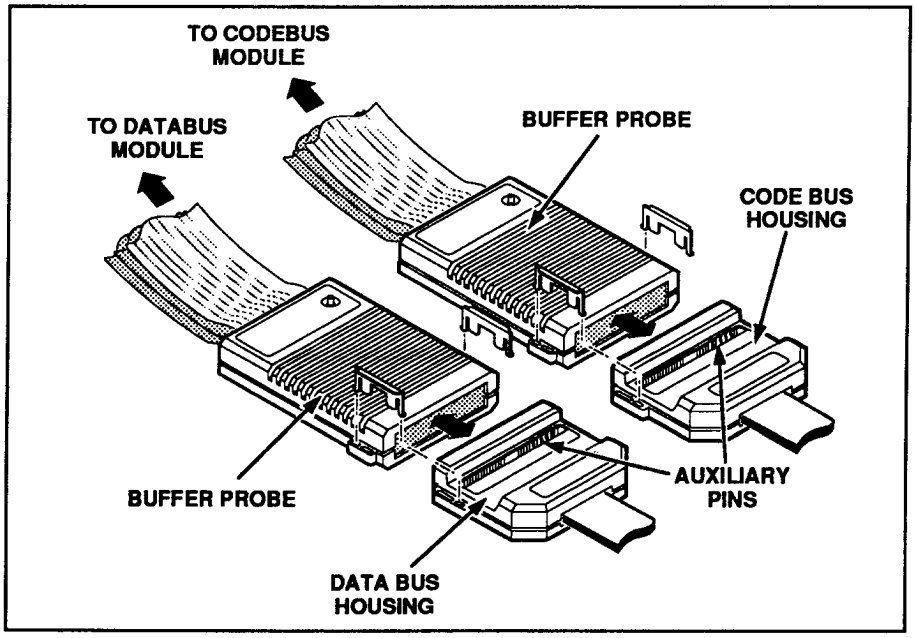


Figure 3-7. Buffer probe connections. These connections are used with 92A90 Modules.

HSMI Connections

If you are using a setup that uses an HSMI, refer to Figure 3-8 and follow these steps:

1. Connect the probe adapter connector for the desired 88100 bus to the single male connector on the HSMI.
2. Connect the two buffer probes from the assigned 92A90 Module to the two female connectors on the HSMI. The buffer probes can connect to either HSMI connector.

NOTE

If you are using an HSMI, make sure that the two 92A90 Modules assigned to either the DataBus or the CodeBus module reside in the same DAS 9200 mainframe. However, if you are using four 92A90 Modules with two HSMIs, the two DataBus modules do not have to be in the same DAS 9200 mainframe as the two CodeBus modules.

3. Repeat steps 2 and 3 for the other 88100 bus if you are acquiring data from both buses.

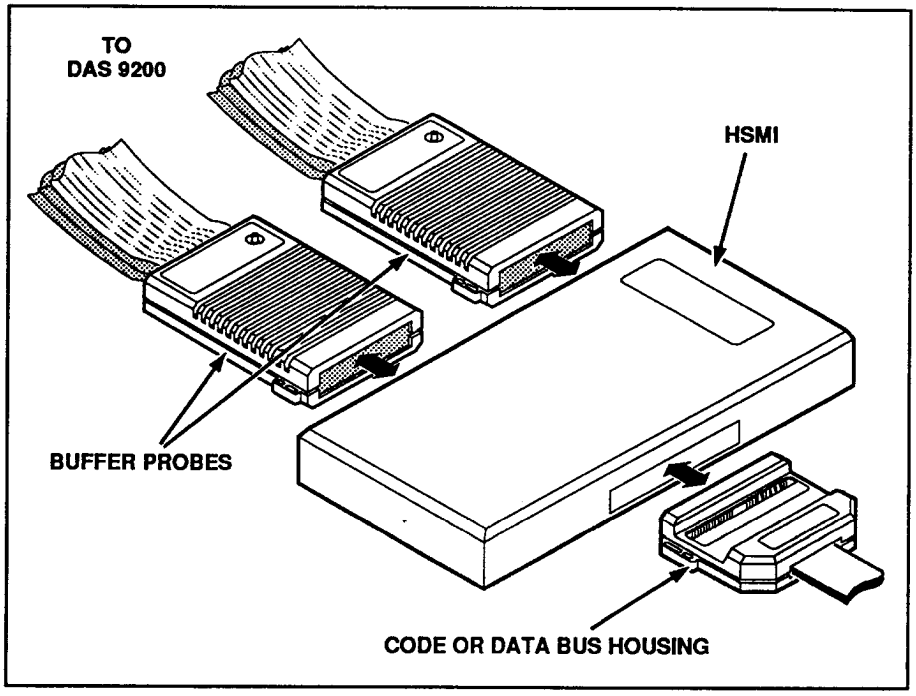


Figure 3-8. HSMI connections.

92A96 Module Connections

After the 92A96 Modules and probe cables are in place, and the probe adapter is configured and in place, you can connect the 90-channel interfaces. All four probe cables from one 92A96 Module connect to one 90-channel interface.

You do not have to deskew the 92A96 Modules.

To connect the 90-channel interfaces to the 92A96 probe cables, refer to Figures 3-9 and 3-10 and follow this procedure:

NOTE

It is important to connect the probe cables to the 90-channel interface in a specific color sequence to avoid miskeying them. The sequence is orange, blue, green, and gray.

1. Match the orange label on the loose end of a 92A96 probe cable to the orange label on one of the 90-channel interface housings.
2. Line up the key and key slot and connect them.
3. Repeat steps 1 and 2 for each of the other three probe cables on that module. Connect the blue cable to the blue slot, the green cable to the green slot, and the gray cable to the gray slot. Make these connections in the color-keyed sequence exactly as described.
4. Connect the probe ID/power cord from the 92A96 Module to the corresponding 90-channel interface. Figure 3-9 shows the keying of the probe ID/power cord connectors on the 90-channel interface and the 92A96 Module.

NOTE

Be careful to match the keying on each end of the probe ID/power cord to the keying of the corresponding connector on the 90-channel interface and 92A96 Module.

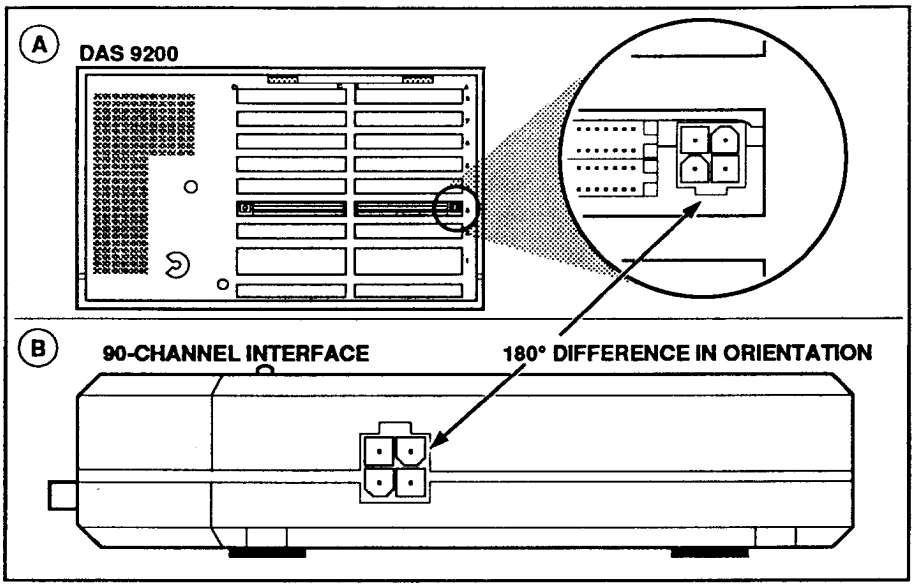


Figure 3-9. Keying of the connectors for the probe ID/power cord. The orientation between the two jacks is different because the 92A96 Module is positioned upside down in the mainframe.

5. Repeat steps 1 through 4 for the probe cables from the other 92A96 Module to the other 90-channel interface.

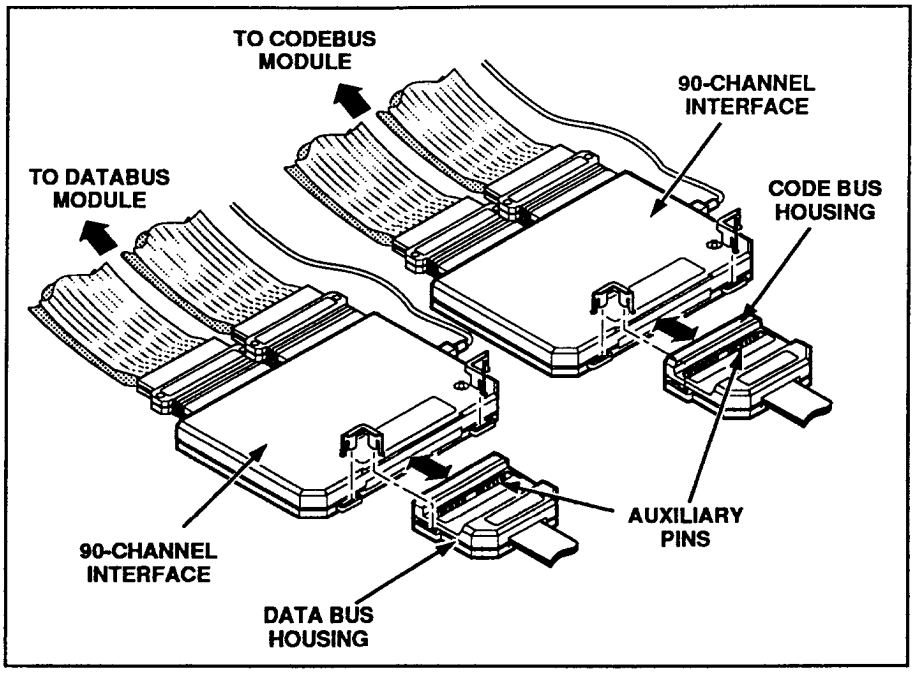


Figure 3-10. 90-channel interface connections. These connections are used with 92A96 Modules only.

To connect the 90-channel interfaces to the probe adapter, refer to Figure 3-10 and follow this procedure:

1. Align the connector from the 90-channel interface connected to the CodeBus module (lower-numbered slot) with the connector on the target head labeled CODE BUS and connect them.
2. Press the Probe ID button on the 90-channel interface to confirm that the connections are correct. A message appears such as **Module:DataBus Pod:6D Pod 1D pressed**, where Module is the module name and Pod:6D is the slot number.
3. Repeat steps 1 and 2 for the DataBus module, the target head connector labeled DATA BUS, and the other 90-channel interface.
4. Attach probe adapter retention clips to secure the connections between the 90-channel interfaces and probe adapter housings.

Auxiliary Channel Connections

To acquire data on the auxiliary channels, connect a 10-inch leadset (Tektronix part number 012-0747-00) to the row of pins on the probe adapter labeled either Aux1 or Aux0. Connect the other end of the leadset to other signals in your 88100 system. Figures 3-7 and 3-10 shows the location of the auxiliary pins on the probe adapter.

Make sure that the black wire of the leadset connects to channel 0. If you are not connecting to square pins in your system, you may need to attach grabber tips (Tektronix part number 020-1386-01) in order to make the connections. Be sure to connect at least one of the two wires connected to the auxiliary pins marked ground to the ground of the 88100 system.

When removing the 10-inch leadset from the probe adapter, do not pull on the wires. Instead, grasp and pull on the leadset's connector.

Section 4: ACQUIRING AND VIEWING DISASSEMBLED DATA

The primary function of this product is to assist you during the design period when you try to execute new or untested software on your 88100 hardware. This section describes how to acquire data and view it in the Disassembly menu.

After you configure the DAS 9200, install the microprocessor support software, make all the connections between the DAS 9200 and the system under test, and restore a cluster setup file, you are ready to complete the setup for the CodeBus and DataBus acquisition modules. To complete the setup, you need to choose a clock type (or use the default) and define a trigger program (or use the default).

CLOCKING

You can use the Clock menu to set clocking choices to control data sampling. The disassembler software offers a customized-clocking selection for the 88100 microprocessor. This clocking choice (Micro for 92A90 Modules and Custom for 92A96 Modules) is used whenever you select the 88100C or 88100D Support in the Configuration menu or restore a cluster setup.

The software provides two modes for acquiring 88100 data: Valid Cycles Only or All Cycles. You can change the clocking mode by changing the Cycles Included option field in the Clock menu. The selection for the Cycles Included option for the CodeBus modules do not have to match the DataBus modules.

Valid Cycles Only. This selection sets up the clocking to acquire all Success, Fault, and Reserved cycles and exclude all Wait, Null, and Stall cycles. Use this selection for most software testing and debugging.

The default setting for clocking is Valid cycles Only.

All Cycles. This selection sets up the clocking to acquire all cycles. Use this selection when you need to differentiate between Wait, Stall, and Null cycles.

A second option field, 88100 Probe Adapter, is available when using 92A90 Modules to acquire data from an 88100 system operating above 20 MHz where HSMIs are required. The selections are With HSMI or Without HSMI. This option must match your actual configuration to acquire valid data.

With HSMI or **Without HSMI.** To use this option, you must have one HSMI connected to two 92A90 Modules or two HSMIs connected to four 92A90 Modules. If you do not use this option when using HSMIs, the acquisition will be invalid.

Figure 4-1 shows the 92A90 Clock menu. Figure 4-2 shows the 92A96 Clock menu. A description of how valid cycles are sampled by the disassembler is in Appendix B.

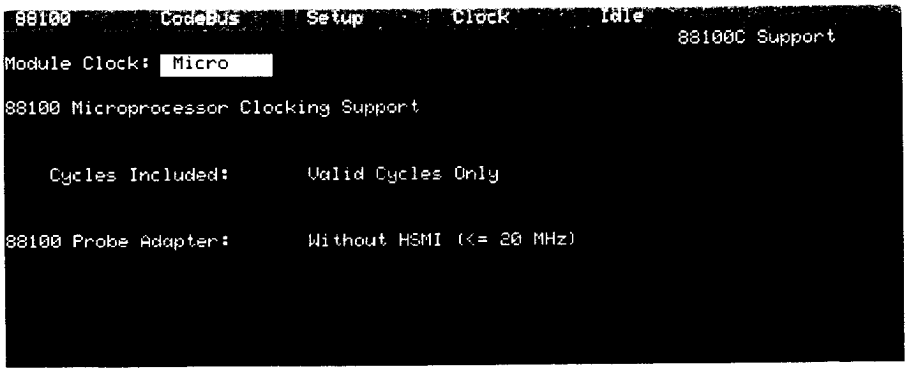


Figure 4-1. The 92A90 Clock menu for the CodeBus module.

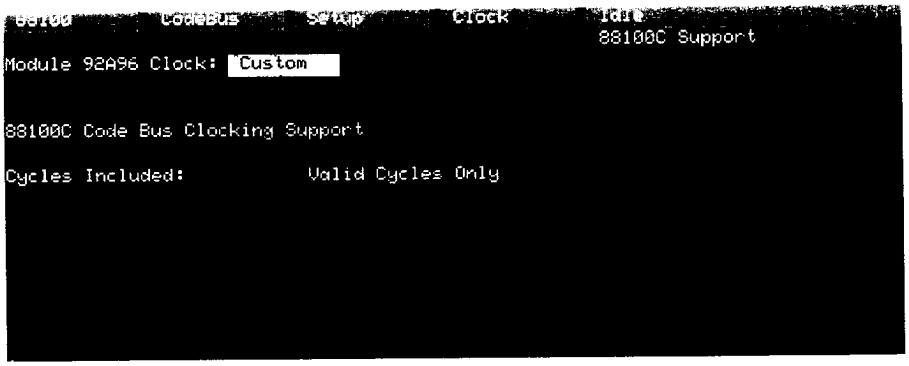


Figure 4-2. The 92A96 Clock menu for the CodeBus module.

TRIGGERING

The 88100 microprocessor support supplies a default trigger program for each multimodule setup. Each default trigger program uses one of the two communication signals dedicated for use with the disassembler. The C-to-D signal is used for communication from the CodeBus module to the DataBus module. The D-to-C signal is used for communication from the DataBus module to the CodeBus module.

The default trigger programs are set up to search for code bus values that you enter in the word recognizer fields in the Trigger menu of the CodeBus module. When these values are found, the CodeBus module sends the C-to-D signal to the DataBus module, triggers, and stores data. The trigger program of the DataBus module is set up to receive the C-to-D signal from the CodeBus module, trigger, and store data.

Due to delays in inter-module signals, the trigger point in acquisition memory for the second module will always be several samples behind the first module. Time correlation of the data from both modules, based on their timestamps, ensures an accurate representation of their relationship in time.

When selecting channel events for 92A96 Modules, do not use channel names with a prefix of an equals sign (=). Using any value other than a Don't Care (X) for the CSTALL channel when defining word recognizers for either 92A90 or 92A96 Modules will cause the acquisition module to function improperly.

Figure 4-3 shows the default trigger program for the CodeBus module.

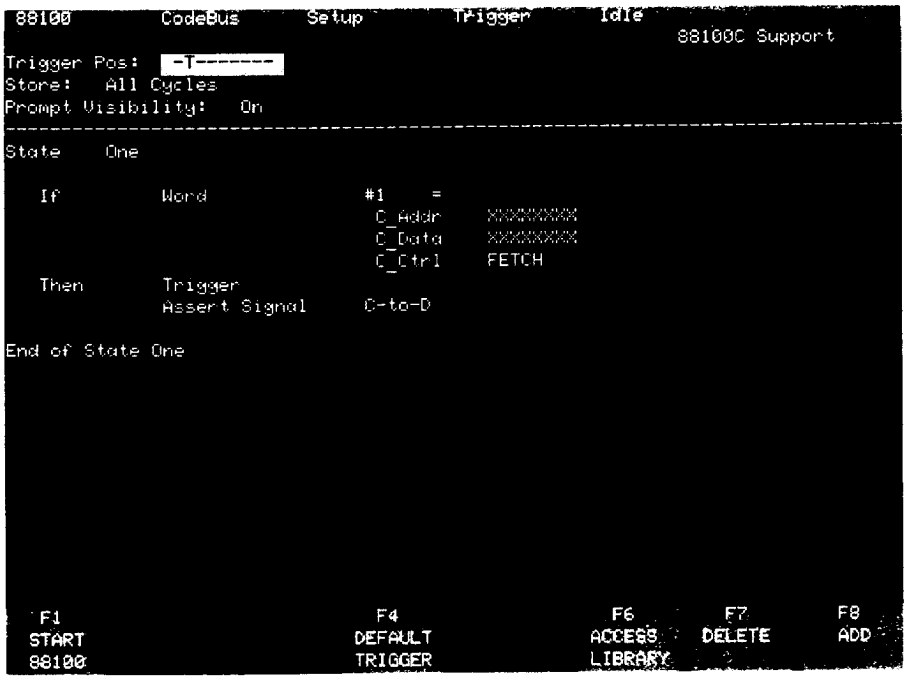


Figure 4-3. Trigger program default setup for the CodeBus module.

Figure 4-4 shows the default trigger program for the DataBus module.

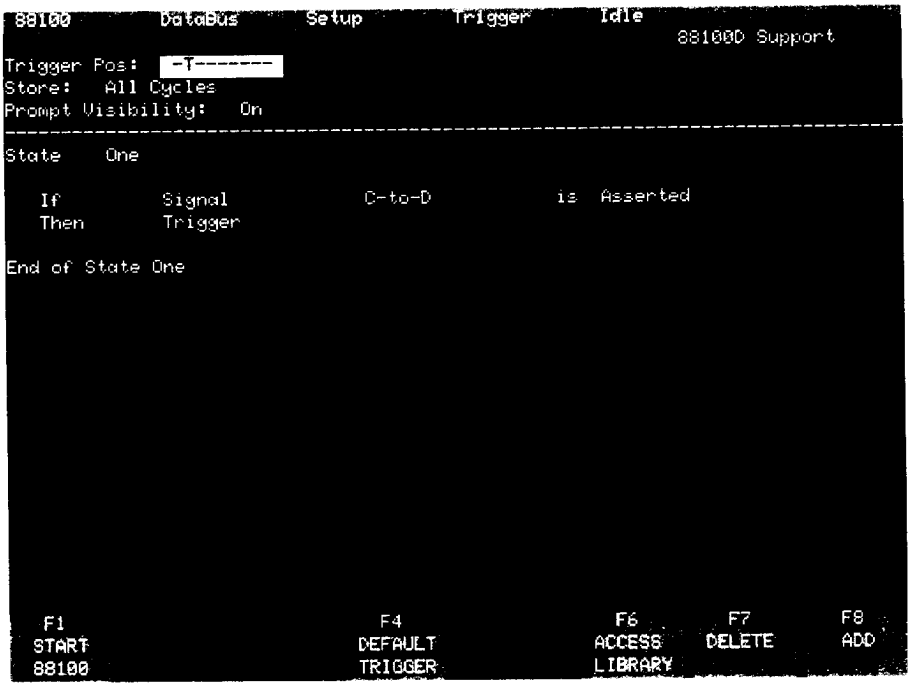


Figure 4-4. Trigger program default setup for the DataBus module.

ACQUIRING DATA

After you set up the disassembler to acquire data from your 88100 system, you can press F1: START to begin the acquisition. After satisfying the trigger program and filling acquisition memory, the DAS 9200 displays data in the format used last. You may need to press F1: STOP if the trigger or stop conditions are not met. The default display format is State. You can change the display format from the Menu Selection overlay (press the Select Menu key).

If the trigger does not occur immediately, the DAS 9200 displays the Module Monitor menu showing the progress of the acquisition. Refer to *Appendix A: Error Messages and Disassembly Problems* for a list of error messages and possible solutions.

DISPLAYING DISASSEMBLED DATA

The DAS 9200 displays disassembled data in the Disassembly menu. This menu shows the disassembled bus cycles, instruction mnemonics, operands and addresses, and data values.

You can display the disassembled data in different formats. You can select the display format and tailor it for your specific needs using the Disassembly Format Definition overlay. Detailed information on this overlay is provided later in this section.

Display Formats

The 88100 disassembler software provides four formats for displaying disassembled data:

- Hardware format shows all acquired cycle types and instruction mnemonics in the order they occurred
- Software format suppresses all reads, writes, and flushed instruction cycles, and displays a menu that looks similar to an assembly language program listing
- Control Flow format only displays the instructions that change the control flow of the microprocessor
- Subroutine format only displays subroutine calls and exceptions

You can further define how the data is displayed and cursor scrolling within the four formats by selecting various display options with the Disassembly Format Definition overlay.

Figure 4-5 shows an example of the Disassembly menu.

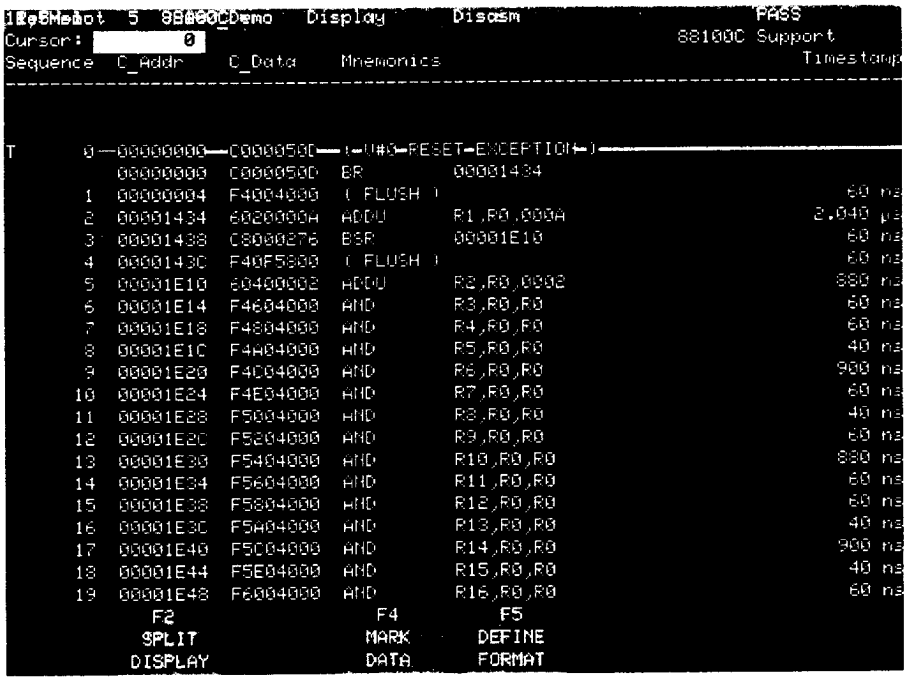


Figure 4-5. Disassembly menu.

No matter which display format you decide to use, the disassembly software displays information in the Disassembly menu in the following columns:

- **Sequence Column.** The sequence column shows the sequence number of the data displayed on that line. The cursor field in the upper-left area of the menu displays the sequence number of the current cursor location.

- **C_Addr or D_Addr Group Columns.** The C_Addr or D_Addr group column shows values for the address portion of the CodeBus or DataBus module at each sequence. You can display the C_Addr or D_Addr group either symbolically or as an eight-digit hexadecimal value.

- **C_Data or D_Data Group Columns.** The C_Data or D_Data group column shows values for the data portion of the CodeBus or DataBus module at each sequence.

- **Mnemonics Group Column.** The instruction mnemonics column shows the disassembled 88100 cycles and instructions. The disassembler software displays disassembled instructions and operands as they are described in the *88100 RISC Microprocessor User's Manual* (Motorola Inc., 1990).

  The disassembler displays immediate data as hexadecimal values. Register numbers are in decimal. Width and offset values of bit-field instructions and the bit number values of branch-on-bit and trap-on-bit instructions are displayed in decimal.

  If the addressing mode is PC-relative (program counter plus displacement), the disassembler software calculates the effective address before displaying it (instead of displaying the displacement). This also applies to trap instructions converting trap numbers to addresses. When you select the Symbol radix for the C_Addr group, the calculated effective addresses for PC-relative branches and for software trap instructions are displayed symbolically.

- **Timestamp Column.** The timestamp column shows the timestamp value, when you choose to display the timestamp values. You can use the Timestamp field of the Disassembly Format Definition overlay to select Absolute, Relative, Delta, or Off.

Timestamp values show the amount of time that has elapsed between data samples. There are three ways to show the timestamp value in the Disassembly menu: Absolute, Relative, and Delta. An Absolute timestamp shows the amount of time elapsed immediately after pressing F1: START and each subsequent sample. A Relative timestamp shows the amount of time elapsed between successive samples. A Delta timestamp shows the amount of time elapsed between the data sample you mark with a delta and each previous and subsequent sample. (To place a delta mark on a sample, use F4: MARK DATA from the Disassembly menu.) If there is no delta mark and you select Delta timestamp, then the first data sample (sequence 0) is used as the default delta mark.

Cycles are assigned the value of the timestamp counter on the respective module at the time that the 92A90 or 92A96 master clock occurs. Because the timestamp counter changes in 10 ns increments on the 92A96 Module, timestamps for data acquired from an 88100 system with a clock rate that is not synchronous with the timestamp counter will be slightly skewed. For example, data acquired from an 88100 system with a clock rate of 30 MHz (33 ns) would be assigned a relative timestamp of 30 or 40 ns. This skewing is not cumulative.

Using this same example with a 92A90 Module, whose timestamp counter increments every 20 ns, data would be assigned a relative timestamp of 20 or 40 ns. This skewing again is not cumulative.

Keep in mind the following characteristics of the Disassembly menu when viewing disassembled data:

- as you scroll through data, the group names will change to reflect the module's group names from which data was acquired
- all numeric values are shown unsigned (non-negative numbers) except for delta timestamp values
- all numeric values are justified from the least significant bit
- the timestamp value is always displayed as a decimal value
- you can only select the Symbolic radix when a symbol table is available for that group

The following discussions describe the four display formats.

Hardware Display Format

In the Hardware format, all acquired bus cycles are shown in the order they occurred. Instruction mnemonics are displayed on instruction Fetch cycles and cycle-type information is displayed for all other cycles. Non-instruction bus cycles are displayed as 32-bit wide data transactions. Invalid data bytes are represented by dashes. Figure 4-6 shows the Hardware display format.

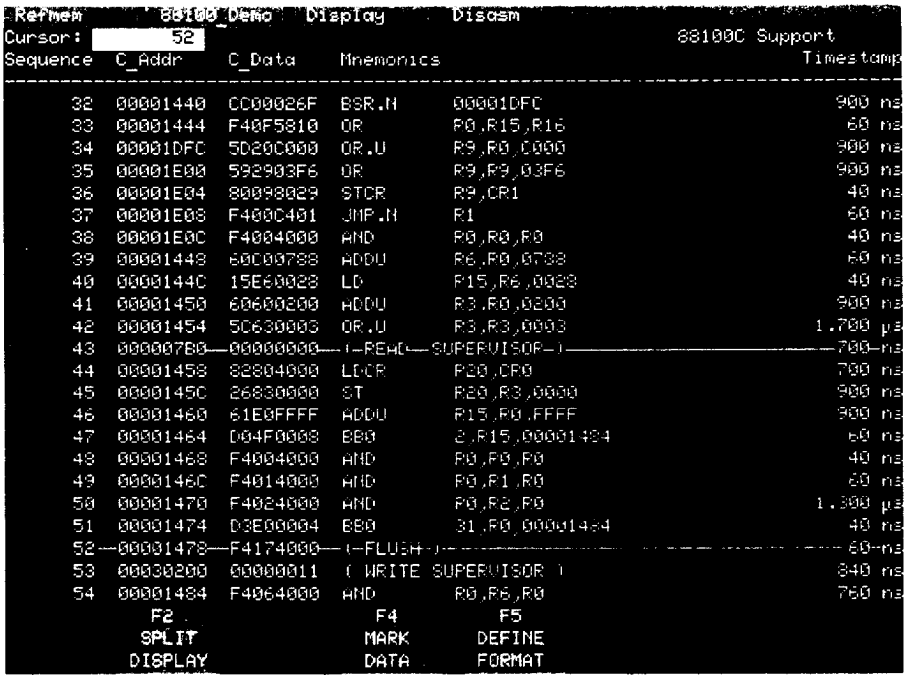


Figure 4-6. Hardware display format.

Software Display Format

In the Software format, only instruction fetches are displayed. All other cycle types are suppressed such as data reads, data writes, and flushed instructions. Figure 4-7 shows the Software display format.

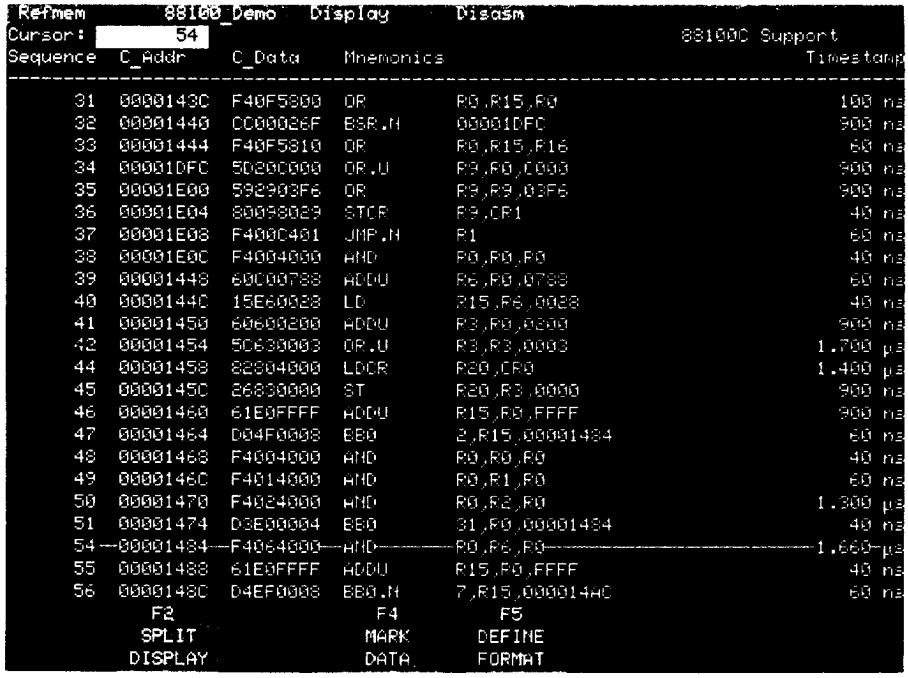


Figure 4-7. Software display format.

Control Flow Display Format

In the Control Flow format, only instructions that change the control flow are displayed. Instructions that do not actually change the control flow are suppressed, such as a conditional branch that is not taken.

Instructions that always generate a change in the flow of control in an 88100 microprocessor are as follows:

BR	JMP	RTE
BSR	JSR	

Instructions that can generate a change in the flow of control in an 88100 microprocessor are as follows:

BB1	BCND	TB0	TCND
BB0	TB1	TBND	

Figure 4-8 shows the Control Flow display format.

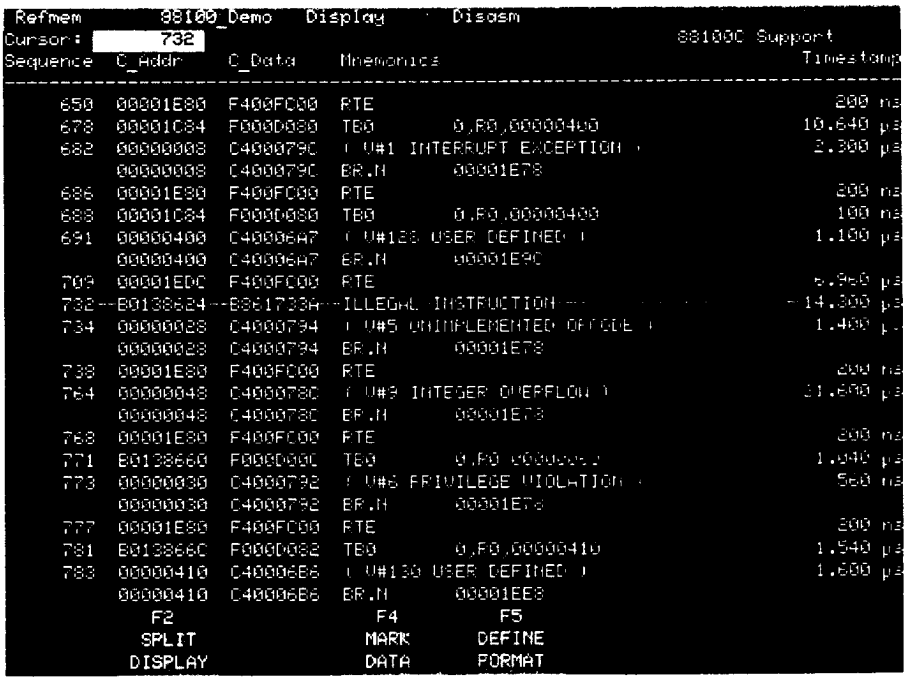


Figure 4-8. Control Flow display format.

Subroutine Display Format

In the Subroutine format, only subroutine branches, jumps, and returns are displayed. All hardware traps, internal or external, and all software traps that are taken are displayed. Software traps that are not taken are not displayed.

Instructions that generate a subroutine branch, jump, or return in an 88100 microprocessor are as follows:

BSR JSR RTE

Figure 4-9 shows the Subroutine display format.

```
Refmem      88100_Demo   Display      Disasm
Cursor:      940                                          88100C Support
Sequence  C_Addr     C_Data    Mnemonics                                Timestamp
-------------------------------------------------------------------------------
     773  00000030  C4000792  ( V#6 PRIVILEGE VIOLATION )                  560 ns
     777  00001E80  F400FC00  RTE                                          200 ns
     781  B013866C  F000D082  TB0       0,R0,00000410                  1.540 µs
     783  00000410  C40006B6  ( V#130 USER DEFINED )                    1.600 µs
     795  00001F10  F400FC00  RTE                                      3.660 µs
     810  00001CBC  C8000055  BSR       00001E10                       7.600 µs
     908  00000390  C40006B4  ( V#114 SFU 1 PRECISE )                  45.640 µs
     912  00001E80  F400FC00  RTE                                      1.060 µs
     920  00000018  C4000798  ( V#3 DATA ACCESS )                      2.240 µs
     924  00001E80  F400FC00  RTE                                      1.060 µs
     933  00000010  C40007C2  ( V#2 INSTRUCTION ACCESS )               1.800 µs
     940  00001F2C  F400FC00  RTE                                      3.900 µs
     944  00001DF8  CBFFFD8F  BSR       00001434                       1.140 µs
     947  00001438  C8000276  BSR       00001E10                         160 ns
     976  00001440  CC00026F  BSR.N     00001DFC                       1.440 µs
    1387  000019B4  F400C80C  JSR       R12                          114.860 µs
    1389  000019C4  F400CC0D  JSR.N     R13                              100 ns
    1466  00001B70  F415F811  TBND      R21,R17                        7.240 µs
    1469  00000038  C4000793  ( V#7 BOUNDS CHK VIOLATION )                160 ns
    1473  00001E8C  F400FC00  RTE                                          200 ns
    1478  00001E80  F8150003  TBND      R21,0003                           240 ns
    1481  00000038  C4000793  ( V#7 BOUNDS CHK VIOLATION )                160 ns
    1485  00001E8C  F400FC00  RTE                                          200 ns
          F2          F4        F5
        SPLIT       MARK      DEFINE
       DISPLAY      DATA      FORMAT
```

Figure 4-9. Subroutine display format.

Disassembly Format Definition Overlay

The Disassembly Format Definition overlay allows you to tailor the Disassembly menu. To access this overlay, press F5: DEFINE FORMAT from the Disassembly menu.

You can use this overlay to do the following:

- choose the format (mode) in which the Disassembly menu displays disassembled data
- set the interval in which the data cursor will scroll through disassembled data
- display and define the format of the timestamp
- highlight various types of disassembled cycles or gaps
- continue disassembly across gaps in the acquisition
- change the order in which the channel groups are displayed in the Disassembly menu
- change the radix for each group
- choose which symbol table to use for each group where symbolic is the selected radix

Figure 4-10 shows the Disassembly Format Definition overlay.

Figure 4-10. Disassembly Format Definition overlay.

1 **Display Mode.** You can display the disassembled cycle types or instruction mnemonics in Hardware, Software, Control Flow, or Subroutine modes.

2 **Timestamp.** You can display the timestamp as an Absolute, Relative, or Delta value. You can also set the timestamp display to Off. Refer to the description of the timestamp column earlier in this section for definitions of these selections.

3 **Scroll By.** You can scroll by Sequence, Instruction, Control Flow, or Subroutine.

4 **Highlight.** You can highlight All, Instructions, Control Flow, or Subroutines. Only the selected type of samples are shown as white text with a black background with highlighting on. All other samples are shown as gray text with a black background.

5 **Highlight Gaps.** You can choose to highlight or not to highlight gaps. Gaps are caused by qualifying data storage in the Trigger menu and are indicated by a gray background behind the address values.

6 **Disasm Across Gaps.** You can choose to continue or to discontinue to disassemble instructions across gaps. Disassembling instructions across gaps causes the disassembler to align the last address or data sample before the gap with the address or data sample immediately following the gap. Disassembled data will be invalid if these samples do not logically match.

7 **Vector Area Base.** You must enter the full base address for the vector. The default vector area base value is 0. Refer to the *MC88100 RISC Microprocessor's User's Manual* (1990) for information about the vector base address. The size is limited to 4 Kbytes.

8 **Group Name.** You can specify the name of the group that displays in the column in which the cursor is positioned. When you move a group, the group is inserted in the new column position and removed from its old position. All the groups to the right of the inserted group are moved over one column position to the right.

9 **Group Radix.** You can select the radix in which each group displays. The radix selections for most groups are Binary, Octal, Hexadecimal, Symbol, and Off. The only selections for the D_Data group are Hexadecimal or Off. The only selections for Mnemonics group are ASCII or Off. You should only select the symbolic radix when a symbol table is available for that group. The timestamp value always displays in decimal.

10 **Symbol Table.** You can specify a symbol table to use for each group where symbolic is the selected radix.

Function Keys

F1: ESCAPE & CANCEL. Closes the overlay and discards any changes you have made since entering it.

F5: RESTORE FORMAT. Displays a list of saved disassembly formats. Use the cursor keys to select the desired format to restore and press the Open/Close or Return key.

F6: SAVE FORMAT. Saves the current selections for the Disassembly Format Definition overlay in a file on disk. You can enter a file name up to ten characters long.

F7: DELETE FORMAT. Displays a list of saved disassembly format files for the current module or cluster setup. Use the cursor keys to select the desired format to delete and press the Open/Close key. You cannot delete the Default format.

F8: EXIT & SAVE. Exits the overlay and executes or saves any changes made.

Bus Cycle Types

Table 4-1 describes the bus cycle types for the code bus that the disassembler software disassembles and displays.

Table 4-1
Bus Cycle Types for the Code Bus

Cycle Type	Description
CODE WAIT	A cycle in which more time is needed to return valid data. This cycle type will not be acquired if Valid Cycles Only is selected in the 88100C Clock menu.
CODE FAULT	A cycle in which the data value received by the CPU is invalid due to a Translation Table search encountering an invalid descriptor or a violation of memory protection.
CODE RESERVED	A bus reply state reserved for Motorola's use. If the 88100 system is operating properly, this cycle should never occur
FLUSH*	An 88100 "success" cycle in which a fetch was performed but not executed due to a change in program flow.
STALL*	An 88100 "success" cycle in which the instruction pipeline is full and the processor is unable to execute the fetched instruction. This cycle type will not be acquired if Valid Cycles Only is selected in the 88100C Clock menu.
CODE NULL	A cycle in which the bus is inactive. This cycle type will not be acquired if Valid Cycles is selected in the 88100C Clock menu.
RESET	A cycle in which the CPU is being reset.
ILLEGAL INSTRUCTION	An 88100 "success" cycle in which a fetch was performed and executed, but which the disassembler does not recognize. This may or may not result in a trap for the 88100.

*These cycles are calculated or predicted by the disassembler. They cannot be used for triggering in the module's Trigger menu and they are not displayed in the State menu.

Table 4-2 describes the bus cycle types for the data bus that the disassembler software disassembles and displays.

Table 4-2
Bus Cycle Types for the Data Bus

Cycle Type	Description
DATA WAIT	A cycle in which more time is needed to return valid data. This cycle type will not be acquired if Valid Cycles Only is selected in the 88100D Clock menu.
DATA FAULT	A cycle in which the data value received by the CPU is invalid due to a Translation Table search encountering an invalid descriptor or a violation of memory protection.
DATA RESERVED	A bus reply state reserved for Motorola's use. If the 88100 system is operating properly, this cycle should never occur.
WRITE SUPERVISOR	A cycle in which a write to supervisor memory occurs.
WRITE USER	A cycle in which a write to user memory occurs.
WRITE SUPERVISOR LOCK	A cycle in which the write to memory is the store portion of an indivisible load/store operation in the Supervisor mode.
WRITE USER LOCK	A cycle in which the write to memory is the store portion of an indivisible load/store operation in the User mode.
READ SUPERVISOR	A cycle in which a read from supervisor memory occurs.
READ USER	A cycle in which a read from user memory occurs.
READ SUPERVISOR LOCK	A cycle in which the read from memory is the load portion of an indivisible load/store operation in the Supervisor mode.
READ USER LOCK	A cycle in which the read from memory is the load portion of an indivisible load/store operation in the User mode.
DATA NULL	A cycle in which the bus is inactive. This cycle type will not be acquired if Valid Cycles is selected in the 88100D Clock menu.
RESET	A cycle in which the CPU is being reset.

Figures 4-11 and 4-12 show how some of these disassembled cycles are displayed by the DAS 9200. Refer to *Appendix B: How Data is Acquired* to see when the various signals used to disassemble data are sampled.

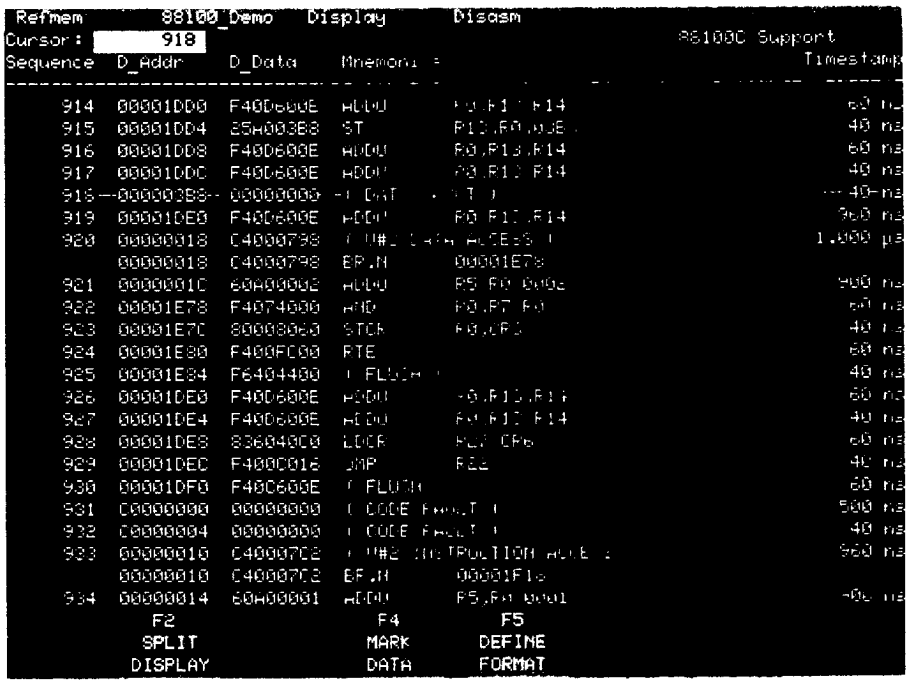


Figure 4-11. Displayed DATA FAULT, CODE FAULT, and FLUSH cycles.

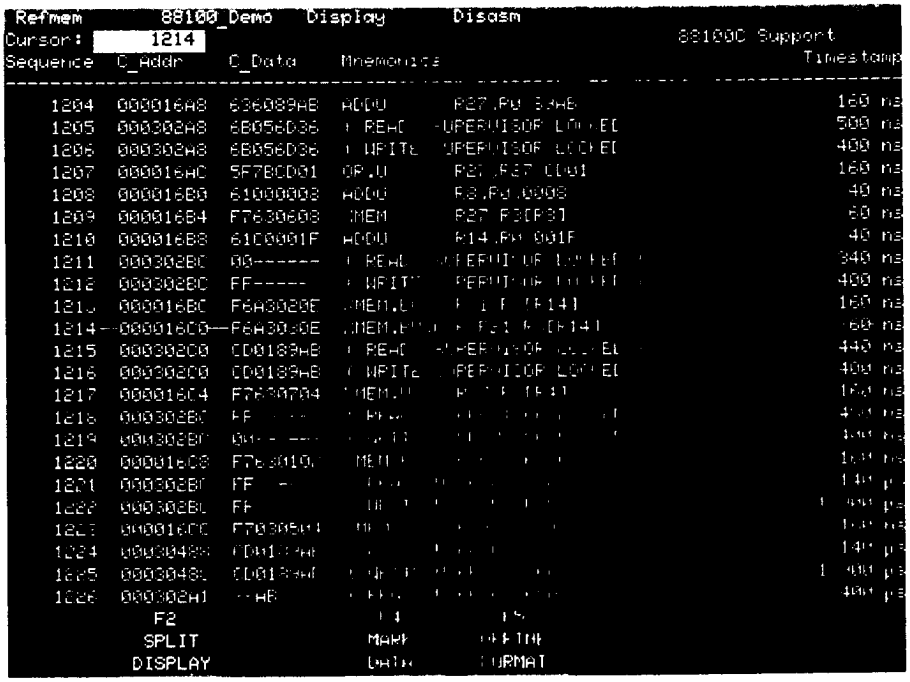


Figure 4-12. Displayed READ SUPERVISOR LOCKED, WRITE SUPERVISOR LOCKED, READ USER LOCKED, and WRITE USER LOCKED cycles.

Byte Ordering and Address Signals DA0 and DA1

You can select either Big- or Little-Endian byte ordering for data reads and writes. Big-Endian byte ordering is when the lowest address is the most significant byte. Little-Endian byte ordering is when the lowest address is the least significant byte. The only difference between these two selections is how the two low-order address bits (DA0 and DA1) are synthesized by the probe adapter. The position of this jumper does not control the operation of the 88100 CPU, which is internally controlled by a bit in its program status register.

The DA0 and DA1 address signals do not exist on the 88100 microprocessor. These two address channels are synthesized by the probe adapter, based on the setting of the byte-order jumper (J1380) for data reads and writes. The default jumper setting is Big-Endian.

CodeBus addresses are always an integral multiple of 4. This means that you can only trigger on an address that ends with a 0, 4, 8, or C for instruction fetch cycles. DataBus cycles are byte-addressable based on the position of the byte-order jumper.

Displaying the C_Addr and D_Addr Groups Symbolically

The C_Addr and D_Addr groups can be displayed as symbol values similar to the way the C_Ctrl and D_Ctrl groups can be displayed as symbol values. You can use the Symbol Editor menu to create symbol tables to assign symbols to specific addresses or various address ranges; then use the Channel menu to change the default radix of the C_Addr or D_Addr groups to SYM and assign to it the newly created symbol table. All effective addresses are sent to the table before being displayed. Refer to your *DAS 9200 System User's Manual* for a description of how to create symbol tables.

You can also change the radix of the C_Addr or D_Addr groups to Sym in the Disassembly Format Definition overlay. Figure 4-13 shows the C_Addr group displayed symbolically. The symbol table file used for the C_Addr group in this figure is the 88100_Demo symbol file. It is only valid for the 88100_Demo reference memory file.

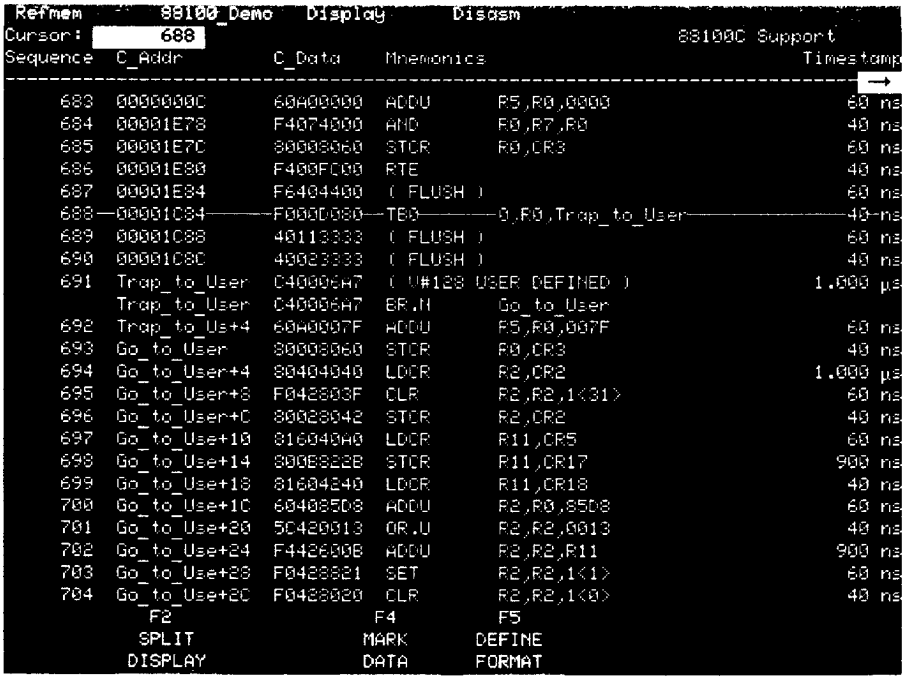


Figure 4-13. C_Addr group displayed symbolically.

Moving the Cursor to Suppressed Sequences

When displaying data in Software, Control Flow, or Subroutine formats, some sequence location numbers will be suppressed. You can still enter a specific sequence location number that has been suppressed. The cursor moves to the sequence nearest the suppressed sequence that can be displayed. If there is a large block of suppressed sequences near the desired sequence, there is a noticeable delay while the system searches for a sequence that can be displayed.

Marking Cycles

You can mark a data sample to easily identify data samples, to move quickly to a data sample, to manually correct a disassembled bus cycle, or to calculate delta timestamp measurements. You can mark a data sample with an A through M, a delta mark (Δ), or to mark flushed opcodes using the F4: MARK DATA feature of the Disassembly menu. An "m" is placed next to any sample that has had the bus cycle manually changed with an opcode mark.

An Undo Mark selection is also available for opcode marks. You can use both data and opcode marks on a data sample.

Manually Overriding Disassembled Instructions

Although the disassembler generally disassembles bus cycles correctly, there are situations where disassembled bus cycles are invalid. The most common occurrence is caused by a hardware trap (interrupt or external). This can also occur with nested software traps. And, when using storage qualification in the Trigger menu.

To manually correct invalid disassembly, you can use the F4: MARK DATA key to change an erroneously disassembled bus cycle. You can mark each instruction of an instruction fetch cycle as a FLUSH cycle. This is defined as a cycle where the instruction is flushed, not executed. The disassembler never marks a cycle that should be disassembled as flushed. The disassembler will not let you change non-instruction cycles such as a read or write.

You can also select Undo Marks which removes the mark from the sample on which the cursor is positioned.

To correct a bus cycle, follow these steps:

1. Place the cursor on the data sample you want to change in the Disassembly menu.
2. Press F4: MARK DATA and select a type of mark.

   When you press F4: MARK DATA, a list of selections appears. The list will change from sample to sample to reflect logical opcode or data mark selections for that individual sample. Unlike data marks that can only be used once, opcode marks can be used as often as necessary.

   If the data sample already has an opcode mark on it, then the selection list appears with the cursor on that mark. To remove the opcode mark from the sample on which the cursor is positioned in the Disassembly menu, select Undo Mark.
3. Press the Return key.

The data sample will reflect the corrected bus cycle, and other samples may be affected depending on the correction. An "m" is placed at the beginning of the data sample that had the disassembled bus cycle manually changed. Figure 4-14 shows two pre-fetched instructions following a hardware trap (interrupt) corrected using the F4: MARK DATA key.

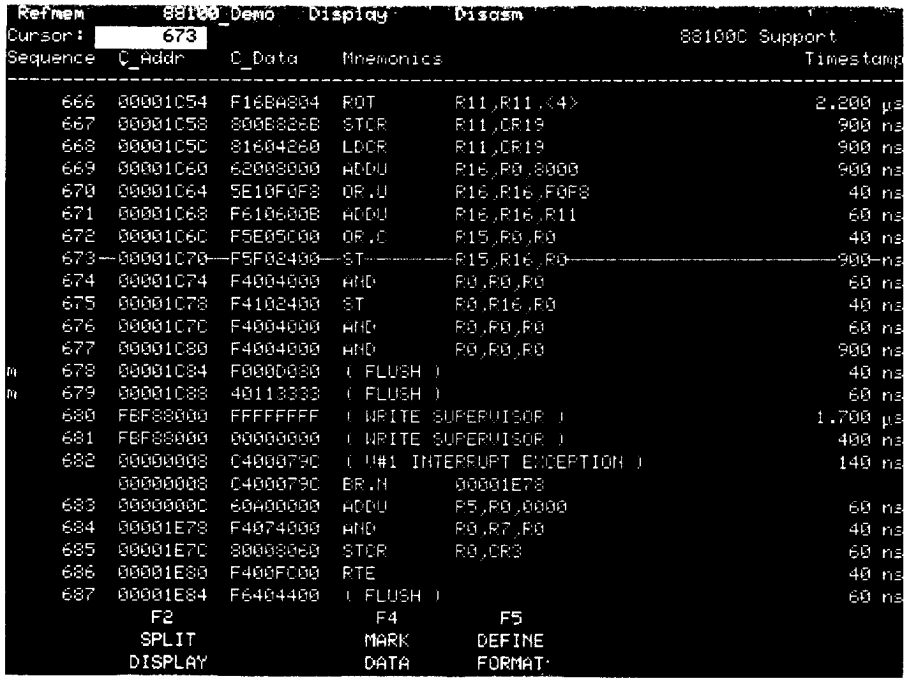


Figure 4-14. Two pre-fetched instructions corrected after using the F4: MARK DATA key.

Marking a Data Sample

Marks can be used to make data samples easy to identify, and to quickly move the cursor to a marked sample. A special mark, the delta mark (Δ), is also used to calculate delta timestamp values.

The available marks are A through M and Δ. When you mark a data sample, the mark is attached to the acquired data and the mark shows with the data sample in all display menus until you change it. If you are viewing the data in a split-screen display, such as when performing a search, the mark is attached only to the window in which it is placed and will not be carried over to the other window.

A small arrow appears at the beginning of the line of the marked data sample to make the mark more visible. The arrow disappears when both a data mark and an opcode mark are placed on the same sample.

To place a mark on a data sample, follow these steps:

1. Place the cursor on the data sample you want to mark in the Disassembly menu.
2. Press F4: MARK DATA and select a mark.

When you press F4: MARK DATA, a selection list appears. The cursor in the selection list is always on the next unused mark provided you don't access another display menu and place a mark in it. If you select a mark that has already been used, the previously marked sample will be unmarked and the current sample will be labeled with that mark when you close the selection list. A data mark can be used only on one data sample.

3. Press the Return key.

You can remove all the data marks in the Disassembly menu by using the State menu. To remove all data marks, follow these steps:

1. Press the Select Menu key to return to the Menu Selection overlay.
2. Select the State menu and press the Return key.
3. Press F5: DEFINE FORMAT.
4. Press F2: REMOVE MARKS and press the Return key. All the data marks will disappear.
5. Press the Select Menu key to return to the Menu Selection overlay.
6. Select the Disassembly menu and press the Return key. No data marks appear in the Disassembly menu; they have all been removed.

You can use the Δ mark to make delta timestamp measurements. After placing a Δ mark on a data sample, you can select the Delta selection in the Timestamp field of the Disassembly Format Definition overlay. When you press F8: EXIT & SAVE, the Disassembly menu samples will show the amount of time elapsed between the data sample with the Δ and each previous and subsequent sample.

To quickly move from one data mark to another, enter the mark for the new location in the Cursor field of the Disassembly menu. Enter an ^ in the Cursor field to move the cursor to a Δ mark.

Searching Through Data

The disassembler does not have a Disassembly Search Definition overlay. However, you can effectively search through disassembled data by using the following procedure:

1. Press F2: SPLIT DISPLAY to use the Split-Screen overlay.
2. Select the Disassembly menu for one half of the split-screen display and the State menu for the other half.
3. Press F5: SPLIT HORIZ to split the screen into two horizontal displays.
4. Press F2: LOCK CURSORS. A selection list appears.
5. Select **lock cursors at the same sequence**.
6. Press the Return key.
7. Press F8: EXIT & SAVE to display the menus in a split screen.
8. If the active menu is the Disassembly menu, press F3: SWITCH WINDOW to make the State menu active. The active menu is the one with the yellow cursor and Cursor field.
9. Press F6: DEFINE SEARCH to use the Search function of the State menu to search for the desired sequence.

To search on C_Ctrl or D_Ctrl group values, change the radix to binary and refer to Tables 3-1 and 3-2 to find the binary equivalent values for the cycles you want to locate.

When searching for data in a clustered module setup in the State menu, the searches are conducted only for the master module. You can, however, define either module to be the master module. Refer to the description of the State Search Definition overlay in your module user's manual for a description of how to search through state data. Also refer to that manual for a description of how to return to a full screen display.

To abort a search, press the Esc (escape) key.

Figure 4-15 shows the screen split into State and Disassembly windows with the cursors locked on the same bus cycle.

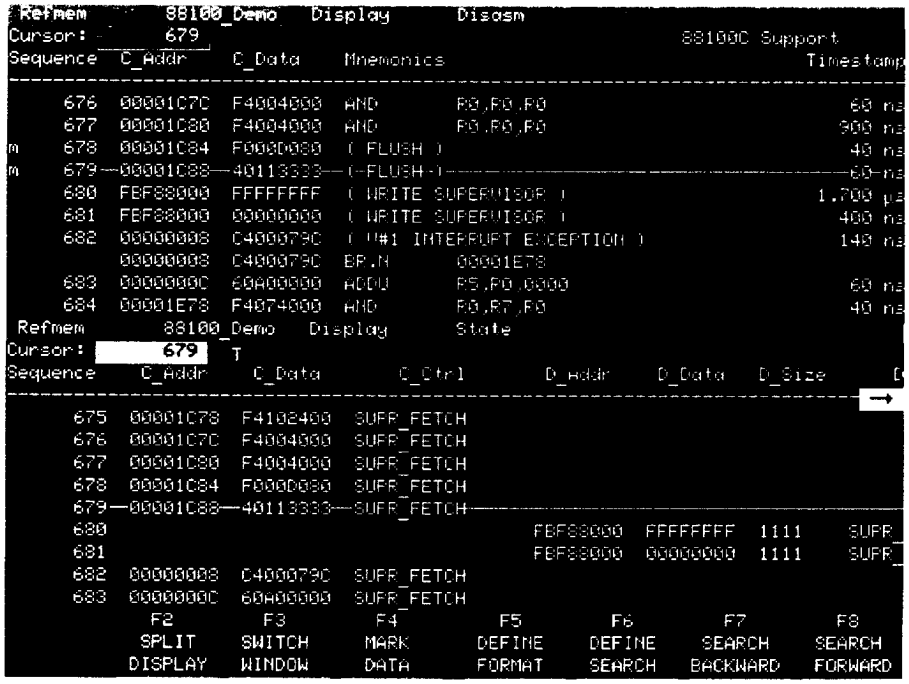


Figure 4-15. State and Disassembly split-screen display used to perform searches.

PRINTING DATA

To print disassembled data use the Disassembly Print overlay. To access this overlay, press the Shift and Print keys at the same time from the Disassembly menu.

You can choose one of two destinations for the disassembled data: the RS-232 Auxiliary Port, or a file stored on the hard disk. The data is formatted the same in both cases. Appendix C in the *DAS 9200 System User's Manual* contains information on connecting the RS-232 Auxiliary Port to a printer.

If the Send Output To field is set for a file, you need to name the file (the default name is Output). The file is stored in the Print Output directory. This file can be renamed, deleted, copied to a floppy disk, and so on from the Disk Services menu.

If the Send Output To field is set for the RS-232 Auxiliary port, the printer attached to this port receives the data for printing. To set the rate of transmission (baud rate) for the Auxiliary port, select the Communications menu and set the baud rate to match the data rate of your printer.

The parameters you can define in the Disassembly Print overlay are as follows:

- characters per line
- lines per page
- spaces to indent
- new line characters
- new page characters
- comment for page headings
- beginning and ending sequence numbers

If the width of the data exceeds the width of the specified line length (maximum 300 characters), greater than symbols (>) are printed to indicate that the data continues past the edge of the page. If you define more characters per line than can fit on a page, the data will either print on the next line or run off the edge of the page, depending on the type of printer being used.

To print the display screen, make the appropriate selections for the Saved Printer Settings (top of the Disassembly Print overlay) and the output specification, and press F5: PRINT. During printing, you can abort the printing sequence at any time by pressing F5: STOP PRINT.

NOTE

The DAS 9200 does not detect printer errors and will not give any error or warning messages if the print sequence cannot be completed.

For information on printer cable connections, refer to Appendix C in your DAS 9200 User's Manual.

Figure 4-16 shows the Disassembly Print overlay.

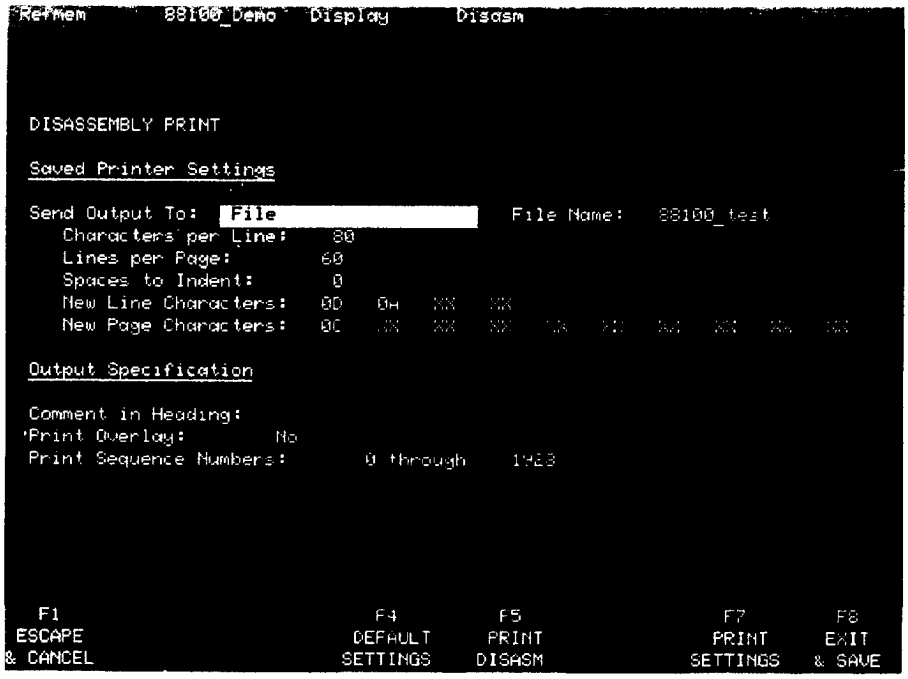


Figure 4-16. Disassembly Print overlay.

Section 5: HARDWARE ANALYSIS

You may need to perform hardware analysis on your 88100 system prior to, during, or after attempting to integrate your software with the 88100 system hardware. When performing hardware analysis you may want to use the data acquisition module to acquire data with a finer resolution. When more data samples are taken in a given period of time the resolution of the display increases, and you can see signal activity that would otherwise go undetected.

CLOCKING

To change the data sampling mode, use the Clock menu.

The default Clock menu is shown in Figures 4-1 and 4-2. Your data acquisition module user's manual contains an in-depth description of the Clock menu. The default clocking mode is Micro (92A90) or Custom (92A96) when microprocessor support is used. Micro or Custom clocking can be used for some kinds of hardware analysis.

When using the data acquisition module for hardware analysis, you may want to use the External clocking mode. The External clock selection samples data on every active clock edge on the clock inputs when using the rising edge of the 88100 clock. Data acquired using External clocking should not be viewed in the Disassembly menu.

Micro or Custom Clocking

Micro or Custom clocking of Valid Cycles Only stores one data sample for each bus transaction, which can take one or more clock pulses. This clocking selection may not be productive for hardware analysis. Refer to Appendix B for a more in-depth description of how Micro or Custom clocking acquires data.

To use Micro or Custom for hardware analysis, select All Cycles in the Cycles Included option field. With All Cycles selected, data is acquired on each clock pulse, de-pipelining occurs, and for Wait replies, address and control information is sampled only on the first Wait reply and not on subsequent replies for that Wait cycle. All Null cycles, Wait replies, and pipeline Stall conditions are acquired.

Figure 5-1 shows data sampled with All Cycles selected in the Cycles Included field of the Custom Clocking menu This data is not from the 88100_Demo reference memory file.

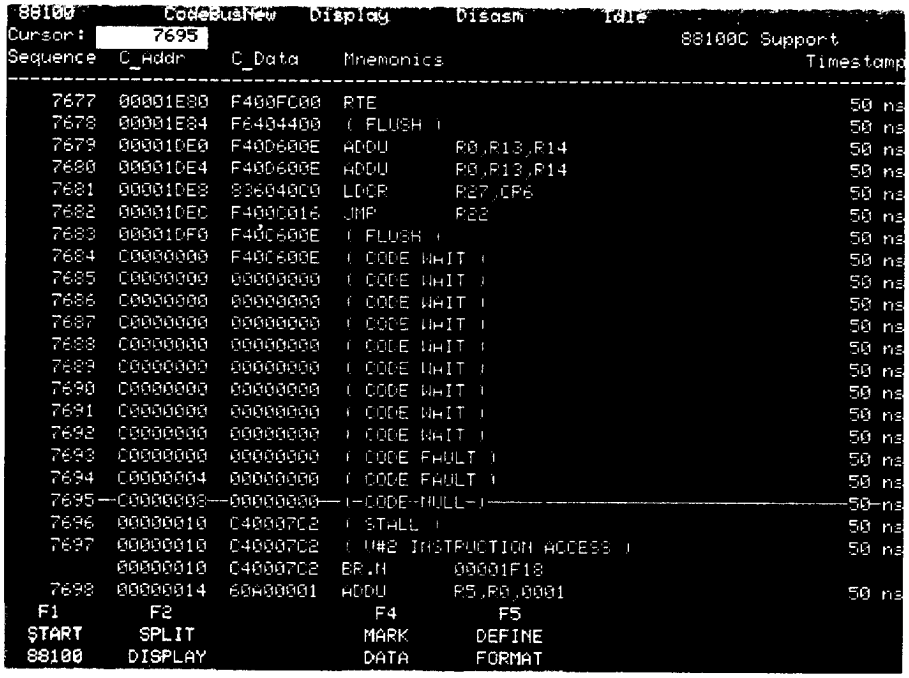


Figure 5-1. Data sampled with All Cycles selected.

You can use storage qualification in the Trigger menu to eliminate storing information for Null cycles and/or Wait replies. However, pipeline Stall conditions cannot be qualified out or used as a condition on which to trigger. When acquiring data in this manner, you should specify no highlighting of gaps and to disassemble across gaps in the Disassembly Format Definition overlay.

You can still view the acquired data in the Disassembly menu if you only use storage qualification to eliminate Null cycles and/or Wait replies. However, if storage qualification affects control flow, the disassembler may not be able to tell which instruction cycles are executed or flushed.

All Cycles does not have to be selected for both the CodeBus and DataBus modules. When using HSMIs, the All Cycles clocking selection must match on both CodeBus modules or on both DataBus modules.

Storage qualification does not have to be identical for both the CodeBus and DataBus modules. When using HSMIs, the storage qualification must match on both CodeBus modules or on both DataBus modules.

External Clocking

When you select External as the clocking mode, the acquisition modules acquire and store data based on the clock channel up to 100 MHz for the 92A96 Module or 20 MHz for the 92A90 Module. This clocking selection is commonly referred to as synchronous. When using HSMIs, each 92A90 Module stores on every other cycle, and therefore, operates at half the clock frequency of the CPU.

The acquisition module samples data on every rising edge of CLK when you select the rising edge of =CLK for the 92A96 Module or CLK for the 92A90 Module as the clock channel. This means that address and control lines are sampled on every rising edge of the clock pulse, even during Wait replies.

When Wait replies occur the address and control information will not occur on the same sample as the data and reply information. Only during Success, Fault, and Reserved replies will the address and control information occur on the same sample as the data and reply information.

You can also use the other clock channels and qualifier channels as clock qualifiers to further modify clocking for your 88100 system. However, you cannot change the signals to which they connect. With the 92A96 Module, the other clock channels and qualifier channels have a prefix of an equals sign (=). With the 92A90 Modules, there is no prefix.

TRIGGERING

All the Trigger menu selections currently available for that data acquisition module are still valid for hardware analysis. Refer to your module user's manual for a list and description of the selections.

When selecting channel events for 92A96 Modules, do not use channel names with a prefix of an equals sign (=). Using any value other than a Don't Care (X) for the CSTALL channel when defining word recognizers for either 92A90 or 92A96 Modules will cause the acquisition module to function improperly.

ACQUIRING DATA

You can acquire data as described in the *Acquiring Data* description in Section 4.

DISPLAYING DATA

Hardware analysis taken with External clocking requires that you view data in either the State or Timing menus. Hardware Analysis taken with Micro or Custom clocking can be viewed in the Disassembly menu as well as in the State or Timing menu.

In the Timing menu, every channel is shown as an individual waveform, or as part of a bus form, or as both. Waveforms and busforms are described in your module user's manual. You can delete any waveforms and reorder them.

In the State menu, all channel group values are shown based on the selected radix in the Channel menu or the State Format Definition overlay. No instruction mnemonics are displayed. CodeBus and DataBus are displayed separately and according to the order in which they occurred during de-pipelining.

VIEWING AND SEARCHING THROUGH DATA

You can view and search through State and Timing data as described in your module user's manual.

PRINTING DATA

To print state data, you can use the State Print overlay. To print timing data, you can use the Timing Print overlay. To access either print overlay, press the Shift and Print keys at the same time from the State or Timing menu. Refer to your module user's manual for a complete description of these overlays.

Appendix A: ERROR MESSAGES AND DISASSEMBLY PROBLEMS

This section describes error messages and disassembly problems you might encounter while acquiring data.

MODULE ERROR MESSAGES

These error messages will appear in the Module Monitor menu when there are problems with acquiring data or satisfying the trigger program. The error messages are listed in alphabetical order.

Slow Clock

This message appears when the active clock channel (or channels) is not changing or is typically changing at 1 ms or slower intervals, or one of the 88100 clock qualifiers is in the wrong state. Check for the following:

1. The 88100 system is powered on and running. Be sure the system is not in the reset state.
2. A cluster setup is restored in the Save/Restore menu and that 88100C and 88100D Support are selected in the respective Configuration menus for the CodeBus and DataBus modules.
3. Micro is selected in the Clock menu for the 92A90 Modules or Custom is selected in the Clock menu for the 92A96 Modules, and the appropriate clocking options are selected.
4. The connections between the CodeBus (lower-numbered slot) and DataBus (higher-numbered slot) modules, and probe adapter housings (labeled CODE BUS and DATA BUS) are correct.
5. The connections between the 90-channel interfaces and 92A96 probe cables have matched color labels and are properly keyed.
6. The connections for the power cable between the 90-channel interface and the 92A96 Module.
7. The connections between the 92A96 probe cables and probe connectors have matched color labels, matched slot numbers, and are properly keyed.
8. The orientation of pin A1 on the 88100 in the probe adapter is correct.
9. The lever on the ZIF socket is locked.

10. The orientation of pin A1 on the probe adapter in the 88100 system is correct.
11. No bent or missing pins on the 88100 microprocessor or on either of the probe adapter sockets.

Waiting for Stop

This message appears when the trigger condition is satisfied and memory is full but the Manual Stop mode is selected in the Cluster Setup menu when using Autorun. The solution is to manually stop the DAS 9200 by pressing F1: STOP.

This message can also appear when other modules in the cluster have not filled their memories. The solution in this case is to wait for the other modules to fill their memory. If the message does not disappear in a short time, press F1: STOP.

Waiting for Stop-Store

This message appears when the trigger condition is satisfied but the amount of post-fill memory specified in the trigger position field is not yet filled. Press F1: STOP to view the acquired data, then check for the following:

1. The trigger program in the Trigger menu is correct.
2. The storage qualification in the Trigger menu is correct.
3. The system or the module does not have an exception or fault. The 88100 system or data acquisition module might have experienced a hardware or software exception or fault after the trigger condition was satisfied.

Waiting for Trigger

This message appears when the trigger condition doesn't occur. Check for the following:

1. The 88100 system is powered on and running. Be sure the system is not halted.
2. The trigger conditions are being satisfied. The Module Monitor menu shows which state events are not occurring. Press F1: STOP, access the Trigger menu, and redefine the conditions for that state. Also refer to the description on *Triggering* in Section 4.

DISASSEMBLER ERROR MESSAGES

These error messages will appear in the Disassembly menu when there are problems with disassembling acquired data. If there is more than one error message, a window will appear listing the messages inside it. If there are more messages than can be displayed in the window, use the Return key to page to the other messages. When you want to close the message window, press the Esc key (escape). The system will always try to recover from an error and will display what action it took to do so in the message window. You will have to make other changes to remedy the problem in the system to override these DAS 9200 recovery actions.

OTHER DISASSEMBLY PROBLEMS

There may be problems with disassembly for which no error messages are displayed. Some of these problems and their suggested solutions follow:

Incorrect Data

If the data acquired is obviously incorrect, check the following:

1. The 92A90 Modules are deskewed when acquiring data from 88100 systems operating above 25 MHz. Refer to the deskew discussion in Section 3 for a description of how to deskew 92A90 Modules.

   92A96 Modules do not need to be deskewed.
2. The lever on the ZIF socket is locked.
3. No bent or missing pins on the 88100 microprocessor or on either of the probe adapter sockets.

No Data

If no data is displayed after satisfying the trigger program, check the following:

1. The modules are correlated.
2. The trigger positions in conjunction with the trigger programs to make sure that data overlaps.

Other Suggestions

If the previous suggestions don't fix the problem with acquiring disassembled bus cycles or instruction mnemonics, try the following:

1. Restore the appropriate cluster setup file from the Save/Restore menu to restore the DAS 9200 to a known state. For single card setups, reload the module setup by selecting 88100C Support or 88100D Support in the module's Configuration menu to restore the DAS 9200 to known state.

2. Possible ac loading problems may be remedied by removing the ZIF socket from the probe adapter. If this doesn't ease the loading problem sufficiently, you should remove one or both of the protective sockets from the probe adapter. These sockets may add enough additional inductance to your 88100 system to affect it. Refer to Appendix C for a description of the proper way to remove sockets from the probe adapter.

If the DAS 9200 still is not acquiring data after trying these suggestions, there may be a problem with the 88100 system. Try performing hardware analysis with your DAS 9200 system to ensure that the 88100 signals are valid at the time the probe adapter samples them.

Refer to *Section 5: Hardware Analysis* for information on data sampling using the External clocking selection in the Clock menu. Also refer to *Appendix B: How Data is Acquired* to see when the disassembler samples the various 88100 system signals.

ACQUIRING DATA AT HIGH SPEEDS

When acquiring data from an 88100 system that operates at high speeds, the ac and dc loading of the probe adapter can distort the waveform of the 88100 Clock signal. In extreme cases, especially when operating above 25 MHz, this can cause the probe adapter to acquire incorrect data; it can also cause the 88100 system to operate improperly. If either the acquisition module or the 88100 system operates improperly, examine the clock waveform for distortion. If distortion of the clock signal is occurring, here are some possible solutions.

If the 88100 system has a back-matching series termination resistor at the output of the clock driver circuit, the effects of probe loading can be reduced by decreasing the value of this resistor or removing it entirely. However, this can have adverse effects on other clock circuit loads. You can avoid this problem by using separate series termination resistors for the CPU and the remaining loads. The resistors could be connected to a single clock driver output or to a device with multiple outputs.

Another solution is to place the clock driver as close as possible to the CPU. This reduces the series termination resistance required and therefore the effects of additional loading due to the probe.

NOTE

It is important that the 92A90 modules be deskewed before acquiring data from a SUT operating above 25 MHz. You can perform the deskew on a warmed-up DAS 9200, save the values in a deskew file, and restore them prior to each use. Refer to the description on Deskewing 92A90 Modules *for directions on how to do this.*

Appendix B:
HOW DATA IS ACQUIRED

This appendix tells how the 92A90 or 92A96 Modules acquire 88100 signals. The modules log in signals from multiple groups of channels at different times when they are valid on the 88100 bus. The modules then send all of the logged-in signals to the trigger machine and to the acquisition memory of each module for storage.

BUS CYCLE TYPES

The module determines various cycle types through a deductive algorithm. The module first checks the cycle to determine if it is a Null cycle. If it is not a Null cycle, then the module checks to see if the cycle is a Success, Fault, Reserved, or Wait cycle. If it is a Success cycle, the module checks to see if the cycle is a Stall cycle. And, if the cycle is not a Stall cycle, then the disassembler determines if it is an instruction mnemonic or a flushed instruction.

MICRO OR CUSTOM CLOCKING

The 92A90 Module Micro clocking and the 92A96 Module Custom clocking with the 88100 uses four sample points. The first sample point is at the beginning of the cycle where the address bus and various control signals are logged in. The second sample point logs in the data bus and one control signal. The third sample point logs in the reply signals and some other control signals, and the fourth sample point logs in the remaining control signals. After being logged in, these signals are sent to the trigger machine and acquisition memory as a master sample (one complete data acquisition record). Figure B-1 shows these four sample points and the master sample.

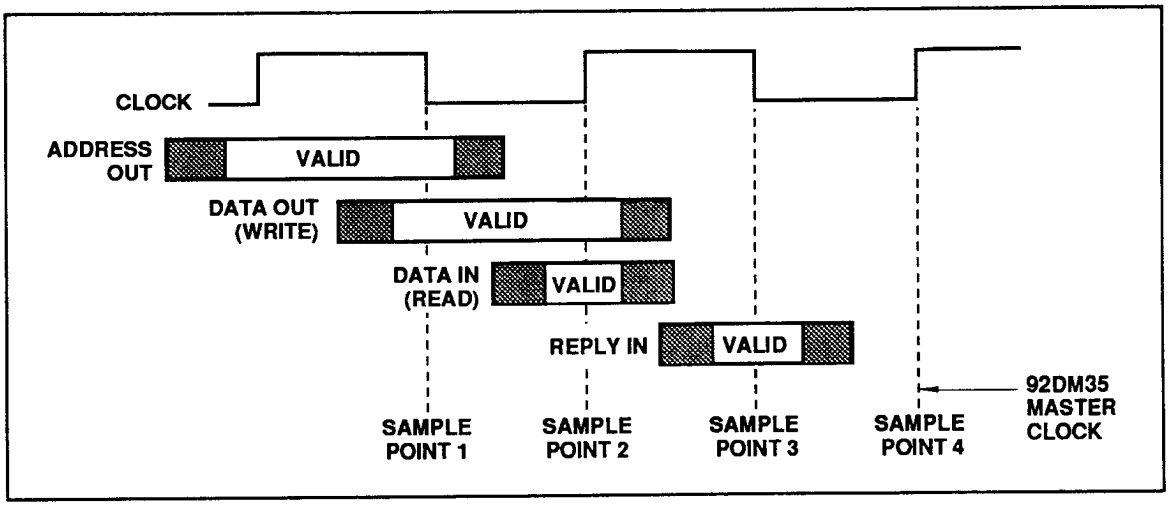


Figure B-1. 88100 bus timing. The 92DM35A samples signals at the points shown above. When the 92DM35A-generated Master Clock occurs, the sampled signals are combined to form one complete data acquisition record.

Table B-1 shows what signals are acquired at each sample point shown in Figure B-1.

Table B-1
Sample Points

Sample Point	Signals Acquired
1	ADDR (31–0), CFETCH, CS/U~,DS/U~, DR/W~, DBE3–0, DLOCK~
2	DATA (31–0), ERR
3	CR1–0, DR1–0, RST~, INT
4	PCE, AUX1, AUX0, PLLEN

The Micro or Custom clocking algorithm has two variations: Valid Cycles Only or All Cycles. The following descriptions apply to the clocking programs for both modules.

Valid Cycles Only

When a Success, Fault, or Reserved reply occurs, the module samples signals according to Figure B-1.

When a Wait reply occurs, the module samples the ADDR, CS/U~, CFETCH, DS/U~, DLOCK~, DR/W~, DBE3-0, ERR, PCE, PLLEN, and AUX0 signals. Upon any following Wait replies, the module does not sample any signals. When the first subsequent Success, Fault, or Reserved reply occurs, the module samples the DATA, RST~, INT, DR1-0, CR1-0, and AUX1 signals and combines them with the previously sampled signals to make up the acquisition record.

When a Null cycle occurs, as indicated by the deassertion of DBE3-0 on the Data bus, or by the deassertion of CFETCH on the Code bus, the module does not sample any signals.

When a pipeline stall occurs, as indicated by the current cycle's Code bus address matching the previous cycle's Code bus address, the acquisition module does not sample any signals.

All Cycles

When you select All Cycles in the Cycles Included field of the Clock menu, the module samples signals as described in Figure B-1 for all cycles except Wait, Null, and Stall cycles. Wait cycles are sampled as described for Valid Cycles Only except that the module samples the DATA, RST~, INT, DR1-0, CR1-0, and AUX1 signals and combines them with the signals sampled on the first Wait reply for each subsequent Wait reply. Null cycles are acquired regardless of the status of the reply signals, and Stall cycles are acquired regardless of whether the current cycle's address matches the previous cycle's address.

SYNTHESIZED SIGNALS

The 88100 probe adapter connects to 88100 signals and enables the 92A90 and 92A96 Modules to acquire them. The disassembler software uses the signal information to disassemble the program executing on your 88100 system. The probe adapter synthesizes seven signals used for acquisition or disassembly.

Table B-2 describes the synthesized signals. Refer to the previous discussions on acquiring Valid Cycles Only and All Cycles for a description of how these signals are used.

Table B-2
Synthesized Signals

Signal	Description
DNULL~	Indicates that a Data bus null state occurred; derived from the status of DBE3 – 0 used by the D_Ctrl symbol table to identify Null cycles when All Cycles is selected.
ERR_LATE	Indicates that an error occurred during a data write cycle; derived by sampling ERR late in the Data bus cycle.
CSTALL	Indicates that the Code bus address for the current cycle is the same as the previous cycle; used to disqualify pipeline stall cycles when Valid Cycles Only is selected.
CA(1:0)	Set to zero since all CodeBus accesses are word aligned.
DA(1:0)	Derived from the status of DBE3 – 0 and the setting of the byte-order jumper.

Warning

The following servicing instructions are for use only by qualified personnel. To avoid personal injury, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so. Refer to General Safety Summary and Service Safety Summary prior to performing any service.

Appendix C:
SERVICE INFORMATION

This appendix contains the following information:

- safety summary
- brief description of the 92DM35A probe adapter and how it works
- care and maintenance
- specification tables
- channel assignment tables
- dimensions of the probe adapter
- removing and replacing sockets
- replaceable electrical parts list
- circuit board component location diagrams
- schematics
- replaceable mechanical parts list
- exploded mechanical diagram

Refer to the *92A96 Module Service Manual* for service information on the 90-channel interface.

SERVICING SAFETY INFORMATION

The following service safety information is for service technicians. Follow these safety precautions, along with the general precautions outlined in your DAS 9200 acquisition module user's manual, while installing or servicing this product.

Do Not Service Alone. Do not perform internal service or adjustment on this product unless another person is present and able to give first aid and resuscitation.

Use Care When Servicing With Power On. To avoid personal injury from dangerous voltages, remove jewelry such as rings, watches, and other metallic objects before servicing. Do not touch the product's exposed connections and components while power is on.

PROBE ADAPTER DESCRIPTION

The probe adapter is a non-intrusive piece of hardware that allows the DAS 9200 to acquire data from an 88100 microprocessor in its own operating environment with little effect, if any, on that system. The probe adapter adds minimum loading to the 88100 system, and does not intercept, modify, or send signals back to the system. The probe adapter consists of a target head circuit board with a ZIF socket for the 88100 microprocessor and a large amount of active circuitry. Four cables connect between the target head board and two Configuration board sets. Each individual Configuration board set is dedicated to either the CodeBus or DataBus module and is labeled as CODE BUS or DATA BUS where the cables connect to the target head board.

When operating with 92A90 Modules, the probe adapter connects to two buffer probes. When operating above 20 MHz with four 92A90 Modules, the probe adapter connects to two HSMIs, each of which connects to two 92A90 Modules. When operating with 92A96 Modules, the probe adapter connects to two 90-channel interfaces.

All 88100 signals are latched with "D" registers and/or buffered at the probe tip. This results in low capacitance loading and small setup and hold time requirements into the probe adapter.

Signals from the 88100 system flow from the probe adapter to either the buffer probes or the 90-channel interfaces. The signals then go across the 92A90 buffer probe cables or 92A96 probe cables to the respective data acquisition modules.

DA0 and DA1, which do not exist on the 88100 microprocessor, are synthesized on the probe adapter for byte and half-word accesses. This allows the DataBus module to acquire and trigger on byte addresses even though the processor only provides word addresses. The CodeBus module always acquires the two least significant address bits as zero because all accesses are words.

The 88100 microprocessor lets you select either Big- or Little-Endian byte ordering. A jumper on the probe adapter, J1380, must be set to match the byte-ordering used in your 88100 system. The byte-enable jumper only affects the two lower-order address bits, DA0 and DA1, and not the 88100 microprocessor. The microprocessor is internally controlled by a bit in its processor status register.

All circuitry on the probe adapter is powered from the SUT.

The probe adapter accommodates the Motorola 88100 microprocessor in a 181-pin PGA package. The probe adapter replaces the microprocessor in the SUT and the microprocessor is then placed back in the ZIF socket on the top of the probe adapter.

CARE AND MAINTENANCE

The probe adapter does not require scheduled or periodic maintenance. To maintain good electrical contact, keep the probe adapter free of dirt, dust and contaminants. Also, ensure that any electrically conductive contaminants are removed.

Dirt and dust can usually be removed with a soft brush. For more extensive cleaning, use only a damp cloth. Abrasive cleaners and organic solvents should never be used.

CAUTION

The semiconductor devices contained on the probe adapter are susceptible to static-discharge damage. To prevent damage, service the probe adapter only in a static-free environment.

Always wear a grounding wrist strap, or similar device, while servicing the instrument.

CAUTION

Exercise care when soldering on a multilayer circuit board. Excessive heat can damage the through-hole plating or lift a run or pad and damage the board beyond repair. Do not apply heat for longer than three seconds. Do not apply heat consecutively to adjacent leads. Allow a moment for the board to cool between each operation.

If you must replace an electrical component on a circuit board, exercise extreme caution while desoldering or soldering the new component. Use a pencil-type soldering iron of less than 18 watts and an approved desoldering tool. Ensure that the replacement is an equivalent part by comparing the description as listed in the replaceable parts list.

SPECIFICATIONS

These specifications are for a 92DM35A probe adapter connected to 92A90 or 92A96 Data Acquisition Modules and the system under test (SUT). Tables C-1 and C-2 show the electrical and physical specifications for the 92DM35A microprocessor support package and its associated options. Table C-3 shows the environmental specifications.

Table C-1
Electrical Specifications

Characteristics	Requirements	
SUT DC Power Requirement		
Voltage	+5 V ± 0.5 V	
Current	200 mA typical (measured)	
Current	500 mA max.	
SUT Clock		
Clock Rate	33 MHz max. with 92A96s 20 MHz max. with 92A90s	
Setup Time		
All signals	1.0 ns	
Hold Time		
Data, ERR	7.5 ns	
All other signals	5.5 ns	
Maximum SUT Signal Loading	AC Load*	DC Load
CLK	<25 pF	3, 74AS1004 loads
RST~	<20 pF	2, 74FCT374 loads
ERR	<25 pF	1, 74F74 + 1, 74AS1004 loads
PCE, PLLEN	<15 pF	1, 74AS1004 load
All other signals	<15 pF	1 74FCT374 load

* The typical loading is 5 pF less than the values listed.

Table C-2
Physical Specifications

Characteristics	Requirements	
Housings	in	cm
Length	3.55	≈9.0
Width	4.20	≈10.67
Height	1.20	≈3.05
Target Head Board		
Length	5.00	≈12.7
Width	4.50	≈11.4
Height	1.20	≈3.0
Overall Cable Length		
Target head cable between the probe adapter housing and the target head board	12.0	≈30.48
Weight	21 oz	(≈.66 kg)

Table C-3
Environmental Specifications

Characteristic	Description
Temperature	
Max. Operating	+50° C (+122° F)
Min. Operating	+0° C (+32° F)
Non-Operating	-62° C to +85° C (-78° F to +185° F)
Humidity	5-95% relative humidity (non-condensing)
Altitude	
Operating	15,000 ft. (4.5 km) maximum
Non-Operating	50,000 ft. (15 km) maximum
Electrostatic Immunity	The probe adapter is static-sensitive

Table C-4 shows the 92A90 and 92A96 section and channel assignments, their grouping and radix for the disassembler, the voltage threshold, polarity, and microprocessor signal and pin connections for the CodeBus module.

Table C-4
92DM35A Channel Assignments (CodeBus Module)

92DM35A Group (Radix)	Group Bit Pos	92A90 Section: Channel	92A96 Section: Channel	Voltage Threshold, Polarity	88100 Signal Name	88100 Pin
C_Addr (Hex)	31	A3: 7	A3: 7	TTL, +	CA31	T17
	30	A3: 6	A3: 6	TTL, +	CA30	T16
	29	A3: 5	A3: 5	TTL, +	CA29	T15
	28	A3: 4	A3: 4	TTL, +	CA28	S15
	27	A3: 3	A3: 3	TTL, +	CA27	R15
	26	A3: 2	A3: 2	TTL, +	CA26	T14
	25	A3: 1	A3: 1	TTL, +	CA25	S14
	24	A3: 0	A3: 0	TTL, +	CA24	R14
	23	A2: 7	A2: 7	TTL, +	CA23	T13
	22	A2: 6	A2: 6	TTL, +	CA22	S13
	21	A2: 5	A2: 5	TTL, +	CA21	R13
	20	A2: 4	A2: 4	TTL, +	CA20	T12
	19	A2: 3	A2: 3	TTL, +	CA19	S12
	18	A2: 2	A2: 2	TTL, +	CA18	T11
	17	A2: 1	A2: 1	TTL, +	CA17	S11
	16	A2: 0	A2: 0	TTL, +	CA16	T10
	15	A1: 7	A1: 7	TTL, +	CA15	S10
	14	A1: 6	A1: 6	TTL, +	CA14	T9
	13	A1: 5	A1: 5	TTL, +	CA13	S9
	12	A1: 4	A1: 4	TTL, +	CA12	T8
	11	A1: 3	A1: 3	TTL, +	CA11	S8
	10	A1: 2	A1: 2	TTL, +	CA10	T7
	9	A1: 1	A1: 1	TTL, +	CA9	S7
	8	A1: 0	A1: 0	TTL, +	CA8	T6
	7	A0: 7	A0: 7	TTL, +	CA7	S6
	6	A0: 6	A0: 6	TTL, +	CA6	T5
	5	A0: 5	A0: 5	TTL, +	CA5	S5
	4	A0: 4	A0: 4	TTL, +	CA4	T4
	3	A0: 3	A0: 3	TTL, +	CA3	S4
	2	A0: 2	A0: 2	TTL, +	CA2	T3
	1	A0: 1	A0: 1	TTL, +	CA1*	none
	0	A0: 0	A0: 0	TTL, +	CA0*	none
C_Data (Hex)	31	D3: 7	D3: 7	TTL, +	C31	B2
	30	D3: 6	D3: 6	TTL, +	C30	B1
	29	D3: 5	D3: 5	TTL, +	C29	C2
	28	D3: 4	D3: 4	TTL, +	C28	C1
	27	D3: 3	D3: 3	TTL, +	C27	D2
	26	D3 2	D3 2	TTL, +	C26	D1
	25	D3: 1	D3: 1	TTL, +	C25	E2
	24	D3: 0	D3: 0	TTL, +	C24	E1
	23	D2: 7	D2: 7	TTL, +	C23	F2
	22	D2: 6	D2: 6	TTL, +	C22	F1
	21	D2: 5	D2: 5	TTL, +	C21	G2

(Cont.)

Table C-4 (Cont.)
92DM35A Channel Assignments (CodeBus Module)

92DM35A Group (Radix)	Group Bit Pos	92A90 Section: Channel	92A96 Section: Channel	Voltage Threshold, Polarity	88100 Signal Name	88100 Pin
C_Data	20	D3: 4	D3: 4	TTL, +	C20	G1
(Hex)	19	D3: 3	D3: 3	TTL, +	C19	H2
	18	D3 2	D3 2	TTL, +	C18	H1
	17	D3: 1	D3: 1	TTL, +	C17	J2
	16	D3: 0	D3: 0	TTL, +	C16	J1
	15	D2: 7	D2: 7	TTL, +	C15	K2
	14	D2: 6	D2: 6	TTL, +	C14	K1
	13	D2: 5	D2: 5	TTL, +	C13	L2
	12	D2: 4	D2: 4	TTL, +	C12	L1
	11	D2: 3	D2: 3	TTL, +	C11	M2
	10	D2 2	D2 2	TTL, +	C10	M1
	9	D2: 1	D2: 1	TTL, +	C9	N2
	8	D2: 0	D2: 0	TTL, +	C8	N1
	7	D1: 7	D1: 7	TTL, +	C7	P2
	6	D1: 6	D1: 6	TTL, +	C6	P1
	5	D1: 5	D1: 5	TTL, +	C5	R2
	4	D1: 4	D1: 4	TTL, +	C4	R1
	3	D1: 3	D1: 3	TTL, +	C3	S2
	2	D1 2	D1 2	TTL, +	C2	S1
	1	D1: 1	D1: 1	TTL, +	C1	T2
	0	D1: 0	D1: 0	TTL, +	C0	T1
C_Ctrl	6	QUAL: 2	C3: 0†	TTL, +	CS/U~	P14
(Sym)	5	QUAL: 3	C3: 4†	TTL, +	CFETCH	R5
	4	C1: 8	C3: 7	TTL, +	INT	R3
	3	CLK: 2	C1: 0†	TTL, +	RST~	S3
	2	C0: 8	C1: 3	TTL, +	ERR	R4
	1	CLK: 1	C0: 4†	TTL, +	CR1	D4
	0	CLK: 0	C0: 0†	TTL, +	CR0	D3
C_Misc	3	CLK: 3	C1: 4†	TTL, +	CLK	N3
(Off)	2	QUAL: 1	C2: 4†	TTL, +	CSTALL*	none
	1	C0: 1	C0: 2	TTL, +	PCE	P4
	0	C0: 0	C0: 1	TTL, +	PLLEN	P3
C_Aux1	7	C1: 7	C3: 6	TTL, +	Aux1-7	none
(Off)	6	C1: 6	C3: 5	TTL, +	Aux1-6	none
	5	C1: 5	C3: 3	TTL, +	Aux1-5	none
	4	C1: 4	C3: 2	TTL, +	Aux1-4	none
	3	C1: 3	C3: 1	TTL, +	Aux1-3	none
	2	C1: 2	C2: 7	TTL, +	Aux1-2	none
	1	C1: 1	C2: 6	TTL, +	Aux1-1	none
	0	C1: 0	C2: 5	TTL, +	Aux1-0	none
C_Aux0	3	C0 7	C1: 2	TTL, +	Aux0-3	none
(Off)	2	C0: 6	C1: 1	TTL, +	Aux0-2	none
	1	C0: 5	C0: 7	TTL, +	Aux0-1	none
	0	C0: 4	C0: 6	TTL, +	Aux0-0	none

* Indicates synthesized signals on the probe adapter.
† Indicates double-probed clock and clock qualifier signals on the 90-channel interface.

Table C-5 shows the 92A90 and 92A96 section and channel assignments, their grouping and radix for the disassembler, the voltage threshold, polarity, and microprocessor signal and pin connections for the DataBus module.

Table C-5
92DM35A Channel Assignments (DataBus Module)

92DM35A Group (Radix)	Group Bit Pos	92A90 Section: Channel	92A96 Section: Channel	Voltage Threshold, Polarity	88100 Signal Name	88100 Pin
D_Addr (Hex)	31	A3: 7	A3: 7	TTL, +	DA31	A1
	30	A3: 6	A3: 6	TTL, +	DA30	A2
	29	A3: 5	A3: 5	TTL, +	DA29	A3
	28	A3: 4	A3: 4	TTL, +	DA28	B3
	27	A3: 3	A3: 3	TTL, +	DA27	A4
	26	A3: 2	A3: 2	TTL, +	DA26	B4
	25	A3: 1	A3: 1	TTL, +	DA25	A5
	24	A3: 0	A3: 0	TTL, +	DA24	B5
	23	A2: 7	A2: 7	TTL, +	DA23	A6
	22	A2: 6	A2: 6	TTL, +	DA22	B6
	21	A2: 5	A2: 5	TTL, +	DA21	A7
	20	A2: 4	A2: 4	TTL, +	DA20	B7
	19	A2: 3	A2: 3	TTL, +	DA19	A8
	18	A2: 2	A2: 2	TTL, +	DA18	B8
	17	A2: 1	A2: 1	TTL, +	DA17	A9
	16	A2: 0	A2: 0	TTL, +	DA16	B9
	15	A1: 7	A1: 7	TTL, +	DA15	A10
	14	A1: 6	A1: 6	TTL, +	DA14	B10
	13	A1: 5	A1: 5	TTL, +	DA13	A11
	12	A1: 4	A1: 4	TTL, +	DA12	B11
	11	A1: 3	A1: 3	TTL, +	DA11	A12
	10	A1: 2	A1: 2	TTL, +	DA10	B12
	9	A1: 1	A1: 1	TTL, +	DA9	A13
	8	A1: 0	A1: 0	TTL, +	DA8	B13
	7	A0: 7	A0: 7	TTL, +	DA7	A14
	6	A0: 6	A0: 6	TTL, +	DA6	B14
	5	A0: 5	A0: 5	TTL, +	DA5	C14
	4	A0: 4	A0: 4	TTL, +	DA4	A15
	3	A0: 3	A0: 3	TTL, +	DA3	B15
	2	A0: 2	A0: 2	TTL, +	DA2	C15
	1	A0: 1	A0: 1	TTL, +	DA1*	none
	0	A0: 0	A0: 0	TTL, +	DA0*	none

(Cont.)

Table C-5 (Cont.)
92DM35A Channel Assignments (DataBus Module)

92DM35A Group (Radix)	Group Bit Pos	92A90 Section: Channel	92A96 Section: Channel	Voltage Threshold, Polarity	88100 Signal Name	88100 Pin
D_Data	31	D3: 7	D3: 7	TTL, +	D31	S16
(Hex)	30	D3: 6	D3: 6	TTL, +	D30	S17
	29	D3: 5	D3: 5	TTL, +	D29	R16
	28	D3: 4	D3: 4	TTL, +	D28	R17
	27	D3: 3	D3: 3	TTL, +	D27	P16
	26	D3 2	D3 2	TTL, +	D26	P17
	25	D3: 1	D3: 1	TTL, +	D25	N16
	24	D3: 0	D3: 0	TTL, +	D24	N17
	23	D2: 7	D2: 7	TTL, +	D23	M16
	22	D2: 6	D2: 6	TTL, +	D22	M17
	21	D2 5	D2 5	TTL, +	D21	L16
	20	D2: 4	D2: 4	TTL, +	D20	L17
	19	D2: 3	D2: 3	TTL, +	D19	K16
	18	D2: 2	D2: 2	TTL, +	D18	K17
	17	D2: 1	D2: 1	TTL, +	D17	J16
	16	D2: 0	D2: 0	TTL, +	D16	J17
	15	D1: 7	D1: 7	TTL, +	D15	H16
	14	D1: 6	D1: 6	TTL, +	D14	H17
	13	D1: 5	D1: 5	TTL, +	D13	G16
	12	D1: 4	D1: 4	TTL, +	D12	G17
	11	D1: 3	D1: 3	TTL, +	D11	F16
	10	D1: 2	D1: 2	TTL, +	D10	F17
	9	D1: 1	D1: 1	TTL, +	D9	E16
	8	D1: 0	D1: 0	TTL, +	D8	E17
	7	D0: 7	D0: 7	TTL, +	D7	D16
	6	D0: 6	D0: 6	TTL, +	D6	D17
	5	D0: 5	D0: 5	TTL, +	D5	C16
	4	D0: 4	D0: 4	TTL, +	D4	C17
	3	D0: 3	D0: 3	TTL, +	D3	B16
	2	D0: 2	D0: 2	TTL, +	D2	B17
	1	D0: 1	D0: 1	TTL, +	D1	A16
	0	D0: 0	D0: 0	TTL, +	D0	A17
D_Size	2	QUAL: 3	C3: 4†	TTL, +	DBE3	C13
(Bin)	1	QUAL: 2	C3: 0†	TTL, +	DBE2	D14
	0	QUAL: 1	C2: 4†	TTL, +	DBE1	D15
	1	QUAL: 0	C2: 0	TTL, +	DBE0	E15
D_Ctrl	8	C0: 3	C0: 5	TTL, +	DS/U~	C5
(Sym)	7	C0: 1	C0: 2	TTL, +	DLOCK~	C3
	6	C0: 2	C0: 3	TTL, +	DR/W~	C4
	5	C0: 0	C0: 1	TTL, +	DNULL~*	none
	4	C1: 8	C3: 7	TTL, +	ERR_LATE*	none
	3	CLK: 2	C1: 0†	TTL, +	RST~	S3
	2	C0: 8	C1: 3	TTL, +	ERR	R4
	1	CLK: 1	C0: 4†	TTL, +	DR1	P15
	0	CLK: 0	C0: 0†	TTL, +	DR0	N15

(Cont.)

Table C-5 (Cont.)
92DM35A Channel Assignments (DataBus Module)

92DM35A Group (Radix)	Group Bit Pos	92A90 Section: Channel	92A96 Section: Channel	Voltage Threshold, Polarity	88100 Signal Name	88100 Pin
D_Misc (Off)	0	CLK: 3	C1: 4†	TTL, +	CLK	N3
D_Aux1 (Off)	7	C1: 7	C3: 6	TTL, +	Aux1-7	none
	6	C1: 6	C3: 5	TTL, +	Aux1-6	none
	5	C1: 5	C3: 3	TTL, +	Aux1-5	none
	4	C1: 4	C3: 2	TTL, +	Aux1-4	none
	3	C1: 3	C3: 1	TTL, +	Aux1-3	none
	2	C1: 2	C2: 7	TTL, +	Aux1-2	none
	1	C1: 1	C2: 6	TTL, +	Aux1-1	none
	0	C1: 0	C2: 5	TTL, +	Aux1-0	none
D_Aux0 (Off)	3	C0: 7	C1: 2	TTL, +	Aux0-3	none
	2	C0: 6	C1: 1	TTL, +	Aux0-2	none
	1	C0: 5	C0: 7	TTL, +	Aux0-1	none
	0	C0: 4	C0 6	TTL, +	Aux0-0	none

* Indicates synthesized signals on the probe adapter.
† Indicates double-probed clock and clock qualifier signals on the 90-channel interface.

As shown in Tables C-4 and C-5, some signals are double-probed (indicated by a † in the table) by the 90-channel interface. Each signal that is double-probed appears in the Channel Definition overlay twice, once with the equals sign as a prefix and once without a prefix. In the External clocking menu, the double-probed signals only appear once with the equals sign prefix and are the correct set of signals to use for clocking.

In the Trigger menu, the double-probed signals, shown as channel events, without a prefix are the correct set of signals to use for triggering. Three of the seven signals with the equals sign prefix also appear in the Trigger menu. Do not use these three signals with the equals sign prefix for triggering.

Figure C-1 shows the dimensions of and minimum clearances for the target head.

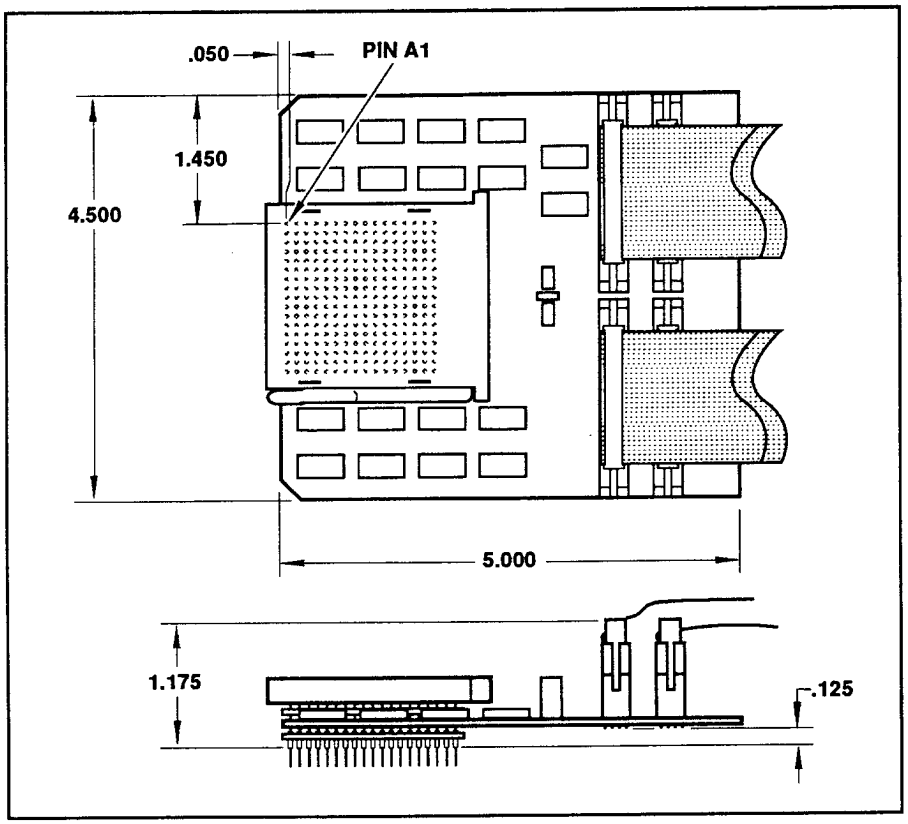


Figure C-1. Dimensions of and minimum clearances for the target head.

REMOVING AND REPLACING SOCKETS

The probe adapter board contains several sockets designed to protect the probe adapter and to make it easy to insert and remove the 88100 microprocessor. Figure C-2 shows a side view of the board, sockets, and pins of the probe adapter. The fixed socket on top of the probe adapter board is soldered and cannot be removed. The following paragraphs describe how to remove and replace the ZIF socket and the protective socket on the bottom of the probe adapter board.

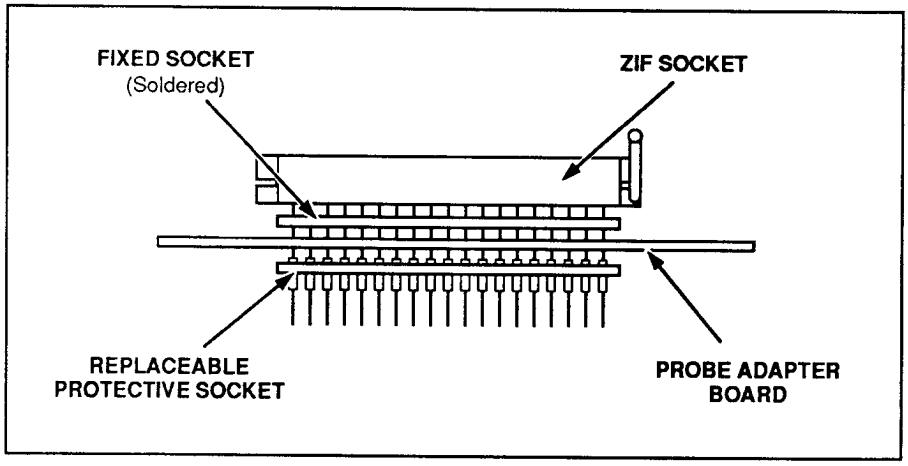


Figure C-2. Side view of the target head board.

ZIF Socket

You should not have to remove the ZIF socket unless there are clearance problems, ac loading problems, or socket-pin damage. To remove the ZIF socket, refer to Figure C-2 and follow these steps:

1. Place a 3/16" flat-blade screwdriver between the fixed socket and the ZIF socket. The screwdriver should rest on the top of the body of the fixed socket.
2. Gently twist the screwdriver against the body of the fixed socket and the ZIF socket until the ZIF socket is loose.

CAUTION

Apply even pressure around the entire socket. Do not pry off one side of the ZIF socket and then the other. Applying uneven pressure can damage the ZIF socket's pins.

3. Remove the ZIF socket from the board.
4. Once the ZIF socket has been removed from the board, store the ZIF socket in protective foam so that the pins are not damaged.

To replace the ZIF socket, follow these steps:

1. Check that the ZIF socket's pins are straight.
2. Refer to Figure 2-3 for pin A1 location information.
3. After locating the correct pin A1 location for the probe adapter align the ZIF socket with the fixed socket on the board, making sure that all pins line up correctly.
4. Apply even pressure on the ZIF socket so that all pins insert evenly.

Replaceable Protective Socket

You should not have to remove the probe adapter's replaceable protective socket unless there is socket-pin damage. To remove the protective socket, refer to Figure C-2 and follow these steps:

CAUTION

It is very difficult to remove the protective socket from the bottom of the probe adapter board. Be careful not to damage any etched circuit board runs or components surrounding the protective socket.

1. Locate the side of the socket adjacent to the edge of the probe adapter board and the side of the socket labeled A through T.
2. Place a 3/16" flat-blade screwdriver between the socket and the board on the side adjacent to the edge of the probe adapter board.
3. Gently twist the screwdriver against the body of the socket until the socket begins to separate from the probe adapter board pins.
4. Twist the screwdriver against the body of the socket next to the board marks A through T, but only where there are no board runs. Use even pressure alternately on both sides of the socket until the socket is loose.

CAUTION

Do not completely pry off one side of the protective socket and then the other. Applying uneven pressure can damage the socket's pins. Do not use board components as leverage to remove the socket.

5. Remove the socket from the board.

To replace the protective socket, follow these steps:

1. Check that the new socket's pins are straight.
2. Place the socket on the pins of the probe adapter board; make sure that all pins line up correctly.
3. Press the socket onto the board by pressing the socket and board against a hard, flat surface while applying even pressure.

Replaceable Electrical Parts

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

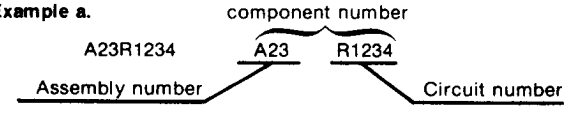
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

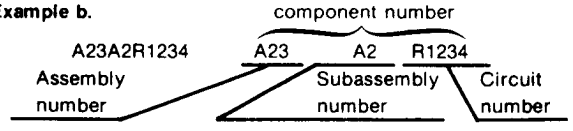
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX – MFR CODE NUMBER TO MANUFACTURER

Mfr Code	Manufacturer	Address	City, State, Zip Code
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPY PO BOX 655012	DALLAS TX 75265
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC	5005 E MCDOWELL RD	PHOENIX AZ 85008-4229
18324	SIGNETICS CORP	4130 S MARKET COURT	SACRAMENTO CA 95834-1222
22526	DU PONT E I DE NEMOURS AND CO INC	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051-0606
50434	HEWLETT-PACKARD CO	370 W TRIMBLE RD	SAN JOSE CA 95131
61772	INTEGRATED DEVICE TECHNOLOGY	3236 SCOTT BLVD	SANTA CLARA CA 95051
63058	MCKENZIE TECHNOLOGY	44370 OLD WARMS SPRINGS BLVD	FREMONT CA 94538
71468	ITT CANNON	666 E DYER RD	SANTA ANA CA 92702
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR	BEAVERTON OR 97077-0001
91637	DALE ELECTRONICS INC	2064 12TH AVE	COLUMBUS NE 68601-3632
TK1462	YAMAICHI ELECTRONICS CO LTD 2ND FLOOR NEW KYOEI	3-CHROME SHIBAURA MINATO-KU	TOKYO JAPAN
TK2156	ACACIA/DEANCO	7763 SW CIRRUS RD	BEAVERTON OR 97005-6452

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A24A13A1	671-1436-00			CIRCUIT BD ASSY:88100 TARGET	80009	671-1436-00
A24A13A2	671-1534-00			CIRCUIT BD ASSY:88100 PROBE ADAPTER CONFIG (QUANTITY OF 2 EA)	80009	671-1534-00
A24A13A1	671-1436-00			CIRCUIT BD ASSY:88100 TARGET	80009	671-1436-00
A24A13A1C1101	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1111	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1121	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1131	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1201	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1211	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1221	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1231	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1380	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1381	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1460	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1461	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1481	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1482	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1501	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1511	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1521	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1531	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1601	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1611	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1621	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C1631	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2141	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2151	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2161	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2171	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2241	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2251	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2261	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2271	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2341	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2342	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2351	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2371	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2381	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2441	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2442	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2443	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2451	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2452	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2453	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2475	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2481	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2541	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2551	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2561	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2571	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2641	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2651	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2661	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1C2671	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A1J1380	131-0608-00			TERMINAL,PIN:PCB/PRESSFIT,:MALE,STR,0.025 Q (QUANTITY OF 3 EA)	22526	48283-036
A24A13A1P1030	131-4454-00			CONN,HDR::PCB,:MALE,STR,2 X 30,0.05 X 0.1	TK1462	NFP-60A-0104
A24A13A1P1040	131-4454-00			CONN,HDR::PCB,:MALE,STR,2 X 30,0.05 X 0.1	TK1462	NFP-60A-0104

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A24A13A1P1130	131-4454-00			CONN,HDR::PCB,:MALE,STR,2 X 30,0.05 X 0.1	TK1462	NFP-60A-0104
A24A13A1P1140	131-4454-00			CONN,HDR::PCB,:MALE,STR,2 X 30,0.05 X 0.1	TK1462	NFP-60A-0104
A24A13A1P1380	131-0993-00			BUS,CONDUCTOR:SHUNT/SHORTING,:FEMALE,STR,1	22526	65474-006
A24A13A1R2471	325-5007-00			RES,FXD,FILM:47K OHM,5%,0.125W	91637	CROW-1206-473JT
A24A13A1R2472	325-5007-00			RES,FXD,FILM:47K OHM,5%,0.125W	91637	CROW-1206-473JT
A24A13A1R2482	325-5007-00			RES,FXD,FILM:47K OHM,5%,0.125W	91637	CROW-1206-473JT
A24A13A1R2483	325-5007-00			RES,FXD,FILM:47K OHM,5%,0.125W	91637	CROW-1206-473JT
A24A13A1U1100	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1110	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1120	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1130	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1200	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1210	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1220	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1230	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1380	156-5165-00			IC,DIGITAL:FTTL,GATE;4-2-3-INPUT AND-OR-INV	04713	74F64
A24A13A1U1460	156-5503-00			IC,DIGITAL:FTTL,GATES;DUAL 5-INPUT NOR	18324	74F260
A24A13A1U1480	156-5165-00			IC,DIGITAL:FTTL,GATE;4-2-3-INPUT AND-OR-INV	04713	74F64
A24A13A1U1500	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1510	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1520	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1530	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1540	156-5902-00			IC,DIGITAL:FCTCMOS,COMPARATOR;8-BIT	61772	74FCT521B
A24A13A1U1600	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1610	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1620	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1630	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U1640	156-5902-00			IC,DIGITAL:FCTCMOS,COMPARATOR;8-BIT	61772	74FCT521B
A24A13A1U2140	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2150	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2160	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2170	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2240	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2250	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2260	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2270	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2340	156-5392-00			IC,DIGITAL:ASTTL,GATE;HEX NONINV DRIVER	01295	74AS1034
A24A13A1U2350	156-5178-00			IC,DIGITAL:ASTTL,GATE;HEX INV DRIVER	01295	74AS1004
A24A13A1U2360	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2380	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2460	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2480	156-5055-00			IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE;74F74	04713	74F74
A24A13A1U2540	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2550	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2560	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2570	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2580	156-5902-00			IC,DIGITAL:FCTCMOS,COMPARATOR;8-BIT	61772	74FCT521B
A24A13A1U2640	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2650	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2660	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2670	156-5593-00			IC,DIGITAL:FCTCMOS,FLIP FLOP;OCTAL D-TYPE,	27014	74FCT374ASC
A24A13A1U2680	156-5902-00			IC,DIGITAL:FCTCMOS,COMPARATOR;8-BIT	61772	74FCT521B
A24A13A2	671-1534-00			CIRCUIT BD ASSY:88100 PROBE ADAPTER CONFIG (QUANTITY OF 2 EA)	80009	671-1534-00
A24A13A2C424	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	W1206X104K1B01
A24A13A2CR121	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR122	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR123	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR124	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A24A13A2CR125	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR126	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR127	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR221	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR222	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR223	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR224	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR225	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR226	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR227	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR228	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR321	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR322	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR323	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR324	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR325	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR326	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR327	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR328	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR421	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR422	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR423	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR425	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR427	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR521	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR522	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR523	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR524	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR531	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR532	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR533	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR534	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR535	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR536	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2CR537	152-0842-00			SEMICOND DVC,DI:SCHOTTKY,SI,COM ANODE PAIR	50434	5082-0087_FMLY
A24A13A2J100	131-0608-00			TERMINAL,PIN:PCB/PRESSFIT,:MALE,STR,0.025 Q (QUANTITY OF 10 EA)	22526	48283-036
A24A13A2J410	131-0608-00			TERMINAL,PIN:PCB/PRESSFIT,:MALE,STR,0.025 Q (QUANTITY OF 10 EA)	22526	48283-036
A24A13A2P100	131-2964-00			CONN,DIN::PCB,:FEMALE,RTANG,3 X 32,0.1 CTR	71468	G60M096P3-BEBM
A24A13A2Q424	151-5001-00			TRANSISTOR,SIG:BIPOLAR,NPN:40V,200MA,300MHZ	04713	MMBT3904
A24A13A2R424	321-5030-00			RES,FXD,FILM:10.0K,1%,0.125W	91637	CRCW12061002FT
A24A13A2W230	174-1208-00			CA ASSY,SP,ELEC:60,30 AWG,15.0 L,RIBBON	TK2156	63995
A24A13A2W240	174-1207-00			CA ASSY,SP,ELEC:60,30 AWG,13.7 L,RIBBON	TK2156	63994

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

SYMBOLS

Graphic symbol and class designation letters are based on ANSI Y32.14, 1973 in terms of positive logic. Logic symbols are depicted according to the manufacturer's data book information (not according to function).

Letter symbols for quantities used in electrical science and electrical engineering are based on ANSI Y10.5, 1968.

Drafting practices, line conventions, and lettering conform to ANSI Y14.15, 1966 and ANSI Y14.2, 1973.

Abbreviations are based on ANSI Y1.1, 1972.

You can inquire about these ANSI standards by contacting:

American National Standard Institute
1430 Broadway
New York, New York 10018

COMPONENT VALUES

Electrical components shown on the diagram are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads(pF)
Values less then one are in microfarads (μF)

Resistors = Ohms (Ω)

ACTIVE-LOW SIGNAL INDICATORS

A common convention used for indicating an active-low signal (a signal performing its intended function when it is in a low state) is an overbar, as shown in the signal name $\overline{\text{RESET}}$. The overbar may be used in this manual whenever a reference is given to an active-low signal. However, the same active-low signal is indicated on the schematic with a tilde (~), or a slash (/) following the signal name (e.g., RESET~ or RESET/).

The information and special symbols below may appear in this manual.

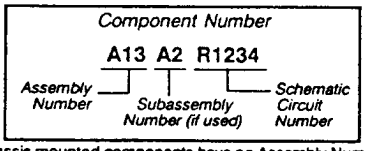
ASSEMBLY NUMBERS

Each assembly in the instrument is assigned an assembly number (e.g., A5). The assembly number appears in the title of each:

- schematic diagram (lower right corner)
- circuit board component location illustration
- schematic or circuit board component location look up table (when shown).

The Replaceable Electrical Parts list is arranged by assemblies in numerical order. The components are listed alphabetically by component location numbers. Look at the following example to see how to construct a component number.

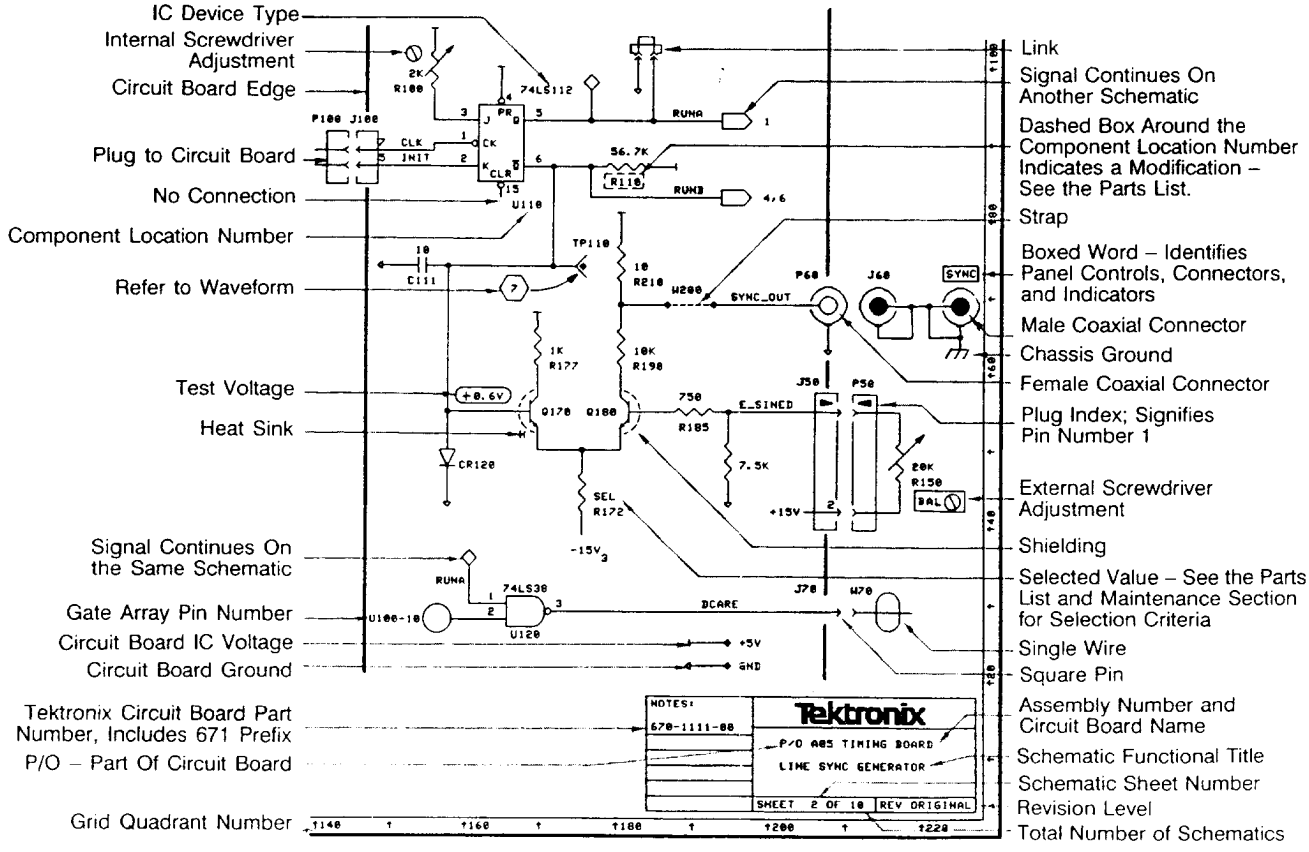
COMPONENT NUMBER EXAMPLE



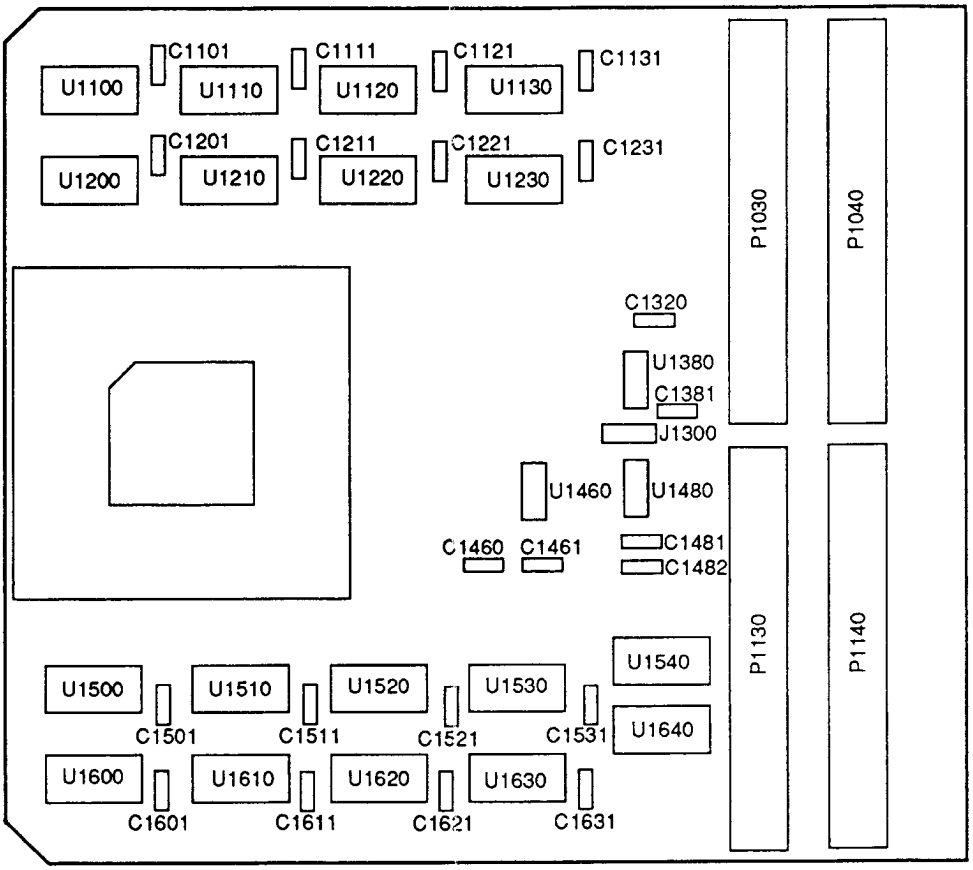
Chassis mounted components have no Assembly Number prefix – see end of Replaceable Parts List.

GRID COORDINATES

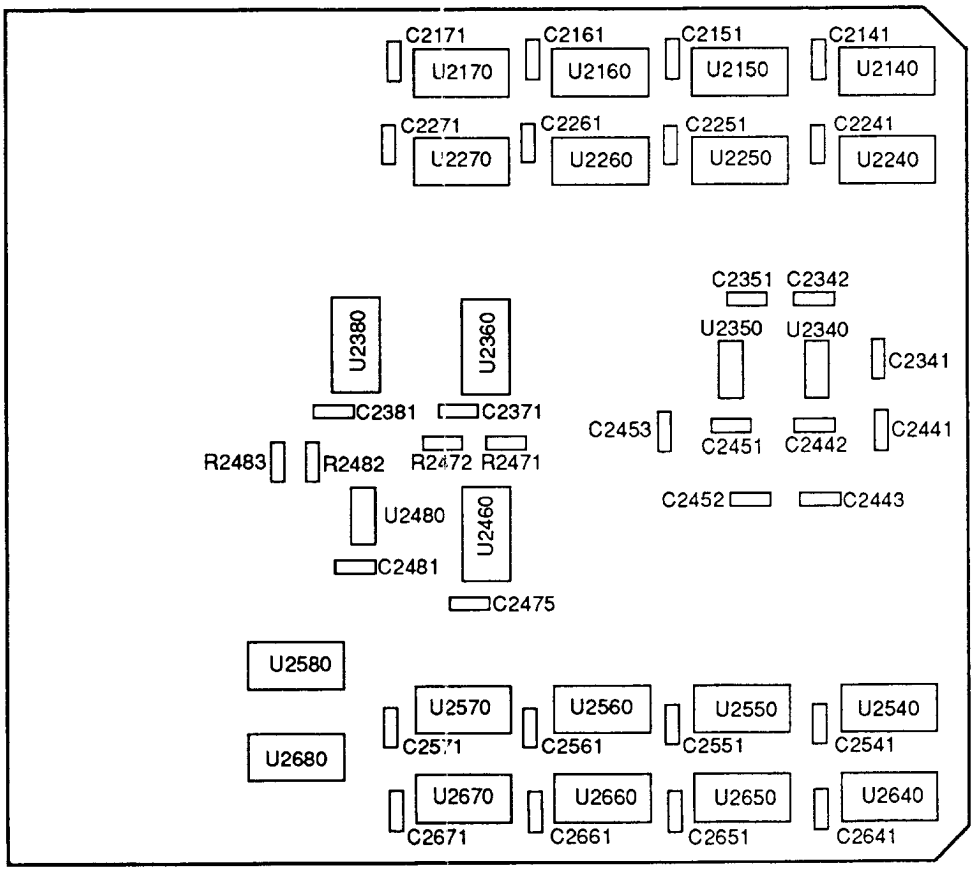
The schematic diagram(s) and circuit board component location illustration both have grids. A look up table (when shown) provides grid coordinates for ease of locating components. There may be two tables for each assembly: one for the circuit board component location illustration and one for the schematic diagram(s).



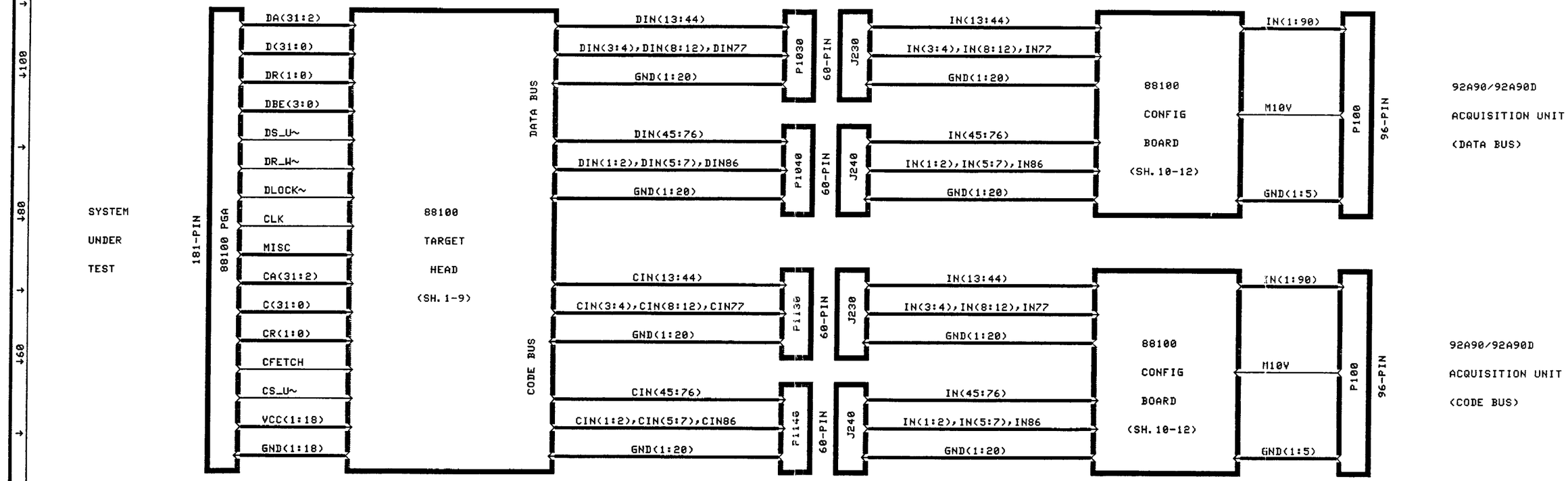
FRONT



BACK



92DM35A Target Head board component locations.



MISC = INT,ERR,PCE,PLLEN,RST~

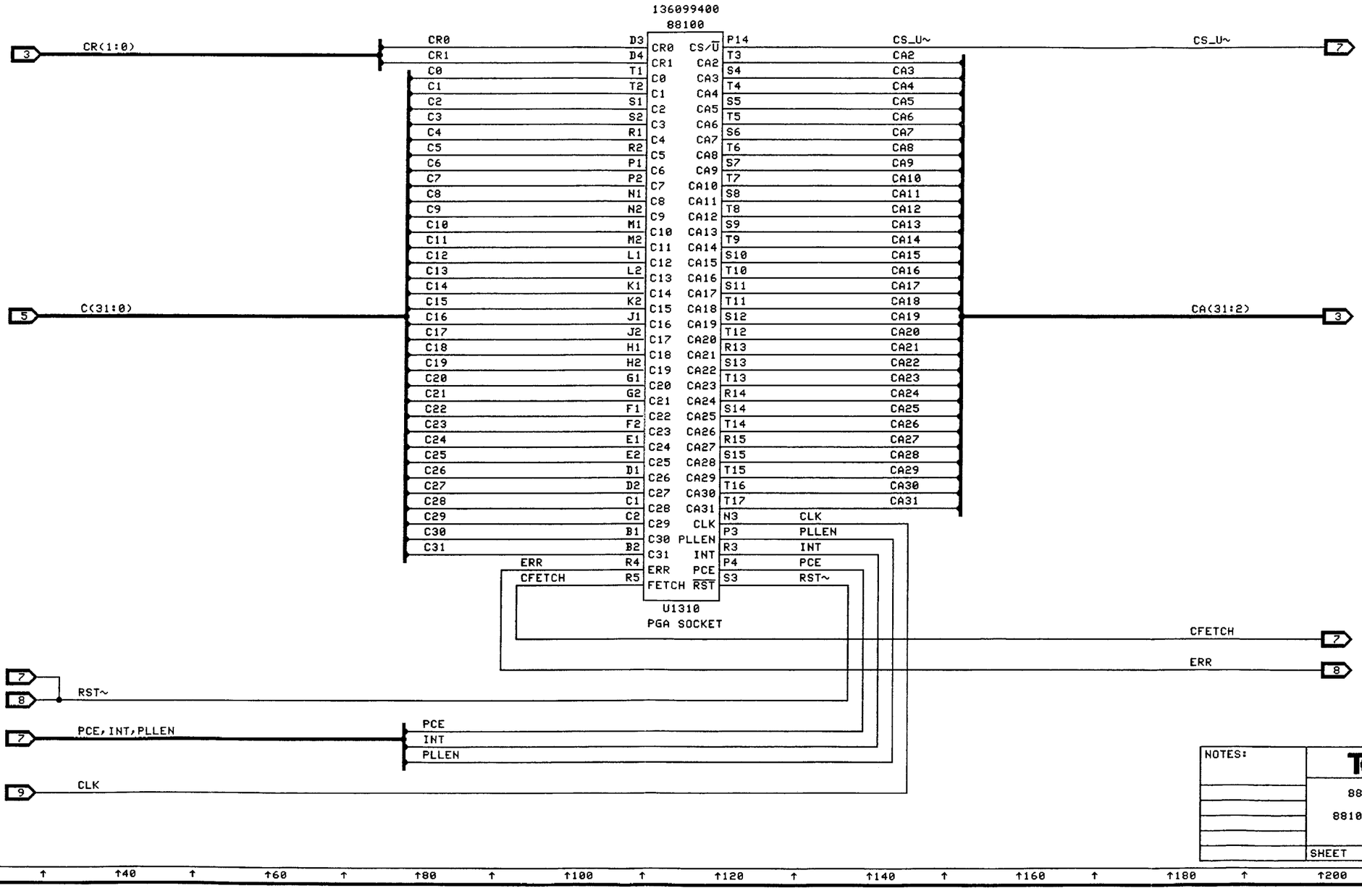
NOTES:

Tektronix

88100 PROBE ADAPTER
BLOCK DIAGRAM

SHEET 0 OF 12 | REV

01 MAY 89 11:04 /$A/USER/JACKP/88100 1.DRAW



NOTES:	Tektronix
	88100 TARGET HEAD
	88100 SOCKET (CODE BUS)
	(PAGE 1 OF 9)
	SHEET 1 OF 12 | REV

01 MAY 89 11:05 /$A/USER/JACKP/88100/TARGET 1.DRAW

136099400
88100

4 DR(1:0)

DR0	N15	DR0	DR/W
DR1	P15	DR1	LOCK
D0	A17	D0	DBE0
D1	A16	D1	DBE1
D2	B17	D2	DBE2
D3	B16	D3	DBE3
D4	C17	D4	DA2
D5	C16	D5	DA3
D6	D17	D6	DA4
D7	D16	D7	DA5
D8	E17	D8	DA6
D9	E16	D9	DA7
D10	F17	D10	DA8
D11	F16	D11	DA9
D12	G17	D12	DA10
D13	G16	D13	DA11
D14	H17	D14	DA12
D15	H16	D15	DA13
D16	J17	D16	DA14
D17	J16	D17	DA15
D18	K17	D18	DA16
D19	K16	D19	DA17
D20	L17	D20	DA18
D21	L16	D21	DA19
D22	M17	D22	DA20
D23	M16	D23	DA21
D24	N17	D24	DA22
D25	N16	D25	DA23
D26	P17	D26	DA24
D27	P16	D27	DA25
D28	R17	D28	DA26
D29	R16	D29	DA27
D30	S17	D30	DA28
D31	S16	D31	DA29
			DA30
DS_U~	C5	DSU	DA31

C4	DR_W~		
C3	DLOCK~		
E15	DBE0		
D15	DBE1		
D14	DBE2		
C13	DBE3		
C15	DA2		
B15	DA3		
A15	DA4		
C14	DA5		
B14	DA6		
A14	DA7		
B13	DA8		
A13	DA9		
B12	DA10		
A12	DA11		
B11	DA12		
A11	DA13		
B10	DA14		
A10	DA15		
B9	DA16		
A9	DA17		
B8	DA18		
A8	DA19		
B7	DA20		
A7	DA21		
B6	DA22		
A6	DA23		
B5	DA24		
A5	DA25		
B4	DA26		
A4	DA27		
B3	DA28		
A3	DA29		
A2	DA30		
A1	DA31		

U1310
PGA SOCKET

DR_W~, DLOCK~, DBE(3:0) → 8

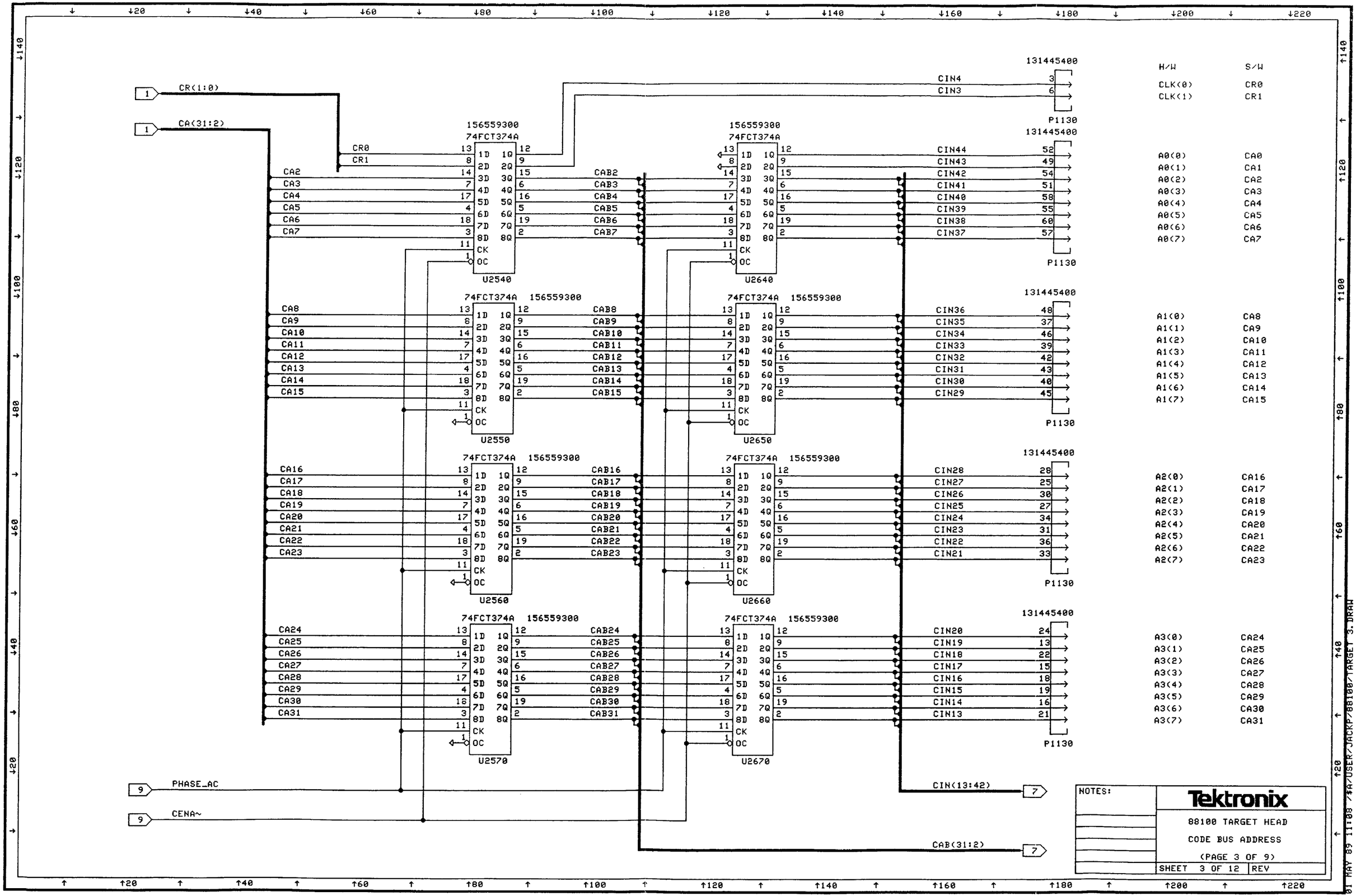
6 D(31:0)

DA(31:2) → 4

DS_U~ → 8

NOTES:	Tektronix
	88100 TARGET HEAD
	88100 SOCKET (DATA BUS)
	(PAGE 2 OF 9)
	SHEET 2 OF 12 | REV

01 MAY 89 11:07 /$A/USER/JACKP/88100/TARGET 2.DRAW


CR(1:0)
CA(31:2)
CR0
CR1
CA2
CA3
CA4
CA5
CA6
CA7
CA8
CA9
CA10
CA11
CA12
CA13
CA14
CA15
CA16
CA17
CA18
CA19
CA20
CA21
CA22
CA23
CA24
CA25
CA26
CA27
CA28
CA29
CA30
CA31
PHASE_AC
CENA~
156559300
74FCT374A
U2540
U2550
U2560
U2570
U2640
U2650
U2660
U2670
CAB2
CAB3
CAB4
CAB5
CAB6
CAB7
CAB8
CAB9
CAB10
CAB11
CAB12
CAB13
CAB14
CAB15
CAB16
CAB17
CAB18
CAB19
CAB20
CAB21
CAB22
CAB23
CAB24
CAB25
CAB26
CAB27
CAB28
CAB29
CAB30
CAB31
131445400
P1130
CIN4
CIN3
CIN44
CIN43
CIN42
CIN41
CIN40
CIN39
CIN38
CIN37
CIN36
CIN35
CIN34
CIN33
CIN32
CIN31
CIN30
CIN29
CIN28
CIN27
CIN26
CIN25
CIN24
CIN23
CIN22
CIN21
CIN20
CIN19
CIN18
CIN17
CIN16
CIN15
CIN14
CIN13
CIN(13:42)
CAB(31:2)
H/W
S/W
CLK(0) CR0
CLK(1) CR1
A0(0) CA0
A0(1) CA1
A0(2) CA2
A0(3) CA3
A0(4) CA4
A0(5) CA5
A0(6) CA6
A0(7) CA7
A1(0) CA8
A1(1) CA9
A1(2) CA10
A1(3) CA11
A1(4) CA12
A1(5) CA13
A1(6) CA14
A1(7) CA15
A2(0) CA16
A2(1) CA17
A2(2) CA18
A2(3) CA19
A2(4) CA20
A2(5) CA21
A2(6) CA22
A2(7) CA23
A3(0) CA24
A3(1) CA25
A3(2) CA26
A3(3) CA27
A3(4) CA28
A3(5) CA29
A3(6) CA30
A3(7) CA31
NOTES:
Tektronix
88100 TARGET HEAD
CODE BUS ADDRESS
(PAGE 3 OF 9)
SHEET 3 OF 12
REV
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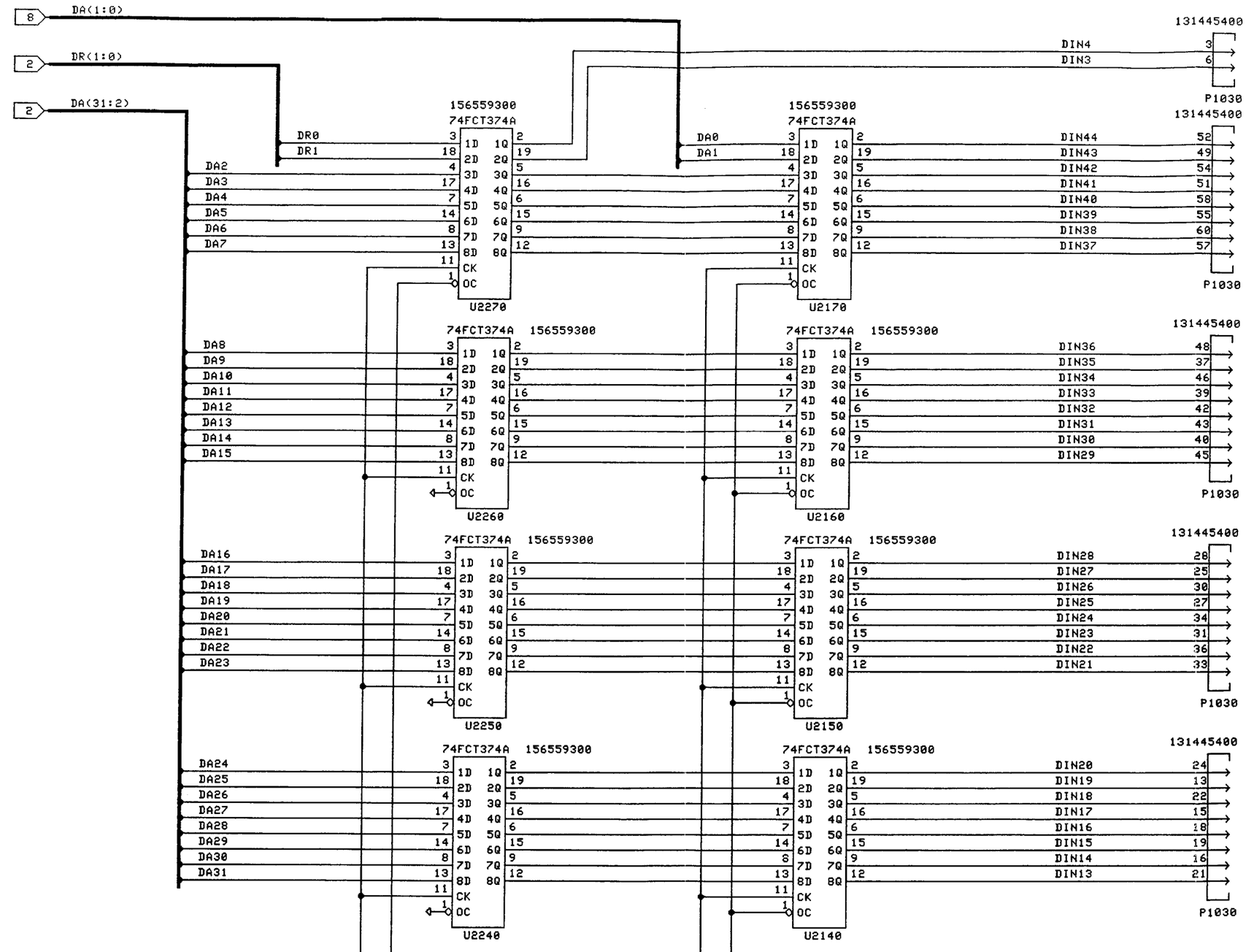


NOTES:

Tektronix

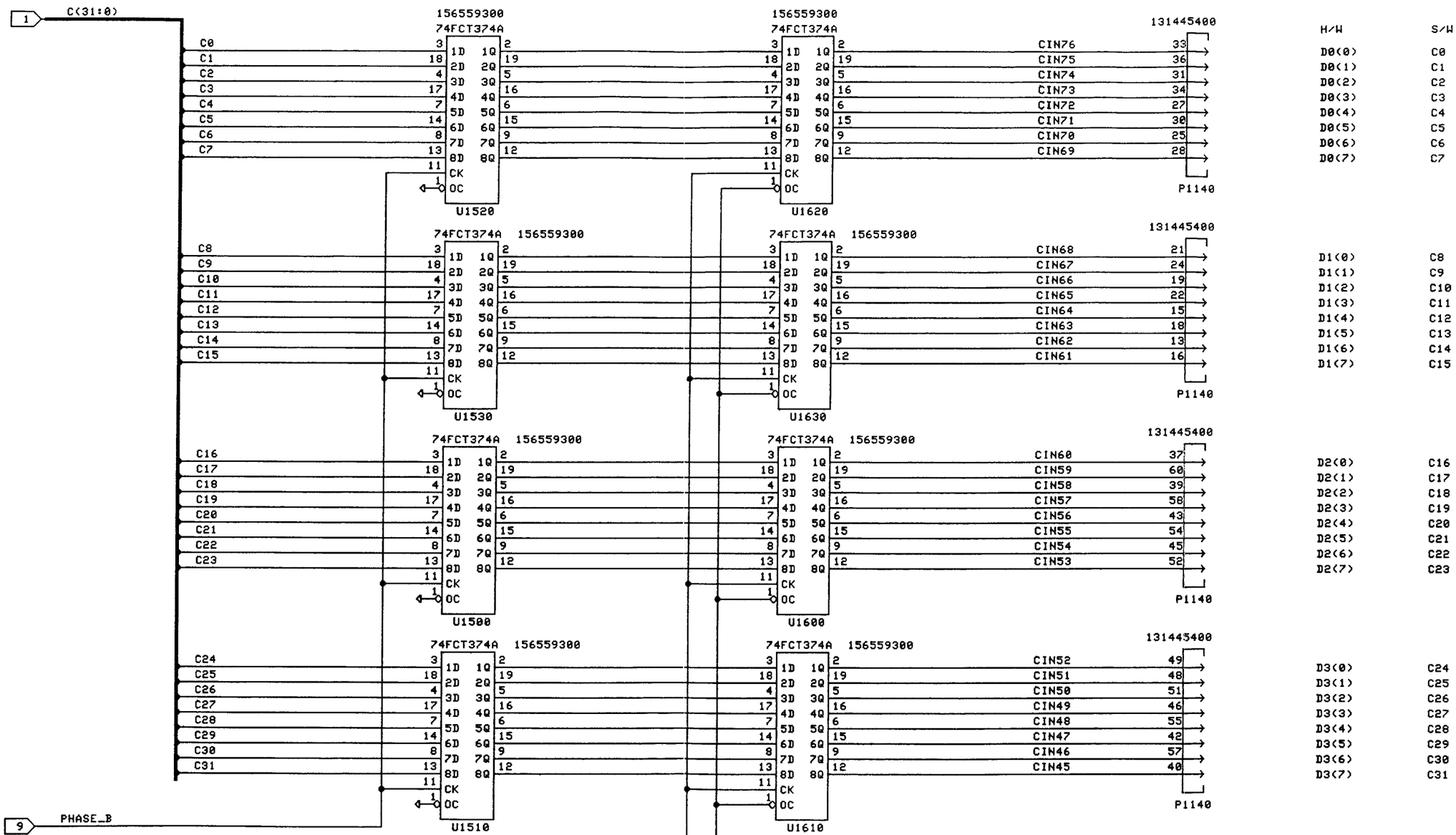
88100 TARGET HEAD

DATA BUS ADDRESS

(PAGE 4 OF 9)

SHEET 4 OF 12 | REV

01 MAY 89 11:11 /#A/USER/JACKP/88100/TARGET 4.DRAW



NOTES:

Tektronix

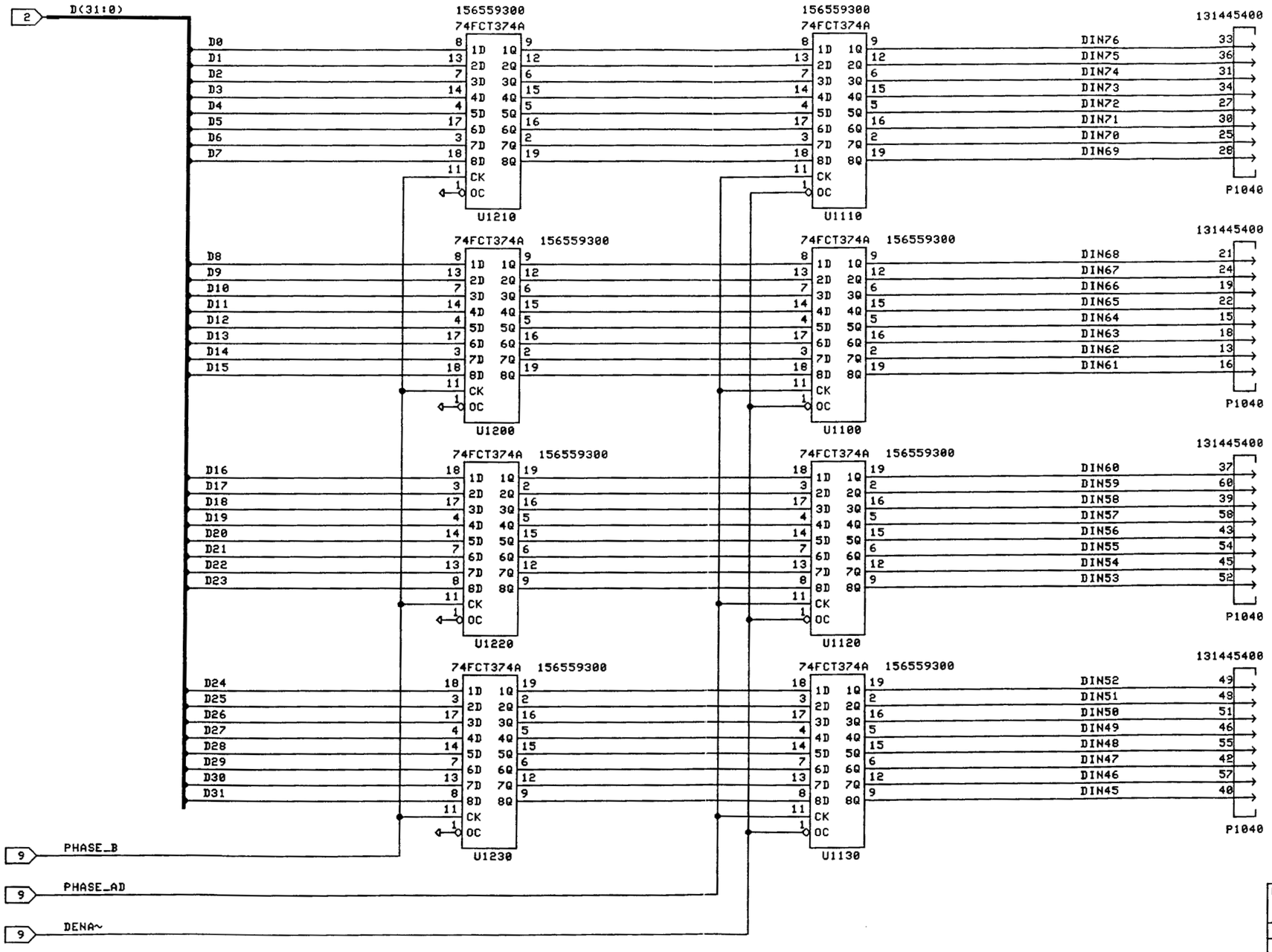
88100 TARGET HEAD

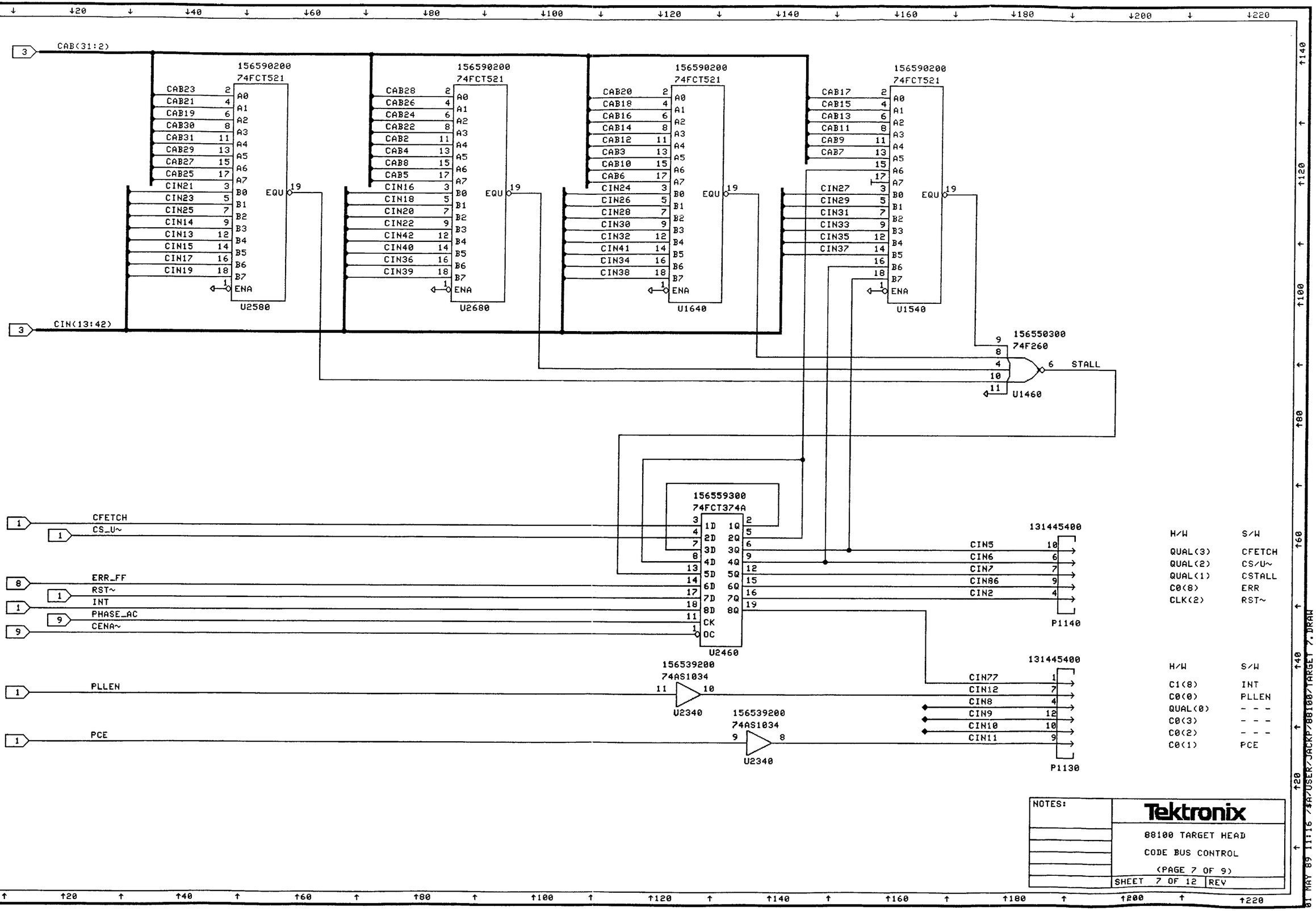
CODE BUS WORD

(PAGE 5 OF 9)

SHEET 5 OF 12 | REV

07 JUL 89 11:58 /USER7/JACKP/88100/TARGET 5.DRAW


2
D(31:0)
156559300
74FCT374A
U1210
U1110
U1200
U1100
U1220
U1120
U1230
U1130
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
1D 1Q
2D 2Q
3D 3Q
4D 4Q
5D 5Q
6D 6Q
7D 7Q
8D 8Q
CK
OC
131445400
P1040
DIN76
DIN75
DIN74
DIN73
DIN72
DIN71
DIN70
DIN69
DIN68
DIN67
DIN66
DIN65
DIN64
DIN63
DIN62
DIN61
DIN60
DIN59
DIN58
DIN57
DIN56
DIN55
DIN54
DIN53
DIN52
DIN51
DIN50
DIN49
DIN48
DIN47
DIN46
DIN45
H/W
S/W
D0(0) D0
D0(1) D1
D0(2) D2
D0(3) D3
D0(4) D4
D0(5) D5
D0(6) D6
D0(7) D7
D1(0) D8
D1(1) D9
D1(2) D10
D1(3) D11
D1(4) D12
D1(5) D13
D1(6) D14
D1(7) D15
D2(0) D16
D2(1) D17
D2(2) D18
D2(3) D19
D2(4) D20
D2(5) D21
D2(6) D22
D2(7) D23
D3(0) D24
D3(1) D25
D3(2) D26
D3(3) D27
D3(4) D28
D3(5) D29
D3(6) D30
D3(7) D31
9
PHASE_B
PHASE_AD
DENA~
NOTES:
Tektronix
88100 TARGET HEAD
DATA BUS WORD
(PAGE 6 OF 9)
SHEET 6 OF 12
REV
07 JUL 89 11:56 /USER2/JACKP/88100/TARGET 6.DRAW


CAB(31:2)
CIN(13:42)
156590200
74FCT521
U2580
U2680
U1640
U1540
EQU
ENA
156550300
74F260
U1460
STALL
156559300
74FCT374A
U2460
CFETCH
CS_U~
ERR_FF
RST~
INT
PHASE_AC
CENA~
156539200
74AS1034
U2340
PLLEN
PCE
131445400
P1140
P1130
H/W S/W
QUAL(3) CFETCH
QUAL(2) CS/U~
QUAL(1) CSTALL
C0(8) ERR
CLK(2) RST~
C1(8) INT
C0(0) PLLEN
QUAL(0) - - -
C0(3) - - -
C0(2) - - -
C0(1) PCE
NOTES:
Tektronix
88100 TARGET HEAD
CODE BUS CONTROL
(PAGE 7 OF 9)
SHEET 7 OF 12 REV
01 MAY 89 11:16 /$R/USER/JACKP/88100/TARGET 7.DRAW

131060800
J1380
BIG END
LITTLE END
325500700
47K
R2483
325500700
47K
R2482
156550300
74F260
U1460
NULL
156505500
74F74
PR
D
Q
CK
CLR
U2480
131445400
P1030
DIN12
156516500
74F64
U1480
DA1
156516500
74F64
U1380
DA0
131445400
P1040
DIN5
DIN6
DIN7
131445400
P1030
DIN8
DIN9
DIN10
DIN11
131445400
P1040
DIN86
DIN2
156539200
74AS1034
U2340
131445400
DIN77
P1030
156559300
74FCT374A
U2360
156559300
74FCT374A
U2380
DBE(3:0),DS_U~,DR_W~,DLOCK~
DBE3
DBE2
DBE1
DBE0
DS_U~
DR_W~
DLOCK~
RST~
PHASE_AD
DENA~
156505500
74F74
U2480
ERR
PHASE_B
ERR_FF
ERR_FF

H/W	S/W
C0(0)	DNULL~
QUAL(3)	DBE3
QUAL(2)	DBE2
QUAL(1)	DBE1
QUAL(0)	DBE0
C0(3)	DS/U~
C0(2)	DR/W~
C0(1)	DLOCK~
C0(8)	ERR
CLK(2)	RST~
C1(8)	ERR_LATE

NOTES:

Tektronix

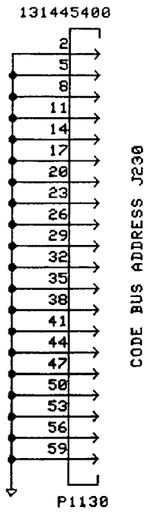
88100 TARGET HEAD

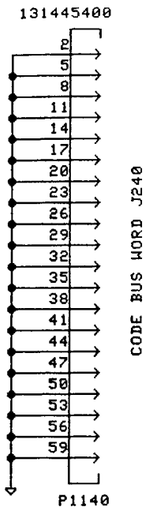
DATA BUS CONTROL

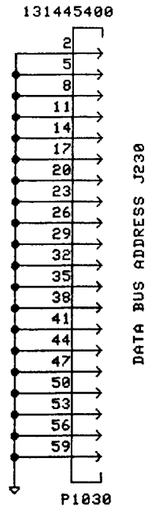
(PAGE 8 OF 9)

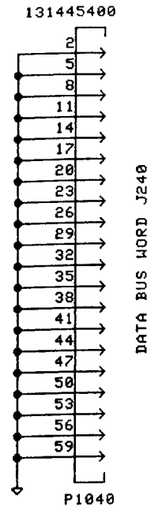
SHEET 8 OF 12 | REV

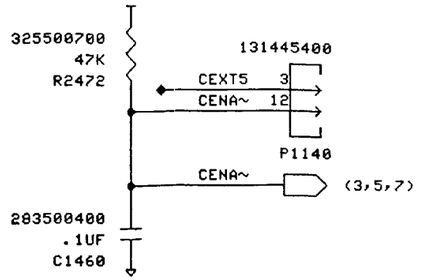
01 MAY 89 11:18 /$A/USER/JACKP/88100/TARGET_8.DRAW

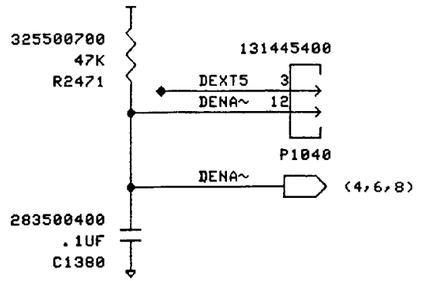


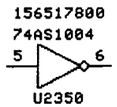


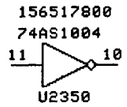


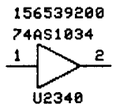


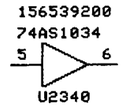


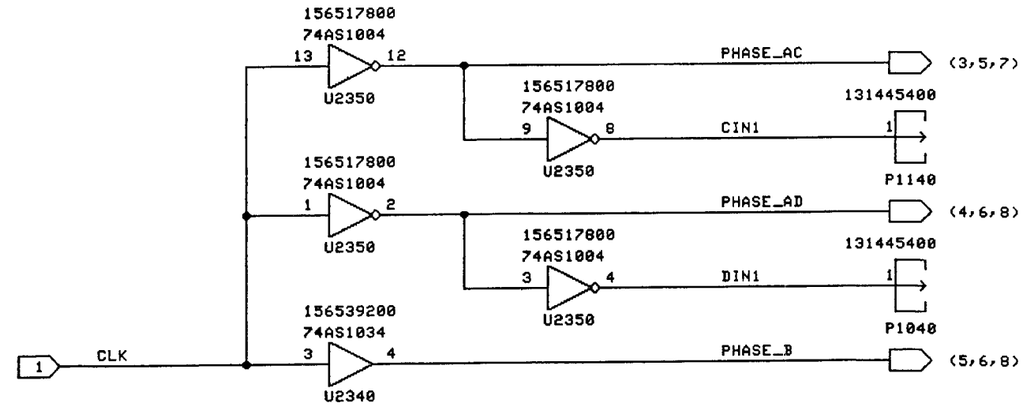


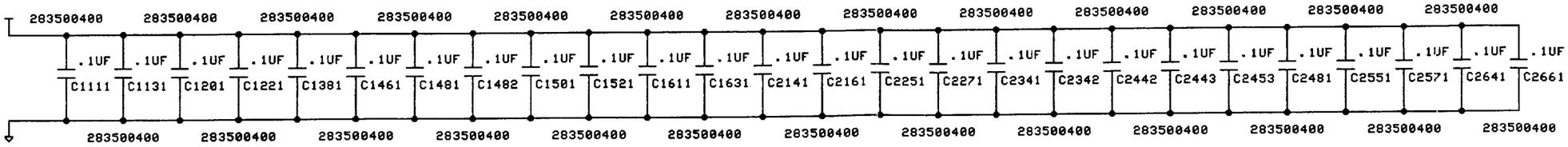


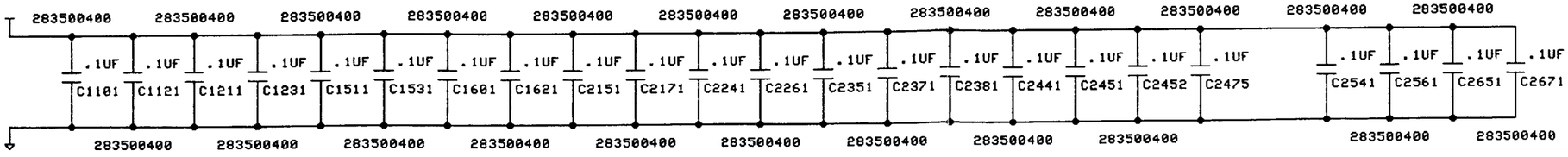












NOTES:

Tektronix

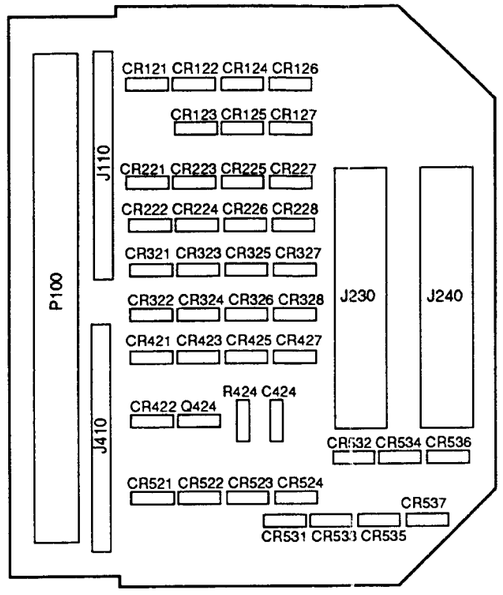
88100 TARGET HEAD

MISCELLANEOUS

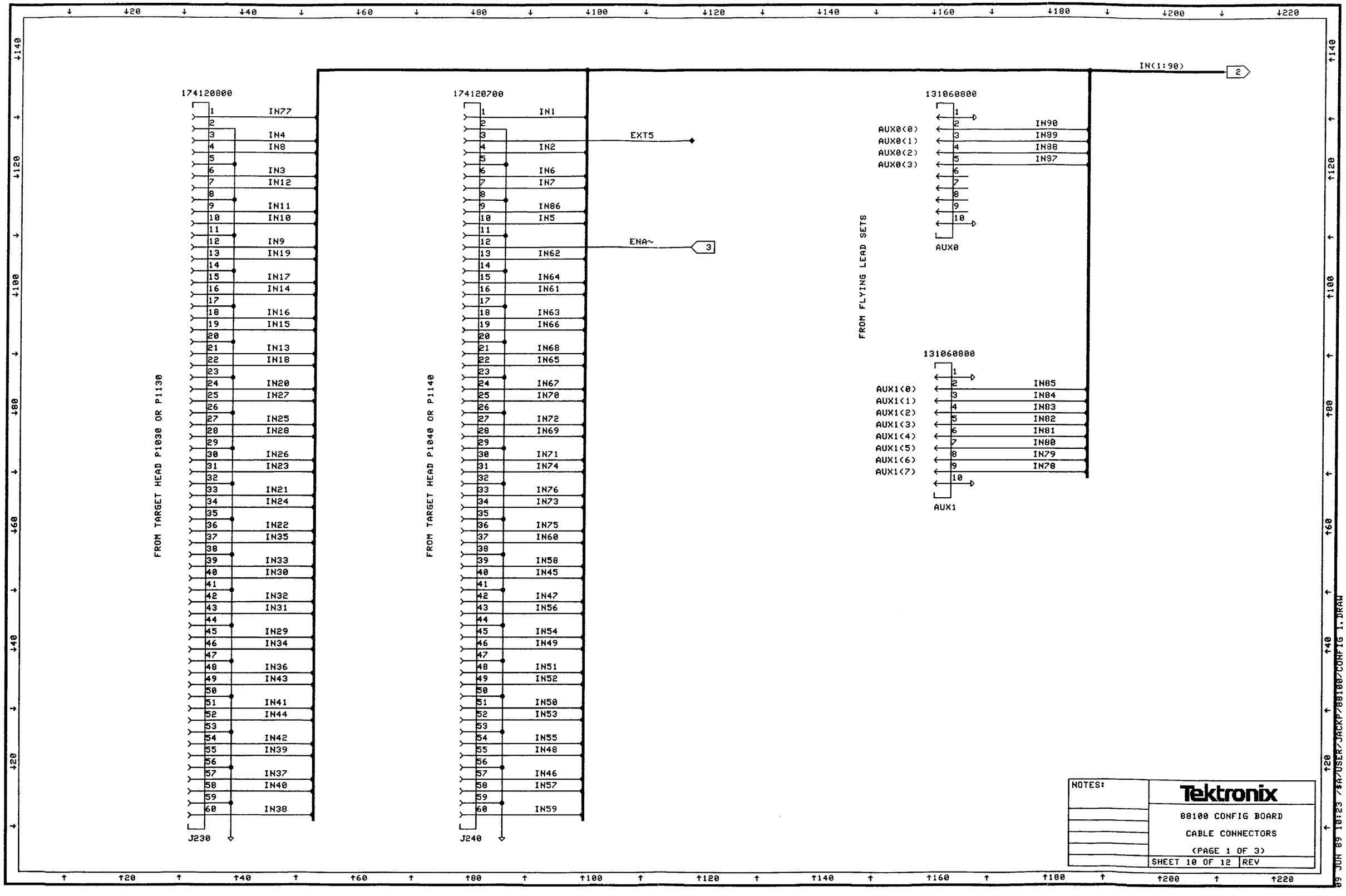
(PAGE 9 OF 9)

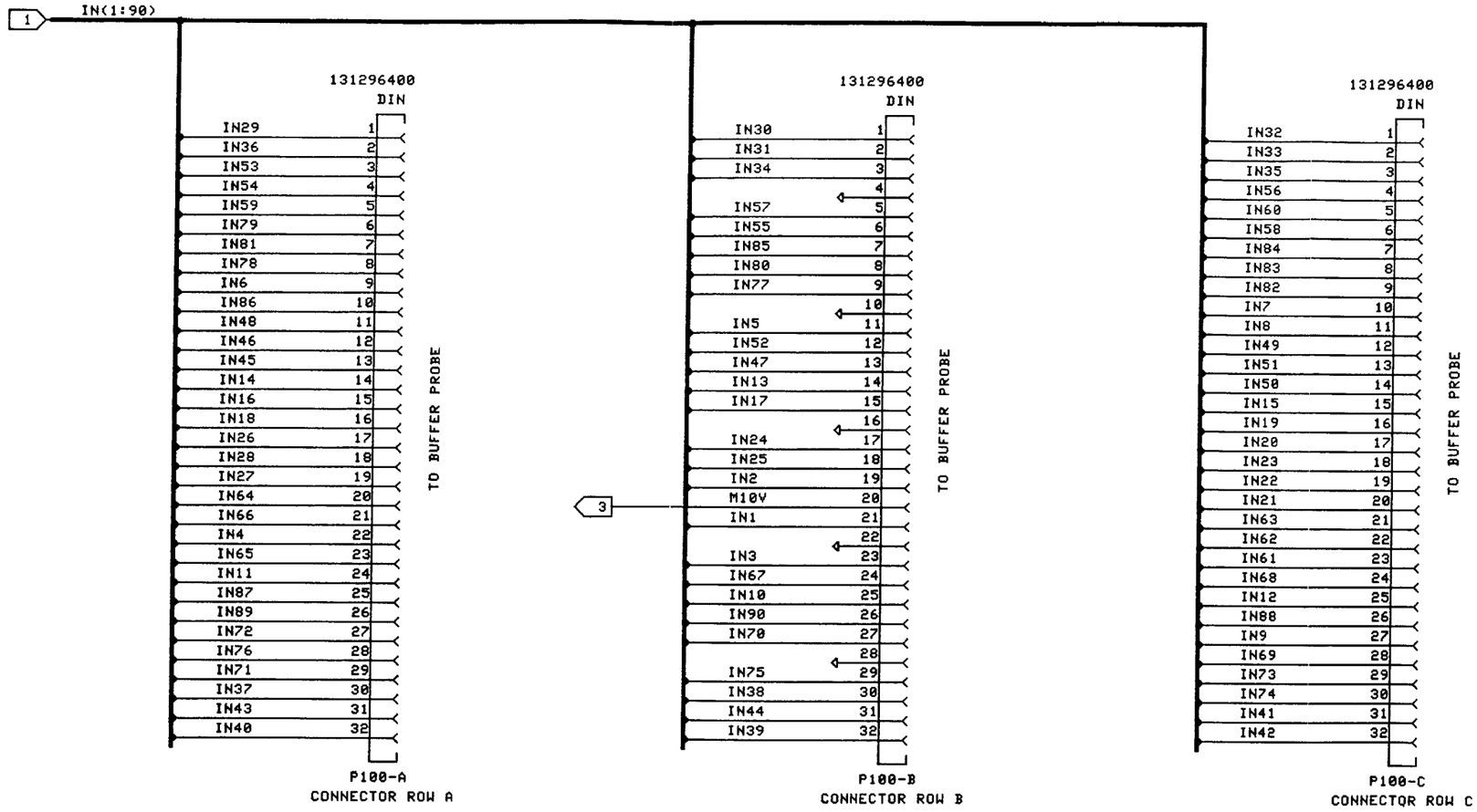
SHEET 9 OF 12 | REV

07 JUL 89 11:54 /USER/JACKP/88100/TARGET 9.DRAW



92DM35A Configuration board component locations.


IN(1:90)
2
174120800
FROM TARGET HEAD P1030 OR P1130
1 IN77
2
3 IN4
4 IN8
5
6 IN3
7 IN12
8
9 IN11
10 IN10
11
12 IN9
13 IN19
14
15 IN17
16 IN14
17
18 IN16
19 IN15
20
21 IN13
22 IN18
23
24 IN20
25 IN27
26
27 IN25
28 IN28
29
30 IN26
31 IN23
32
33 IN21
34 IN24
35
36 IN22
37 IN35
38
39 IN33
40 IN30
41
42 IN32
43 IN31
44
45 IN29
46 IN34
47
48 IN36
49 IN43
50
51 IN41
52 IN44
53
54 IN42
55 IN39
56
57 IN37
58 IN40
59
60 IN38
J230
174120700
FROM TARGET HEAD P1040 OR P1140
1 IN1
2
3 EXT5
4 IN2
5
6 IN6
7 IN7
8
9 IN86
10 IN5
11
12 ENA~
13 IN62
14
15 IN64
16 IN61
17
18 IN63
19 IN66
20
21 IN68
22 IN65
23
24 IN67
25 IN70
26
27 IN72
28 IN69
29
30 IN71
31 IN74
32
33 IN76
34 IN73
35
36 IN75
37 IN60
38
39 IN58
40 IN45
41
42 IN47
43 IN56
44
45 IN54
46 IN49
47
48 IN51
49 IN52
50
51 IN50
52 IN53
53
54 IN55
55 IN48
56
57 IN46
58 IN57
59
60 IN59
J240
3
131060800
FROM FLYING LEAD SETS
1
AUX0(0) 2 IN90
AUX0(1) 3 IN89
AUX0(2) 4 IN88
AUX0(3) 5 IN87
6
7
8
9
10
AUX0
131060800
1
AUX1(0) 2 IN85
AUX1(1) 3 IN84
AUX1(2) 4 IN83
AUX1(3) 5 IN82
AUX1(4) 6 IN81
AUX1(5) 7 IN80
AUX1(6) 8 IN79
AUX1(7) 9 IN78
10
AUX1
NOTES:
Tektronix
88100 CONFIG BOARD
CABLE CONNECTORS
(PAGE 1 OF 3)
SHEET 10 OF 12
REV
09 JUN 89 10:23 /$A/USER/JACKP/88100/CONFIG 1.DRAW



NOTES:

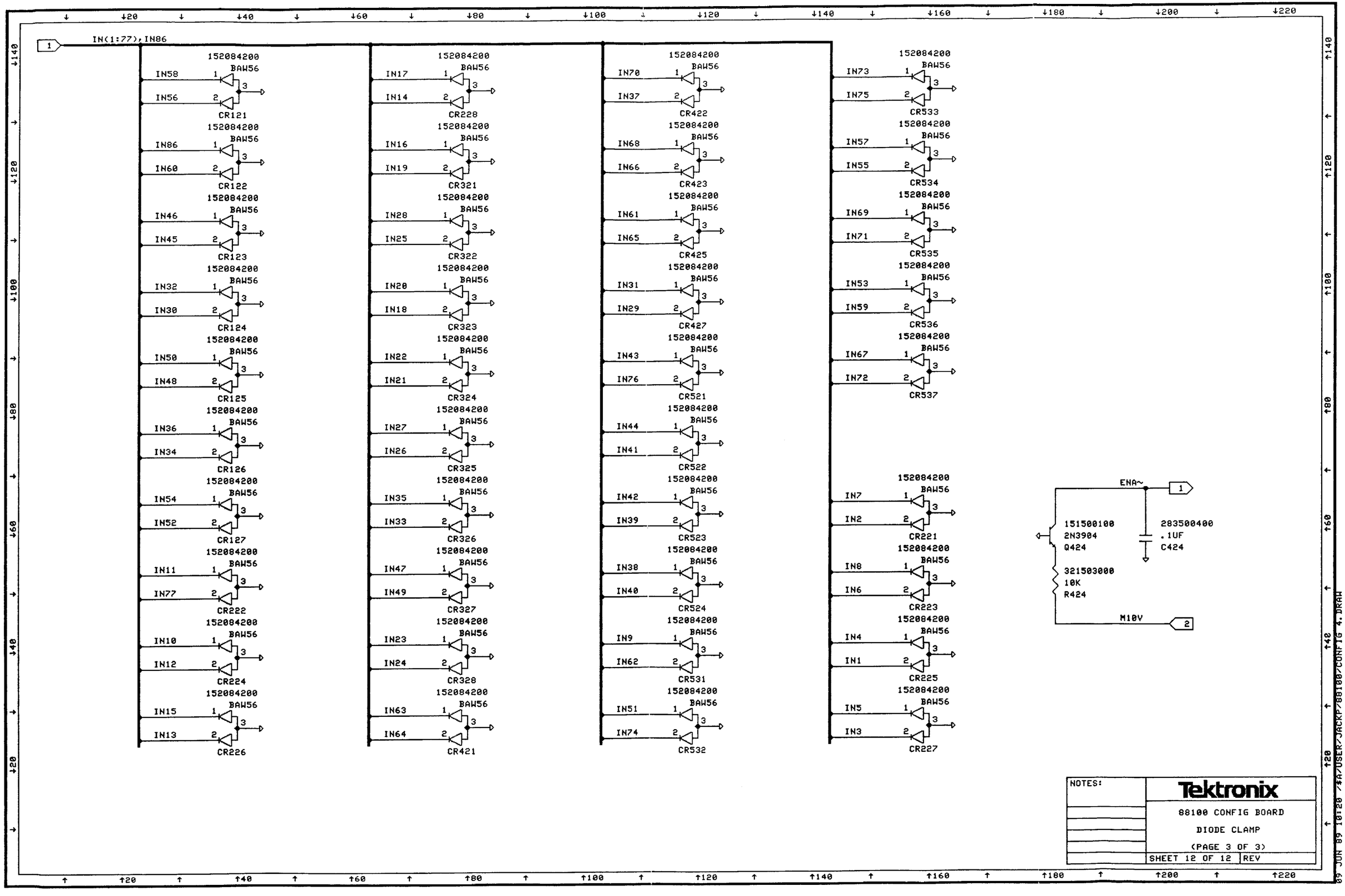
Tektronix

88100 CONFIG BOARD

BUFFER PROBE CONNECTOR

(PAGE 2 OF 3)

SHEET 11 OF 12 | REV


1
IN(1:77),IN86
152084200
BAW56
IN58
IN56
CR121
IN86
IN60
CR122
IN46
IN45
CR123
IN32
IN30
CR124
IN50
IN48
CR125
IN36
IN34
CR126
IN54
IN52
CR127
IN11
IN77
CR222
IN10
IN12
CR224
IN15
IN13
CR226
IN17
IN14
CR228
IN16
IN19
CR321
IN28
IN25
CR322
IN20
IN18
CR323
IN22
IN21
CR324
IN27
IN26
CR325
IN35
IN33
CR326
IN47
IN49
CR327
IN23
IN24
CR328
IN63
IN64
CR421
IN70
IN37
CR422
IN68
IN66
CR423
IN61
IN65
CR425
IN31
IN29
CR427
IN43
IN76
CR521
IN44
IN41
CR522
IN42
IN39
CR523
IN38
IN40
CR524
IN9
IN62
CR531
IN51
IN74
CR532
IN73
IN75
CR533
IN57
IN55
CR534
IN69
IN71
CR535
IN53
IN59
CR536
IN67
IN72
CR537
IN7
IN2
CR221
IN8
IN6
CR223
IN4
IN1
CR225
IN5
IN3
CR227
ENA~
151500100
2N3904
Q424
283500400
.1UF
C424
321503000
10K
R424
M10V
2
NOTES:
Tektronix
88100 CONFIG BOARD
DIODE CLAMP
(PAGE 3 OF 3)
SHEET 12 OF 12
REV
09 JUN 89 10:20 /#A/USER/JACKP/88100/CONFIG 4.DRAW

Replaceable Mechanical Parts

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```
1 2 3 4 5                    Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
     **** END ATTACHING PARTS ****
  Detail Part of Assembly and/or Component
  Attaching parts for Detail Part
       **** END ATTACHING PARTS ****
    Parts of Detail Part
    Attaching parts for Parts of Detail Part
         **** END ATTACHING PARTS ****
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX – MFR CODE NUMBER TO MANUFACTURER

Mfr Code	Manufacturer	Address	City, State, Zip Code
01536	TEXTRON INC CAMCAR DIV	1818 CHRISTINA ST	ROCKFORD IL 61108
07416	NELSON NAME PLATE CO	3191 CASITAS	LOS ANGELES CA 90039-2410
0JR05	TRIQUEST CORP	3000 LEWIS AND CLARK HWY	VANCOUVER WA 98661-2999
0KB05	NORTH STAR NAMEPLATE	1281-S NE 25TH	HILLSBORO OR 97124
22526	DU PONT E I DE NEMOURS AND CO INC	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
63058	MCKENZIE TECHNOLOGY	44370 OLD WARMS SPRINGS BLVD	FREMONT CA 94538
71468	ITT CANNON	666 E DYER RD	SANTA ANA CA 92702
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR	BEAVERTON OR 97077-0001
TK1163	POLYCAST INC	9898 SW TIGARD ST	TIGARD OR 97223
TK1462	YAMAICHI ELECTRONICS CO LTD	2ND FLOOR NEW KYOEI BLDG 17-11 3-CHROME SHIBAURA MINATO-KU	TOKYO JAPAN
TK1947	NORTHWEST ETCH TECHNOLOGY	3223 C ST NE	AUBURN WA 98002
TK2156	ACACIA/DEANCO	7763 SW CIRRUS RD	BEAVERTON OR 97005-6452

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Qty	12345 Part Name & Description	Mfr Code	Mfr Part Number
C3-	010-6622-00			1	PROBE,ADAPTER:88100	80009	010-6622-00
-1	334-6919-02			2	.MARKER,IDENT:MARKED AUX & GND	0KB05	334-6919-02
-2	334-6421-15			2	.MARKER,IDENT:MARKED PROBE ADAPTER	07416	334-6421-15
-3	380-0790-02			2	.HOUSING,PLUG:UPPER	TK1163	380-0790-02
-4	211-0259-00			4	.SCR,ASSEM WSHR:2-56 X 0.437,PNH,STL,POZ	01536	4821-00021
-5	671-1534-00			2	.CIRCUIT BD ASSY:88100 PROBE ADAPTER CONFIG	80009	671-1534-00
-6	131-0608-00			20	..TERMINAL,PIN:PCB/PRESSFIT,:MALE,STR,0.025	22526	48283-036
-7	131-2964-00			1	..CONN,DIN::PCB,:FEMALE,RTANG,3 X 32,0.1 CT	71468	G60M096P3-BEBM
-8	337-3388-00			1	..SHIELD,ELEC:	TK1947	ORDER BY DESCRIPTION
-9	174-1208-00			1	..CA ASSY,SP,ELEC:60,30 AWG,15.0 L,RIBBON	TK2156	63995
-10	174-1207-00			1	..CA ASSY,SP,ELEC:60,30 AWG,13.7 L,RIBBON	TK2156	63994
-11	671-1436-00			1	.CIRCUIT BD ASSY:88100 TARGET	80009	671-1436-00
-12	131-4454-00			4	..CONN,HDR::PCB,:MALE,STR,2 X 30,0.05 X 0.1	TK1462	NFP-60A-0104
-13	131-0608-00			3	..TERMINAL,PIN:PCB/PRESSFIT,:MALE,STR,0.025	22526	48283-036
-14	131-0993-00			1	..BUS,CONDUCTOR:SHUNT/SHORTING,:FEMALE,STR,	22526	65474-006
-15	----- -----			1	..SOCKET,PGA::PCB,:181 POS,17 X 17,0.1 CTR (NOT REPLACEABLE;ORDER 671-1436-00)		
-16	136-0993-00			2	..SOCKET,PGA::PCB,:181 POS,17 X 17,0.1 CTR	63058	PGA 181H101B1-1738F
-17	136-1105-00			1	.SKT,PL-IN ELEK:PGA,ZIF,17 X 17,181 PIN	TK1462	NP35-28916-G42AF-PES
-18	334-7350-00			1	.MARKER,IDENT:MARKED SOCKET WARNING	0KB05	334-7350-00
-19	380-0791-01			2	.HOUSING,PLUG:LOWER	TK1163	380-0791-01
-20	105-1007-00			8	.LATCH,PROBE:POLYCARBONATE	0JR05	15-1007-00
					STANDARD ACCESSORIES		
	070-8311-00			1	MANUAL,TECH:INSTR,92DM35A,88100	80009	070-8311-00
					OPTIONAL ACCESSORIES		
-21	012-0747-00			1	LEAD SET,ELEC:10 WIDE,25 CML	TK2156	61501
-22	020-1386-01			1	ACCESSORY KIT:PACKAGE OF 12 (206-0364-00)	80009	020-1386-01

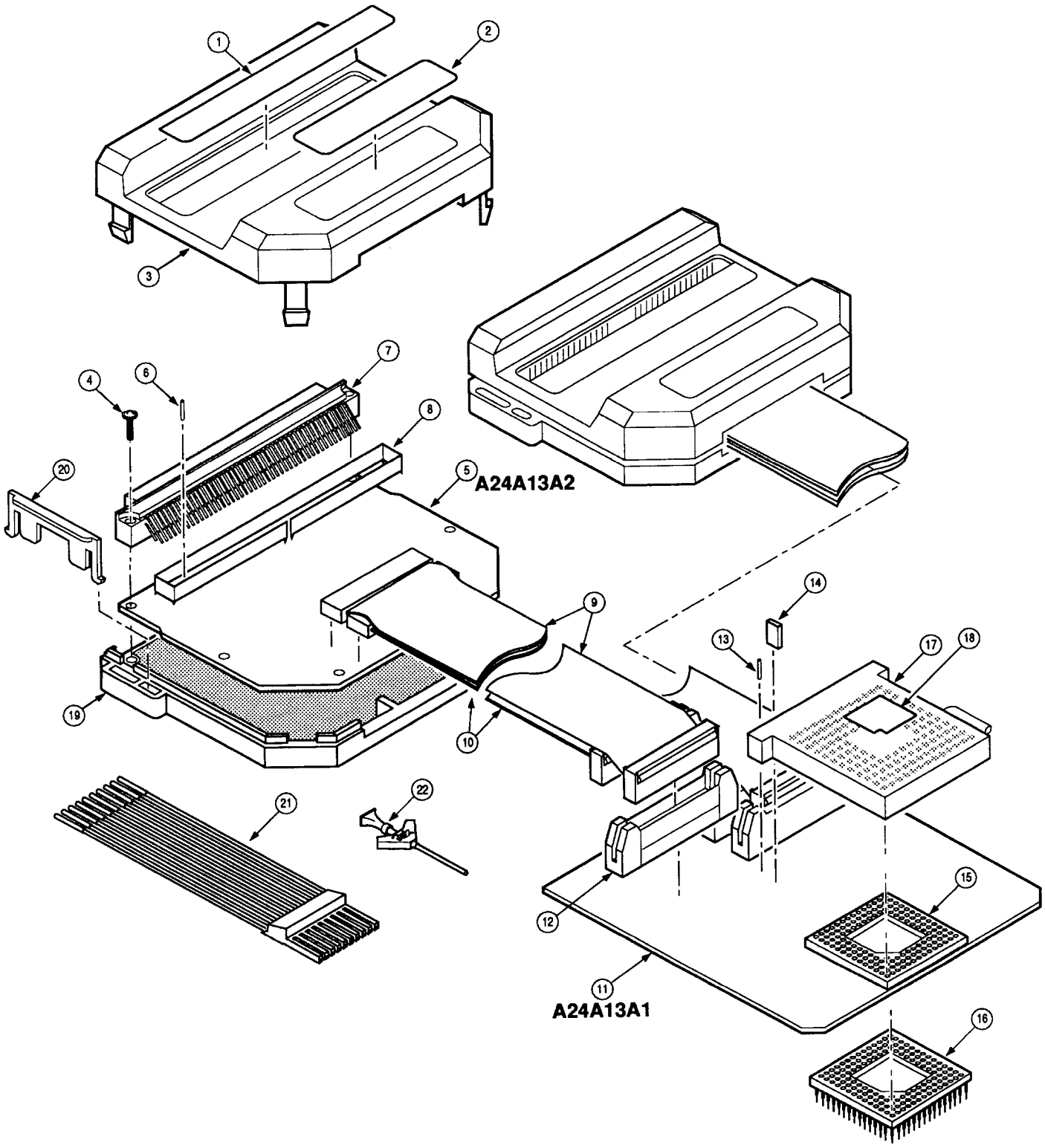


Figure C-3. Probe adapter exploded view.

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