

Instruction Manual



TMS 202 68020 & 68EC020 Microprocessor Support 070-9820-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning

The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:



WARNING. Warning statements identify conditions or practices that could result in injury or loss of life.



CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:



WARNING
High Voltage



Protective Ground
(Earth) Terminal



CAUTION
Refer to Manual



Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 202 68020 and 68EC020 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 202 68020 and 68EC020 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term “XXX” or “P54C” used in field selections and file names can be replaced with 68020. This is the name of the microprocessor in field selections and file names you must use to operate the 68020 and 68EC020 support.
- The phrase “system under test (SUT)” refers to the microprocessor-based system from which data will be acquired.

- The phrase “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.
- The term “module” refers to a 102/136-channel or 96-channel module.
- 68020 refers to all supported variations of the 68020 and 68EC020 microprocessor unless otherwise noted.
- A signal that is active low has a tilde (~) following its name.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The user manual provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	<p>For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time</p> <p>Or, contact us by e-mail: tm_app_supp@tek.com</p> <p>For product support outside of North America, contact your local Tektronix distributor or sales office.</p>
Service Support	<p>Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations.</p> <p>http://www.tek.com</p>
For other information	<p>In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.</p>
To write us	<p>Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000</p>



Getting Started

Getting Started

This chapter provides information on the following topics:

- The TMS 202 68020 and 68EC020 microprocessor support
- Logic analyzer software compatibility
- Logic analyzer configuration
- Your 68020 and 68EC020 system requirements
- 68020 and 68EC020 support restrictions
- How to configure the probe adapter
- How to connect to the system under test (SUT)

Support Description

The TMS 202 microprocessor support disassembles data from systems that are based on the Motorola 68020 and 68EC020 microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module, or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 202 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 202 support can acquire and disassemble data.

Table 1–1: Product support

Microprocessor	Package
68020	PGA
68EC020	PGA
68020	CQFP

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *MC68020 and 68EC020 Microprocessor User's Manual*, (Motorola, MC68020UM/AD, Rev. 3, 1990).

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the 68020 and 68EC020 support, the Tektronix logic analyzer must be equipped with a 102/136-channel module, or a 96-channel module. The module must be equipped with enough probes to acquire clock and channel data from signals in your 68020 and 68EC020-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other 68020 and 68EC020 support requirements and restrictions.

System Clock Rate. The microprocessor support product supports the 68020 and 68EC020 microprocessor at speeds of up to 33 MHz¹ and the 68EC020 microprocessor at speeds of up to 25 MHz¹.

Disabling the Instruction Cache. To disassemble acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so that they can be acquired and disassembled.

Disassembling Storage-Qualified Data. The disassembler is designed to work with available gaps in the acquisition data. Disassembly of storage-qualified data is indeterminate and will likely be incorrect.

¹ Specification at time of printing. Contact your logic analyzer sales representative for current information on the fastest devices supported.

Configuring the Probe Adapter

Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled. The probe adapter contains a jumper you can use to disable the 68020 cache.

With the cache jumper in the NORM position, the SUT controls the cache and the CDIS~ signal is not affected.

With the cache jumper in the DIS position, the CDIS~ signal connects to a 332 Ω pull-down resistor on the probe adapter, which disables the cache. For the PGA probe adapters, you should also cut or remove pin T5 from the protective socket on the underside of the probe adapter to prevent contention with the driving signal. For a CQFP probe adapter, you should disable any devices on the SUT that drive the CDIS~ signal to prevent contention with the driving signal.

Figure 1–1 shows the location of J210 on the 68020 PGA probe adapter.

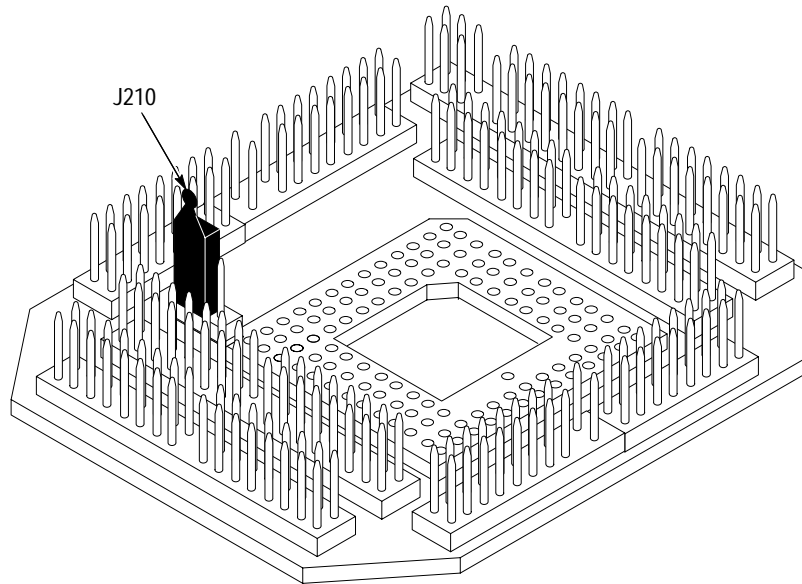


Figure 1–1: Jumper location on the 68020 PGA probe adapter

Figure 1–2 shows the location of J210 on the 68EC020 PGA probe adapter.

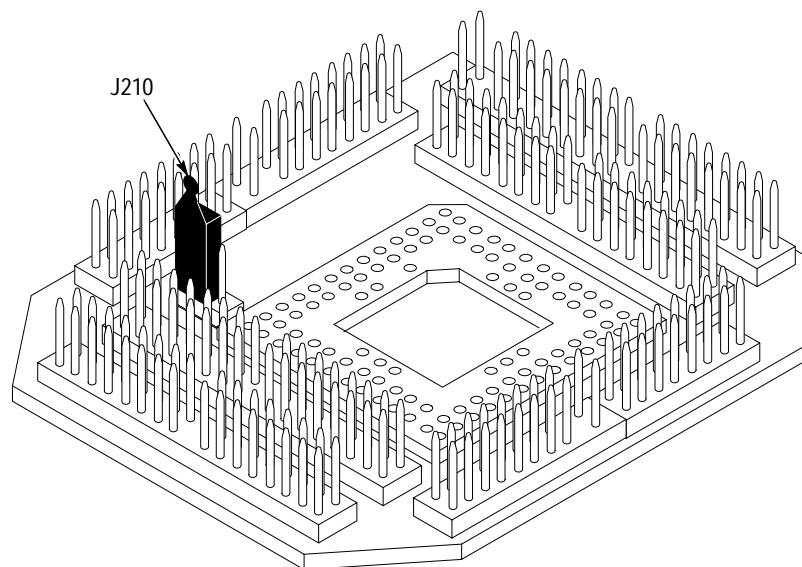


Figure 1–2: Jumper location on the 68EC020 PGA probe adapter

Figure 1–3 shows the location of J1150 on the 68020 CQFP probe adapter.

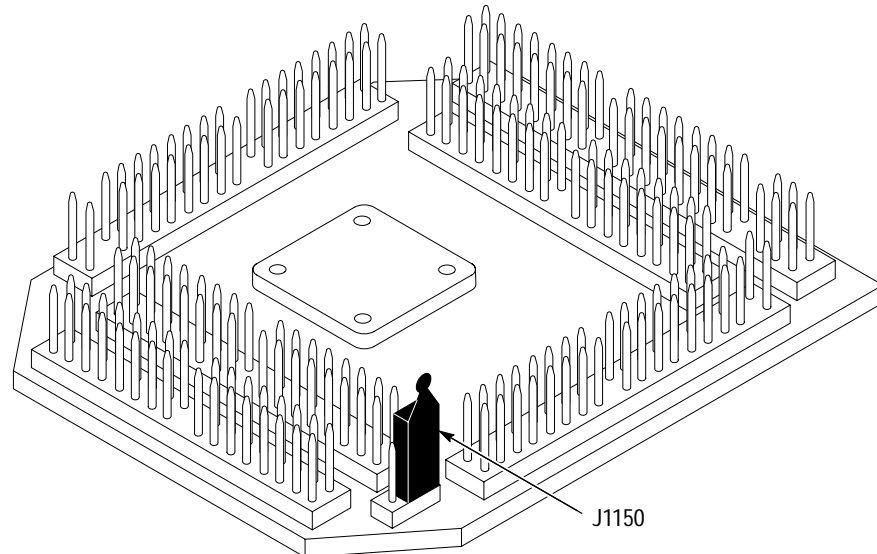


Figure 1–3: Jumper location on the 68020 CQFP probe adapter

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. Your probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PGA Probe Adapter

To connect the logic analyzer to a SUT using a PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.



CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–4. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the microprocessor from your SUT.
5. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.



CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–4.

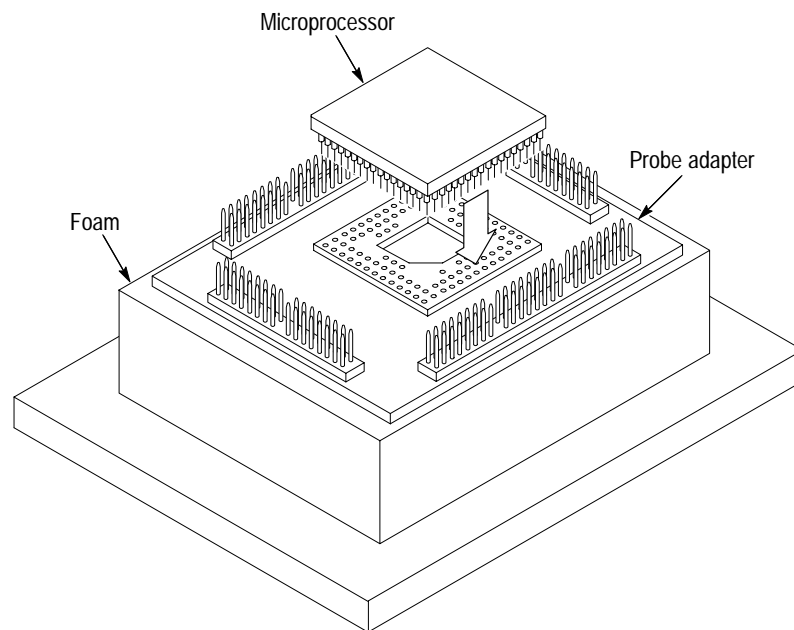


Figure 1-4: Placing a microprocessor into a PGA probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1-5. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

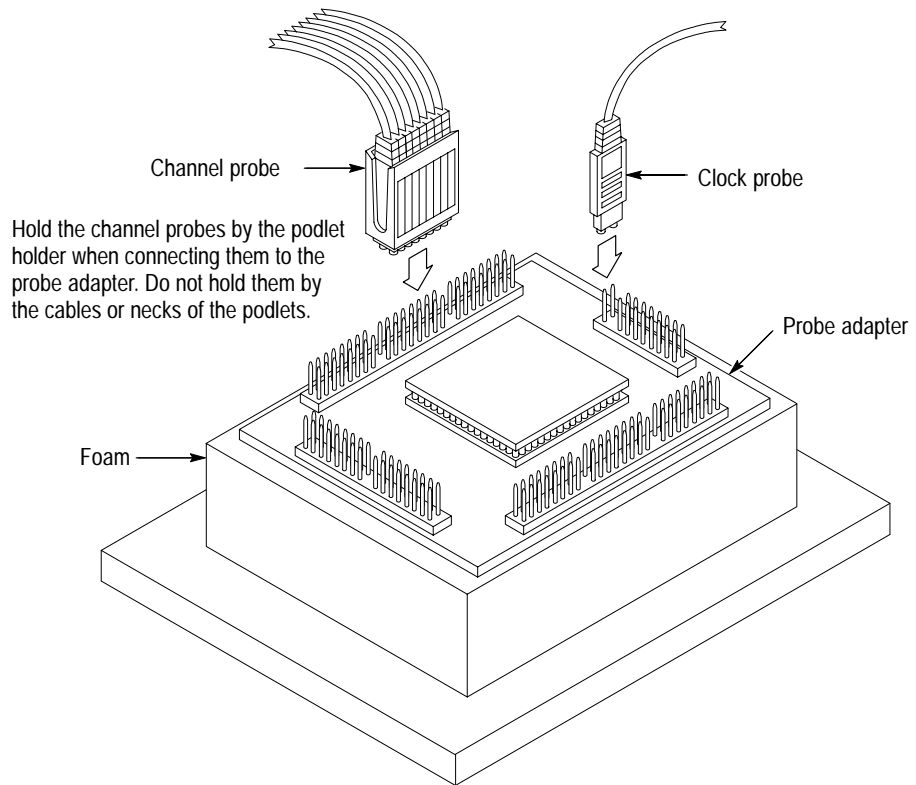


Figure 1-5: Connecting probes to a PGA probe adapter

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.
9. Place the probe adapter onto the SUT as shown in Figure 1-6.

NOTE. You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.

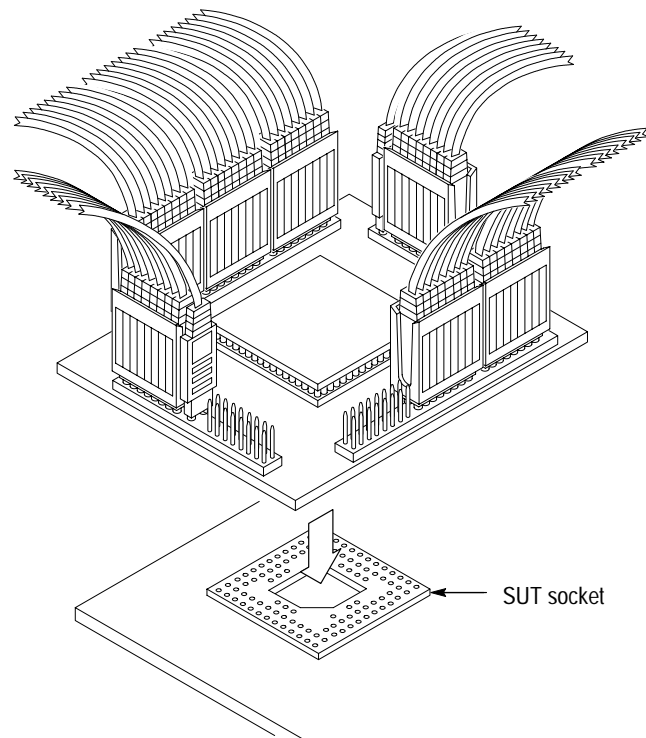


Figure 1-6: Placing a PGA probe adapter onto the SUT

CQFP Probe Adapter

To connect the logic analyzer to a SUT using a CQFP probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.



CAUTION. Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all the above only in a static-free environment.

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1-7. This prevents the circuit board from flexing.

4. Connect the channel and clock probes to the probe adapter as shown in Figure 1–7. Match the channel groups and numbers on the probe labels to the corresponding probe adapter pins. Match the ground pins on the probes to the corresponding pins on the probe adapter.

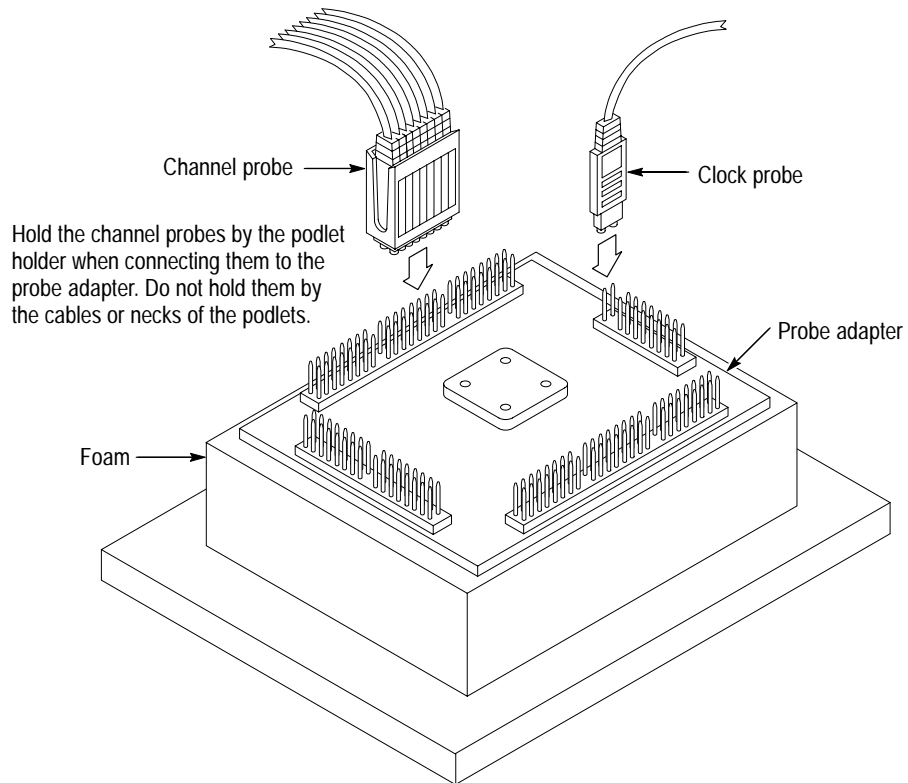


Figure 1–7: Connecting probes to a CQFP probe adapter



CAUTION. This JEDEC (Quad Flat Pack) probe adapter has been equipped with a clip that has been designed for tight tolerances.

The clip supports only Quad Flat Pack devices that conform to the JEDEC M0-069 October 1990 specification. Attaching the clip to a device that does not conform to this JEDEC standard can easily damage the clip's connection pins and/or the microprocessor, causing the probe adapter to malfunction.

Please contact your IC manufacturer to verify that the microprocessor you are targeting conforms to the JEDEC specification.

For best performance and long probe life, exercise extreme care when connecting the probe adapter to the microprocessor.

5. Place a little glue on each corner of the CQFP-to-PQFP converter.

6. Place the CQFP-to-PQFP converter over your CQFP microprocessor as shown in Figure 1–8.

NOTE. Do not allow the glue to touch the pins of your microprocessor. This might interfere with the connection between the microprocessor and the probe adapter. An open connection will cause errors.

7. Allow the glue to dry.

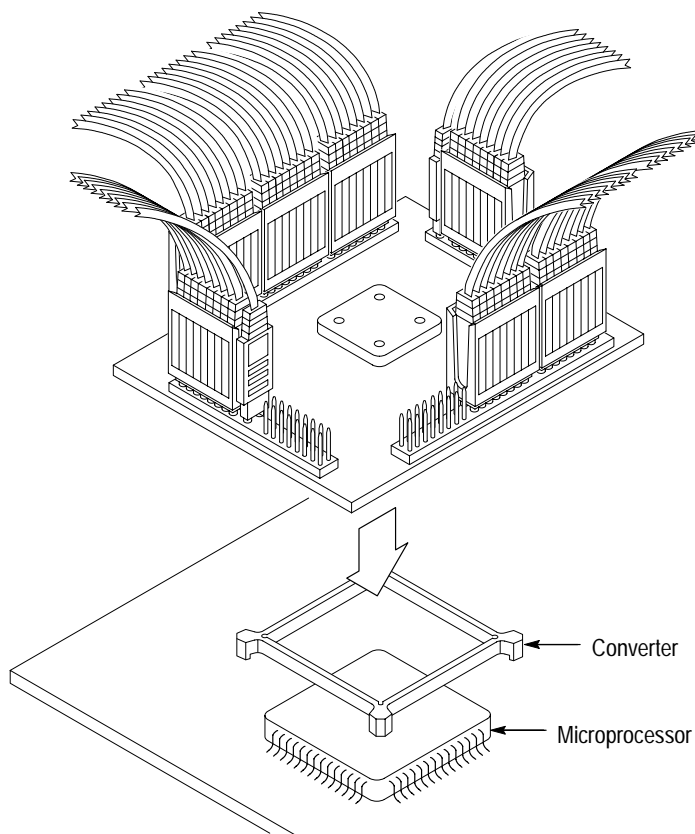


Figure 1–8: Placing a CQFP probe adapter onto the SUT

8. Line up the pin 1 indicator on CQFP clip on the probe adapter with the pin 1 indicator on the microprocessor.



CAUTION. Failure to correctly place the probe adapter onto the microprocessor might permanently damage all electrical components when power is applied.

Center the clip on the microprocessor and apply an equal downward force on all four sides of the clip, slightly rocking the probe adapter in a clockwise circle.

Do not apply leverage to the probe adapter when installing or removing it.

9. Place the probe adapter onto the SUT as shown in Figure 1–8.

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to 68020 and 68EC020 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.



CAUTION. Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.



CAUTION. Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the microprocessor.

3. Place the SUT on a horizontal static-free surface.
4. Use Table 1–2 to connect the channel probes to 68020 and 68EC020 signal pins on the test clip or in the SUT.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Table 1–2: 68020 and 68EC020 signal connections for channel probes

Section:channel	68020 and 68EC020 signal	Section:channel	68020 and 68EC020 signal
A3:7	A31	D3:7	D31
A3:6	A30	D3:6	D30
A3:5	A29	D3:5	D29
A3:4	A28	D3:4	D28
A3:3	A27	D3:3	D27
A3:2	A26	D3:2	D26
A3:1	A25	D3:1	D25
A3:0	A24	D3:0	D24
A2:7	A23	D2:7	D23
A2:6	A22	D2:6	D22
A2:5	A21	D2:5	D21
A2:4	A20	D2:4	D20
A2:3	A19	D2:3	D19
A2:2	A18	D2:2	D18
A2:1	A17	D2:1	D17
A2:0	A16	D2:0	D16
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11
A1:2	A10	D1:2	D10
A1:1	A9	D1:1	D9
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2
A0:1	A1	D0:1	D1
A0:0	A0	D0:0	D0

Table 1–2: 68020 and 68EC020 signal connections for channel probes (cont.)

Section:channel	68020 and 68EC020 signal	Section:channel	68020 and 68EC020 signal
C3:7	R/W~	C2:7	FC2
C3:6	HALT~	C2:6	FC0
C3:5	BERR~	C2:5	RMC~
C3:4	DSACK1~	C2:4	CLK=*
C3:3	DSACK0~	C2:3	AS~
C3:2	SIZ1	C2:2	ECS_L~*
C3:1	SIZ0	C2:1	RESET~ [†]
C3:0	FC1	C2:0	BGACK~, BG~
C1:7	Not connected	C0:7	Not connected
C1:6	Not connected	C0:6	BR~
C1:5	Not connected	C0:5	BG~
C1:4	Not connected	C0:4	OCS~L~
C1:3	DBEN~	C0:3	IPEND~
C1:2	AVEC~	C0:2	IPL2~
C1:1	CDIS~	C0:1	IPL0~
C1:0	DS~	C0:0	IPL1~

* Signal not required for disassembly.

Table 1–3 shows the clock probes and the 68020 and 68EC020 signal to which they must connect for disassembly to be correct.

Table 1–3: 68020 and 68EC020 signal connections for clock probes

Section:channel	68020 and 68EC020 signal
CK:3	Not connected
CK:2	CLK~ (buffered, inverted), CLK (labeled CLK_B~)
CK:1	Not connected
CK:0	Not connected

- Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the 68020 and 68EC020 microprocessor in your SUT and attach the clip to the microprocessor.



Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 202 68020 and 68EC020 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking, and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the 68020 and 68EC020 support are Address, Data, Control, DataSize, Intr, and Misc 2. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–10.

Clocking Options

The TMS 202 support offers a microprocessor-specific clocking mode for the 68020 and 68EC020 microprocessor. This clocking mode is the default selection whenever you load the 68020 support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking options for the TMS 202 support are Probe Adapter Type, DMA Cycles, and Cache & Queue Hits.

Probe Adapter Type Select the type of microprocessor and probe adapter you are using. Choose 68020A PGA or 68020A CQFP if you are using a 68020 PGA or CQFP probe adapter. Choose EC020 if you are using the 68EC020 PGA probe adapter.

DMA Cycles Determine if DMA cycles are acquired. Choose Excluded to ignore DMA cycles or Included to acquire all visible DMA cycles. Excluded is the default.

Cache & Queue Hits Determine if cache and queue hit cycles are acquired. Choose Excluded to ignore cache and queue hits. This is the default.

Choose Included to acquired all visible cache and queue hit cycles. (This works for the 68020 only since the 68EC020 does not have an ECS~ signal.) The data bus is undefined for cache hits.

Symbols

The TMS 202 support supplies two symbol table files. The 68020A_Ctrl file and 68020A_Intr replaces specific Control channel and Interrupt group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file 68020A_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value												Meaning					
	BGACK- FC2	FC1	FC0	RMC- AS-	RESET- R/W-	HALT- BERR- SIZ1 SIZ0												
ACK_ERROR	1	1	1	1	X	X	1	1	X	0	X	X	CPU space acknowledge error					
B_ERR_RTY	X	X	X	X	X	X	1	X	0	0	X	X	Bus error and retry					
BUS_ERROR	X	X	X	X	X	X	1	X	1	0	X	X	Bus error					
PREFETCH?	1	X	1	0	X	0	1	1	X	X	X	X	Read from program space					
CACHE_HIT	1	X	1	0	X	1	1	1	X	X	0	0	Read from Cache or Cache Holding Register					
DMA_READ	0	X	X	X	X	0	1	1	X	X	X	X	DMA read cycle					
DMA_WRITE	0	X	X	X	X	0	1	0	X	X	X	X	DMA write cycle					
DMA*	0	X	X	X	X	X	1	X	X	X	X	X	Any DMA cycle					
CPU_RD	X	1	1	1	X	X	1	1	X	X	X	X	CPU space read access					
CPU_WR	X	1	1	1	X	X	1	0	X	X	X	X	CPU space write access					
CPU_SPACE*	X	1	1	1	X	X	1	X	X	X	X	X	CPU space access					
RMW_READ	X	X	X	X	0	0	1	1	X	X	X	X	Read of read-modify-write cycle					

Table 2-1: Control group symbol table definitions (cont.)

Symbol	Control group value								Meaning
	BGACK- FC2 FC1 FC0	RMC- AS- RESET- RW-	HALT- BERR- SIZ1 SIZ0						
RMW_WRITE	X X X X	0 0 1 0	X X X X						Write of read-modify-write cycle
RMW*	X X X X	0 0 1 X	X X X X						Any read-modify-write cycle
DATA_RD	X X 0 1	X X 1 1	X X X X						Read from data space
DATA_WR	X X 0 1	X X 1 0	X X X X						Write to data space
PROG_RD	X X 1 0	X X 1 1	X X X X						Read from program space
PROG_WR	X X 1 0	X X 1 0	X X X X						Write to program space
READ*	X X X X	X X 1 1	X X X X						Read
WRITE*	X X X X	X X 1 0	X X X X						Write
SUPER_DAT*	X 1 0 1	X X 1 X	X X X X						Supervisor data space
SUPER_PRG*	X 1 1 0	X X 1 X	X X X X						Supervisor program space
SUPERVISR*	X 1 X X	X X 1 X	X X X X						Supervisor space
USER_DATA*	X 0 0 1	X X 1 X	X X X X						User data space
USER_PROG*	X 0 1 0	X X 1 X	X X X X						User program space
USER*	X 0 X X	X X 1 X	X X X X						User space
PRG_SPACE*	X X 1 0	X X 1 X	X X X X						Program space access
DAT_SPACE*	X X 0 1	X X 1 X	X X X X						Data space access
RESET	X X X X	X X 0 X	X X X X						RESET~ signal asserted
HALT_REQ*	X X X X	X X 1 X	0 1 X X						Halt*

* Symbols used only for triggering; they do not appear in the Disassembly or State displays.

Table 2–2 shows the name, bit pattern, and meaning for the symbols in the file 68020A_Intr, the Control channel group symbol table.

Table 2–2: Intr group symbol table definitions

Symbol	Intr group value	Meaning
	IPL2- IPL1- IPL0-	
-	1 1 1	No interrupt
IPL_1	1 1 0	Level 1 interrupt request
IPL_2	1 0 1	Level 2 interrupt request
IPL_3	1 0 0	Level 3 interrupt request
IPL_4	0 1 1	Level 4 interrupt request
IPL_5	0 1 0	Level 5 interrupt request
IPL_6	0 0 1	Level 6 interrupt request
IPL_7	0 0 0	Level 7 interrupt request

Information on basic operations describes how to use symbolic values for triggering and displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics:

- Acquiring data
- Viewing disassembled data in various display formats
- Changing the way data is displayed
- How to view an example of disassembled data

Acquiring Data

Once you load the 68020A support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four different display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to Changing How Data is Displayed on page 2–11.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–3 shows the special characters and strings displayed by the 68020 and 68EC020 disassembler and gives a definition of what they represent.

Table 2–3: Special characters in the display and their meaning

Character or string displayed	Meaning
#	Indicates an immediate value
>> or m	The instruction was manually marked
t	Indicates the number shown is in decimal, such as #12t
**	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Two asterisks represent a byte.
* ILLEGAL INSTRUCTION *	Decoded as an illegal instruction
A-LINE OPCODE	Displayed for an A-Line trap instruction
F-LINE OPCODE	Displayed for an F-Line trap instruction

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–4 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2-4: Cycle type definitions

Cycle type	Definition
(CPU SPACE BUS ERROR)	A CPU space bus error
(BUS ERROR RETRY)	Processor reruns a cycle
(BUS ERROR)	External logic abort of the current bus cycle
(CACHE/QUEUE HIT)	Instruction fetch from the cache or queue
(DMA READ)	Direct read from memory
(DMA WRITE)	Direct write to memory
(DMA)	Device other than the processor controls the bus
(CPU READ)	Read cycle from CPU space
(CPU WRITE)	Write cycle to CPU space
(RMW READ)	Read from memory during a read-modify-write cycle
(RMW WRITE)	Write to memory during a read-modify-write cycle
(READ)	Data read from memory
(WRITE)	Data written to memory
(RESET CYCLE)	Processor asserts RESET - signal
(UNKNOWN)	Unrecognized/unexpected combination of control bits
(BREAKPOINT n)*	Breakpoint instruction executed (breakpoint number is n)
(ACCESS READ REG: Rn)*	Read cycle accesses MMU (Rn is the MMU register)
(ACCESS WRITE REG: Rn)*	Write cycle accesses the MMU (Rn is the MMU register)
(COPROCESSOR #n READ REG: Rm)*	Read cycle accesses the coprocessor (#n is the coprocessor number, Rm is the register number)
(COPROCESSOR #n WRITE REG: Rm)*	Write cycle accesses the coprocessor (#n is the coprocessor number, Rm is the register number)
(INTERRUPT ACK LEVEL: n)*	Interrupt acknowledge
(EXTENSION)*	Fetch spans an additional cycle
(FLUSH)*	Fetch not executed due to a change in control flow

* Computed cycle types.

Figure 2–1 shows an example of the Hardware display.

	1	2	3	4	5	6
	Sample	Address	Data	Mnemonic		Timestamp
T	0	00084CE6	-----4E7A--	MOVEC-VBR, D0	(S)	
	1	00084CEA	08012440	MOVEA.L D0, A2	(S)	280 ns
	2	00084CEC	257C0008	MOVE.L #00084E08, (00A8, A2)	(S)	360 ns
	3	00084CF0	4E0800A.	(EXTENSION)	(S)	480 ns
	4	00084CF4	227C0048	MOVEA.L #00480400, A1	(S)	360 ns
	5	004000A8	00084E08	(WRITE)	(S)	400 ns
	6	00084CFA	0400o28F	MOVE.L A7, (A1)	(S)	0 ns
	7	00084CFC	48790008	PEA 00085C9A	(S)	840 ns
	8	00084D02	5C9A4879	PEA 00085CB2	(S)	360 ns
	9	00480400	004FFFE8	(WRITE)	(S)	360 ns
	10	00084D04	00085CB2	(EXTENSION)	(S)	0 ns
	11	004FFFE4	00085C9A	(WRITE)	(S)	400 ns
	12	00084D08	48790008	PEA 00085CB6	(S)	400 ns
	13	004FFFE0	00085CB2	(WRITE)	(S)	360 ns
	14	00084D0E	5CB64879	PEA 00085CC8	(S)	0 ns
	15	00084D10	00085CC8	(EXTENSION)	(S)	360 ns
	16	004FFFD8	00085CB6	(WRITE)	(S)	360 ns
	17	00084D14	48790008	PEA 00085D14	(S)	400 ns
	18	004FFFD8	00085CC8	(WRITE)	(S)	360 ns
	19	00084D1A	5D140240	ANDI.W #0000, D0	(S)	0 ns
	20	00084D1E	0000303C	MOVE.W #0001, D0	(S)	360 ns
	21	004FFFD4	00085D14	(WRITE)	(S)	360 ns

Figure 2–1: Hardware display format

- 1 **Sample Column.** Lists the memory locations for the acquired data.
- 2 **Address Group.** Lists data from channels connected to the 68020 and 68EC020 Address bus.
- 3 **Data Group.** Lists data from channels connected to the 68020 and 68EC020 Data bus.
- 4 **Mnemonic Column.** Lists the disassembled instructions and cycle types.
- 5 The disassembler displays an (S) or (U) in the mnemonic column to indicate the mode in which the microprocessor is operating, Supervisor or User.
- 6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

The Software display format also displays the following information:

- Reset cycle
- Halt cycle
- Bus Error cycle
- Special cycles: Breakpoint Ack, Int Ack, Internal Reg Access, Reset Vector
- Reads from the vector table that appear due to servicing interrupts or traps
- Illegal instructions will be displayed
- Unknown cycle types; the disassembler does not recognize the control group value

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

The Control Flow display format displays the following information:

- Reset cycle
- CPU space bus error cycle
- Bus error cycles (bus error and retry)
- Special cycles
- Emulated instructions that cause exceptions
- Reset Vector
- Reads from the vector table that appear due to servicing interrupts or traps
- Illegal instructions
- Unknown cycle types; the disassembler does not recognize the control group value

Instructions that generate a change in the flow of control in the 68020 and 68EC020 microprocessor are as follows:

BKPT	BRA	BSR
CALLM	ILLEGAL	JMP
JSR	RESET	RTD
RTE	RTM	RTR
RTS	STOP	TRAP

Instructions that might generate a change in the flow of control in the 68020 and 68EC020 microprocessor are as follows:

Bcc	FBcc	TRAPcc
DBcc (test condition, decrement, and branch)		TRAPV
CHK	CHK2	DIVS
DIVSL	DIVU	DIVUL

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

The Subroutine display format also displays the following information:

- Reset cycle
- CPU space bus error cycle
- Bus error cycles (bus error and retry)
- Special cycles
- Emulated instructions that cause exceptions
- Reset Vector
- Reads from the vector table that appear due to servicing interrupts or traps
- Illegal instructions
- Unknown cycle types; the disassembler does not recognize the control group value

Instructions that generate a subroutine call or a return in the 68020 and 68EC020 microprocessor are as follows:

BKPT	BSR	CALLM
ILLEGAL	JSR	RESET
RTD	RTE	RTM
RTR	RTS	STOP
TRAP		

Instructions that might generate a subroutine call or a return in the 68020 and 68EC020 microprocessor are as follows:

CHK	CHK2	DIVS
DIVSL	DIVU	DIVUL
TRAPcc	TRAPV	

Changing How Data is Displayed

There are fields and features that allow you to further modify displayed data to suit your needs. You can make selections unique to the 68020 and 68EC020 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Optional Display Selections

You can make optional display selections for disassembled data to help you analyze the data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify the starting address of the exception vector table.
- Specify the size of the exception vector table.

The 68020 and 68EC020 support has two additional fields: Vector Base Address, and Vector Table Size. These fields appear in the area indicated in the information on basic operations.

Vector Base Register. You can specify the starting address of the vector base register in hexadecimal. The default starting address is 0x00000000.

Vector Table Size. You can specify the size of the vector table in hexadecimal. The default size is 0x400 (the size must be divisible by 4).

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a prefetch cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)

- Flush (an opcode or extension that is fetched but not executed)
- Read (marks a memory reference read as data)

Mark selections for a 32-bit bus are as follows:

Opcode	Anything
Opcode	Opcode
Opcode	Flush
Flush	Flush
Flush	Opcode
Read	Read
Extension	Extension
Extension	Opcode
Extension	Flush

Undo Mark

Mark selections for an 8-bit or 16-bit bus are as follows:

Opcode
Extension
Read
Flush

Undo Mark

Information on basic operations contains more details on marking cycles.

Displaying Exception Vectors

The disassembler software also displays 68020 and 68EC020 exception vectors.

The disassembler initially places the exception vector table at address 00000000 (the default value). However, you can relocate the table using the Disassembly Format Definition overlay by entering the starting address in the Vector Base Register field. The Vector Base Register field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Vector Table Size field lets you specify a three-digit hexadecimal size for the table.

Interrupt cycle types are computed and cannot be used to control triggering. When the 68020 and 68EC020 microprocessor processes an interrupt, the disassembler software displays the type of interrupt, if known.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Table 2–5 lists the 68020 and 68EC020 exception vectors.

Table 2-5: Interrupt vectors

Exception number	Location in IV* table (in Hexadecimal)	Displayed interrupt name
0	0000	RESET: STACK POINTER
1	0004	RESET: PROGRAM COUNTER
2	0008	BUS ERROR VECTOR
3	000C	ADDRESS ERROR VECTOR
4	0010	ILLEGAL INSTRUCTION VECTOR
5	0014	ZERO DIVIDE VECTOR
6	0018	CHK, CHK2 VECTOR
7	001C	TRAP _{cc} , TRAPV VECTOR
8	0020	PRIV VIOLATION VECTOR
9	0024	TRACE VECTOR
10	0028	LINE 1010 EMULATOR VECTOR
11	002C	LINE 1111 EMULATOR VECTOR
12	0030	RESERVED VECTOR #12t
13	0034	COP PROT VIOLATION VECTOR
14	0038	FORMAT ERROR VECTOR
15	003C	UNINIT INTERRUPT VECTOR
16-23	0040-005C	RESERVED VECTOR #16t-23t
24	0060	SPURIOUS INTERRUPT VECTOR
25	0064	IPL 1 AUTO VECTOR
26	0068	IPL 2 AUTO VECTOR
27	006C	IPL 3 AUTO VECTOR
28	0070	IPL 4 AUTO VECTOR
29	0074	IPL 5 AUTO VECTOR
30	0078	IPL 6 AUTO VECTOR
31	007C	IPL 7 AUTO VECTOR
32-47	0080-00BC	TRAP #0-15 VECTOR
48	00C0	FPCP UNORDERED COND VECTOR
49	00C4	FPCP INEXACT RESULT VECTOR
50	00C8	FPCP ZERO DIVIDE VECTOR
51	00CC	FPCP UNDERFLOW VECTOR
52	00D0	FPCP OPERAND ERROR VECTOR
53	00D4	FPCP OVERFLOW VECTOR
54	00D8	FPCP SIGNALING NAN VECTOR
55	00DC	RESERVED VECTOR #55t
56	00E0	PMMU CONFIGURATION VECTOR

Table 2-5: Interrupt vectors (cont.)

Exception number	Location in IV* table (in Hexadecimal)	Displayed interrupt name
57	00E4	PMMU ILLEGAL OP VECTOR
58	00E8	PMMU ACCESS LEVEL VECTOR
59-63	00EC-00FC	RESERVED VECTOR #59t-63t
64-255	0100-03FC	USER INT VECTOR #64t-255t

* IV means interrupt vector.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your 68020 and 68EC020 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.



Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Channel assignment tables
- How the data is acquired
- Alternate Microprocessor Connections

Probe Adapter Description

The probe adapter is a nonintrusive piece of hardware that allows the logic analyzer to acquire data from a 68020 and 68EC020 microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a 68020 and 68EC020 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

The 68020 PGA probe adapter accommodates the Motorola 68020 microprocessor in a 114-pin PGA package.

The 68EC020 PGA probe adapter accommodates the Motorola 68020 microprocessor in a 100-pin PGA package.

The 68020 CQFP probe adapter accommodates the Motorola 68020 microprocessor in a 132-pin CQFP package.

Configuring the Probe Adapter

Disabling the cache makes all instruction prefetches visible on the bus so that they can be acquired and disassembled. The probe adapter contains a jumper you can use to disable the 68020 cache.

With the cache jumper in the NORM position, the SUT controls the cache and the CDIS~ signal is not affected.

With the cache jumper in the DIS position, the CDIS~ signal connects to a 332 Ω pull-down resistor on the probe adapter which disables the cache. For the PGA probe adapters, you should also cut or remove pin T5 from the protective socket on the underside of the probe adapter to prevent contention with the driving signal. For a CQFP probe adapter, you should disable any devices on the SUT that drive the CDIS~ signal to prevent contention with the driving signal.

Table 3–1 shows the jumper positions.

Table 3–1: Jumper positions

Cache jumper	Probe adapter	Positions
J210	68020 PGA	1–2 (NORM) 2–3 (DIS)
J210	68EC020 PGA	1–2 (NORM) 2–3 (DIS)
J1150	68020 CQFP	1–2 (NORM) 2–3 (DIS)

Figure 3–1 shows the location of J210 on the 68020 PGA probe adapter.

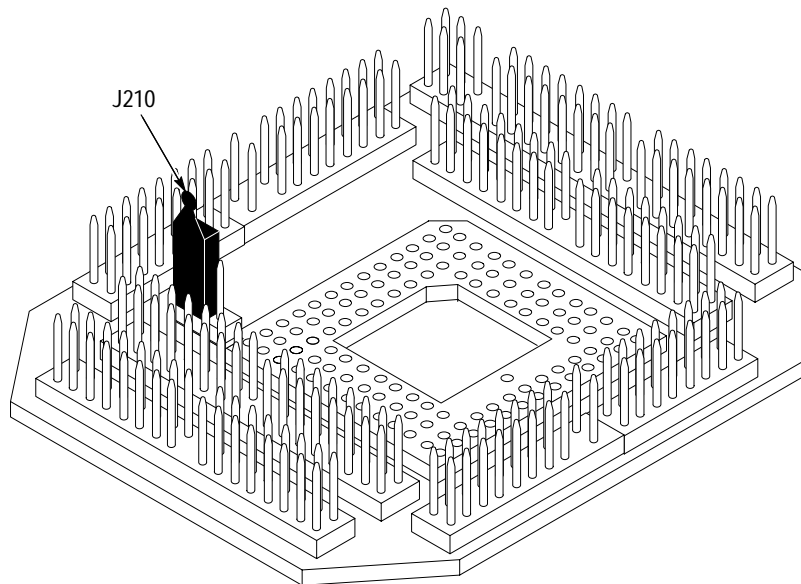


Figure 3–1: Jumper location on the 68020 PGA probe adapter

Figure 3–2 shows the location of J210 on the 68EC020 PGA probe adapter.

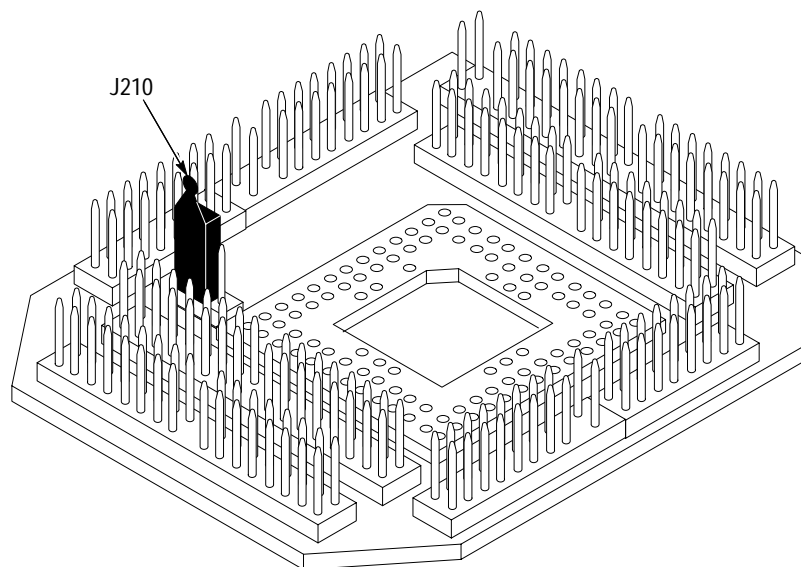


Figure 3–2: Jumper location on the 68EC020 PGA probe adapter

Figure 3–3 shows the location of J1150 on the 68020 CQFP probe adapter.

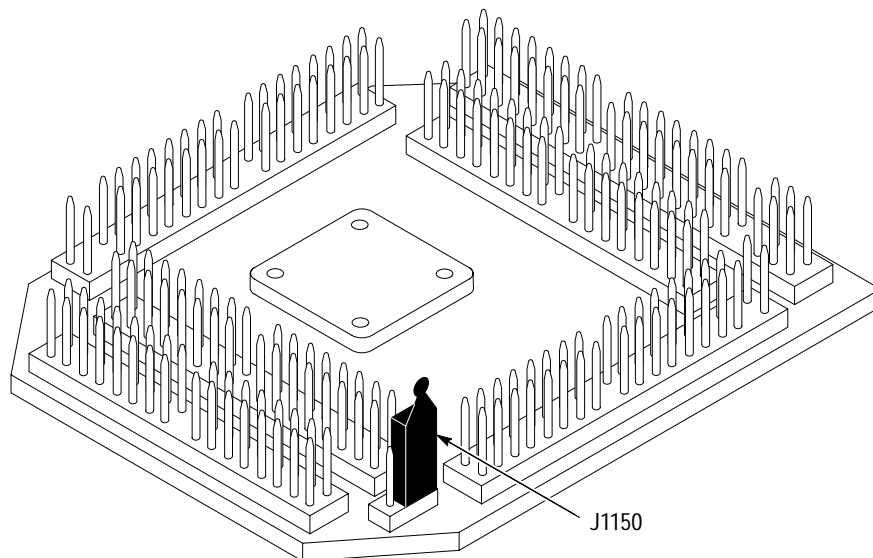


Figure 3–3: Jumper location on the 68020 CQFP probe adapter

Specifications

These specifications are for a probe adapter connected to a compatible Tektronix logic analyzer, and the SUT. Table 3–2 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–2, for the 102/136-channel module, one podlet load is 20 k Ω in parallel with 2 pF. For the 96-channel module, one podlet load is 100 k Ω in parallel with 10 pF.

Table 3–2: Electrical specifications

Characteristics	Requirements	
SUT DC Power Requirements		
Voltage	4.75-5.25 VDC	
Current	I max (calculated)	87 mA
	I typ (measured)	56 mA
SUT Clock		
Clock Rate	Min.	8 MHz
	Max.	33 MHz (25 MHz for the 68EC020)
Minimum Setup Time Required		68020 @33 MHz
Address	4 ns	9 ns
Data	4 ns	5 ns
AS~	4 ns	15 ns
All Other Signals	4 ns	---
Minimum Setup Time Required		680EC20 @25 MHz
Address	5 ns	5 ns
All Other Signals	5 ns	---
Minimum Hold Time Required		68020 @33 MHz
Address, Data, AS~	3 ns	0 ns
All Other Signals	3 ns	---
Minimum Hold Time Required		68EC020 @25 MHz
Data	0 ns	0 ns
All Other Signals	0 ns	---
	Specification	
	AC Load	DC Load
Measured Typical SUT Signal Loading		
Address	4 pF + podlet	(1) podlet
Data	4 pF + podlet	(1) podlet
CLK	7 pF	(1) 74AS1004 (68020)

Table 3–2: Electrical specifications (cont.)

Characteristics	Requirements	
CLK	6 pF + 2 podlets	(2) podlets only (68EC020)
ECS-, OCS-	12 pF + podlet	(1) 745074 parallel with podlet (68020 only)
RESET	15 pF + podlet	(2) 745074 parallel with podlet (68020)
RESET	6 pF + podlet	(1) podlet only (68EC020)
Other Signals	6 pF + podlet	(1) podlet

Table 3–3 shows the environmental specifications.

Table 3–3: Environmental specification

Characteristic	Description
Temperature	
Maximum Operating	+50° C (+122° F)*
Minimum Operating	0° C (+32° F)
Non-Operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity†
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-Operating	15 km (50,000 ft) maximum
Electrostatic Immunity	The probe adapter is static sensitive

* Not to exceed 68020 and 68EC020 thermal considerations. Forced air cooling may be required across the CPU.

† Designed to meet Tektronix standard 062-2847-00 class 5.

Table 3–4 shows the certifications and compliances that apply to the probe adapter.

Table 3–4: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.
Pollution Degree 2	Do not operate in environments where conductive pollutants might be present.

Figures 3-4, 3-5, and 3-6 show the dimensions of the probe adapter with the podlet holders attached. Figure 3-4 shows the 68020 PGA probe adapter.

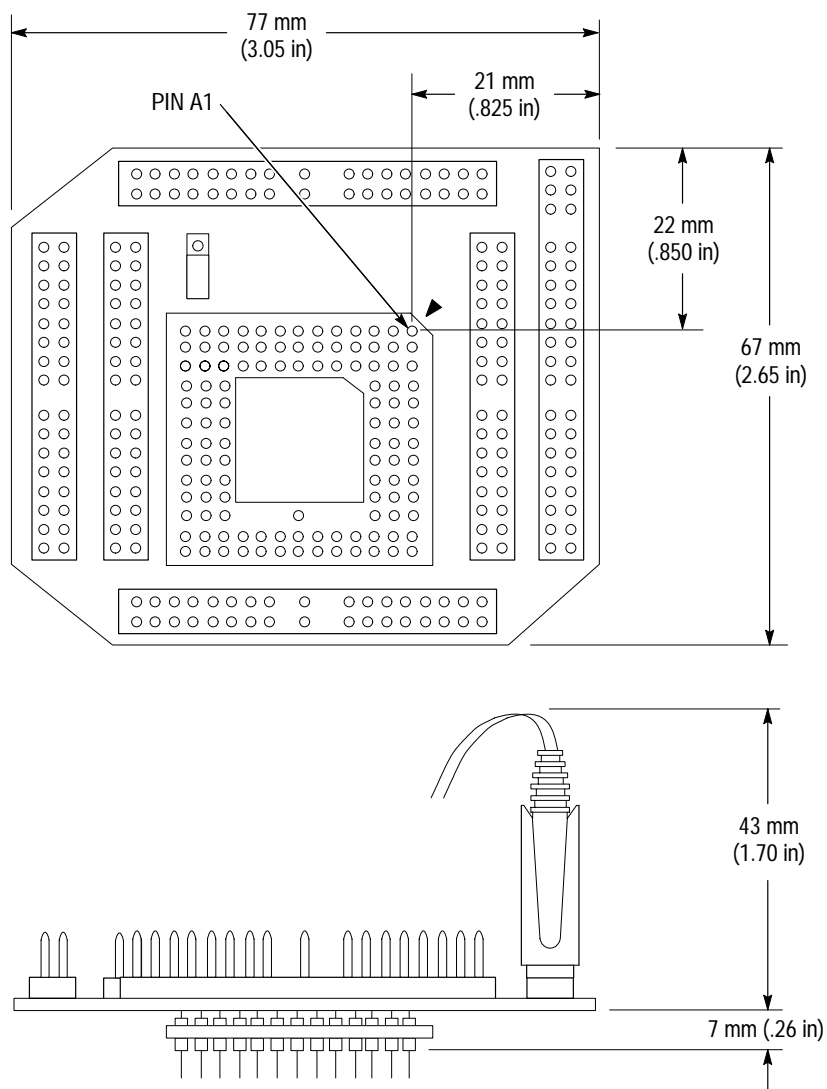


Figure 3-4: Minimum clearance of the 68020 PGA probe adapter

Figure 3-5 shows the 68EC020 PGA probe adapter

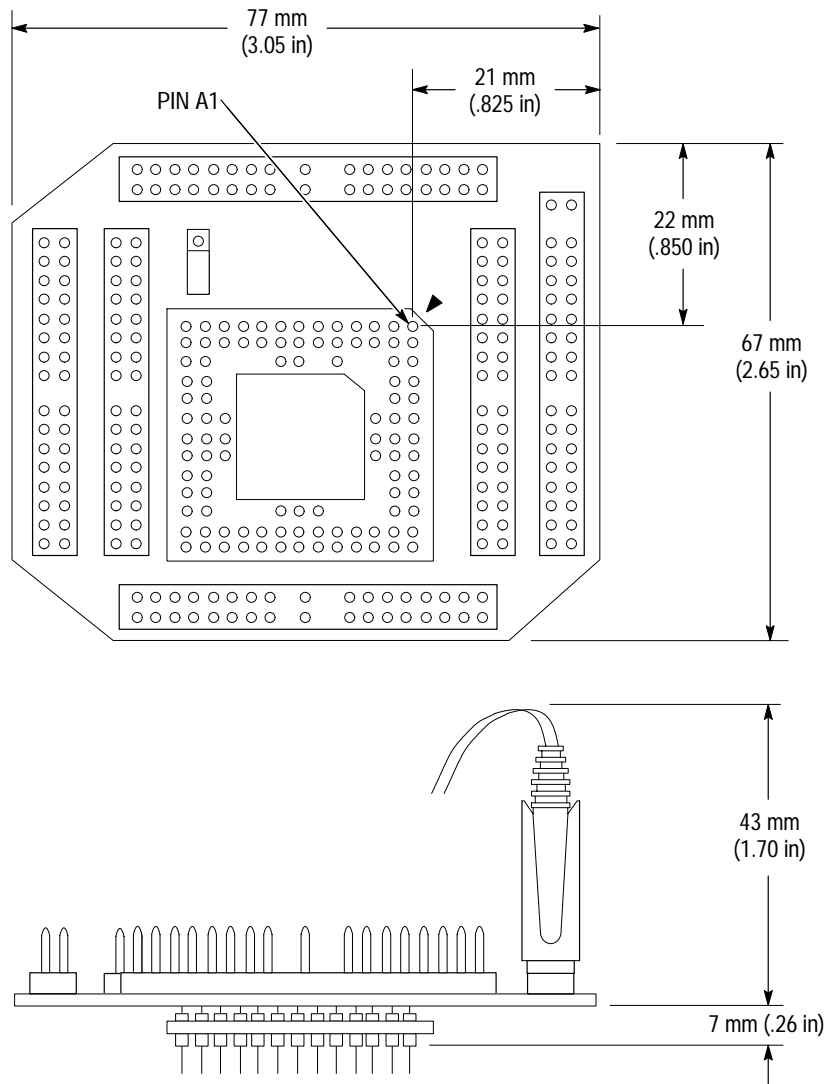


Figure 3-5: Minimum clearance of the 68EC020 PGA probe adapter

Figure 3–6 shows the 68020 CQFP probe adapter

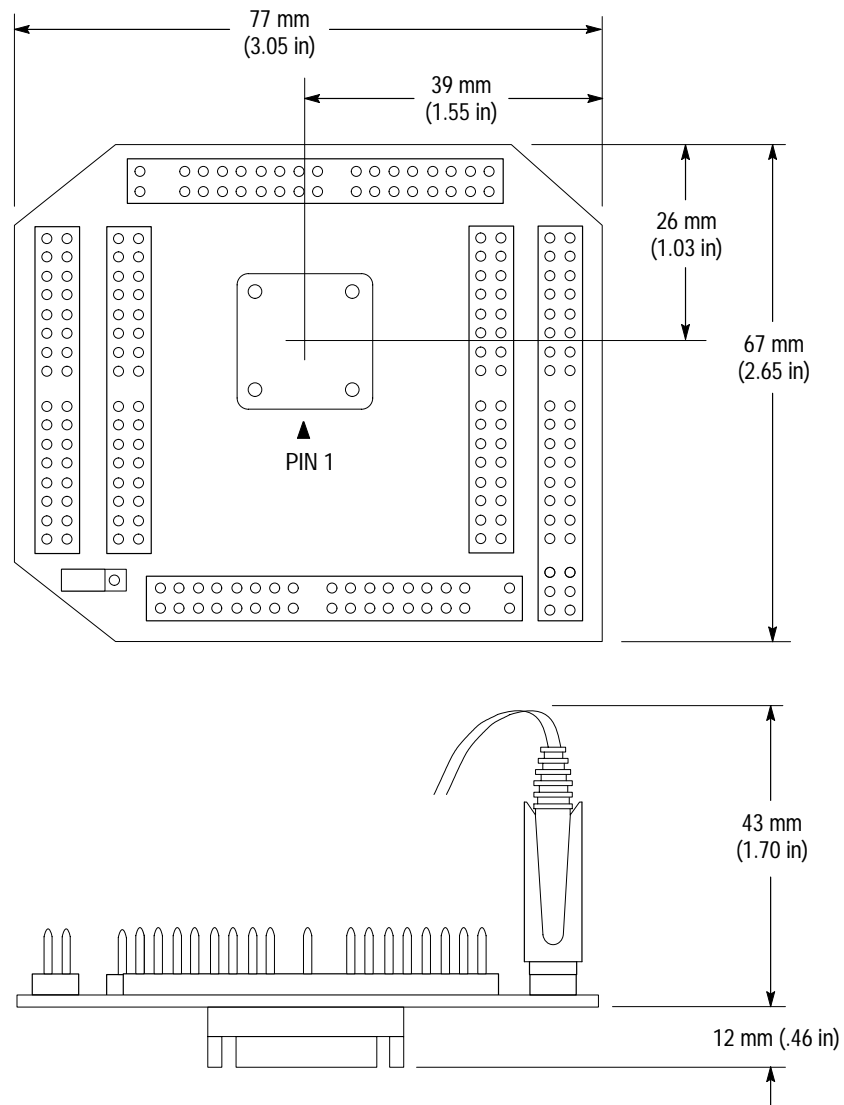


Figure 3–6: Minimum clearance of the 68020 CQFP probe adapter

Channel Assignments

Channel assignments shown in Table 3–5 through Table 3–15 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

Table 3–5 shows the probe section and channel assignments for the Address group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-5: Address group channel assignments (68020)

Bit order	Channel	68020 signal name
31	A3:7	A31
30	A3:6	A30
29	A3:5	A29
28	A3:4	A28
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–6 shows the probe section and channel assignments for the Address group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–6: Address group channel assignments (68EC020)

Bit Order	Channel	68EC020 signal name
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–7 shows the probe section and channel assignments for the Data group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–7: Data group channel assignments (68020 & 68EC020)

Bit order	Channel	68020 and 68EC020 signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–8 shows the probe section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–8: Control group channel assignments (68020)

Bit order	Channel	68020 signal name
11	C2:0*	BGACK~
10	C2:7	FC2
9	C3:0	FC1
8	C2:6	FC0
7	C2:5	RMC~
6	C2:3*	AS~
5	C2:1*	RESET~ [†]
4	C3:7	R/W~
3	C3:6	HALT~
2	C3:5	BERR~
1	C3:2	SIZ1
0	C3:1	SIZ0

* Denotes a qualifier channel.

[†] Signal not required for disassembly.

Table 3–9 shows the probe section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–9: Control group channel assignments (68EC020)

Bit order	Channel	68EC020 signal name
11	C2:0*	BG~
10	C2:7	FC2
9	C3:0	FC1
8	C2:6	FC0
7	C2:5	RMC~
6	C2:3*	AS~
5	C2:1*	RESET~ [†]
4	C3:7	R/W~
3	C3:6	HALT~

Table 3–9: Control group channel assignments (68EC020) (cont.)

Bit order	Channel	68EC020 signal name
2	C3:5	BERR~
1	C3:2	SIZ1
0	C3:1	SIZ0

* Denotes a qualifier channel.

† Signal not required for disassembly.

Table 3–10 shows the probe section and channel assignments for the Intr group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–10: Intr group channel assignments

Bit order	Section:channel	68020 and 68EC020 signal name
2	C0:2	IPL2~
1	C0:0	IPL1~
0	C0:1	IPL0~

Table 3–11 shows the probe section and channel assignments for the DataSize group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–11: DataSize group channel assignments (68020) & (68EC020)

Bit order	Channel	68020 and 68EC020 signal name
1	C3:4	DSACK1~
0	C3:3	DSACK0~

Table 3–12 shows the probe section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–12: Misc group channel assignments (68020) and (68EC020)

Bit order	Channel	68020 and 68EC020 signal name
1	C2:2	ECS_L~ ^{†*}
0	C2:4	CLK= [†]

[†] Signal not required for disassembly.

= Signal is double probed.

* Denotes a qualifier channel.

Table 3–13 shows the probe section and channel assignments for the Misc2 group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible (off).

Table 3–13: Misc2 group channel assignments

Bit order	Section:channel	68020 and 68EC020 signal name
7	C0:4	OSC_L~
6	C1:3	DBEN~
5	C0:3	IPEND~
4	C1:2	AVEC~
3	C0:6	BR~
2	C0:5	BG~
1	C1:0	DS~
0	C1:1	CDIS~

Table 3–14 shows the probe section and channel assignments for the clock channels (not part of any group), and the microprocessor signal to which each channel connects. These channels are used only to clock in data; they are not acquired or displayed.

Table 3–14: Clock channel assignments (68020)

Channel	68020 signal name
CK:0	Not connected
CK:1	Not connected
CK:2	CLK~ (buffered, inverted)
CK:3	Not connected

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–14, you must connect another channel probe to the signal, a technique called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

Table 3–15 shows the probe section and channel assignments for the clock channels (not part of any group), and the microprocessor signal to which each channel connects. These channels are used only to clock in data; they are not acquired or displayed.

Table 3–15: Clock channel assignments (68EC020)

Channel	68EC020 signal name
CK:0	Not connected
CK:1	Not connected
CK:2	CLK (labeled CLK_B~)
CK:3	Not connected

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–15, you must connect another channel probe to the signal, a technique called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This part of this chapter explains how the module acquires 68020 and 68EC020 signals using the TMS 202 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

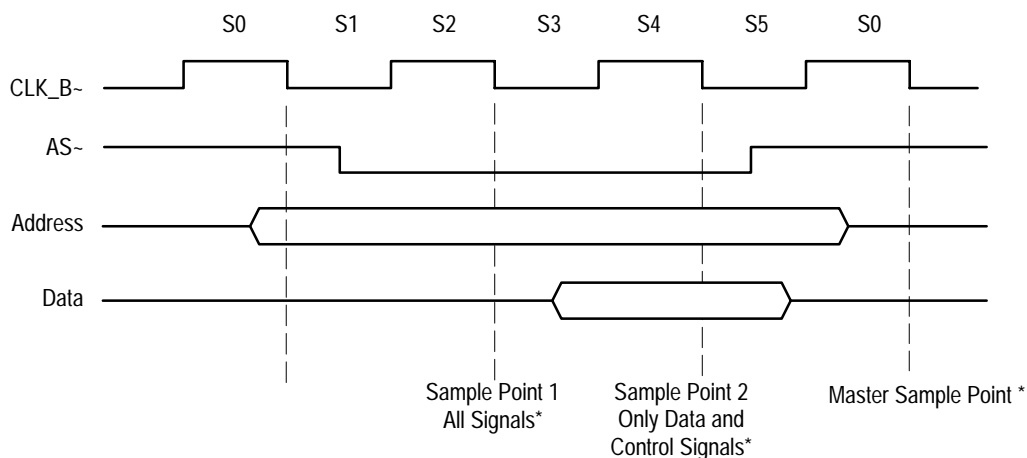
Custom Clocking

A special clocking program is loaded to the module every time you load the 68020 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the 68020 and 68EC020 bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–7 shows the sample points and the master sample point.



* Address and Control signals are logged in from the previous falling edge of AS-, including the Master Sample Point. Data is logged in from the indicated falling edge of AS-.

Figure 3–7: 68020 and 68EC020 bus timing

Clocking Options

The clocking algorithm for the 68020 and 68EC020 support has several variations: Probe Adapter Type, DMA Cycles, and Cache and Queue Hits.

68020A PGA or 68020A CQFP. Choose if you are using a 68020 PGA or CQFP probe adapter.

EC020. Choose if you are using a 68EC020 PGA probe adapter.

DMA Cycles Excluded. DMA bus cycles are ignored and not logged in.

DMA Cycles Included. All bus cycles, including DMA bus cycles, are logged in.

The TMS 202 uses three sample points for logging and clocking 68020 data into the logic analyzer. The first sample point is at the beginning of the cycle, where the address bus and latched ECS $\bar{~}$ and OCS $\bar{~}$ control signals are logged in. The second sample point occurs at the end of the cycle, where the data bus and control signals are logged in. The third sample point occurs when the bus cycle is completed; all of the signals are sent to the trigger state machine and the acquisition memory as a master sample (one complete data acquisition record).

The 68EC020 cannot detect cache/queue hits because it does not have an ECS $\bar{~}$ signal. Clocking for the 68EC020 is similar to that for the 68020 but relies mostly upon sensing the status of AS $\bar{~}$. When AS $\bar{~}$ is first sensed as asserted, all address, data, and control signals are logged in. Data and some control signals continue to be logged repetitively in every CLK cycle until AS $\bar{~}$ is negated, at which time all of the previously logged data is stored as a bus cycle by a Master Clock from the clocking state machine.

For the 68EC020 in SUTs having DMA cycles, some bus cycles may be acquired with both DSACK1 $\bar{~}$ and DSACK0 $\bar{~}$ appearing inactive, even though they may actually be asserted. This can occur whether or not DMA cycles are selected as included.

Cache & Queue Hits Excluded. Cache and queue hits are ignored and not logged in.

Cache & Queue Hits Included. All visible cache and queue hit cycles are acquired. (This works for the 68020 only since the 68EC020 does not have an ECS $\bar{~}$ signal). The data bus is undefined for cache hits.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–10.

Signals On the Probe Adapter

All 68020 and 68EC020 microprocessor signals are accessible on the probe adapter.

Extra Channels

Table 3–16 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Channels that are not defined in a channel group by the TMS 202 software are logged in with the Master sample point.

Table 3–16: Extra module sections and channels

Module	Section: channels
102-channels	C1:7-0, C0:7-0, Qual:1, Qual:0
136-channels	C1:7-0, C0:7-0, E3:7-0, E2:7-0, E1:7-0, E0:7-0, Qual:3-0
96-channels	C1:7-0, C0:7-0

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.



Maintenance

Maintenance

This section contains information on the following topics:

- Probe adapter circuit description
- How to replace a signal lead
- How to replace a protective socket

Probe Adapter Circuit Description

On the probe adapters, the CLK is buffered by the fastest available buffer that is inverting. The clocking compensates easily by using the rising edge. CLK= (CLK as data) is not inverted, but is buffered to provide hold time for accurate acquisition. The unlatched versions of ECS~ and OCS~ are available for timing analysis at J140.

The 68EC020 probe adapter has no active circuitry. Since there are not ECS~ or OCS~ signals on the 68EC020, no circuitry is required. Cache hit cycles are not discernable, and the 68EC020 probe adapter does not acquire them.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.



Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 202 68020 and 68EC020 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2058	TDK CORPORATION OF AMERICA	1600 FEEHANVILLE DRIVE	MOUNT PROSPECT, IL 60056
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPY PO BOX 655303	DALLAS TX 75262-5303
1CH66	PHILIPS SEMICONDUCTORS	811 E ARQUES AVENUE PO BOX 3409	SUNNYVALE CA 94088-3409
50139	ALLEN-BRADLEY CO ELECTRONIC COMPONENTS	1414 ALLEN BRADLEY DR	EL PASO TX 79936
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769-2963
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discontinued	Name & description	Mfr. code	Mfr. part number
A01	671-2334-00			CIRCUIT BD ASSY:68020 PROBE ADAPTER(LASI III);	80009	671233400
A02	671-2335-00			CIRCUIT BD ASSY:68EC020,PROBE ADAPTER(LASIII);	80009	671233500
A03	671-2538-00			CIRCUIT BD ASSY:CQFP132,SOLDERED,PROBE ADAPTER;	80009	671253800
A01	671-2334-00			CIRCUIT BD ASSY:68020 PROBE ADAPTER(LASI III);	80009	671233400
A01C100	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A01C220	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A01C230	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A01C320	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A01C420	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A01C500	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A01C540	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A01J100	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE REPL FIG.1)		
A01J101	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01J120	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01J130	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01J140	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01J300	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01J301	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01J340	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01J341	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01J510	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01J520	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01J540	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01J541	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A01R220	321-5012-00			RES,FXD:THICK FILM;332 OHM,1%,0.125W,TC=100	50139	BCK3320FT

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01U230	156-5178-00			IC,DIGITAL:ASTTL,GATE;HEX INV DRIVER	01295	SN74AS1004AD
A01U231	-----			SOCKET,PGA::PCB,;114 POS,13 X 13,0.1 CTR,0.170 H X 0.275 TAIL,OPEN CTR,NON SYMMETRICAL ,PAT 1337 (SEE RMPL FIG.1)		
A01U4320	156-5908-00			IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE, METASTABLE IMMUNITY	1CH66	N74F5074D
A01U420	156-5908-00			IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE, METASTABLE IMMUNITY	1CH66	N74F5074D
A02	671-2335-00			CIRCUIT BD ASSY:68EC020,PROBE ADAPTER(LASIII);	80009	671233500
A02C100	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A02C230	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A02C320	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A02C420	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A02C500	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A02C540	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A02J100	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J101	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J120	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J130	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J140	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J210	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J300	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J301	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J340	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J341	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J510	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J520	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A02J540	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A02J541				(SEE RMPL FIG.2)		
A02R220	321-5012-00			RES,FXD:THICK FILM;332 OHM,1%,0.125W,TC=100	50139	BCK3320FT
A02R225	321-5012-00			RES,FXD:THICK FILM;332 OHM,1%,0.125W,TC=100	50139	BCK3320FT
A02U231	-----			SOCKET,PGA:PCB,;100 POS,13 X 13,0.1 CTR,0.1 73 H X 0.273 L 0.02 DIA TAIL,OPEN CTR,PAT 1 3F4F,MODIFIED 13B5,GOLD/GOLD (SEE RMPL FIG.2)		
A03	671-2538-00			CIRCUIT BD ASSY:CQFP132,SOLDERED,PROBE ADAPTER;	80009	671253800
A03C1220	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A03C1221	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A03C1222	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A03C1228	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A03C1231	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A03C1500	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A03C1550	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A03J1110	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03J1120	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03J1130	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03J1150	-----			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION (SEE RMPL FIG.3)		
A03J1200	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03J1201	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03J1240	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03J1241	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03J1300	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03J1301	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03J1340	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A03J1341	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03J1510	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03J1521	-----			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.3)		
A03R1230	321-5012-00			RES,FXD:THICK FILM;332 OHM,1%,0.125W,TC=100	50139	BCK3320FT
A03U1225	156-5908-00			IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE, META STABLE IMMUNITY	1CH66	N74F5074D
A03U1230	156-5178-00			IC,DIGITAL:ASTTL,GATE;HEX INV DRIVER	01295	SN74AS1004AD
A03U1230	156-5908-00			IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE, META STABLE IMMUNITY	1CH66	N74F5074D



Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 202 68020 and 68EC020 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1-1972.

Chassis Parts Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656-4548
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769-2963
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1-0	010-0529-00			1	PROBE ADAPTER:68020,PGA114 SOCKETED;	80009	010052900
-1	131-4530-00			1	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230MLG X 0.120 TAIL,30GOLD,BD RETENTION (J210)	00779	104344-1
-2	131-4356-00			1	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER (P210)	26742	9618-302-50
-3	131-5267-00			2	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J100,J101,J120,J130,J140,J300,J301,J340,J341,J510,J520,J540,J541)	53387	2480-6122-TB
-4	671-2334-00			1	CIRCUIT BD ASSY:68020 PROBE ADAPTER(LASI III);	80009	671233400
-5	136-0942-00			2	SOCKET,PGA::PCB,;114 POS,13 X 13,0.1 CTR,0.170 H X 0.275 TAIL,OPEN CTR,NON SYMMETRICAL,PAT 1337 (U231)	63058	PGA 114H115B1-1
STANDARD ACCESSORIES							
	070-9820-00			1	MANUAL, TECH:INSTRUCTION,68020	80009	070-9820-00
	070-9803-00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070-9803-00

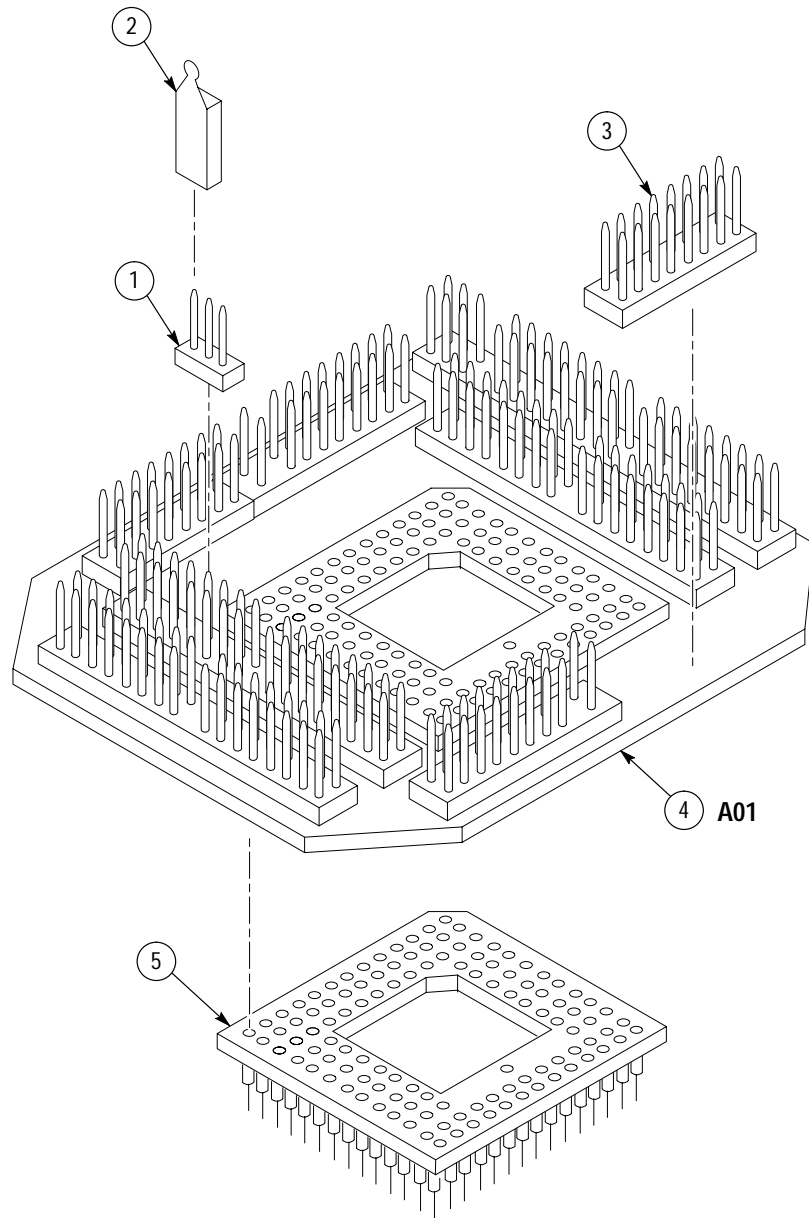


Figure 7: 68020 PGA Probe Adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2-0	010-0530-00			1	PROBE ADAPTER:68EC020,SUB PGA100 SOCKETED;	80009	010053000
-1	131-4530-00			1	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230MLG X 0.120 TAIL,30GOLD,BD RETENTION (J210)	00779	104344-1
-2	131-4356-00			1	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER (P210)	26742	9618-302-50
-3	131-5267-00			2	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J100,J101,J120,J130,J140,J300,J301,J340,J341,J510,J520,J540,J541)	53387	2480-6122-TB
-4	671-2335-00			1	CIRCUIT BD ASSY:68EC020,PROBE ADAPTER(LASIII);	80009	671233500
-5	136-1168-00			2	SOCKET,PGA:PCB,;100 POS,13 X 13,0.1 CTR,0.173 H X 0.273 L 0.02 DIA TAIL,OPEN CTR,PAT 13F4F,MODIFIED 13B5, GOLD/GOLD (U2310)	63058	PGA100H115B1-13
STANDARD ACCESSORIES							
	070-9820-00			1	MANUAL,TECH:INSTRUCTION,68020	80009	070-9820-00

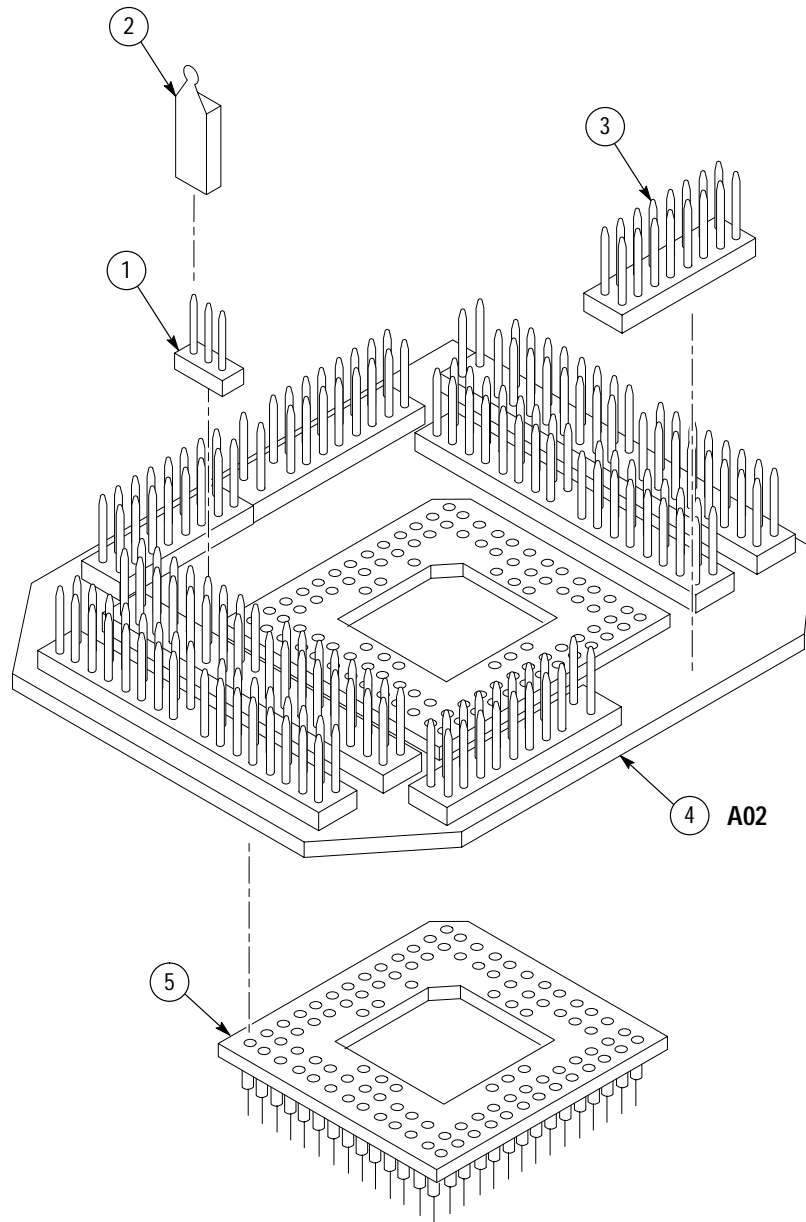


Figure 8: 680EC20 PGA Probe Adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
3-1	131-4530-00			1	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230MLG X 0.120 TAIL,30GOLD,BD RETENTION (J1150)	00779	104344-1
-2	131-4356-00			1	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR, 0.63 H,BLK,W/HANDLE,JUMPER (P1150)	26742	9618-302-50
-3	131-5267-00			3	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J1110,J1120,J1130,J1200,J1201,J1240,J1241,J1300,J1301, J1340,J1341,J1510,J1520)	53387	2480-6122-TB
-4	671-2538-00			1	CIRCUIT BD ASSY:CQFP132,SOLDERED,PROBE ADAPTER;	80009	671253800
STANDARD ACCESSORIES							
	070-9820-00			1	MANUAL,TECH:INSTRUCTION,68020	80009	070982000

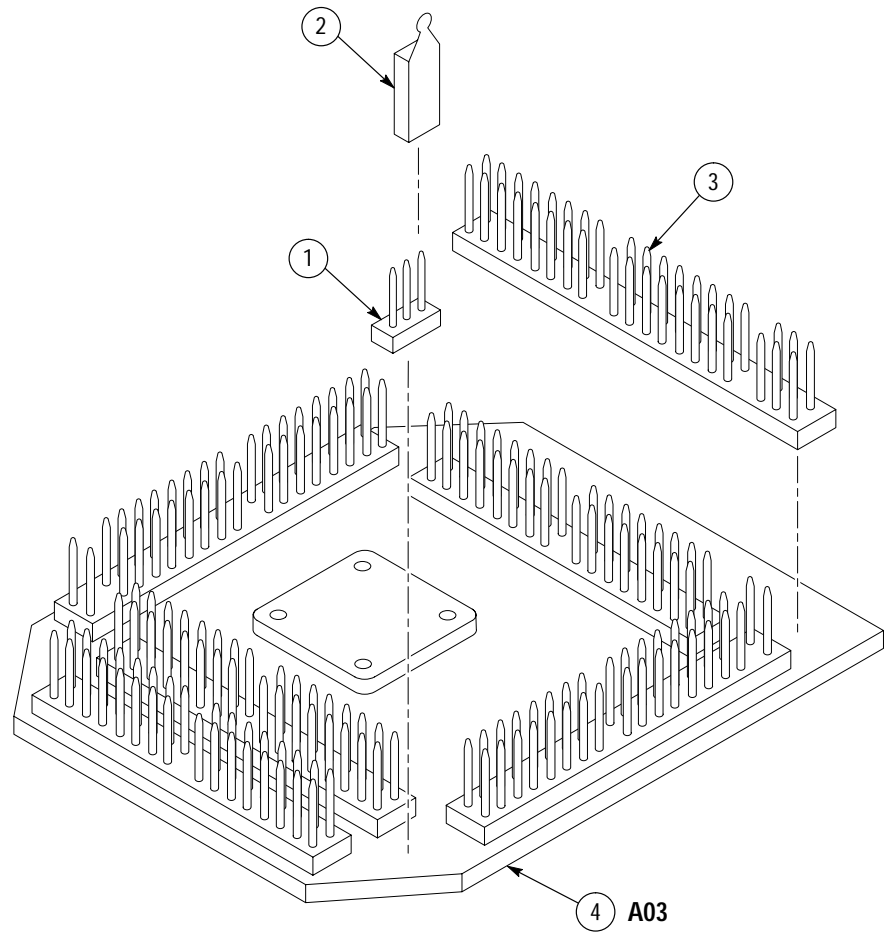


Figure 9: 68020 CQFP Probe Adapter exploded view



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