

Instruction Manual



TMS 702

TMS320C3X Digital Signal Processor Support

070-9831-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning

The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:



WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*



CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:



WARNING
High Voltage



Protective Ground
(Earth) Terminal



CAUTION
Refer to Manual



Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Digital Signal Processor Support Documentation

This instruction manual contains specific information about the TMS 702 TMS320C3X digital signal processor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating digital signal processor support packages on the logic analyzer for which the TMS 702 TMS320C3X support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating digital signal processor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of digital signal processor support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of digital signal processor supports user manual.
- The term SUT (System Under Test) refers to the digital signal processor-based system from which data will be acquired.
- The term Processor refers to the TMS320C3X digital signal processor.

- In the information on basic operations, the term XXX or P54C used in field selections and file names must be replaced with processor. This is the name of the digital signal processor in field selections and file names you must use to operate the TMS320C3X support.
- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 102/136-channel or a 96-channel module.
- processor refers to all supported variations of the TMS320C3X digital signal processor unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

This chapter provides information on the following topics and tasks:

- A description of the TMS 702 digital signal processor support package
- Logic analyzer software compatibility
- Your System Under Test (SUT) requirements
- Support restrictions
- How to configure your probe adapter
- How to connect to your SUT

Support Description

The TMS 702 digital signal processor support package disassembles data from systems that are based on the Texas Instruments TMS320C3X digital signal processor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 702 digital signal processor support.

Table 1–1 shows the digital signal processors and packages from which the TMS 702 support can acquire and disassemble data.

Table 1–1: Supported digital signal processors

Name	Package
TMS320C30	181-Pin PGA
TMS320C31	132-Pin PQFP

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations, as well as the *TMS320C3X User's Guide*, Texas Instruments Digital Signal Processing Products, June 1991.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the digital signal processor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the TMS 702 support, the Tektronix logic analyzer must be equipped with either a 102/136-channel module or a 96-channel module at a minimum. The module must be equipped with enough probes to acquire channel and clock data from signals in your TMS320C3X-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of digital signal processor supports in the information on basic operations as they pertain to your SUT.

You should review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your SUT, as well as the following descriptions of other TMS320C3X support requirements and restrictions.

System Clock Rate¹. The TMS 702 support can acquire data from the TMS320C30 at speeds of up to 40 MHz, and the TMS320C31 at speeds of up to 33 MHz.

¹ Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.

Configuring the Probe Adapter

There is one jumper on the probe adapter used to configure the probe adapter for disassembler analysis or timing analysis.

The Disassembly and Timing jumper (J120 on the PGA probe adapter, J520 on the PQFP probe adapter) should be placed in the D position to acquire disassembled data, and in the T position to acquire timing data. Table 1–2 shows how to position this jumper depending on the type of clocking you’re using and the type of window you want to view.

Table 1–2: Disassembly and Timing jumper information

Jumper position	Clocking	Data window
D (Disassembly)	Custom	Listing window, Disassembly, State, or Graph displays
T (Timing)	Internal	Waveform window, or Timing display

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the processor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. The probes will look different if you are using a 96-channel module.

The general requirements and restrictions of digital signal processor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PGA Probe Adapter

To connect the logic analyzer to a SUT using a PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.



CAUTION. *Static discharge can damage the processor the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the processor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–1. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the processor from your SUT.
5. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the processor.

6. Place the processor into the probe adapter as shown in Figure 1–1.

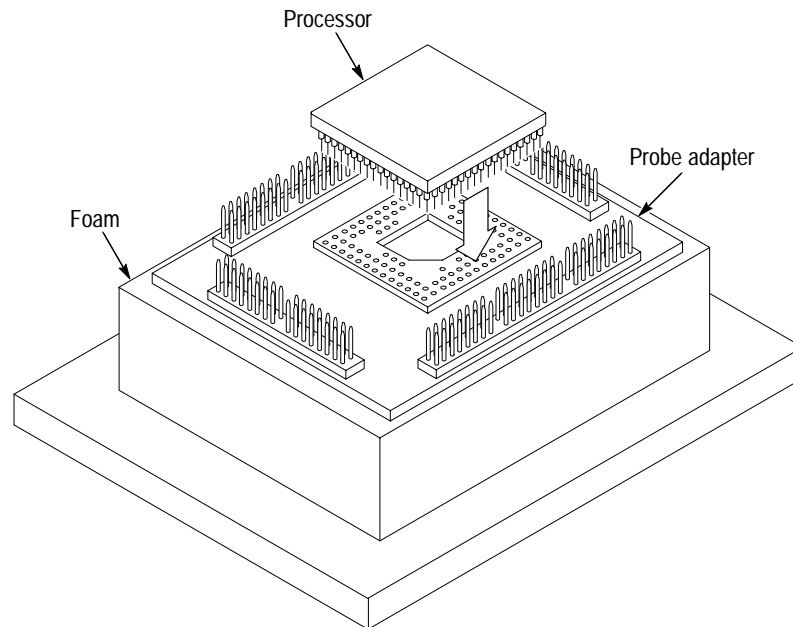


Figure 1–1: Placing the processor into a PGA probe adapter



CAUTION. Failure to correctly place the processor into the probe adapter may permanently damage the processor once power is applied.

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–2. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

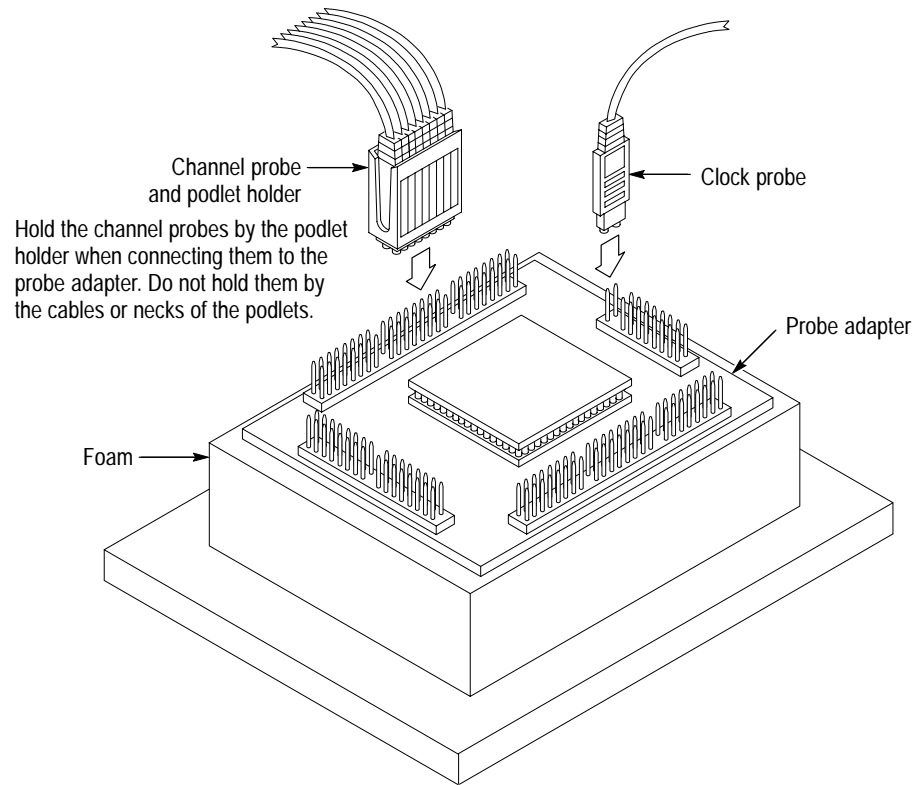


Figure 1–2: Connecting probes to a PGA probe adapter

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.
9. Place the probe adapter onto the SUT as shown in Figure 1–3.

NOTE. You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.

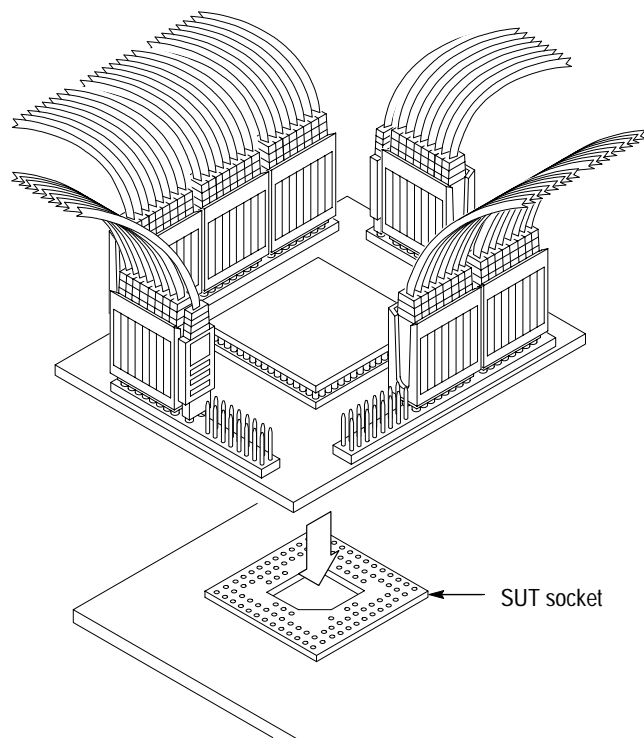


Figure 1-3: Placing a PGA probe adapter onto the SUT

PQFP Probe Adapter

To connect the logic analyzer to a SUT using a PQFP probe adapter, follow these steps:

NOTE. The PQFP probe adapter connects to the primary bus only. There are no connections to the expansion bus.

10. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.



CAUTION. Static discharge can damage the processor, the probe adapter, the probes, or the module. To prevent static damage, handle all the above only in a static-free environment.

Always wear a grounding wrist strap or similar device while handling the processor and probe adapter.

11. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.

12. Place the probe adapter onto the antistatic shipping foam to support the probe as shown Figure 1–4. This prevents the circuit board from flexing.
13. Connect the channel and clock probes to the probe adapter as shown in Figure 1–4. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

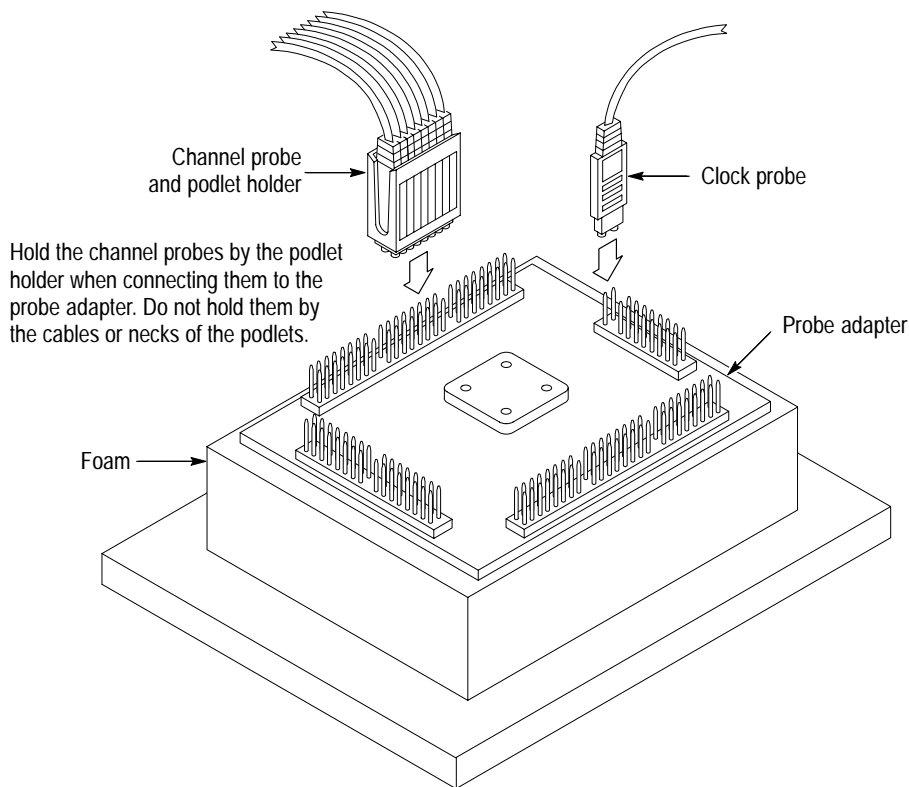


Figure 1–4: Connecting probes to a PQFP probe adapter



CAUTION. This JEDEC PQFP (Plastic Quad Flat Pack) probe adapter has been equipped with a clip that has been designed for tight tolerances.

The clip supports only Plastic Quad Flat Pack devices that conform to the JEDEC M0-069 October 1990 specification. Attaching the clip to a device that does not conform to this JEDEC standard can easily damage the clip's connection pins and/or the processor, causing the probe adapter to malfunction.

Please contact your IC manufacturer to verify that the processor you are targeting conforms to the JEDEC specification.

For best performance and long probe life, exercise extreme care when connecting the probe to the processor.

14. Line up the pin 1 indicator on the processor with the pin 1 indicator on the target head of the circuit board.



CAUTION. Failure to correctly place the probe adapter onto the processor might permanently damage all electrical components when power is applied.

Center the clip on the processor and apply an equal downward force on all four sides of the clip, slightly rocking the probe adapter in a clockwise circle.

Do not apply leverage to the probe adapter when installing or removing it.

15. Place the probe adapter onto the SUT as shown in Figure 1–5.

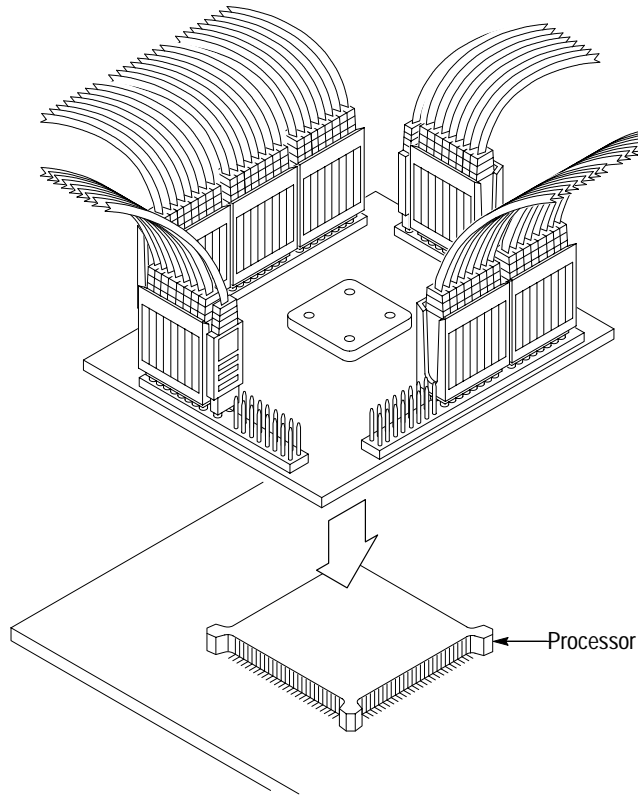


Figure 1–5: Placing a PQFP probe adapter onto the SUT



CAUTION. The probe adapter board might slip off or slip to one side of the processor because of the extra weight of the probes. This can damage the processor and the SUT. To prevent this from occurring, stabilize the probe adapter by placing a non-conductive object (such as foam) between the probe adapter and the SUT.

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to processor signals in the SUT using a test clip, follow these steps:

16. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.



CAUTION. Static discharge can damage the processor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.

Always wear a grounding wrist strap or similar device while handling the processor.

17. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.



CAUTION. Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the processor.

18. Place the SUT on a horizontal static-free surface.
19. Use Table 1–3 to connect the channel probes to processor signal pins on the test clip or in the SUT.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Table 1–3 lists the primary bus signal connections for the channel probes.

Table 1–3: TMS320C3X Primary bus signal connections for channel probes

Section:channel	TMS320C3X signal	Section:channel	TMS320C3X signal
A3:7	INT3~ *	D3:7	D31
A3:6	INT2~ *	D3:6	D30
A3:5	INT1~ *	D3:5	D29
A3:4	INT0~ *	D3:4	D28
A3:3	unused	D3:3	D27
A3:2	HOLD~ *	D3:2	D26
A3:1	H1 *	D3:1	D25
A3:0	H3 *	D3:0	D24
A2:7	A23	D2:7	D23
A2:6	A22	D2:6	D22
A2:5	A21	D2:5	D21
A2:4	A20	D2:4	D20
A2:3	A19	D2:3	D19
A2:2	A18	D2:2	D18
A2:1	A17	D2:1	D17

Table 1–3: TMS320C3X Primary bus signal connections for channel probes (cont.)

Section:channel	TMS320C3X signal	Section:channel	TMS320C3X signal
A2:0	A16	D2:0	D16
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11
A1:2	A10	D1:2	D10
A1:1	A9	D1:1	D9
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2
A0:1	A1	D0:1	D1
A0:0	A0	D0:0	D0
C3:7	EMU3	C2:7	MC/MP~ *
C3:6	EMU1	C2:6	R/W~
C3:5	EMU4/SHZ~	C2:5	RESET~
C3:4	EMU2	C2:4	RDY_D~ *
C3:3	EMU0	C2:3	STRB~
C3:2	XF1 *	C2:2	IOSTRB~
C3:1	XF0 *	C2:1	HOLDA~
C3:0	IACK~	C2:0	MSTRB~
C1:7		C0:7	
C1:6		C0:6	
C1:5		C0:5	
C1:4		C0:4	
C1:3		C0:3	
C1:2		C0:2	
C1:1		C0:1	
C1:0		C0:0	

* Signal not required for disassembly.

Table 1–4 lists the expansion bus signal connections for the channel probes.

Table 1–4: TMS320C3X Expansion bus signal connections for channel probes

Section:channel	TMS320C3X signal	Section:channel	TMS320C3X signal
A3:7		XD3:7	XD31
A3:6		XD3:6	XD30
A3:5		XD3:5	XD29
A3:4		XD3:4	XD28
A3:3		XD3:3	XD27
A3:2		XD3:2	XD26
A3:1		XD3:1	XD25
A3:0		XD3:0	XD24
A2:7		XD2:7	XD23
A2:6		XD2:6	XD22
A2:5		XD2:5	XD21
A2:4		XD2:4	XD20
A2:3		XD2:3	XD19
A2:2		XD2:2	XD18
A2:1		XD2:1	XD17
A2:0		XD2:0	XD16
A1:7		XD1:7	XD15
A1:6		XD1:6	XD14
A1:5		XD1:5	XD13
XA1:4	XA12	XD1:4	XD12
XA1:3	XA11	XD1:3	XD11
XA1:2	XA10	XD1:2	XD10
XA1:1	XA9	XD1:1	XD9
XA1:0	XA8	XD1:0	XD8
XA0:7	XA7	XD0:7	XD7
XA0:6	XA6	XD0:6	XD6
XA0:5	XA5	XD0:5	XD5
XA0:4	XA4	XD0:4	XD4
XA0:3	XA3	XD0:3	XD3
XA0:2	XA2	XD0:2	XD2
XA0:1	XA1	XD0:1	XD1
XA0:0	XA0	XD0:0	XD0

Table 1–4: TMS320C3X Expansion bus signal connections for channel probes (cont.)

Section:channel	TMS320C3X signal	Section:channel	TMS320C3X signal
C3:7		XC2:7	MC/MP~
C3:6		XC2:6	XR/W~
C3:5		XC2:5	RESET~
C3:4		XC2:4	XRDY_D~
C3:3		XC2:3	STRB~
C3:2		XC2:2	IOSTRB~
C3:1		XC2:1	HOLDA~
C3:0		XC2:0	MSTRB~
C1:7		C0:7	
C1:6		C0:6	
C1:5		C0:5	
C1:4		C0:4	
C1:3		C0:3	
C1:2		C0:2	
C1:1		C0:1	
C1:0		C0:0	

* Signal not required for disassembly.

Table 1–5 shows the clock probes and the processor signal to which they must connect for disassembly to be correct.

Table 1–5: Clock channel assignments

Clock channel	Clock or Qualifier	Active clock edge	TMS320C3X signal name
Clock:2	Qualifier	N/A	RDY~ =
Clock:1	Qualifier	N/A	RESET~ =
Clock:0	Clock	Both	H1 =
XClock:2	Qualifier	N/A	XRDY~ =
XClock:1	Qualifier	N/A	RESET~ =
XClock:0	Clock	Both	H1 =

= Indicates the signal is doubled probed.

20. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the processor digital signal processor in your SUT and attach the clip.

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 702 TMS320C3X support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the TMS320C3X support are Address, Data, and Control. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–6.

Clocking Options

The TMS 702 support offers a digital signal processor-specific clocking mode for the TMS320C3X processor. This clocking mode is the default selection whenever you load the TMS320C3X support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking options for the TMS 702 support are: Wait State Mode, Number of SW Wait, and Alternate Bus Master Cycles.

Wait State Mode The Wait State Mode field contains four selections that correspond to the particular wait state mode you are using. The selections are Hardware Only, Software Only, HW or SW, and HW and SW.

Hardware Only. This wait state depends only on the status of the external RDY~ line. The software wait state (SW Waits) are ignored.

Software Only. This wait state depends only on the number of SW Waits programmed in the Num of SW Wait field. The status of the external RDY~ line is ignored.

HW or SW. This wait state depends on either the status of the external RDY~ line, or the number of SW Waits selected in the Num of SW Wait field, whichever occurs earlier.

HW and SW. This wait state depends on both the status of the external RDY~ line and the number of SW Waits selected in the Num of SW Wait field, whichever occurs earlier. HW and SW is the default setting.

The TMS320C3X digital signal processors occasionally generate redundant read or prefetch cycles when there is a contention for the internal pipeline resources or external memory. The disassembly software identifies these redundant cycles and flags them as “PIPELINE/MEMORY CONFLICT” cycles. Incorrect setting of the “Wait State Mode” or the “Num of SW Wait” states fields can cause incorrect disassembly.

Num of SW Wait This field provides the number of SW Waits programmed discussed under *Wait State Mode*. This selection allows you to program the support to acquire correct bus data when software-programmed wait-states are used. You enter the number of wait states that the support is to insert in external cycles for the bus you are monitoring. You can enter a value from zero to seven which will be used by the Clocking State Machine (CSM) to track the completion of the bus cycle precisely as the processor does. The default setting is zero (none). If the Wait State Mode selected is HW Only, then the setting of this value does not matter.

Alternate Bus Master (ABM) Cycles The TMS 702 support has a select field with the label ABM Cycles. This field has two selections, Excluded and Included.

Excluded. Alternate Bus Master (ABM) Cycles are not acquired or displayed. Alternate Bus Master Cycles Excluded, is the default selection.

Included. All cycles are acquired.

Symbols

The TMS 702 support supplies one symbol table file. The processor_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file processor_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value				Meaning
	RESET- HOLDA- IACK-		STRB- MSTRB- IOSTRB- R/W-		
WR_PRI_BS	X 1 X		0 1 1 0		
RD_PRI_BS	X 1 X		0 1 1 1		
ACCESS_PRI	X 1 X		0 1 1 X		
WR_MEM_XP	X 1 X		1 0 1 0	XR/W~ mapped on to R/W~	
RD_MEM_XP	X 1 X		1 0 1 1	XR/W~ mapped on to R/W~	
MEM_XP_BS	X 1 X		1 0 1 X	XR/W~ mapped on to R/W~	
WR_I/O_XP	X 1 X		1 1 0 0	XR/W~ mapped on to R/W~	
RD_I/O_XP	X 1 X		1 1 0 1	XR/W~ mapped on to R/W~	
I/O_XP_BS	X 1 X		1 1 0 X	XR/W~ mapped on to R/W~	
ABM_READ	X 0 X		X X X 1		
ABM_WRITE	X 0 X		X X X 0		
ABM	X 0 X		X X X X		

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Triggering

Triggering on the Expansion Address Bus

The TMS320C3X expansion bus is 13-bits wide. The TMS320C3X probe adapter ties the remaining most significant bits to ground. Therefore, when entering values for the expansion address bus in the trigger menus, you must enter those remaining bits as zeros. The disassembler synthesizes the upper bits to match the memory map of the TMS320C3X data book.

You must also indicate either the MSTRB~ or the IOSTRB~ in the Control section of the trigger menus. A convenient method would be to enter the symbols provided by the TMS320C3X support.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- Changing the way data is displayed
- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the TMS320C3X support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to Changing How Data is Displayed on page 2–8.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows these special characters and strings, and gives a definition of what they represent.

Table 2–2: Meaning of special characters in the display

Character or string displayed	Meaning
>> or m	The instruction was manually marked
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle-type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–3: Cycle type definitions

Cycle type	Definition
(FLUSH)	A fetch cycle computed to be an opcode flush
(PIPELINE/MEMORY CONFLICT) †	The processor is rereading something
(WRITE)	Write to the primary bus
(READ)	Read from the primary bus
(ACCESS_PRI)	Primary bus access
(WRITE_EXP)	Memory Write to the expansion bus
(READ_EXP)	Memory Read from the expansion bus
(MEM_EXP_BS)	Memory access the expansion bus
(WR_I/O_EXP)	I/O Write to the expansion bus
(I/O_READ)	I/O Read from the expansion bus
(I/O_WRITE)	I/O Write to the expansion bus
(ALT_BUS_MSTR_READ)	Alternate Bus Master Read cycle
(ALT_BUS_MSTR_WRITE)	Alternate Bus Master Write cycle
(UNKNOWN)	The combination of control bits is unexpected and/or unrecognized

† The disassembler only does PIPELINE/MEMORY CONFLICT analysis on what the disassembler determines as fetches. The disassembler will not do analysis on writes or what the disassembler considers as non-fetch reads.

Figure 2–1 shows an example of the Hardware display.

1	2	3	4	5
Sample	Address	Data	Mnemonics	Timestamp
420	0001D8	0B62FFE8	NEGB FFE8,R2	70 ns
421	0001D9	17620018	SUBC 0018,R2	60 ns
422	0001DA	18E2000B	SUBRB 000B,R2	70 ns
423	0001DB	08200100	LDI @000100,R0	70 ns
424	0001DC	1540C400	STI R0,*AR4	70 ns
425	000100	00400F04	(READ)	60 ns
426	0001DD	0C800000	NOP	70 ns
427	000000	00400F04	(WRITE)	130 ns
428	0001DE	0F200000	PUSH R0	140 ns
429	0001DF	0FA20000	PUSHF R2	60 ns
430	0001E0	0EA20000	POPF R2	70 ns
431	0001E1	0E200000	POP R0	70 ns
432	0001E2	0DC55811	NOT *--AR0(IR0),R5	60 ns
433	0001E3	0DC22101	NOT *AR1++(01),R2	70 ns
434	0001E4	0DC61102	NOT *++AR1(02),R6	70 ns
435	0001E5	62000291	CALL 000291	60 ns
436	0001E6	09412901	(FLUSH)	70 ns
437	000291	1A870007	(READ)	260 ns
438	000292	08670004	LDI 0004,R7	70 ns
439	000293	18670001	SUBI 0001,R7	70 ns
440	000294	6A06FFFE	BNE 000293	70 ns

Figure 2–1: Hardware display format

- 1 **Sample Column.** Lists the memory locations for the acquired data.
- 2 **Address Group.** Lists data from channels connected to the TMS320C3X address bus.
- 3 **Data Group.** Lists data from channels connected to the TMS320C3X data bus.
- 4 **Mnemonics Column.** Lists the disassembled instructions and cycle types.
- 5 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that unconditionally generate a change in the flow of control in the TMS320C3X digital signal processor are as follows:

BR	BRD	CALL
SWI	RPTS	RPTB

Instructions that conditionally generate a change in the flow of control in the TMS320C3X digital signal processor are as follows:

Bcond	BcondD	CALLcond	DBcond
DBcondD	RETIcond	RETScond	TRAPcond

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that unconditionally generate a subroutine call or a return in the TMS320C3X digital signal processor are as follows:

CALL	SWI
------	-----

Instructions that conditionally generate a subroutine call or a return in the TMS320C3X digital signal processor are as follows:

CALLcond	RETIcond	RETScond	TRAPcond
----------	----------	----------	----------

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the TMS320C3X support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), the TMS320C3X support has one optional display selection, Data Page Pointer.

- Data page Pointer – Pointer to the page of data to be addressed in direct addressing mode. All of the values displayed are displayed in hexadecimal.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode – the first word of an instruction
- Flush – an opcode or extension that is fetched but not executed
- Read – marks a memory reference read as data
- Undo Marks – Removes all marks from the current sequence

You can also use the Mark Opcode function to specify the default segment size mode (16-bit or 32-bit) for the cycle. The segment size selection changes the cycle the cursor is on and the remaining cycles to the end of memory or to the next mark.

Information on basic operations contains more details on marking cycles.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your TMS320C3X digital signal processor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires processor signals
- List of other accessible TMS320C3X signals and extra probe channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a digital signal processor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a TMS320C3X processor. The probe adapter connects to the processor in the SUT. Signals from the TMS320C3X-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

The probe adapter accommodates the Texas Instruments TMS320C3X digital signal processor in a 181-pin PGA package, and in the 132-pin PQFP package.

Configuration

Place the Disassembly and Timing jumper in the D position to acquire disassembled data, and in the T position to acquire timing data. Table 3–1 shows how to position this jumper depending on the type of clocking you are using, and the type of window you want to view.

Table 3–1: Jumper positions and function

Jumper	Position	Function
J120 on the PGA probe adapter, J520 on the PQFP probe adapter	D	Use when acquiring disassembled data
	T	Use when acquiring timing data

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–2 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–2, for the 102/136-channel module, one podlet load is 20 k Ω in parallel with 2 pF. For the 96-channel module, one podlet load is 100 k Ω in parallel with 10 pF.

Table 3–2: Electrical specifications

Characteristics	Requirements	
SUT DC power requirements		
Voltage	4.75-5.25 VDC	
Current	I max (calculated)	16 mA
	I max (measured)	3.5 mA
SUT clock		
Clock rate	Minimum	3.3 MHz
	Maximum	33 MHz
Minimum setup time required	5 ns	
Minimum hold time required	0 ns	
	Specification	
Measured typical SUT signal loading	AC load [†]	DC load
RESET~	8 pF + 2 podlets	2 podlets
H1	6 pF + 2 podlets	2 podlets
MC/MP~	6 pF + 1 podlet	1 podlet
R/W~, XR/W~	4 to 7 pF + 2 podlets	2 podlets
STRB~, MSTRB~, IOSTRB~	4 to 7 pF + 1 podlet	1 podlet
HOLDA~, IACK~	4 to 7 pF + 1 podlet	1 podlet
RDY~, XRDY~	4 to 7 pF + 1 U. L.	1 U. L.
All others	4 to 7 pF + 1 podlet	1 podlet

[†] The AC loading capacitance includes run capacitance and the input capacitance of the ICs.

Table 3–3 shows the environmental specifications.

Table 3–3: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

* **Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed TMS320C3X digital signal processor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–4 shows the certifications and compliances that apply to the probe adapter.

Table 3–4: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.
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Figure 3–1 shows the dimensions of the PGA probe adapter. The figure also shows the minimum vertical clearance of the high-density probe cable.

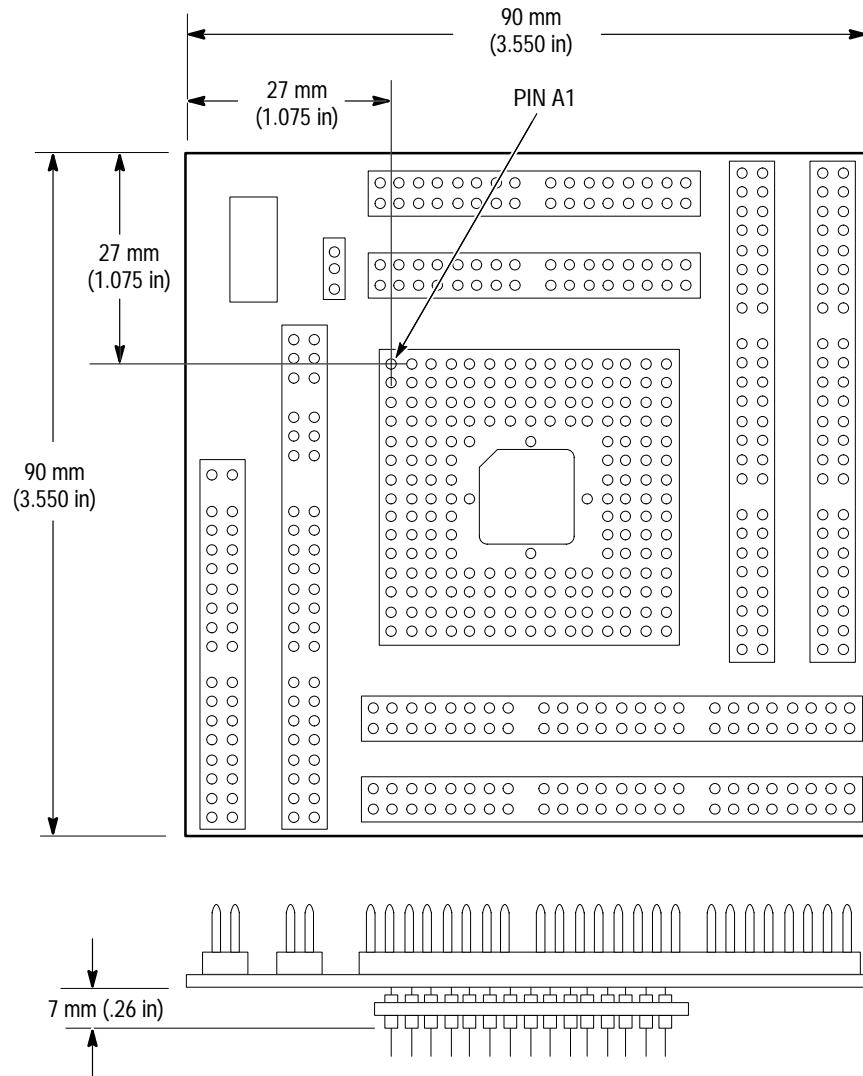


Figure 3–1: Dimensions of the PGA probe adapter

Figure 3–2 shows the dimensions of the PQFP probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter.

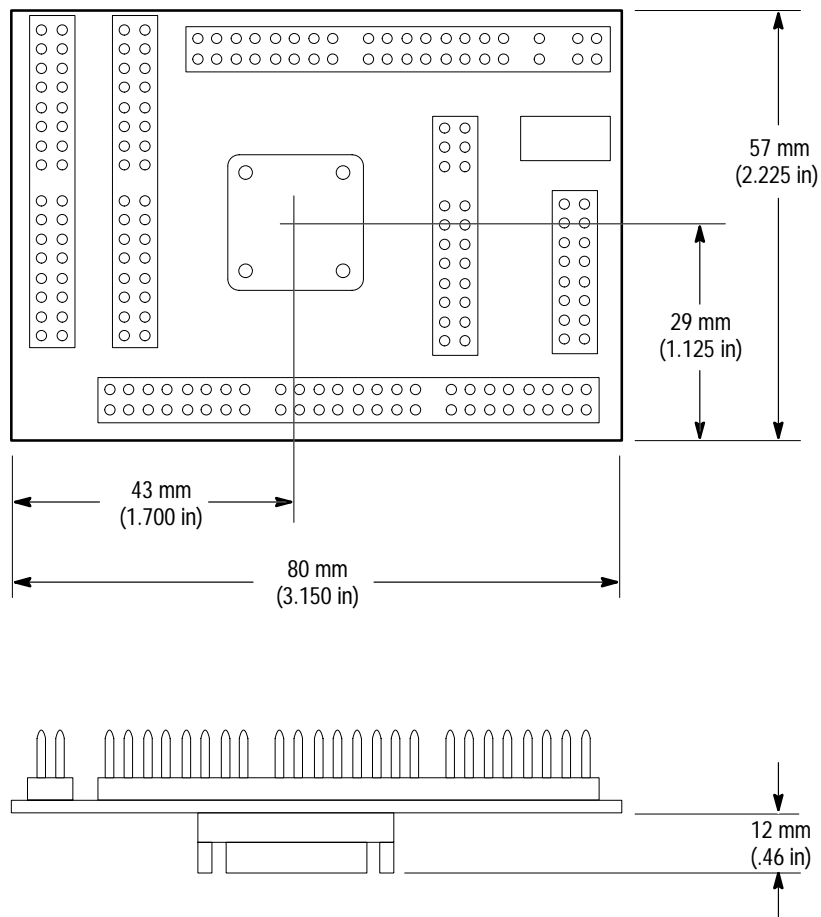


Figure 3–2: Dimensions of the PQFP probe adapter

Channel Assignments

Channel assignments shown in Table 3–5 through Table 3–14 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- An tilde (~) following a signal name indicates that the signal is active low.
- An equals sign (=) following a signal name indicates that it is double probed.
- If there are two modules (such as used to form 96-channels), the module in the higher-numbered slot is referred to as the HI module and the module in the lower-numbered slot is referred to as the LO module.

Table 3–5 shows the probe section and channel assignments for the Primary bus Address group and the TMS320C3X signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: Primary bus Address group channel assignments

Bit order	Section:channel	TMS320C3X signal name
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6

Table 3–5: Primary bus Address group channel assignments (cont.)

Bit order	Section:channel	TMS320C3X signal name
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–6 shows the probe section and channel assignments for the Expansion bus Address group and the TMS320C3X signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

The TMS320C3X Expansion address bus is 13-bits wide. Therefore, address pins XA1:5 through XA1:7, and XA2:0 through XA2:7 on the probe adapter are tied to ground.

Table 3–6: Expansion bus Address group channel assignments

Bit order	Section:channel	TMS320C3X signal name
12	XA1:4	XA12
11	XA1:3	XA11
10	XA1:2	XA10
9	XA1:1	XA9
8	XA1:0	XA8
7	XA0:7	XA7
6	XA0:6	XA6
5	XA0:5	XA5
4	XA0:4	XA4
3	XA0:3	XA3
2	XA0:2	XA2
1	XA0:1	XA1
0	XA0:0	XA0

Table 3–7 shows the probe section and channel assignments for the Primary bus Data group and the TMS320C3X signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–7: Primary bus Data group channel assignments

Bit order	Section:channel	TMS320C3X signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2

Table 3–7: Primary bus Data group channel assignments (cont.)

Bit order	Section:channel	TMS320C3X signal name
1	D0:1	D1
0	D0:0	D0

Table 3–8 shows the probe section and channel assignments for the Expansion bus Data group and the TMS320C3X signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–8: Expansion bus Data group channel assignments

Bit order	Section:channel	TMS320C3X signal name
31	D3:7	XD31
30	D3:6	XD30
29	D3:5	XD29
28	D3:4	XD28
27	D3:3	XD27
26	D3:2	XD26
25	D3:1	XD25
24	D3:0	XD24
23	D2:7	XD23
22	D2:6	XD22
21	D2:5	XD21
20	D2:4	XD20
19	D2:3	XD19
18	D2:2	XD18
17	D2:1	XD17
16	D2:0	XD16
15	D1:7	XD15
14	D1:6	XD14
13	D1:5	XD13
12	D1:4	XD12
11	D1:3	XD11
10	D1:2	XD10
9	D1:1	XD9
8	D1:0	XD8

Table 3–8: Expansion bus Data group channel assignments (cont.)

Bit order	Section:channel	TMS320C3X signal name
7	D0:7	XD7
6	D0:6	XD6
5	D0:5	XD5
4	D0:4	XD4
3	D0:3	XD3
2	D0:2	XD2
1	D0:1	XD1
0	D0:0	XD0

Table 3–9 shows the probe section and channel assignments for the Primary bus Control group and the TMS320C3X signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–9: Primary bus Control group channel assignments

Bit order	Section:channel	TMS320C3X signal name
6	C2:5	RESET~
5	C2:1	HOLDA~
4	C3:0	IACK~
3	C2:3	STRB~
2	C2:0	MSTRB~
1	C2:2	IOSTRB~
0	C2:6	R/W~

Table 3–10 shows the probe section and channel assignments for the Expansion bus Control group and the TMS320C3X signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–10: Expansion bus Control group channel assignments

Bit order	Section:channel	TMS320C3X signal name
6	XC2:5	RESET~
5	XC2:1	HOLDA~
4	XC3:0	IACK~
3	XC2:3	STRB~
2	XC2:0	MSTRB~
1	XC2:2	IOSTRB~
0	XC2:4	XR/W~

Table 3–11 shows the probe section and channel assignments for the Intr group and the TMS320C3X signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–11: Intr group channel assignments

Bit order	Section:channel	TMS320C3X signal name
3	A3:7	INT3~ *
2	A3:6	INT2~ *
1	A3:5	INT1~ *
0	A3:4	INT0~ *

* Signal not required for disassembly.

Table 3–12 shows the probe section and channel assignments for the Misc group and the TMS320C3X signal to which each channel connects. By default, this channel group is not visible.

Table 3–12: Misc group channel assignments

Bit order	Section:channel	TMS320C3X signal name
6	C2:4	RDY_D~
5	C2:7	MC/MP~

Table 3–12: Misc group channel assignments (cont.)

Bit order	Section:channel	TMS320C3X signal name
4	A3:0	H3 *
3	A3:1	H1 *
2	C3:2	XF1 *
1	C3:1	XF0 *
0	A3:2	HOLD~ *

* Signal not required for disassembly.

Table 3–13 shows the probe section and channel assignments for the Emulatn group and the TMS320C3X signal to which each channel connects. By default, this channel group is not visible.

Table 3–13: Emulatn group channel assignments

Bit order	Section:channel	TMS320C3X signal name
4	C3:5	EMU4/SHZ~
3	C3:7	EMU3
2	C3:4	EMU2
1	C3:6	EMU1
0	C3:3	EMU0

* Signal not required for disassembly.

Table 3–14 shows the channel assignments for the clock channels (not part of any group) and the TMS320C3X signal to which each channel connects.

Table 3–14: Clock channel assignments

Clock channel	Clock or Qualifier	Active clock edge	TMS320C3X signal name
Clock:2	Qualifier	N/A	RDY~ =
Clock:1	Qualifier	N/A	RESET~ =
Clock:0	Clock	Both	H1 =
XClock:2	Qualifier	N/A	XRDY~ =
XClock:1	Qualifier	N/A	RESET~ =
XClock:0	Clock	Both	H1 =

= Indicates the signal is doubled probes.

How Data is Acquired

This part of this chapter explains how the module acquires digital signal processor signals using the TMS 702 software and probe adapter. This part also provides additional information on digital signal processor signals accessible on or not accessible on the probe adapter, and on extra probe channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the TMS320C3X support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the processor bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module Clocking State Machine (CSM) generates one master sample for each processor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–3 shows the sample points and the master sample point when data is acquired from the Primary and Expansion bus.

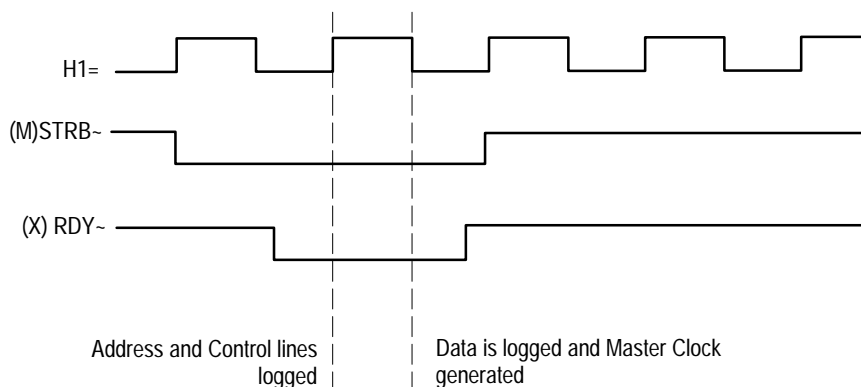


Figure 3–3: TMS320C3X Primary and Expansion bus timing

Figure 3–4 shows the sample points and the master sample point when data is acquired from the Expansion bus.

Data from I/O Expansion bus is acquired as follows. When the IOSTRB~ is low the address and control signals are logged in at the falling edge of the clock (H1). At the next rising edge the XRDY~ signal is sampled and if low the Data lines are logged in. Under TMS320C3X micro clocking, IACK~ is not sampled at valid times.

Figure 3–4 shows the sample points and the master clock for the Expansion bus.

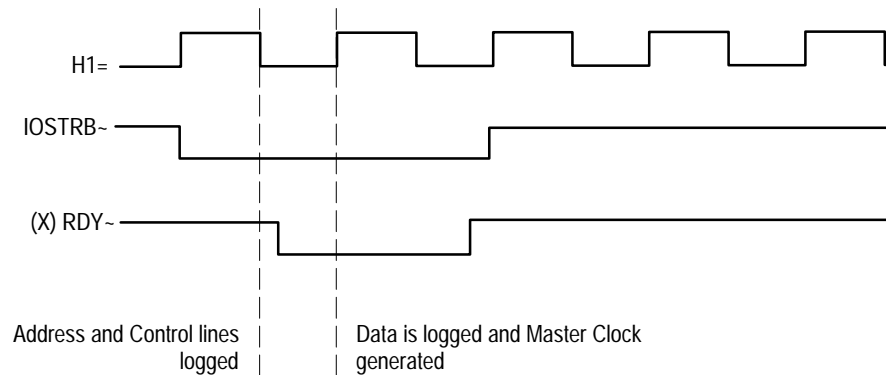


Figure 3–4: TMS320C3X Expansion bus timing

Clocking Options

The TMS320C3X support has provisions for three types of clocking options. The clock option establishes the type of bus cycle to include in, or exclude from the acquisition. The three select fields that you can choose from to customize your clocking are:

- Alternate Bus Master (ABM) Cycles, excluded or included.
- Wait State Mode
- Num of SW wait

Alternate Bus Master Cycles Excluded. DMA cycles are not acquired or displayed.

Alternate Bus Master Cycles Included. All bus cycles, including Alternate Bus Master cycles are acquired.

Wait State Mode. The Wait State Mode field contains four selections that correspond to the particular wait state mode you are using. The Wait State Modes are:

Hardware Only – The wait state depends only on the status of the external RDY~ line. The software wait state (SW Waits) are ignored.

Software Only – The wait state depends only on the number of SW Waits programmed in the Num of SW Wait field. The status of the external RDY~ line is ignored.

HW or SW – The wait state depends on either the status of the external RDY~ line, or the number of SW Waits selected in the Num of SW Wait field., whichever occurs earlier.

HW and SW – The wait state depends on both the status of the external RDY~ line and the number of SW Waits selected in the Num of SW Wait field., whichever occurs later.

Num of SW Wait. This field provides the number of SW Waits programmed in the Wait State Mode field. A total of eight SW Waits can be programmed in this field.

Alternate Microprocessor Connections

You can connect to other signals that are not required by the support so that you can analyze other signal activity in your system. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–6. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals Not On the Probe Adapter

The probe adapter does not provide access for the following signals:

- X1
- X2_CLKIN
- VBBP
- EMU6
- EMU5
- RSV10–RSV0

Extra Channels Table 3–15 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Channels not defined in a channel group by the TMS 702 software are logged in with the Master sample point.

Table 3–15: Extra module sections and channels

Module	Section: channels
102-channels	Qual:1, Qual:0, A3:3
136-channels	E3:7-0, E2:7-0, E1:7-0, E0:7-0, Qual:3-0, A3:3
96-channels	None

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

Maintenance

This chapter contains information on the following topics:

- Probe adapter circuit description

Probe Adapter Circuit Description

One transparent latch chip (74FCT373C) is used to ensure that the RDY~ and XRDY~ signals meet setup/hold time requirements. These requirements are needed for signals used as qualifiers. All other signals go directly to the podlets. To correctly acquire the RDY~ and XRDY~ for timing analysis, J120 must be in the T position.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 702 TMS320C3X digital signal processor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

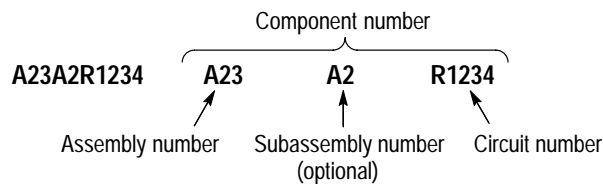
Parts list column descriptions

Column	Column name	Description
1	Component number	<p>The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the <i>Diagrams</i> section, and on the mechanical exploded views in the <i>Replaceable Mechanical Parts</i> list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table).</p> <p>The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts).</p> <p>Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.</p>
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1-1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
0TJ19	QUALITY SEMICONDUCTOR INC	851 MARTIN AVENUE	SANTA CLARA CA 95050-2903
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
01121	ALLEN-BRADLEY CO	1201 S 2ND ST	MILWAUKEE WI 53204-2410
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077-0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	671-2589-00			CIRCUIT BD ASSY:320C30,PROBE ADAPTER,PGA	80009	671258900
A02	671-2621-00			CIRCUIT BD ASSY:320C31,PROBE ADAPTER,PQFP	80009	671262100
A01	671-2589-00			CIRCUIT BD ASSY:320C30,PROBE ADAPTER,PGA	80009	671258900
A01C100	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	12063C104KAT3A
A01C350	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	12063C104KAT3A
A01C351	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	12063C104KAT3A
A01C352	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	12063C104KAT3A
A01C353	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	12063C104KAT3A
A01C354	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	12063C104KAT3A
A01C355	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	12063C104KAT3A
A01J120	131-4530-00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230	00779	104344-1
A01J150	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A01J155	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A01J310	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A01J400	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A01J550	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A01J650	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A01J700	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A01J800	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A01R120	321-5026-00			RES,FXD:THICK FILM:4.75K OHM,1%,0.125W,TC=1	01121	BCK4751FT
A01U100	156-6275-00			IC,DIGITAL:FCTCMOS,LATCH;OCTAL D-TYPE	0TJ19	74FCT373DSO

Replaceable Electrical Parts

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discontinued	Name & description	Mfr. code	Mfr. part number
				OPTION 1S		
A02	671-2621-00			CIRCUIT BD ASSY:320C31,PROBE ADAPTER PQFP	80009	671262100
A02C1225	283-5007-00			CAP,FXD,CER DI:8PF,+/- 0.5PF,50V	04222	12061A8R0DATMA
A02C1255	283-5007-00			CAP,FXD,CER DI:8PF,+/- 0.5PF,50V	04222	12061A8R0DATMA
A02C1260	283-5007-00			CAP,FXD,CER DI:8PF,+/- 0.5PF,50V	04222	12061A8R0DATMA
A02C1310	283-5007-00			CAP,FXD,CER DI:8PF,+/- 0.5PF,50V	04222	12061A8R0DATMA
A02C1450	283-5007-00			CAP,FXD,CER DI:8PF,+/- 0.5PF,50V	04222	12061A8R0DATMA
A02C1460	283-5007-00			CAP,FXD,CER DI:8PF,+/- 0.5PF,50V	04222	12061A8R0DATMA
A02C1660	283-5007-00			CAP,FXD,CER DI:8PF,+/- 0.5PF,50V	04222	12061A8R0DATMA
A02J1190	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A02J1200	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A02J1290	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A02J1520	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A02J1720	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A02J1790	131-5267-00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A01R1560	321-5026-00			RES,FXD:THICK FILM;4.75K OHM,1%,0.125W,TC=1	01121	BCK4751FT
A02U1760	156-6275-00			IC,DIGITAL:FCTCMOS,LATCH;OCTAL D-TYPE,	0TJ19	74FCT373DSO

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 702 TMS320C3X digital signal processor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1-1972.

**Mfr. Code to Manufacturer
Cross Index**

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656-4548
63058	MCKENZIE TECHNOLOGY	44370 OLD WARMS SPRINGS BLVD	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077-0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
LOW-PROFILE PROBE ADAPTER							
1-0	010-0552-00			1	PROBE ADAPTER: 320C30, PGA181, SOCKETED	80009	010055200
-4	671-2589-00			1	CIRCUIT BD ASSY: 320C30, PROBE ADAPTER, PGA	80009	671258900
-5	131-5267-00			4.5	CONN, HDR:PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235 (SEE REPL A01 J150, J155, J310, J400, J550, J650, J700, J800)		
-1	131-4356-00			1	CONN, BOX: SHUNT/SHORTING, FEMALE, 1 X 2, 0.1 (A01 P120)	26742	9618-302-50
-3	131-4530-00			1	CONN, HDR: PCB, MALE, STR, 1 X 3, 0.1 CTR, 0.230 (SEE REPL A01 J120)		
-2	136-1199-00			2	SOCKET, PGA, 181 POS, 15 X 15, 0.1 CTR (SEE A01 USED WITH U350)	63058	181H115B11504F
OPTIONAL ACCESSORIES							
	070-9802-00			1	MANUAL, TECH: BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070-9802-00

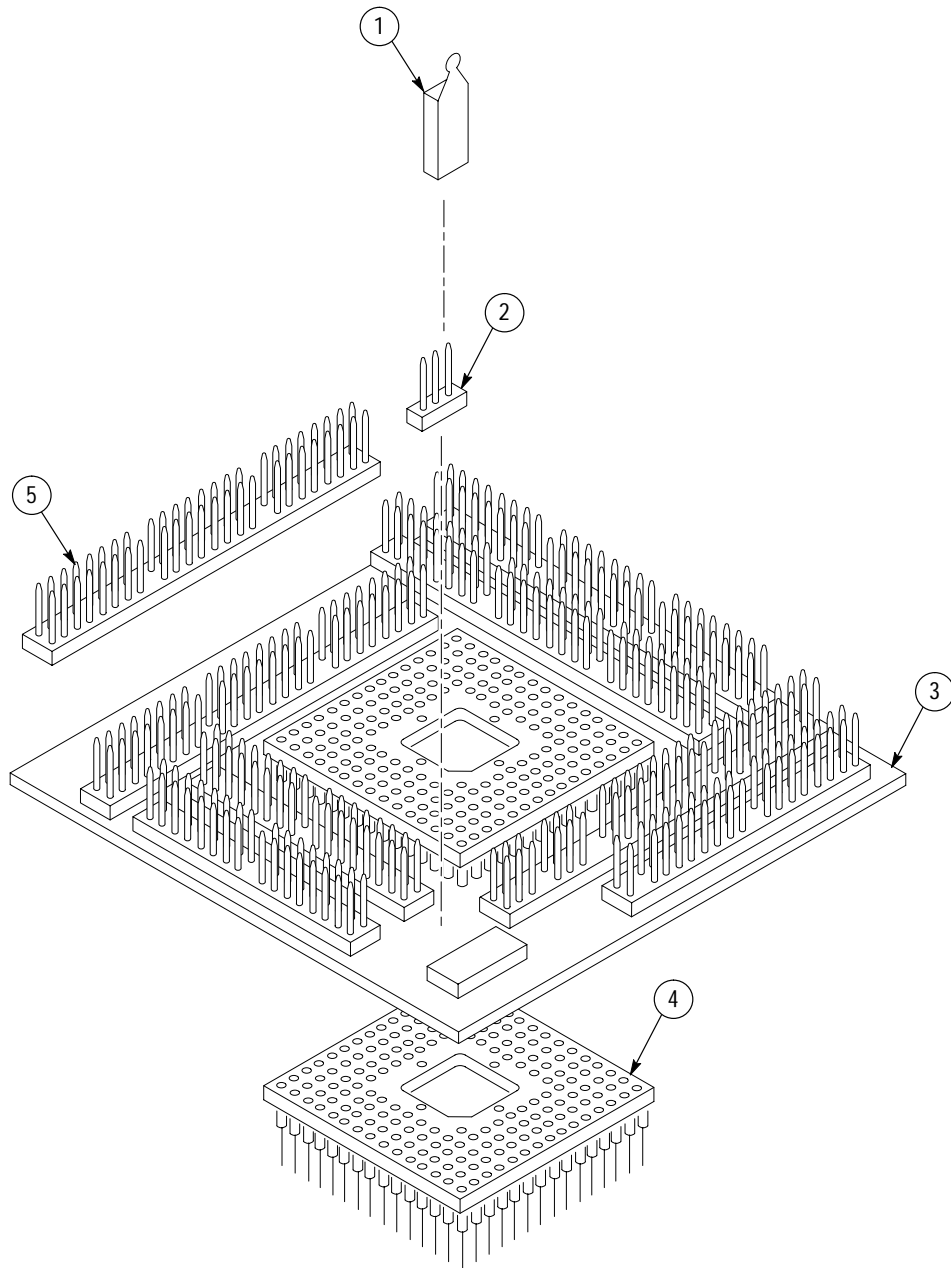


Figure 1: TMS320C3X probe adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
STANDARD ACCESSORIES							
	070-9831-00			1	MANUAL, TECH: INSTRUCTION, 320C3X, DISSASSEMBLER, TMS 702	80009	070-9831-00
	070-9803-00			1	MANUAL, TECH: TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070-9803-00
2-3	671-2621-00			1	CIRCUIT BD ASSY: 320C31, PROBE ADAPTER	80009	671262100
-2	131-5267-00			4.5	CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235 (SEE A02 REPL J1190, J1200, J1290, J1520, J1720, J1790)		
-1	131-4356-00			2	CONN, BOX: SHUNT/SHORTING, FEMALE, 1 X 2, 0.1 (P1520)	26742	9618-302-50
OPTIONAL ACCESSORIES							
	070-9802-00			1	MANUAL, TECH: BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070-9802-00

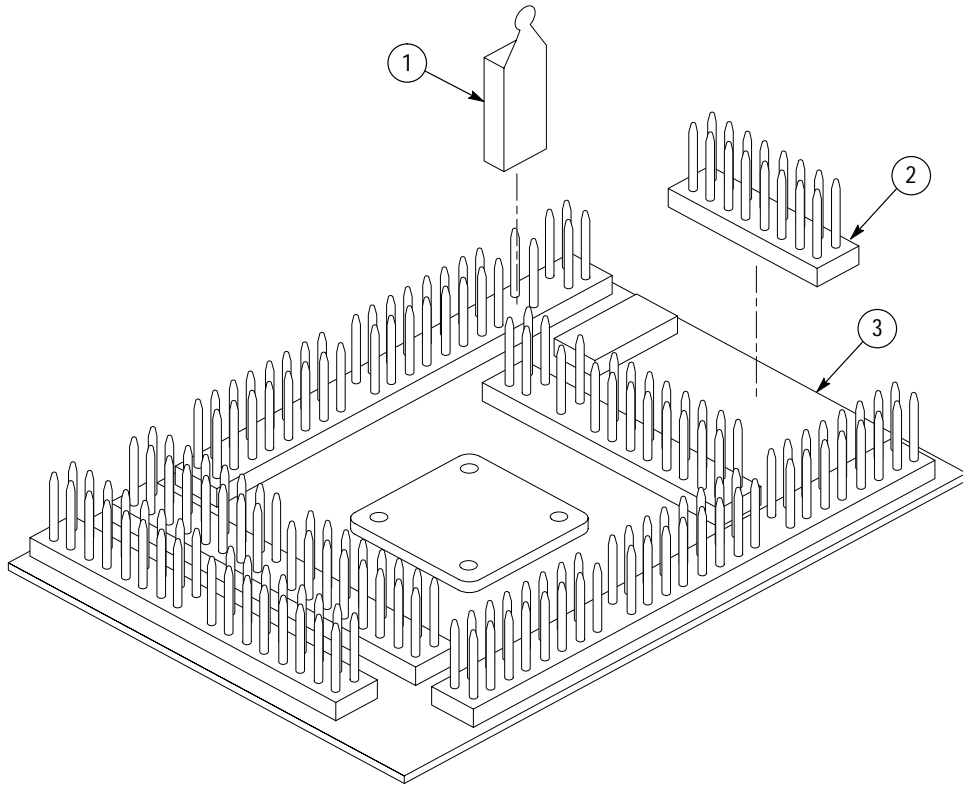


Figure 2: TMS320C3X probe adapter exploded view

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