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Tektronix

TMS 810
Rambus Direct RIMM Bus Support
Troubleshooting Tips

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Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

Read This First

The following information relates to what may be, or appear to be, incorrectly acquired data by the TMS 810 Rambus probe adapter.

RESET

If any of the following conditions occur, you must reset the probe adapter to acquire correct data:

- The Rambus clock has been stopped
- The System under test has been rebooted
- The system under test is powered off
- The probe adapter is powered off

NOTE. Do not power off the probe adapter, or the system under test may crash.

Pressing the reset button on the probe adapter has no effect on the system under test. When in doubt, press reset before starting an acquisition.

Error Correcting Code (ECC)

When ECC (Error correcting code) is enabled, some early Rambus chipsets are known to transpose certain data bits with ECC bits. Specifically, the most significant data bit of each of the respective four data bytes of long-words, D0[63:32] and D1[63:32], are transposed with their adjacent ECC bits. As a result, this may display incorrectly acquired data. Therefore, if you suspect this is happening in your system, you should disable ECC in the BIOS. With ECC disabled, the data will display correctly.

If you are using the Intel 820 chipset and must operate with ECC enabled, then under the File pulldown menu, select Load Module and then select:

```
C:\Program Files\TLA 700\Supports\RAMBUS\Camino_ECC
```

This module setup can be used along with the provided trigger programs. Perform this Load Module before performing the Load Trigger. Refer to pages 2–4 through 2–7 for trigger programs in the *TMS 810 Instruction Manual* for details.

Front Side Bus (FSB) verses Rambus Display

The front side bus is a parallel bus, and Rambus is a serial bus. The TMS 810 support package provides two ways to view the data:

- In the order the data bytes appear on the front side bus
- In the order the data bytes are serialized on the Rambus

Refer to pages 2–1 and 2–2 of the *TMS 810 Instruction* manual for information about the differences in byte order between FSB and Rambus.

SIO Support

Whenever a Power State Transition of NAP Exit or PDN Exit occurs on the SIO bus, the status of the SIO line is captured and recorded in the SIO group, with 1 or 0 corresponding to the level of the SIO signal. At the same time, the device address is captured and recorded in the least significant byte of D0[31:00] or DA[31:00], device address 20 is the broadcast all-devices address.

Unlike Row, Column, and Write Data packets, the timing of SIO information is only approximate relative to Row, Column, and Write Data packets. Refer to the *TMS 810 Instruction Manual*, page 2–15, for timing between Row, Column, and Write Data packets.

If you observe two consecutive NAP/PDN Exit commands on consecutive samples and the difference in their timestamps is four Rambus clock cycles (that is 10 ns for a 400 MHz Rambus clock), then you must adjust the SIO group setup/hold time. Refer to the *TMS 810 Instruction Manual*, page 2–16 for details. An improper adjustment can also result in the wrong or missing device address.

Cross Triggering Capability

The TMS 810 support package along with the TDS 694C 10 GS/s oscilloscope can capture the precise Rambus signal waveform at the point of interest. Refer to www.tektronix.com on logic analyzers for application notes on how to setup the TDS 694C oscilloscope, along with the TMS 810 support, to adjust its trigger point. The application note on *Cross Triggering a TDS694C with a TLA700* is generic, but a more specific application note for TMS 810 will be available soon, you may also want to check the TMS 810 Rambus support link. Once the precise bit has been located, an informed investigation can be based on an oscilloscope capture (TDS 694C) of the specific signal in question.