Technical Reference

Tektronix

DTG5078, DTG5274, and DTG5334 Data Timing Generators Specifications and Performance Verification

071-1611-03

This document applies to firmware version 2.1.1 and above.

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- In North America, call 1-800-833-9200.
- Worldwide, visit www.tektronix.com to find contacts in your area.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Power Disconnect The power cord disconnects the product from the power source.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

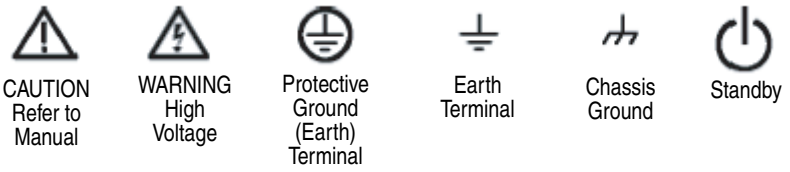
Symbols and Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

The following symbols may appear on the product:



Preface

This manual provides information necessary for users or service technicians to verify the performance of the DTG5000 Series Data Timing Generator.

Manual Structure

The DTG5000 Series Data Timing Generator Technical Reference contains the following sections:

The *Performance Verification* section contains an introduction, a list of equipment required, and procedures that, when passed, ensure that the product meets its specifications.

The *Specifications* section contains a brief product description and characteristics tables. These tables cover the electrical, mechanical, environmental characteristics and certification.

Related Manuals and Online Documents

This manual is part of a document set of standard accessory manuals and online documentation; this manual mainly focuses on the performance verification and specifications information needed to verify the product performance. See the following list for other documents supporting the data timing generator operation and service.

Document name	Description
DTG5000 Series Online Help	An online help system, integrated with the user interface application that ships with this product. The help is preinstalled in the instrument.
DTG5000 Series User Manual 1	A quick reference to major features of the instrument and how they operate. It also provides several tutorials to familiarize the user with basic instrument features.
DTG5000 Series User Manual 2 (a PDF file on the Document CD)	A comprehensive guide to instrument operation, function, and menus.
DTG5000 Series Programmer (a PDF file on the Document CD)	Complete information on programming commands and remote control of the instrument.
DTG5000 Series Service Manual	Instructions for servicing the instrument to the module level. This optional manual must be ordered separately.

Performance Verification

Performance Verification

Two types of Performance Verification procedures can be performed on this product: *Self Tests and Performance Tests.* You may not need to perform all of these procedures, depending on what you want to accomplish.

- Verify that the DTG5000 Series Data Timing Generators are operating correctly by running the *Self Tests*, which begin on page 1-3.

  Advantages: These procedures require minimal time to perform, and test the internal hardware of the DTG5000 Series Data Timing Generators.

- If a more extensive confirmation of performance is desired, complete the self tests, and then do the *Performance Tests* beginning on page 1-10.

  Advantages: These procedures add direct checking of warranted specifications. These procedures require suitable test equipment and more time to execute. (Refer to *Required Equipment* on page 1-11).

Conventions in this manual

Throughout these procedures the following conventions apply:

- Each test procedure uses the following general format:

  Title of Test

  Equipment Required

  Prerequisites

  Procedure

- Each procedure consists of as many steps, substeps, and subparts as required to do the test. Steps, substeps, and subparts are sequenced as follows:

  1. First Step

  a. First Substep

  - First Subpart
  - Second Subpart

  b. Second Substep

  2. Second Step

- Where instructed to use a control in the display or a front-panel button or knob, the name of the control, button or knob appears in boldface type.

Menu Selections

Instructions for menu selection use the following format:

Menu button → Left or right Allow button (by using this button, you can move to desired menu category) → **Upper or down Allow button** (by using this button, you can move to desired menu item) → **SELECT or Enter key** (this completes the selection).

You can use a mouse as a pointer, use keyboard shortcuts for quick operation, or use front panel knob instead of sticking to above menu selection format.

User Manual

The *DTG5078 & DTG5274 & DTG5334 Data Timing Generators User Manual 1* is strongly recommended to familiarize the first-time user with instrument controls and features.

Install the Output Modules

Any output modules ordered are shipped separately. For complete instructions on how to install the output modules, refer to the User Manual. (Output modules do not ship preinstalled.)

CAUTION. *Do not install or remove any output modules while the instrument is powered on.*

Always power the instrument down before attempting to remove or install any output module.

Self Tests

There are two types of tests in this section that provide a quick way to confirm basic functionality and proper adjustment:

- Diagnostics
- Calibration (You must perform this calibration before the performance tests.)

These procedures use internal diagnostics to verify that the instrument passes the internal circuit tests, and calibration routines to check and adjust the instrument internal calibration constants.

NOTE. *To perform the Self Tests, at least one output module (DTGM10, DTGM20, DTGM21, DTGM30, DTGM31, or DTGM32) must be installed in the DTG5000 series Data Timing Generator mainframes. You can select any slot when you perform the tests even though the descriptions below are assuming the Slot A is used.*

Diagnostics

This procedure uses internal routines to verify that the instrument is operating correctly. No test equipment or hookups are required.

The instrument automatically performs the internal diagnostics when powered on; you can also run the internal diagnostics using the menu selections described in this procedure. The difference between these two methods of initiating the diagnostics is that the menu method does a more detailed memory check than the power on method.

Do the following steps to run the internal routines that confirm basic functionality and proper adjustment.

Equipment required	**None**
Prerequisites	First, at least one output module must be installed properly in the mainframe. Second, power on the instrument and allow a twenty-minute warmup before doing this procedure.

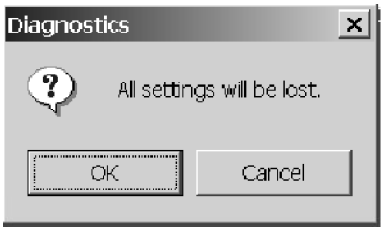
1. Set up the instrument:
   - Confirm that there is no output being performed by verifying that the **RUN** button indicator is not on. If the indicator is on, push the **RUN** button to turn it off.

- Verify that the output module LEDs are not on. If any output module LEDs are on, push the **ALL OUTPUTS ON/OFF** button to turn the LEDs off.

2. Internal diagnostics: Perform these substeps to verify internal diagnostics.

a. Display the Diagnostics dialog box:

- From the application menu bar, select **System**, and then select **Diagnostics...**. The following dialog box appears if you have changed the settings



- Select **OK** to display the Diagnostics dialog box. See Figure 1-1.

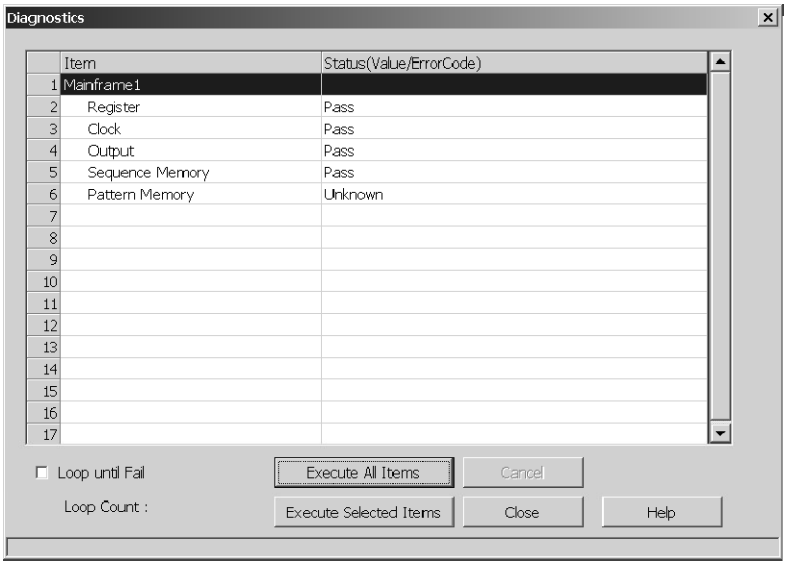


Figure 1-1: Diagnostics dialog box

- Verify that the **Loop until Fail** box is not checked. If it is checked, click the box to remove the check mark.
- Select **Execute All Items** to start the diagnostics.

b. Wait: The internal diagnostics takes one to six minutes. When complete, the resulting status appears in the diagnostics control window.

c. Verify that no failures are found and reported: All tests should pass. Confirm that the word **Pass** appears in all the **Status** fields. If any failures occur, record the failure information and contact your local Tektronix service personnel for more information.

3. Select **Close** to exit the diagnostics.

Calibration

Two types of calibrations are provided in the DTG5000 Series Data Timing Generator.

- The *Level Calibration* uses internal calibration routines that check electrical characteristics such as DC accuracy of data output, and then adjust the internal calibration constants as necessary.
- The *Skew Calibration* checks the delay time of data output, and then adjust the internal calibration constants as necessary. The calibration is performed by connecting each channel output to Skew Cal In.

NOTE. Level Calibration *and* Skew Calibration *are not valid until the instrument reaches a valid temperature.*

Level Calibration.

Equipment required	None
Prerequisites	Power on the instrument and allow a 20 minute warmup at an ambient temperature between +20 °C and +30 °C before doing this procedure. The calibration routine must be performed whenever the ambient temperature changes by 5 °C or more.

1. Set up the instrument:

- Confirm that there is no output being performed by verifying that the **RUN** button indicator is not on. If the indicator is on, push the **RUN** button to turn it off.
- Verify that the output module LEDs are not on. If any output module LEDs are on, push the **ALL OUTPUTS ON/OFF** button to turn the LEDs off.

2. Perform the calibration suite:

   a. From the application menu bar, select **System**, and then select **Level Calibration...**. The Level Calibration dialog box appears. See Figure 1-2.

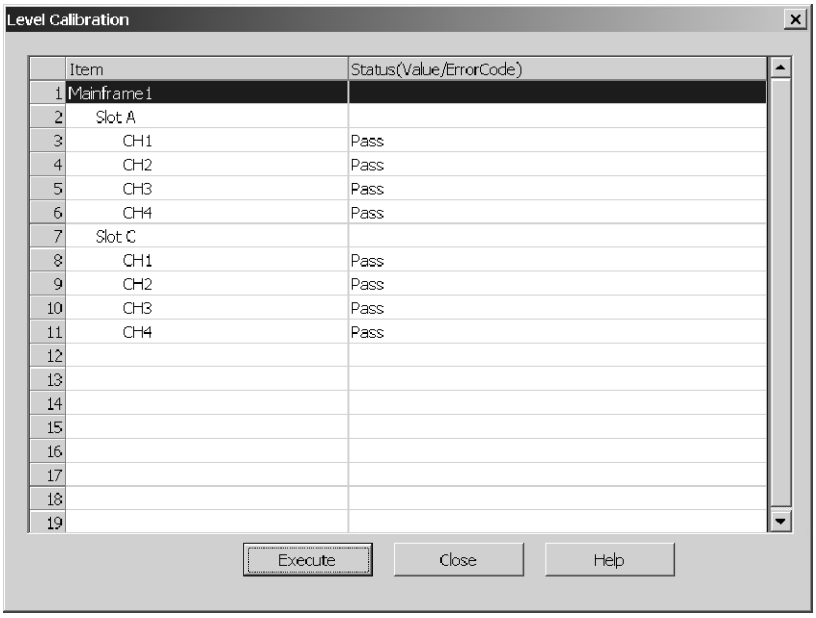


Figure 1-2: Level Calibration dialog box

   b. Select **Execute**.

   c. All the Status fields must be **Pass**. If any failures occur, record the failure information and contact your local Tektronix service personnel for more information.

3. Select **Close** to exit the calibration.

Skew Calibration.

Equipment required	One 50 Ω SMA coaxial cable, Tektronix part number 174-1427-00 Refer to test equipment list on page 1-12.
Prerequisites	Power on the instrument and allow a 20 minute warmup at an ambient temperature between +20 °C and +30 °C before doing this procedure. The calibration routine must be performed whenever the ambient temperature changes by 5 °C or more.

1. Set up the instrument:

- Confirm that there is no output being performed by verifying that the **RUN** button indicator is not on. If the indicator is on, push the **RUN** button to turn it off.
- Verify that the output module LEDs are not on. If any output module LEDs are on, push the **ALL OUTPUTS ON/OFF** button to turn the LEDs off.

2. Perform the calibration suite:

a. From the application menu bar, select **System**, and then select **Skew Calibration**. The following dialog box appears if you have changed the settings. Click **OK**.

b. The Skew Calibration dialog box appears. See Figure 1-3.

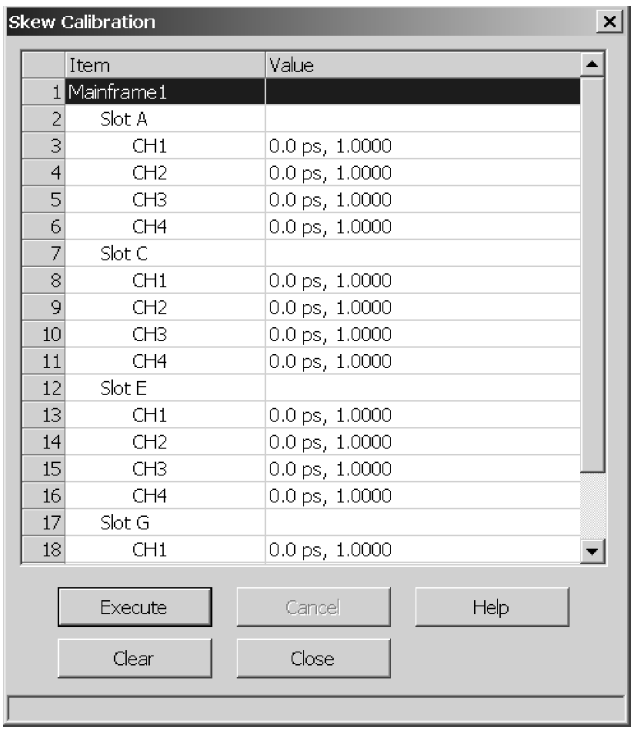
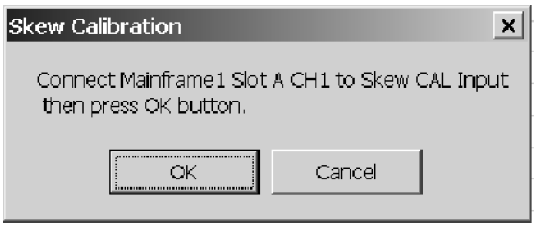


Figure 1-3: Skew Calibration dialog box

c. Attach an SMA coaxial cable to the **SKEW CAL IN** on the front panel of the data timing generator mainframe.

d. Select **Execute** to display the dialog box shown below.



e. Connect the opposite end of the SMA coaxial cable to the **CH1** connector of output module and select **OK** to start the calibration. Wait until the calibration completes.

f. Follow the on-screen instruction to continue the calibration:

- Disconnect the cable from the channel and reconnect it to next channel.

- Repeat the same calibration procedure for all channels.

NOTE. *When you connect the output module and* Skew Cal In*, use the identical cable. If you use different cables, the calibration result may be affected.*

g. When complete, the resulting status appears on the screen. See Figure 1-4.

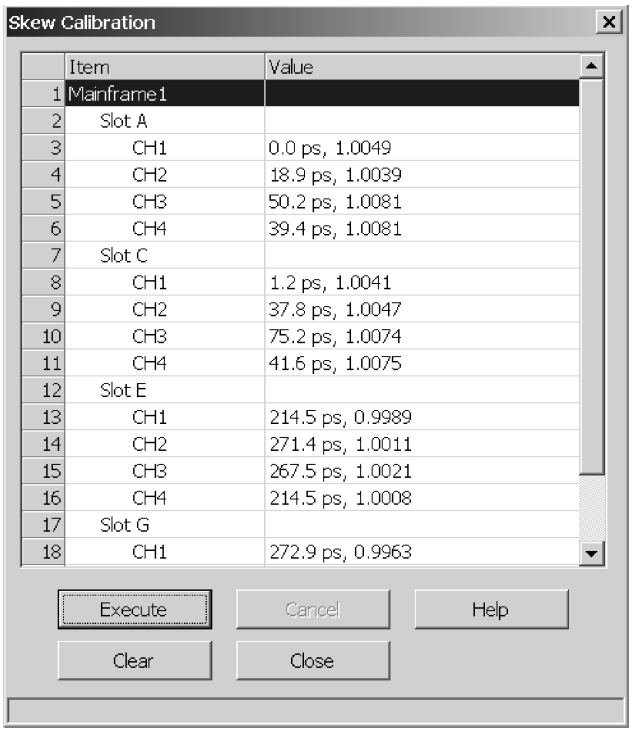


Figure 1-4: Skew Calibration results screen

h. Verify that no failures are found and reported on the screen.

i. If any failures occur, record the failure information and contact your local Tektronix service personnel for more information.

3. Select **Close** to exit the calibration.

NOTE. *The calibration data in the memory may be lost if the instrument is powered off while the calibration is executed.*

Performance Tests

The *Performance Tests* include functional test items, such as the interface functional test, in this manual.

- The *Functional Tests* verify the functions, that is, they verify that the DTG5000 Series Data Timing Generator features operate. They do not verify that they operate within limits.
- The *Performance Tests* verify that the DTG5000 Series Data Timing Generator performs as warranted. The *Performance Tests* check all the characteristics that are designated as checked in *Specifications*. (The characteristics that are checked appear with a 4 in *Specifications.*)

Table 1-1: Performance test items

Titles	Test items	Reference page
DTG5000 series mainframe[1]		
Sync output	Output level	page 1-29
Internal clock frequency	Internal clock output frequency accuracy	page 1-32
External clock output	External clock output amplitude, rise time/ fall time, and aberration	page 1-34
External clock input	External clock input function and external clock input frequency accuracy	page 1-36
10 MHz reference input	10 MHz reference input function	page 1-39
10 MHz reference output	10 MHz reference output frequency and output level	page 1-40
Phase lock input	Phase lock input function	page 1-42
Internal automatic trigger	Internal auto trigger function	page 1-44
Trigger input	Trigger input function	
Event input and sequence function	Event input function, jump out function for master-slave operation, and sequence operation	page 1-48
All jitter generation	Jitter profile and jitter volume	page 1-53
Partial jitter generation	Jitter profile and jitter volume	page 1-55
DC output	DC output accuracy	page 1-57
Skew and delay timing	Skew time between channels (after skew calibration)	page 1-59
Clock out random jitter	Clock out random jitter	page 1-63
Random jitter	Random jitter	page 1-66
Total jitter	Total jitter	page 1-69
PG Mode	Frequency, Duty, and Mode	page 1-72
Master-Slave operation	Master-Slave operation	page 1-75

Table 1-1: Performance test items (cont.)

Titles	Test items	Reference page
Output module		
Data output DC level	Output level accuracy	page 1-80
Data format	NRZ, RZ, and NRI	page 1-86
Jitter input	Jitter control	page 1-89
Inhibit input	Inhibit control	page 1-93

[1] **At least one output module, which operates correctly, must be installed into the DTG5000 series mainframe slot when you execute the performance tests.**

Prerequisites

The tests in this section comprise an extensive, valid confirmation of performance and functionality when the following requirements are met:

- The cabinet must be installed on the instrument.
- Allow 20 minutes warm up period.
- You must have performed and passed the procedures under *Self Tests,* found on page 1-3.
- The data timing generator must have been last adjusted at an ambient temperature between +20 °C and +30 °C, and must have been operating for a warm-up period of at least 20 minutes.
- The *Performance Tests* must be executed at an ambient temperature between +10 °C and +40 °C.

Required Equipment

Table 1-2 lists the required equipment used to complete the performance tests.

Table 1-2: Test equipment

Item number and description	Minimum requirements	Recommended equipment or equivalent	Purpose
1. Frequency Counter	50 kHz to 5 GHz, Accuracy: <0.2 ppm	Agilent 53181A op.050/010	Checks clock frequency.
2. Digital Multi Meter	DC volts range: – 10 V to +10 V, Accuracy: ±1%	Fluke 175	Measures voltage. Used in multiple procedures.
3. Oscilloscope	Bandwidth: >1 GHz, Number of channel: >4, 1 MΩ and 50 Ω inputs	Tektronix TDS7154	Checks output signals. Used in multiple procedures.
4. Sampling Oscilloscope	Bandwidth: >20 GHz, Rise time: <17.5 ps, 50 Ω input	Tektronix CSA8000B, 80E03 [2]	Checks output signals. Used in multiple procedures.
5. Function Generator	Output voltage: –5 V to +5 V, Frequency accuracy: <0.01%	Tektronix AFG320	Generates external input signals. Used in multiple input signal test procedures.

Table 1-2: Test equipment (cont.)

Item number and description	Minimum requirements	Recommended equipment or equivalent	Purpose
6. SMA Coaxial Cable (3 required)	50 Ω, male to male SMA connector	Tektronix part number 174-1427-00	Signal interconnection
7. BNC Coaxial Cable (3 required)	50 Ω, male to male BNC connector	Tektronix part number 012-0076-00	Signal interconnection
8. Adapter (2 required)	SMA (male) to BNC (female), 50 Ω	Tektronix part number 015-0554-00	Signal interconnection
9. Adapter (2 required)	SMA (female) to BNC (male), 50 Ω	Tektronix part number 015-0572-00	Signal interconnection
10. Adapter	N (male) to SMA (male), 50 Ω	Tektronix part number 015-0369-00	Signal interconnection
11. Adapter	SMA (female) to SMA (female), 50 Ω	Tektronix part number 015-1012-00	Signal interconnection
12. Lead set for DC output	16-CON twisted pair, 60 cm (24 in)	Tektronix part number 012-A229-00	Signal interconnection
13. Dual-Banana Plug	BNC (female) to dual banana	Tektronix part number 103-0090-00	Signal interconnection
14. BNC-T Connector	BNC (male) to BNC (female) to BNC (female)	Tektronix part number 103-0030-00	Signal interconnection
15. Feed-through Termination	50 Ω, 0.1%, BNC	Tektronix part number 011-0129-00	Signal termination
16. SMA Termination	50 Ω, SMA	Tektronix part number 015-0706-00	Signal termination
17. Attenuator (2 required)	12 dB, SMA	---	Signal attenuation
18. SMB-BNC Cable	SMB (female) to BNC (male) connector	Tektronix part number 012-1459-00	Signal interconnection
19. DTG5000 series mainframe		DTG5078	Four channel performance tests for DTGM10/DTGM20/DTGM21
20. DTG5000 series output module		DTGM20 or DTGM21	Random Jitter and Total Jitter tests for DTG5078
21. DTG5000 series output module		DTGM30	Random Jitter and Total Jitter tests for DTG5274 and DTG5334

[2] **For best repeatability and to prolong the life of both connectors, use a torque wrench (5/16 in) and tighten the connection to the range of 7-10 lb-in (79-112 N-cm) when you connect an SMA cable to a sampling module. For more information, refer to your sampling module user manual**

CAUTION. *Sampling modules are inherently vulnerable to static damage. Always observe static-safe procedures and cautions as outlined in the sampling module user manual.*

Loading Files

The following steps explain how to load files from the DTG5000 Series Data Timing Generator.

1. From the application menu bar, select **File**, and then select **Open Setup**. The Open Setup dialog box appears. See Figure 1-5.
2. Specify **C:\Program Files\Tektronix\DTG5000\PV\DTG5078** (or **C: \Program Files\Tektronix\DTG5000\PV\DTG5274** or **C:\Program Files\Tektronix\DTG5000\PV\DTG5334**) to **Look in** field.

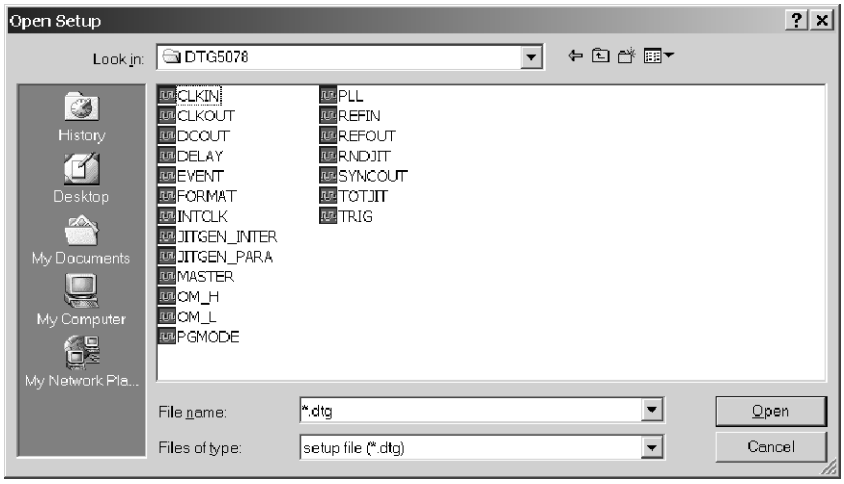
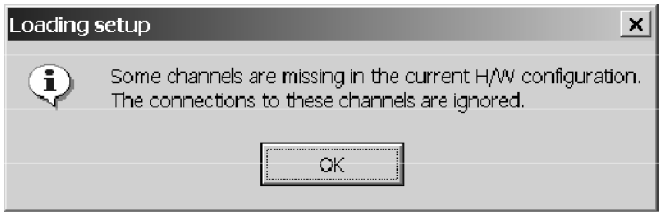


Figure 1-5: Open Setup dialog box

3. Select the necessary file in the **File name:**, and then click **Open**.
4. The Open Setup dialog box automatically disappears, and then the selected waveform and sequence file are loaded.

   If your data timing generator mainframe is not equipped with maximum output module configuration, the following dialog box appears.



5. Click **OK** to complete the instrument setup.

Performance Check Files

Table 1-3 lists the setup files on the internal hard disk drive that are used in these performance tests. A specified file must be loaded each time you execute Performance Test procedure. Test pattern data and setup information are included in the file.

Table 1-3: Performance check files

No.	File name	Clock frequency	Test item
1	SYNCOUT.dtg	Internal: 10 MHz	Sync output
2	INTCLK.dtg	Internal: 100 MHz	Internal clock frequency
3	CLKOUT.dtg	Internal: 10 MHz	External clock output
4	CLKIN.dtg	External clock: 10 MHz	External clock input
5	REFIN.dtg	External reference: 100 MHz	10 MHz reference
6	PLL.dtg	External PLL: 10 MHz	Phase lock input
7	TRIG.dtg	Internal: 3.35 GHz (DTG5334) Internal: 2.7 GHz (DTG5274) Internal: 750 MHz (DTG5078)	Trigger input
8	EVENT.dtg	Internal: 3.35 GHz (DTG5334) Internal: 2.7 GHz (DTG5274) Internal: 750 MHz (DTG5078)	Event input and sequential function
9	JITGEN_INTER.dtg	Internal: 100 MHz	Total jitter
10	JITGEN_PARA.dtg	Internal: 100 MHz	Partial jitter
11	DCOUT.dtg		
12	REFOUT.dtg	Internal: 100 MHz	10 MHz reference output
13	DELAY.dtg		
14	PGMODE.dtg	Internal: 100 MHz	PG mode
15	OM_H.dtg		
16	OM_L.dtg		
17	FORMAT.dtg	Internal: 10 MHz	Data format
18	MASTER.dtg	Internal: 20 MHz	Master-Slave operation
19	RNDJIT.dtg		Random jitter
20	TOTJIT.dtg		Total jitter
21	JITIN.dtg	Internal: 100 MHz	Jitter input
22	INHIBIT.dtg	Internal: 100 MHz	Inhibit control

DTG5000 Series Test Record

Photocopy this test record and use to record the performance test results for your DTG5000 Series Data Timing Generator.

DTG5000 Series Test Record

Instrument Serial Number: _____ Certificate Number: _____
Temperature: _____ RH %: _____
Date of Calibration: _____ Technician: _____

DTG5000 Series Diagnostics and Calibration

Diagnostics	Minimum	Incoming	Outgoing	Maximum
Register	Pass/Fail	----------	----------	Pass/Fail
Clock	Pass/Fail	----------	----------	Pass/Fail
Sequence Memory	Pass/Fail	----------	----------	Pass/Fail
Pattern Memory	Pass/Fail	----------	----------	Pass/Fail
Calibration	**Minimum**	**Incoming**	**Outgoing**	**Maximum**
Level Calibration	Pass/Fail	----------	----------	Pass/Fail
Skew Calibration	Pass/Fail	----------	----------	Pass/Fail

DTG5000 series Performance Verification

Mainframe	Minimum	Incoming	Outgoing	Maximum
Sync Output				
Pulse width (400ns)	Pass/Fail	----------	----------	Pass/Fail
High Level				
Low Level				
Internal Clock Frequency				
DTG5078				
Clock Frequency at 100.00000 MHz	99.999 90 MHz			100.00010 MHz
Clock Frequency at 750.00000 MHz	745.99925 MHz			750.00075 MHz
Clock Frequency at 500.00000 MHz	499.99950 MHz			500.00050 MHz
Clock Frequency at 499.99999 MHz	499.99949 MHz			500.00049 MHz
Clock Frequency at 50.000000 kHz	49.999950 kHz			50.000050 kHz

DTG5000 series Performance Verification

Mainframe	Minimum	Incoming	Outgoing	Maximum
DTG5274 / DTG5334				
Clock Frequency at 100.00000 MHz	99.99990 MHz			100.00010 MHz
Clock Frequency at 3.3500000 GHz	3.34999665 GHz			3.35000335 GHz
Clock Frequency at 2.7000000 GHz	2.699973 GHz			2.7000027 GHz
Clock Frequency at 2.0000000 GHz	1.9999980 GHz			2.0000020 GHz
Clock Frequency at 1.9999999 GHz	1.9999979 GHz			2.0000019 GHz
Clock Frequency at 50.000000 kHz	49.999950 kHz			50.000050 kHz
External Clock Output (These are typical values and provided for user convenience. Not guaranteed.)				
DTG5078				
At 1.000p-p amplitude				
Amplitude (1.000 V_{p-p})	Pass/Fail	----------	----------	Pass/Fail
Aberration (<10%)	Pass/Fail	----------	----------	Pass/Fail
Rise Time and Fall Time (<100 ps)				
At 0.100_{p-p} amplitude				
Amplitude (0.100 V_{p-p})	Pass/Fail	----------	----------	Pass/Fail
Aberration (<10%)	Pass/Fail	----------	----------	Pass/Fail
Rise Time and Fall Time (<85 ps)				
DTG5274				
At 1.000_{p-p} amplitude				
Amplitude (1.000 V_{p-p})	Pass/Fail	----------	----------	Pass/Fail
Aberration (<10%)	Pass/Fail	----------	----------	Pass/Fail
Rise Time and Fall Time (<80 ps)				
At 0.100_{p-p} amplitude				
Amplitude (0.100 V_{p-p})	Pass/Fail	----------	----------	Pass/Fail
Aberration (<10%)	Pass/Fail	----------	----------	Pass/Fail
Rise Time and Fall Time (<70 ps)				
DTG5334				
At 1.000_{p-p} amplitude				
Amplitude (1.000 V_{p-p})	Pass/Fail	----------	----------	Pass/Fail
Aberration (<10%)	Pass/Fail	----------	----------	Pass/Fail
Rise Time and Fall Time (<100 ps)				

DTG5000 series Performance Verification

Mainframe	Minimum	Incoming	Outgoing	Maximum
External Clock Input				
10 MHz, 1 V_{p-p} Clock pattern	Pass/Fail	----------	----------	Pass/Fail
Frequency (10 MHz, 4digits) on the Clock Frequency field of DTG5000 series	Pass/Fail	----------	----------	Pass/Fail
10MHz Reference Input				
100MHz, 1 V_{p-p} Clock pattern	Pass/Fail	----------	----------	Pass/Fail
10MHz Reference Output				
10MHz, 1.2 V_{p-p} Clock pattern at 50 Ω termination	Pass/Fail	----------	----------	Pass/Fail
10MHz, 2.4 V_{p-p} Clock pattern 1 MΩ termination	Pass/Fail	----------	----------	Pass/Fail
Phase Lock Input				
10MHz, 1 V_{p-p} Clock pattern	Pass/Fail	----------	----------	Pass/Fail
20MHz, 1 V_{p-p} Clock pattern	Pass/Fail	----------	----------	Pass/Fail
30MHz, 1 V_{p-p} Clock pattern	Pass/Fail	----------	----------	Pass/Fail
40MHz, 1 V_{p-p} Clock pattern	Pass/Fail	----------	----------	Pass/Fail
Internal Auto Trigger and Trigger Input				
Confirm the displayed waveforms: Ch1 and CH2	Pass/Fail	----------	----------	Pass/Fail
Observe the trigger level change effects	Pass/Fail	----------	----------	Pass/Fail
Change the trigger impedance and observe the waveform	Pass/Fail	----------	----------	Pass/Fail
Observe the trigger level change effects	Pass/Fail	----------	----------	Pass/Fail
Change the trigger level and trigger slope, and then observe the waveform	Pass/Fail	----------	----------	Pass/Fail
Change the trigger source and trigger level, and then observe the waveform	Pass/Fail	----------	----------	Pass/Fail
Change the trigger source and interval, and then observe the waveform	Pass/Fail	----------	----------	Pass/Fail
Change the Interval setting and observe the waveform	Pass/Fail	----------	----------	Pass/Fail

DTG5000 series Performance Verification

Mainframe	Minimum	Incoming	Outgoing	Maximum
Event Input and Sequence Function				
Verify that the oscilloscope displays data pattern such as shown in Figure 1-15	Pass/Fail	----------	----------	Pass/Fail
Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal rising edge on the oscilloscope screen	Pass/Fail	----------	----------	Pass/Fail
Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal falling edge on the oscilloscope screen	Pass/Fail	----------	----------	Pass/Fail
Confirm that the oscilloscope does not trigger	Pass/Fail	----------	----------	Pass/Fail
.Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal falling edge on the oscilloscope screen	Pass/Fail	----------	----------	Pass/Fail
Confirm that the oscilloscope does not trigger	Pass/Fail	----------	----------	Pass/Fail
Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal falling edge on the oscilloscope screen	Pass/Fail	----------	----------	Pass/Fail
Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal falling edge on the oscilloscope screen	Pass/Fail	----------	----------	Pass/Fail
DTG5078 only				
Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal falling edge on the oscilloscope screen	Pass/Fail	----------	----------	Pass/Fail
Each time you push the MANUAL EVENT button on the front panel of DTG5000 series mainframe, the oscilloscope screen is updated with data pattern same as step 12-b	Pass/Fail	----------	----------	Pass/Fail

DTG5000 series Performance Verification

Mainframe	Minimum	Incoming	Outgoing	Maximum
All Jitter Generation				
In the example of Figure 1-17, a 4 ns width jitter appears on the rising and falling edges of every pulse	Pass/Fail	----------	----------	Pass/Fail
Partial Jitter Generation				
Confirm the jitter generation: In the example of Figure 1-18, a 4 ns width jitter appears on the rising and falling edges of one pulse	Pass/Fail	----------	----------	Pass/Fail
DC Output				
DC Level at 3.00 V	2.86 V			3.14 V
Confirm the H Limit	Pass/Fail	----------	----------	Pass/Fail
DC Level				
–3.00 V	–3.14 V			–2.86 V
–2.00 V	–2.11 V			–1.89 V
–1.00 V	–1.08 V			–0.92 V
0.00 V	–0.05 V			0.05 V
2.00 V	1.89 V			2.11 V
3.00 V	2.86 V			3.14 V
4.00 V	3.83 V			4.17 V
5.00 V	4.80 V			5.20 V
Skew and Delay Timing				
Skew Time between channels				
DTG5274 / DTG5334 / DTG5078 (Slots A to D)	----------			100 ps
DTG5078 (Slots A to H)	----------			200 ps
Lead Delay Time accuracy				
DTG5274 / DTG5334 / DTG5078 (Slot A, B, C, and D)	–100 ps			100 ps
DTG5078 (Slot E, F, G, and H)	–150 ps			150 ps
Trail Delay Time accuracy				
DTG5274 / DTG5334 / DTG5078 (Slot A, B, C, and D)	–100 ps			100 ps

DTG5000 series Performance Verification

Mainframe	Minimum	Incoming	Outgoing	Maximum
Clock Out Random Jitter				
Verify that the oscilloscope displays the waveforms as shown in Figure 1-22	Pass/Fail	----------	----------	Pass/Fail
RMS jitter (<3 ps)	Pass/Fail	----------	----------	Pass/Fail
Random Jitter				
Verify that the oscilloscope displays the waveforms as shown in Figure 1-24	Pass/Fail	----------	----------	Pass/Fail
RMS Jitter				
DTG5078 (<4 ps)	Pass/Fail	----------	----------	Pass/Fail
DTG5274 (<3 ps)	Pass/Fail	----------	----------	Pass/Fail
DTG5334 (<3 ps)	Pass/Fail	----------	----------	Pass/Fail
Total Jitter				
Verify that the oscilloscope displays the waveforms as shown in Figure 1-25	Pass/Fail	----------	----------	Pass/Fail
RMS Jitter				
DTG5078 (<18 ps)	Pass/Fail	----------	----------	Pass/Fail
DTG5274 (<16 ps)	Pass/Fail	----------	----------	Pass/Fail
DTG5334 (<15 ps)	Pass/Fail	----------	----------	Pass/Fail
PG Mode				
Verify that 100 MHz square waveform is displayed on the oscilloscope screen	Pass/Fail	----------	----------	Pass/Fail
Verify the PG mode functions	Pass/Fail	----------	----------	Pass/Fail
Verify the CH1 duty	Pass/Fail	----------	----------	Pass/Fail
Verify Slew Rate function (DTGM10 and DTGM20 only)	Pass/Fail	----------	----------	Pass/Fail
Master-Slave Operation				
Confirm that the oscilloscope displays the waveforms such as shown in Figure 1-29	Pass/Fail	----------	----------	Pass/Fail
Verify that the oscilloscope displays the same waveforms as step 4 on the screen	Pass/Fail	----------	----------	Pass/Fail

DTG5000 series Performance Verification

Mainframe	Minimum	Incoming	Outgoing	Maximum
DTG5078 only				
Verify that the oscilloscope displays the same waveforms as step 4 on the screen	Pass/Fail	----------	----------	Pass/Fail

Output Module	Minimum	Incoming	Outgoing	Maximum
Data output DC Level				
DTGM10				
Ch1 High Level Voltage Accuracy				
–1.0 V at Low = –1.5 V	–1.08 V			–0.92 V
0 V at Low = –1.5 V	–0.05 V			0.05 V
1 V at Low = –1.5 V	0.92 V			1.08 V
2 V at Low = –1.5 V	1.89 V			2.11 V
Ch1 Low Level Voltage Accuracy				
–1.0 V at High = 2.0 V	–1.08 V			–0.92 V
0 V at High = 2.0 V	–0.05 V			0.05 V
1 V at High = 2.0 V	0.92 V			1.08 V
1.75 V at High = 2.0 V	1.6475 V			1.8525 V
Ch2 High Level Voltage Accuracy				
–1.0 V at Low = –1.5 V	–1.08 V			–0.92 V
0 V at Low = –1.5 V	–0.05 V			0.05 V
1 V at Low = –1.5 V	0.92 V			1.08 V
2 V at Low = –1.5 V	1.89 V			2.11 V
Ch2 Low Level Voltage Accuracy				
–1.0 V at High = 2.0 V	–1.08 V			–0.92 V
0 V at High = 2.0 V	–0.05 V			0.05 V
1 V at High = 2.0 V	0.92 V			1.08 V
1.75 V at High = 2.0 V	1.6475 V			1.8525 V

Output Module	Minimum	Incoming	Outgoing	Maximum
Ch3 High Level Voltage Accuracy				
–1.0 V at Low = –1.5 V	–1.08 V			–0.92 V
0 V at Low = –1.5 V	–0.05 V			0.05 V
1 V at Low = –1.5 V	0.92 V			1.08 V
2 V at Low = –1.5 V	1.89 V			2.11 V
Ch3 Low Level Voltage Accuracy				
–1.0 V at High = 2.0 V	–1.08 V			–0.92 V
0 V at High = 2.0 V	–0.05 V			0.05 V
1 V at High = 2.0 V	0.92 V			1.08 V
1.75 V at High = 2.0 V	1.6475 V			1.8525 V
Ch4 High Level Voltage Accuracy				
–1.0 V at Low = –1.5 V	–1.08 V			–0.92 V
0 V at Low = –1.5 V	–0.05 V			0.05 V
1 V at Low = –1.5 V	0.92 V			1.08 V
2 V at Low = –1.5 V	1.89 V			2.11 V
Ch4 Low Level Voltage Accuracy				
–1.0 V at High = 2.0 V	–1.08 V			–0.92 V
0 V at High = 2.0 V	–0.05 V			0.05 V
1 V at High = 2.0 V	0.92 V			1.08 V
1.75 V at High = 2.0 V	1.6475 V			1.8525 V
DTGM20				
Ch1 High Level Voltage Accuracy				
–0.9 V at Low = –1.0 V	–1.08 V			–0.92 V
0 V at Low = –1.0 V	–0.05 V			0.05 V
1 V at Low = –1.0 V	0.92 V			1.08 V
2 V at Low = –1.0 V	1.89 V			2.11 V
Ch1 Low Level Voltage Accuracy				
–0.9 V at High = 2.5 V	–1.08 V			–0.92 V
0 V at High = 2.5 V	–0.05 V			0.05 V
1 V at High = 2.5 V	0.92 V			1.08 V
2 V at High = 2.5 V	1.89 V			2.11 V

Output Module	Minimum	Incoming	Outgoing	Maximum
Ch2 High Level Voltage Accuracy				
–0.9 V at Low = –1.0 V	–1.08 V			–0.92 V
0 V at Low = –1.0 V	–0.05 V			0.05 V
1 V at Low = –1.0 V	0.92 V			1.08 V
2 V at Low = –1.0 V	1.89 V			2.11 V
Ch2 Low Level Voltage Accuracy				
–0.9 V at High = 2.5 V	–1.08 V			–0.92 V
0 V at High = 2.5 V	–0.05 V			0.05 V
1 V at High = 2.5 V	0.92 V			1.08 V
2 V at High = 2.5 V	1.89 V			2.11 V
Ch3 High Level Voltage Accuracy				
–0.9 V at Low = –1.0 V	–1.08 V			–0.92 V
0 V at Low = –1.0 V	–0.05 V			0.05 V
1 V at Low = –1.0 V	0.92 V			1.08 V
2 V at Low = –1.0 V	1.89 V			2.11 V
Ch3 Low Level Voltage Accuracy				
–0.9 V at High = 2.5 V	–1.08 V			–0.92 V
0 V at High = 2.5 V	–0.05 V			0.05 V
1 V at High = 2.5 V	0.92 V			1.08 V
2 V at High = 2.5 V	1.89 V			2.11 V
Ch4 High Level Voltage Accuracy				
–0.9 V at Low = –1.0 V	–1.08 V			–0.92 V
0 V at Low = –1.0 V	–0.05 V			0.05 V
1 V at Low = –1.0 V	0.92 V			1.08 V
2 V at Low = –1.0 V	1.89 V			2.11 V
Ch4 Low Level Voltage Accuracy				
–0.9 V at High = 2.5 V	–1.08 V			–0.92 V
0 V at High = 2.5 V	–0.05 V			0.05 V
1 V at High = 2.5 V	0.92 V			1.08 V
2 V at High = 2.5 V	1.89 V			2.11 V

Output Module	Minimum	Incoming	Outgoing	Maximum
DTGM21: Output impedance=23 Ω				
Ch1 High Level Voltage Accuracy				
–1.55 V at Low = –1.65 V	–1.6465 V			–1.4535 V
0.5 V at Low = –1.65 V	0.565 V			0.435 V
2 V at Low = –1.65 V	2.11 V			1.89 V
3.7 V at Low = –1.65 V	3.861 V			3.539 V
Ch1 Low Level Voltage Accuracy				
–1.65 V at High = 3.7 V	–1.7495 V			–1.5505 V
0.5 V at High = 3.7 V	0.565 V			0.435 V
2 V at High = 3.7 V	2.11 V			1.89 V
3.6 V at High = 3.7 V	3.539 V			3.861 V
Ch2 High Level Voltage Accuracy				
–1.55 V at Low = –1.65 V	–1.6465 V			–1.4535 V
0.5 V at Low = –1.65 V	0.565 V			0.435 V
2 V at Low = –1.65 V	2.11 V			1.89 V
3.7 V at Low = –1.65 V	3.861 V			3.539 V
Ch2 Low Level Voltage Accuracy				
–1.65 V at High = 3.7 V	–1.7495 V			–1.5505 V
0.5 V at High = 3.7 V	0.565 V			0.435 V
2 V at High = 3.7 V	2.11 V			1.89 V
3.6 V at High = 3.7 V	3.539 V			3.861 V
Ch3 High Level Voltage Accuracy				
–1.55 V at Low = –1.65 V	–1.6465 V			–1.4535 V
0.5 V at Low = –1.65 V	0.565 V			0.435 V
2 V at Low = –1.65 V	2.11 V			1.89 V
3.7 V at Low = –1.65 V	3.861 V			3.539 V
Ch3 Low Level Voltage Accuracy				
–1.65 V at High = 3.7 V	–1.7495 V			–1.5505 V
0.5 V at High = 3.7 V	0.565 V			0.435 V
2 V at High = 3.7 V	2.11 V			1.89 V
3.6 V at High = 3.7 V	3.539 V			3.861 V

Output Module	Minimum	Incoming	Outgoing	Maximum
Ch4 High Level Voltage Accuracy				
–1.55 V at Low = –1.65 V	–1.6465 V			–1.4535 V
0.5 V at Low = –1.65 V	0.565 V			0.435 V
2 V at Low = –1.65 V	2.11 V			1.89 V
3.7 V at Low = –1.65 V	3.861 V			3.539 V
Ch4 Low Level Voltage Accuracy				
–1.65 V at High = 3.7 V	–1.7495 V			–1.5505 V
0.5 V at High = 3.7 V	0.565 V			0.435 V
2 V at High = 3.7 V	2.11 V			1.89 V
3.6 V at High = 3.7 V	3.539 V			3.861 V
DTGM21: Output impedance = 50 Ω				
Ch1 High Level Voltage Accuracy				
–1.1 V at Low = –1.2 V	–1.183 V			–1.017 V
0 V at Low = –1.2 V	–0.05 V			0.05 V
1.5 V at Low = –1.2 V	1.405 V			1.595 V
2.7 V at Low = –1.2 V	2.569 V			2.831 V
Ch1 Low Level Voltage Accuracy				
–1.2 V at High = 2.7 V	–1.286 V			–1.114 V
0 V at High = 2.7 V	–0.05 V			0.05 V
1.5 V at High = 2.7 V	1.405 V			1.595 V
2.6 V at High = 2.7 V	2.472 V			2.728 V
Ch2 High Level Voltage Accuracy				
–1.1 V at Low = –1.2 V	–1.183 V			–1.017 V
0 V at Low = –1.2 V	–0.05 V			0.05 V
1.5 V at Low = –1.2 V	1.405 V			1.595 V
2.7 V at Low = –1.2 V	2.569 V			2.831 V
Ch2 Low Level Voltage Accuracy				
–1.2 V at High = 2.7 V	–1.286 V			–1.114 V
0 V at High = 2.7 V	–0.05 V			0.05 V
1.5 V at High = 2.7 V	1.405 V			1.595 V
2.6 V at High = 2.7 V	3.539 V			2.728 V

Output Module	Minimum	Incoming	Outgoing	Maximum
Ch3 High Level Voltage Accuracy				
–1.1 V at Low = –1.2 V	–1.183 V			–1.017 V
0 V at Low = –1.2 V	–0.05 V			0.05 V
1.5 V at Low = –1.2 V	1.405 V			1.595 V
2.7 V at Low = –1.2 V	2.569 V			2.831 V
Ch3 Low Level Voltage Accuracy				
–1.2 V at High = 2.7 V	–1.286 V			–1.114 V
0 V at High = 2.7 V	–0.05 V			0.05 V
1.5 V at High = 2.7 V	1.405 V			1.595 V
2.6 V at High = 2.7 V	2.472 V			2.728 V
Ch4 High Level Voltage Accuracy				
–1.1 V at Low = –1.2 V	–1.183 V			–1.017 V
0 V at Low = –1.2 V	–0.05 V			0.05 V
1.5 V at Low = –1.2 V	1.405 V			1.595 V
2.7 V at Low = –1.2 V	2.569 V			2.831 V
Ch4 Low Level Voltage Accuracy				
–1.2 V at High = 2.7 V	–1.286 V			–1.114 V
0 V at High = 2.7 V	–0.05 V			0.05 V
1.5 V at High = 2.7 V	1.405 V			1.595 V
2.6 V at High = 2.7 V	2.472 V			2.728 V
DTGM30				
Ch1 High Level Voltage Accuracy				
–0.97 V at Low = –1.0 V	–1.0491 V			–0.8909 V
0.5 V at Low = -0.75	0.435 V			0.565 V
2.0 V at Low = 1.50 V	1.89 V			2.11 V
2.47 V at Low = 2.44 V	2.3459 V			2.5941 V
Ch1 Low Level Voltage Accuracy				
–1.0 V at High = 0.25 V	–1.08 V			–0.92 V
0.5 V at High = 1.50 V	0.435 V			0.565 V
2.0 V at High = 2.25 V	1.89 V			2.11 V
2.44 V at High = 2.47 V	2.3168 V			2.5632 V

Output Module	Minimum	Incoming	Outgoing	Maximum
Ch2 High Level Voltage Accuracy				
–0.97 V at Low = –1.0 V	–1.0491 V			–0.8909 V
0.5 V at Low = –0.75	0.435 V			0.565 V
2.0 V at Low = 1.50 V	1.89 V			2.11 V
2.47 V at Low = 2.44 V	2.3459 V			2.5941 V
Ch2 Low Level Voltage Accuracy				
–1.0 V at Low = 0.25 V	–1.08 V			–0.92 V
0.5 V at High = 1.50 V	0.435 V			0.565 V
2.0 V at High = 2.25 V	1.89 V			2.11 V
2.44 V at High = 2.47 V	2.3168 V			2.5632 V
DTGM31				
Ch1 High Level Voltage Accuracy				
–0.97 V at Low = –1.0 V	–1.0491 V			–0.8909 V
0.5 V at Low = –0.75 V	0.435 V			0.565 V
2.0 V at Low = 1.50 V	1.89 V			2.11 V
2.47 V at Low = 2.44 V	2.3459 V			2.5941 V
Ch1 Low Level Voltage Accuracy				
–1.0 V at High = 0.25 V	–1.08 V			–0.92 V
0.5 V at High = 1.50 V	0.435 V			0.565 V
2.0 V at High = 2.25 V	1.89 V			2.11 V
2.44 V at High = 2.47 V	2.3168 V			2.5632 V
DTGM32				
Ch1 High Level Voltage Accuracy				
–0.97 V at Low = –1.0 V	–1.0491 V			–0.8909 V
0.5 V at Low = –0.75	0.435 V			0.565 V
2.0 V at Low = 1.50 V	1.89 V			2.11 V
2.47 V at Low = 2.44 V	2.3459 V			2.5941 V
Ch1 Low Level Voltage Accuracy				
–1.0 V at High = 0.25 V	–1.08 V			–0.92 V
0.5 V at High = 1.50 V	0.435 V			0.565 V
2.0 V at High = 2.25 V	1.89 V			2.11 V
2.44 V at High = 2.47 V	2.3168 V			2.5632 V

Output Module	Minimum	Incoming	Outgoing	Maximum
Data Format				
NRZ	Pass/Fail	----------	----------	Pass/Fail
RZ	Pass/Fail	----------	----------	Pass/Fail
R1	Pass/Fail	----------	----------	Pass/Fail

Mainframe

The following procedures check those characteristics that relate to the mainframe that are checked under *Mainframe* in *Specifications*. Refer to page 2-4.

NOTE. *To perform the Performance Tests, at least one output module must be installed in the DTG5000 Series Data Timing Generator mainframe. You can select any slot when you perform the tests even though the descriptions below are assuming the Slot A is used.*

Sync Output

This test verifies that the DTG5000 series mainframe sync output is functional.

Equipment required	One oscilloscope (TDS7154) (item 3) Two 50 Ω SMA coaxial cables (item 6) Two SMA (female)-BNC (male) adapters (item 9)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:
   a. Hook up the oscilloscope:
      - Attach SMA (female)-BNC (male) adapters to the oscilloscope **CH1 input** and **CH2 input** connectors.
      - Connect an SMA coaxial cable from the **CH2** connector of output module, which is in slot A of the DTG5000 series mainframe, to the SMA-BNC adapter (CH2 input of oscilloscope).
      - Connect an SMA coaxial cable from the **SYNC OUT** on the front panel of the DTG5000 series mainframe to the SMA-BNC adapter (CH1 input of the oscilloscope). See Figure 1-6.

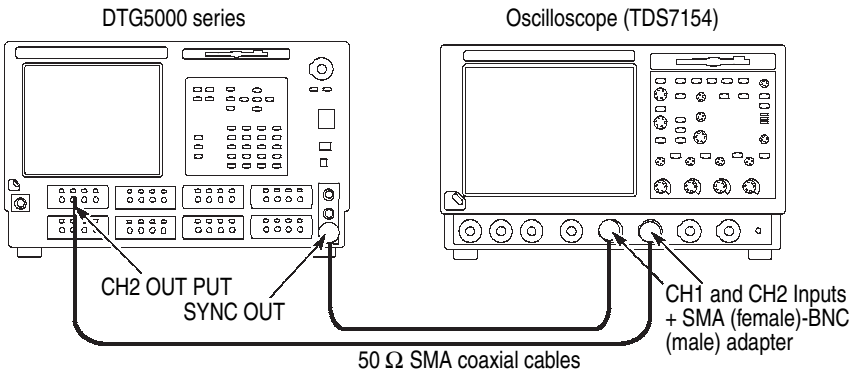


Figure 1-6: Sync output tests

b. Set the oscilloscope controls as follows:

Vertical	
CH1 and CH2 coupling	DC
CH1 scale	100 mV/div
CH2 scale	200 mV/div
CH1 and CH2 input impedance	50 Ω
CH1 offset	–200 mV
Horizontal	
Scale	100 ns/div
Acquisition	
Mode	Average
Number of running averages	32
Trigger	
Source	CH2
Coupling	DC
Slope	Positive
Level	500 mV
Mode	Auto
Measurement	CH1 High CH1 Low

2. Set the data timing generator controls and load the setup file:

a. Load the setup file (SYNCOUT.dtg). Refer to *Loading Files* on page 1-13.

b. After the file is loaded, the **Frequency** of data timing generator is set to 10 MHz.

3. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.
4. Confirm the oscilloscope screen: Verify that the 400 ns width square waveform appears in the CH1 display.
5. Using the oscilloscope Measurement functions, verify that the High Level and Low Level values of Sync Out are as follows:
   - High Level: approximately 0 V
   - Low Level: approximately –0.4 V

Internal Clock Frequency

This test verifies the frequency accuracy of internal clock.

Equipment required	One frequency counter (item 1) One 50 Ω SMA coaxial cable (item 6) One SMA (female)-BNC (male) adapter (item 9) One N (male)-SMA (male) adapter (item 10) One SMA (female)-SMA (female) adapter (item 11)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:

a. Hook up the frequency counter:

- Attach an SMA (female)-BNC (male) adapter to the **CHANNEL 1** input of frequency counter.
- Attach a N (male)-SMA (male) adapter to the **CHANNEL 2** input of frequency counter, and then attach an SMA (female)-SMA (female) adapter to the N-SMA adapter.
- Connect an SMA coaxial cable from the **CLOCK OUT** on the rear panel (DTG5078, DTG5274) or the front panel (DTG5334) through the SMA-BNC adapter to the frequency counter **CHANNEL 1** input. See Figure 1-7.

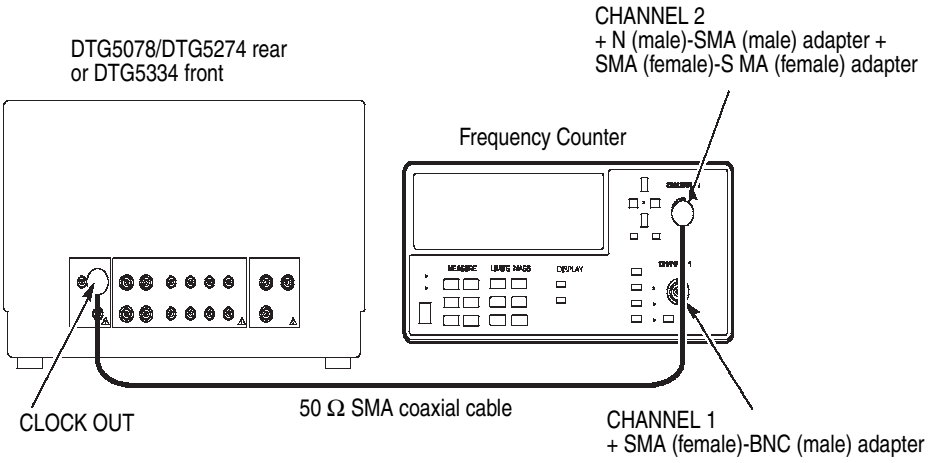


Figure 1-7: Internal clock frequency tests

b. Power on the frequency counter, and verify that the frequency counter is set to frequency measurement mode (default setting).

2. Load the setup file (INTCLK.dtg). Refer to *Loading Files* on page 1-13.
3. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.
4. Set the frequency counter trigger to an appropriate value, and then verify that the frequency counter reading is between 99.9999 MHz and 100.0001 MHz.
5. From the application menu bar, select **Settings**, and then select **Timing**.
6. Move cursor to **Clock Frequency** with the TAB key, and then set frequency counter as follows:

DTG5078

Setup frequency	Range	Frequency counter input
50.000000 kHz	49.999950 kHz to 50.000050 kHz	CHANNEL 1
499.99999 MHz	499.99949 MHz to 500.00049 MHz	CHANNEL 2
500.00000 MHz	499.99950 MHz to 500.00050 MHz	CHANNEL 2
750.00000 MHz	745.99925 MHz to 750.00075 MHz	CHANNEL 2

DTG5274/DTG5334

Setup frequency	Range	Frequency counter input
50.000000 kHz	49.999950 kHz to 50.000050 kHz	CHANNEL 1
1.9999999 GHz	1.9999979 GHz to 2.0000019 GHz	CHANNEL 2
2.0000000 GHz	1.9999980 GHz to 2.0000020 GHz	CHANNEL 2
2.7000000 GHz	2.699973 GHz to 2.7000027 GHz	CHANNEL 2
3.3500000 GHz	3.34999665 GHz to 3.35000335 GHz	CHANNEL 2

7. Verify that the frequency measurements are within the specified range.

NOTE. *For 100 MHz and 50 kHz measurements, connect the SMA coaxial cable to CHANNEL 1 input of the frequency counter. For the other measurements, connect the cable to CHANNEL 2.*

External Clock Output

This test verifies the rise time/fall time and aberration of external clock output.

Equipment required	One sampling oscilloscope with an 80E03 sampling module (item 4) Three 50 Ω SMA coaxial cables (item 6) Two attenuators (item 17)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:

a. Hook up the oscilloscope:

- Attach the attenuator to **CH1 input** and **CH2 input** of the 80E03 sampling module.
- Connect an SMA coaxial cable from the **CLOCK OUT** on the rear panel (DTG5078, DTG5274) or the front panel (DTG5334) to the **CH1 input** of the 80E03 sampling module.
- Connect an SMA coaxial cable from the **CLOCK $\overline{\text{OUT}}$** on the rear panel (DTG5078, DTG5274) or the front panel (DTG5334) to the **CH2 input** of the 80E03 sampling module.
- Connect an SMA coaxial cable from the **SYNC OUT** on the front panel of DTG5000 series mainframe to the **Trigger Direct Input** of sampling oscilloscope. See Figure 1-8.

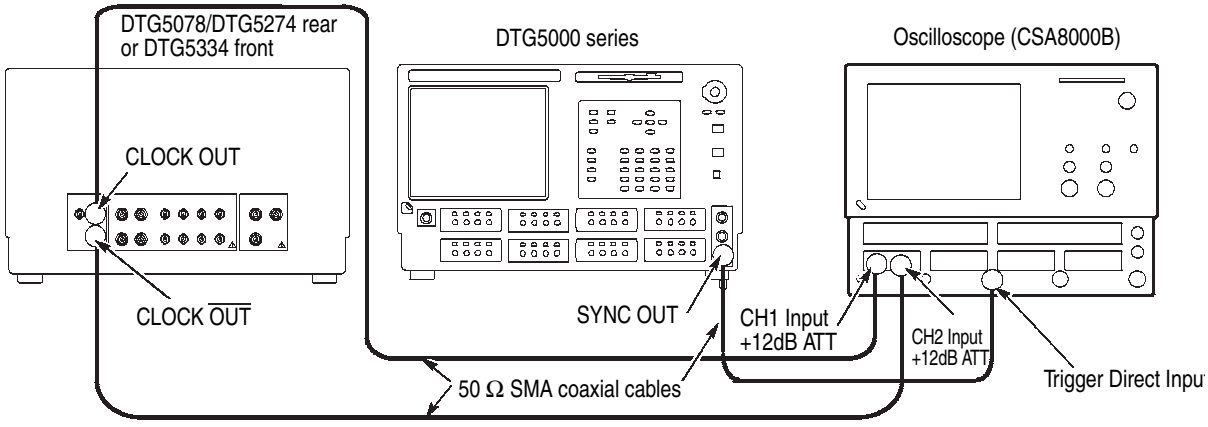


Figure 1-8: External clock output tests

b. Set the oscilloscope controls as follows:

Vertical	
CH1 scale	200 mV/div (with a 12 dB ATT)
CH2 scale	200 mV/div (with a 12 dB ATT) Select **Setup** -> **Vertical** -> **External Attenuation**, then select **12 dB**.
Horizontal	
Scale	2 ns/div
Trigger	
Source	External Direct
Slope	Positive
Level	–200 mV
Measurement	Common to CH1 and CH2
Amplitude	
Positive Overshoot	
Negative Overshoot	
Rise Time	High Ref = 80%, Low Ref = 20%
Fall Time	High Ref = 80%, Low Ref = 20%

2. Load the setup file (CLKOUT.dtg). Refer to *Loading Files* on page 1-13.

3. Push the **RUN** (front) button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** (front) button to activate the output.

4. From the application menu bar, select **Settings**, and then select **Time Base**.

5. Move cursor to **Amplitude** with the TAB key.

6. Set the **Amplitude** values as shown in the following table.

Setup value	Typical value	
Amplitude	Aberration (Positive Overshoot and Negative Overshoot) [3]	Rise Time and Fall Time [3]
1.000 V_{p-p}	<10%	<100 ps (DTG5334) <80 ps (DTG5274) <100 ps (DTG5078)
0.100 V_{p-p}	---	<70 ps (DTG5274) <85 ps (DTG5078)

[3] **These are typical values. Typical specifications are provided for user convenience, but are not guaranteed.**

7. Perform the following measurements for the oscilloscope CH1 input:

   a. Verify the aberration: Confirm that the measurement results are approximately the same as stated in the list by observing the rising and falling edges of displayed waveform while adjusting the horizontal position.

   b. Verify the rise time: Measure the rise time while observing the rising edge. Confirm that the measurement results are approximately the same values as stated in the list.

   c. Verify the fall time: Measure the fall time while observing the falling edge. Confirm that the measurement results are approximately the same values as stated in the list.

   d. Verify the amplitude: Confirm on the oscilloscope screen that the amplitude values are approximately the same level as specified by step **6** above.

8. Repeat the same measurements as **7a** through **7d** for the CH2 input.

External Clock Input

This test verifies the external clock input function and frequency measurement accuracy of the DTG5000 series mainframe.

Equipment required	One sampling oscilloscope with a 80E03 sampling module (item 4) One function generator (item 5) Two 50 Ω SMA coaxial cables (item 6) One 50 Ω BNC coaxial cable (item 7) One SMA (male)-BNC (female) adapter (item 8) One attenuator (item 17)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:

   a. Hook up the oscilloscope and function generator:

   - Attach the attenuator to **CH1 input** of the 80E03 sampling module.
   - Attach an SMA (male)-BNC (female) adapter to the **CLOCK EXTERNAL IN** on the rear panel (DTG5078, DTG5274) or the front panel (DTG5334).
   - Connect a BNC coaxial cable from the front panel **CH1 Out** of function generator to the SMA-BNC adapter (Clock External In).

- Connect an SMA coaxial cable from the **CLOCK OUT** on the rear panel (DTG5078, DTG5274) or the front panel (DTG5334) to the **CH1 input** of the 80E03 sampling module.
- Connect an SMA coaxial cable from the **SYNC OUT** on the front panel of DTG5000 series mainframe to the **Trigger Direct Input** of sampling oscilloscope. See Figure 1-9.

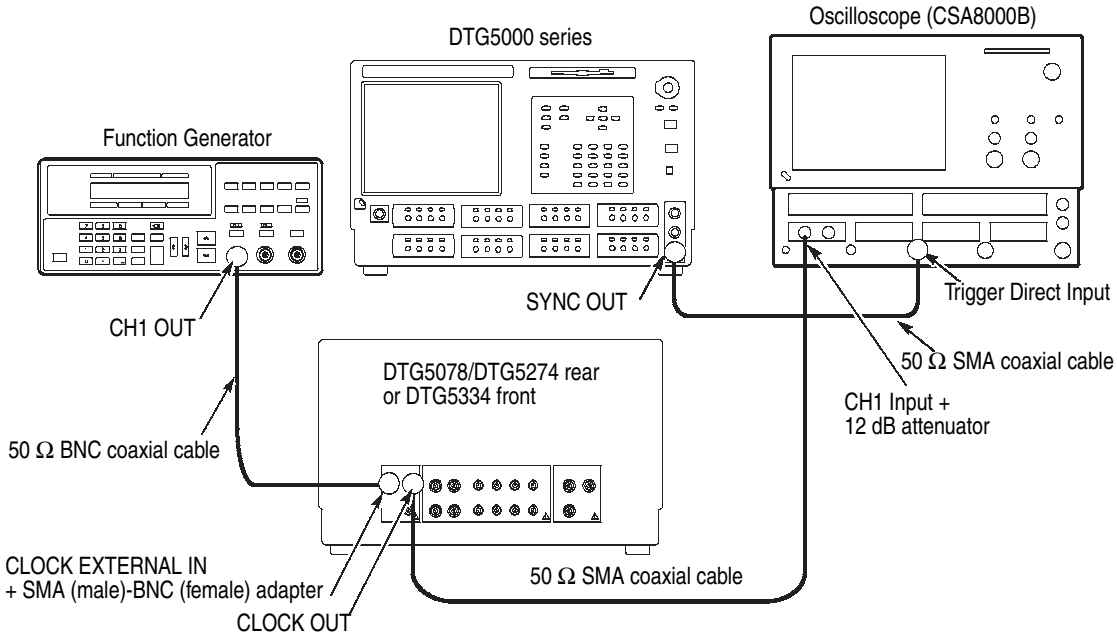


Figure 1-9: External clock input tests

b. Set the oscilloscope controls as follows:

Vertical
- CH1 scale . . . . . 200 mV/div (with a 12 dB ATT) Select **Setup** -> **Vertical** -> **External Attenuation**, then select **12 dB**.

Horizontal
- Scale . . . . . 50 ns/div

Trigger
- Source . . . . . External Direct
- Slope . . . . . Positive
- Level . . . . . –0.2 V

c. Set the function generator controls:

Output channel	CH1
Function	Square
Parameters	
Frequency	10 MHz
Amplitude	1.0 V into 50 Ω
Offset	0 mV
Output	Off

2. Load the setup file (CLKIN.dtg). Refer to *Loading Files* on page 1-13.

3. Turn the function generator **Output** on.

4. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

5. Verify the displayed waveform: A 10 MHz, approximately 1 V_{p-p} clock pattern is displayed on the oscilloscope screen.

6. Verify the frequency: Push the **TIMING** button on the front panel of DTG5000 series mainframe and verify that 10.00 MHz (four digits) is displayed at the **Clock Frequency** field.

10 MHz Reference Input

This test verifies that the 10 MHz reference input of the DTG5000 series mainframe is functional.

Equipment required	One oscilloscope (TDS7154) (item 3) One function generator (item 5) Two BNC coaxial cables (item 7) One SMA (male)-BNC (female) adapter (item 8)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:
   a. Hook up the oscilloscope and function generator:
      - Use an SMA (male)-BNC (female) adapter and a BNC coaxial cable to connect the **CLOCK OUT** on the rear panel (DTG5078, DTG5274) or the front panel (DTG5334) and the **CH1 input** of oscilloscope.
      - Connect a BNC coaxial cable from the **CH1 Out** on the front panel of function generator to the **EXTERNAL 10MHz REF IN** on the rear panel of DTG5000 series mainframe. See Figure 1-10.

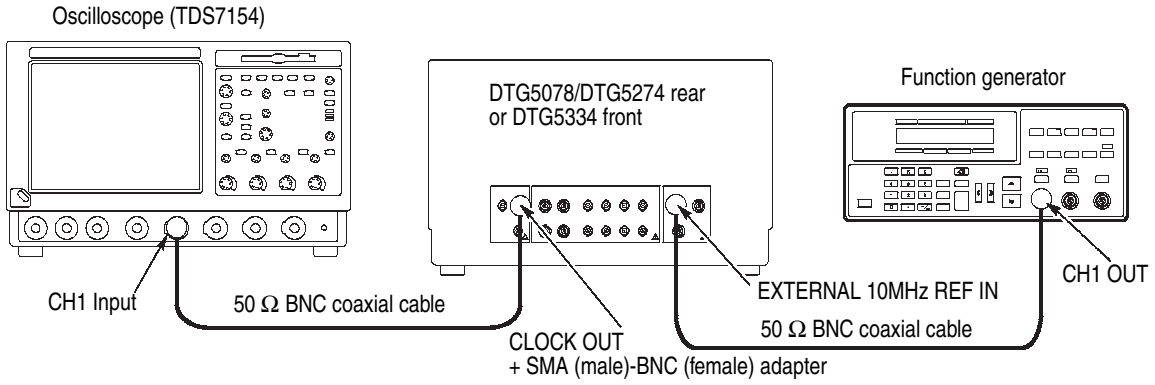


Figure 1-10: 10 MHz reference input tests

b. Set the oscilloscope controls as follows:

Vertical	CH1
CH1 scale	500 mV/div
CH1 input impedance	50 Ω
Horizontal	
Scale	10 ns/div
Trigger	
Source	CH1
Slope	Positive
Level	+0.5 V

c. Set the function generator controls:

Output channel	CH1
Function	Square
Parameters	
Frequency	10 MHz
Amplitude	1.0 V into 50 Ω
Offset	0 mV

2. Load the setup file (REFIN.dtg). Refer to *Loading Files* on page 1-13.

3. Turn the function generator **Output** on.

4. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

5. Verify the displayed waveform: A 100 MHz, approximately 1 V_{p-p} clock pattern is displayed on the oscilloscope screen.

10 MHz Reference Output

This test verifies that the 10 MHz reference output of the DTG5000 series mainframe is functional.

Equipment required	One oscilloscope (TDS7154) (item 3) One BNC coaxial cable (item 7)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:

   a. Hook up the oscilloscope:

      - Connect a BNC coaxial cable from the **10 MHz REF OUT** on the rear panel of DTG5000 series mainframe to the CH1 input of oscilloscope. See Figure 1-11.

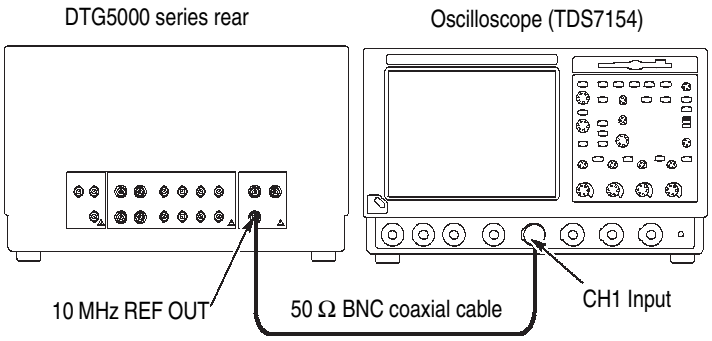


Figure 1-11: 10 MHz reference output tests

   b. Set the oscilloscope controls as follows:

Vertical	CH1
CH1 scale	500 mV/div
CH1 input impedance	50 Ω
CH1 offset	0.6 V
Horizontal	
Scale	50 ns/div
Trigger	
Source	CH1
Slope	Positive
Level	0.5 V

2. Load the setup file (REFOUT.dtg). Refer to *Loading Files* on page 1-13.

3. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

4. Verify the displayed waveform: A 10 MHz, approximately 1.2 V_{p-p} clock pattern is displayed on the oscilloscope screen.

5. Modify the oscilloscope setting and verify the displayed waveform:

   a. Change the CH1 impedance setting of oscilloscope to **1 MΩ**.

   b. Verify that the amplitude of the clock pattern changes to approximately 2.4 V_{p-p}.

Phase Lock Input

This test verifies that the phase lock input of the DTG5000 series mainframe is functional.

Equipment required	One oscilloscope (TDS7154) (item 3) One function generator (item 5) Two BNC coaxial cables (item 7) One SMA (male)-BNC (female) adapter (item 8)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:
   a. Hook up the oscilloscope and function generator:
      - Connect a BNC coaxial cable from the **CH1 Out** on the front panel of function generator to the **PHASE LOCK IN** on the rear panel of DTG5000 series mainframe.
      - Use an SMA (male)-BNC (female) adapter and a BNC coaxial cable to connect the **CLOCK OUT** on the rear panel (DTG5078, DTG5274) or the front panel (DTG5334) and the oscilloscope **CH1 input**. See Figure 1-12.

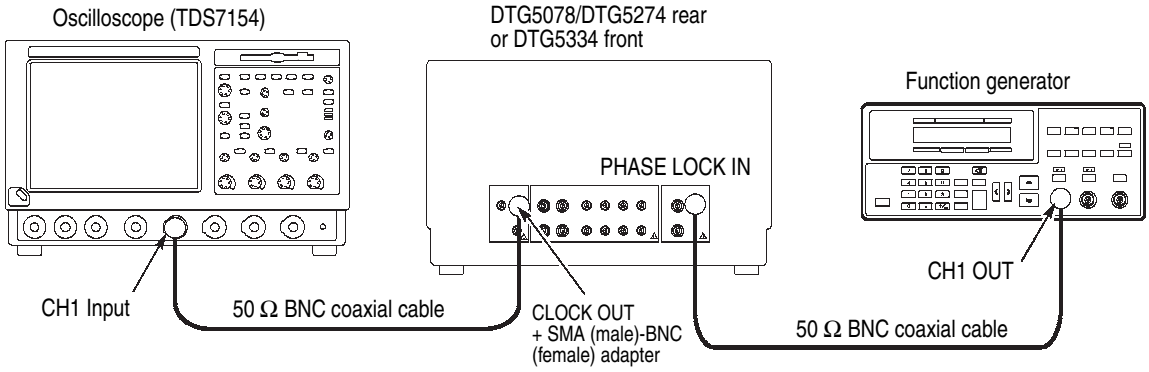


Figure 1-12: Phase lock input tests

b. Set the oscilloscope controls as follows:

Vertical	CH1
CH1 scale	200 mV/div
CH1 input impedance	50 Ω
Horizontal	
Scale	50 ns/div
Trigger	
Source	CH1
Slope	Positive
Level	+0.5 V

c. Set the function generator controls:

Output channel	CH1
Function	Square
Parameters	
Frequency	10.0 MHz
Amplitude	1.0 V into 50 Ω
Offset	0 mV
Output	Off

2. Load the setup file (PLL.dtg). Refer to *Loading Files* on page 1-13.

3. Turn the function generator **Output** on.

4. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

5. Verify the displayed waveform: A 10 MHz, 1 V_{p-p} clock pattern is displayed on the oscilloscope screen.

6. Observe the clock pattern change:

a. From the application menu bar of DTG5000 series mainframe, select **Settings**, and then select **Timing**.

b. Move cursor to **Clock Frequency** with the TAB key.

c. Change the **Clock Frequency** to 20 MHz, 30 MHz, and 40 MHz in this sequence.

d. Verify the displayed waveform on the oscilloscope screen:
A 10 MHz, 1 V_{p-p} clock pattern is changed to 20 MHz, 30 MHz, and 40 MHz in response to the clock frequency change.

Internal Auto Trigger and Trigger Input

This test verifies that the internal trigger is functional.

Equipment required	One oscilloscope (TDS7154) (item 3) One function generator (item 5) Three BNC coaxial cables (item 7) One SMA (male)-BNC (female) adapter (item 8)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:

a. Hook up the oscilloscope and function generator:

- Connect a BNC coaxial cable from the **CH1 OUT** on the front panel of function generator to the **TRIGGER IN** on the front panel of DTG5000 series mainframe.
- Connect a BNC coaxial cable from the **CH2 OUT** on the front panel of function generator to the **CH2 input** of oscilloscope
- Use an SMA (male)-BNC (female) adapter and a BNC coaxial cable to connect the **SYNC OUT** on the front panel of DTG5000 series mainframe and the **CH1 input** of oscilloscope. See Figure 1-13.

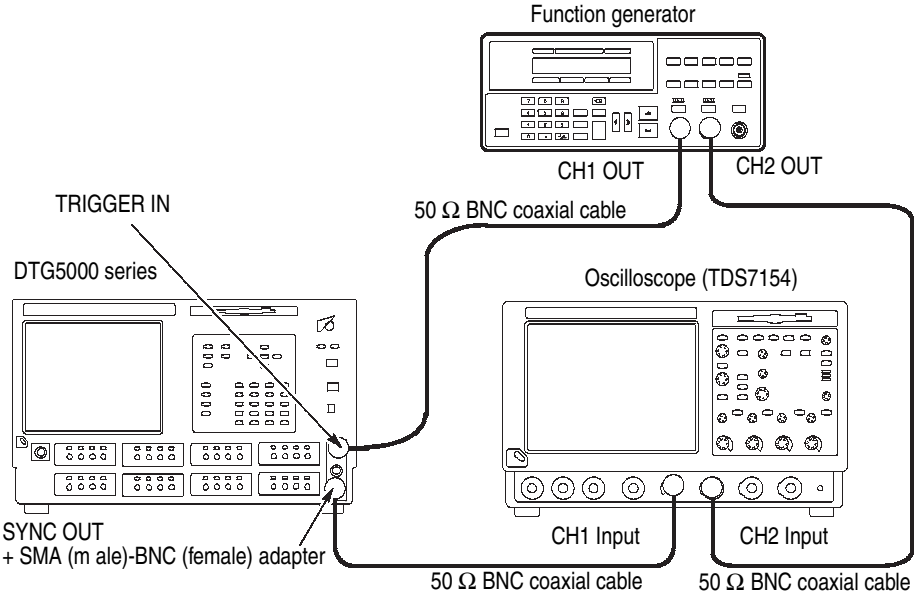


Figure 1-13: Internal trigger tests

b. Set the oscilloscope controls as follows:

Vertical	
CH1 scale	200 mV/div
CH2 scale	1 V/div
CH1 and CH2 input impedance	50 Ω
Horizontal	
Scale	200 ns/div
Acquisition	
Mode	Peak Detect
Trigger	
Source	CH2
Mode	Normal
Slope	Positive
Level	0.5 V

c. Set the function generator controls:

Output channel	CH1, CH2
Function	Square (CH1, CH2)
Parameters	
Frequency	1 MHz (CH1, CH2)
Amplitude	1.0 V into 50 Ω (CH1, CH2)
Offset	0.5 V (CH1, CH2)
BOTH CH	Press **SHIFT** key, then press **CH**.

2. Load the setup file (TRIG.dtg). Refer to *Loading Files* on page 1-13.

3. Turn the function generator CH1 and CH2 Outputs **on**.

4. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

5. Confirm the displayed waveforms: Verify that an approximately 0.4 V_{p-p} amplitude pulse waveform is generated from CH 1 every 1.00 μs synchronizing with CH2 signal rising edge on the oscilloscope screen.

6. Observe the trigger level change effects:

a. From the application menu bar of DTG5000 series mainframe, select **Settings** and then select **Time Base**.

b. Move cursor to **Trigger Level** with the TAB key and set the trigger level to +1.1 V.

c. Verify that the CH1 pulse signal disappears from the oscilloscope screen and that the data timing generator screen message changes to **Waiting Trigger**.

7. Change the trigger impedance and observe the waveform:

a. From the application menu bar of DTG5000 series mainframe, select **Settings**, and then select **Time Base**.

b. Move cursor to **Trigger Impedance** with the TAB key and set the trigger impedance to **1 kΩ**.

c. Verify that an approximately 0.4 V_{p-p} amplitude pulse waveform is generated from CH 1 every 1.00 µs synchronizing with CH2 signal rising edge on the oscilloscope screen.

8. Observe the trigger level change effects:

a. From the application menu bar of DTG5000 series mainframe, select **Settings** and then select **Time Base**.

b. Move cursor to **Trigger Level** with the TAB key and set the trigger level to –0.4 V.

c. Verify that the CH1 pulse signal disappears from the oscilloscope screen and that the data timing generator screen message changes to **Waiting Trigger**.

9. Change the trigger level and trigger slope, and then observe the waveform:

a. From the application menu bar of DTG5000 series mainframe, select **Settings** and then select **Time Base**.

b. Move cursor to **Trigger Level** and **Trigger Slope** with TAB key. Set the trigger level to +1.0 V and trigger slope to **Negative**.

c. Confirm the displayed waveform: Verify that an approximately 0.4 V_{p-p} amplitude pulse waveform is generated from CH 1 every 1.00 µs synchronizing with CH2 signal falling edge on the oscilloscope screen.

10. Turn the function generator CH1 and CH2 Outputs **off**.

11. Change the trigger source and trigger level, and then observe the waveform:

a. Set the oscilloscope trigger source to **CH1** and trigger level to **–0.2 V**.

b. Confirm the displayed waveform: Each time you push the **MANUAL TRIGGER** button on the front panel of DTG5000 series mainframe, the oscilloscope screen is updated with a pulse waveform.

12. Push the **RUN** button of the data timing generator to turn the RUN LED off.

13. Change the trigger source and interval, and then observe the waveform:

a. From the application menu bar of DTG5000 series mainframe, select **Settings** and then select **Time Base**.

b. Move cursor to **Trigger Source** with the TAB key and set to **Internal**.

c. Set the **Interval** to 1.00 µs.

d. Push the **RUN** button of the data timing generator to light the RUN LED.

e. Verify that an approximately 0.4 V_{p-p} amplitude pulse waveform is generated every 1.00 µs on the oscilloscope screen.

14. Change the Interval setting and observe the waveform:

a. Change the **Interval** from 1.00 µs to 1.00 ms.

b. Change the horizontal scale of the oscilloscope from 200 ns/div to **200 µs/div**.

c. Verify that an approximately 0.4 V_{p-p} amplitude pulse waveform is generated every 1.00 ms on the oscilloscope screen.

Event Input and Sequence Function

This test verifies that the event input and sequence of the DTG5000 series mainframe are functional.

Equipment required	One oscilloscope (TDS7154) (item 3) One function generator (item 5) One 50 Ω SMA coaxial cable (item 6) Three 50 Ω BNC coaxial cables (item 7) One SMA (female)-BNC (male) adapter (item 9) One BNC-T connector (item 14)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:
   a. Hook up the oscilloscope and function generator:
      - Attach a BNC-T connector to the **CH3 input** of the oscilloscope.
      - Connect a BNC coaxial cable from the **CH1 Out** of function generator to the **CH3 input** of the oscilloscope (through BNC-T connector).
      - Connect a second BNC coaxial cable to the **EVENT IN** on the front panel of DTG5000 series mainframe, and then connect the opposite end of the cable to the **CH3 input** of the oscilloscope (through BNC-T connector).
      - Connect a third BNC coaxial cable from the **JUMP OUT1** on the rear panel of DTG5000 series mainframe to the **CH2 input** of oscilloscope.
      - Attach an SMA (female)-BNC (male) adapter to the oscilloscope **CH1 input** connector.
      - Connect an SMA coaxial cable from the **CH1** connector of the output module, which is in slot A of the DTG5000 series mainframe, to the SMA-BNC adapter (CH1 input of the oscilloscope).
        See Figure 1-14.

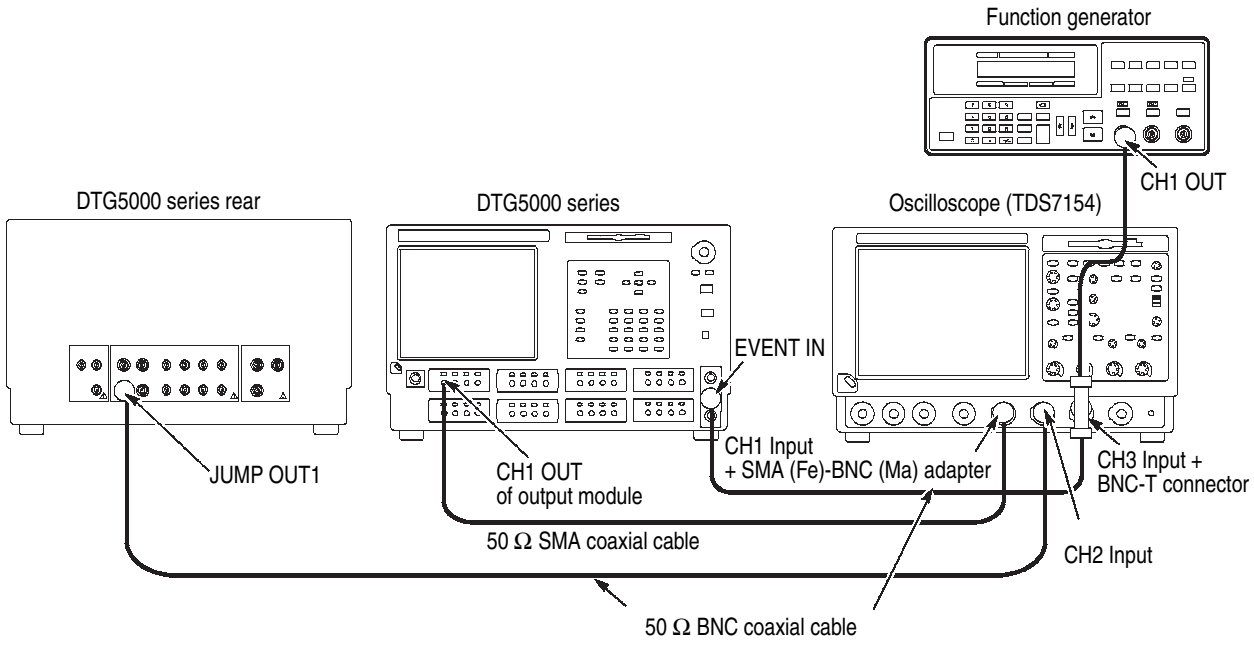


Figure 1-14: Event input and sequence tests

b. Set the oscilloscope controls as follows:

Vertical	
CH1 and CH3 scale	1 V/div
CH2 scale	2 V/div
CH1 input impedance	50 Ω
CH2 and CH3 input impedance	1 MΩ
Horizontal	
Scale	200 ns/div
Acquisition	
Mode	Peak Detect
Sequence	RUN/STOP button Only
Trigger	
Source	CH3
Mode	Normal
Slope	Positive
Level	+0.5 V
Coupling	DC
Position	50%

c. Set the function generator controls:

Output channel	CH1
Function	Square (CH1)
Parameters	
Frequency	500 Hz (CH1)
Amplitude	1.0 V into 50 Ω (CH1)
Offset	0.5 V (CH1)

2. Load the setup file (EVENT.dtg). Refer to *Loading Files* on page 1-13.

3. Turn the function generator **Output** on.

4. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

5. Verify that the oscilloscope displays data pattern such as shown in Figure 1-15.

NOTE. *The CH1 and CH2 signals appear to have jitters. The DTG5274 and DTG5334 has 120 clocks width jitter and the DTG5078 has 30 clocks width jitter compared to CH3 trigger signal.*

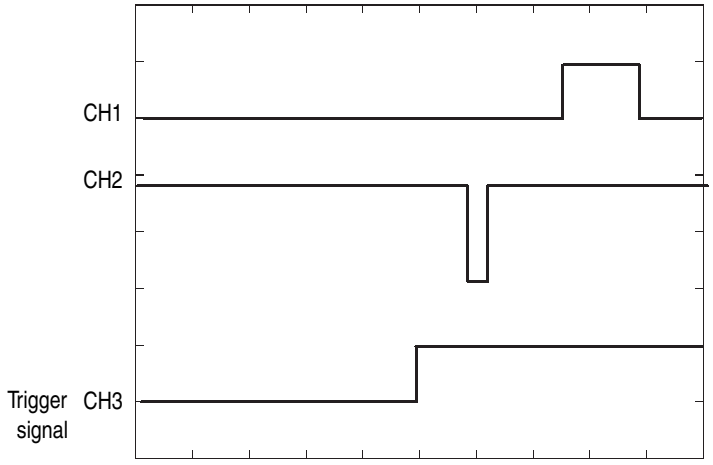


Figure 1-15: Data pattern example

6. Verify the waveform after changing the **trigger source** and **trigger level** settings of the oscilloscope:

   a. Set the trigger source to **CH2** and the trigger level to **+1.4 V**.

   b. Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal rising edge on the oscilloscope screen.

7. Change the DTG5000 series mainframe settings and verify the waveform:

   a. From the application menu bar of DTG5000 series mainframe, select **Settings** and then select **Time Base**.

   b. Set the **Event Input Polarity** to **Invert**.

   c. Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal falling edge on the oscilloscope screen.

8. Change the DTG5000 series mainframe settings and verify that the oscilloscope untriggered:

   a. From the application menu bar of DTG5000 series mainframe, select **Settings** and then select **Time Base**.

   b. Set the **Event Input Threshold** to **+1.1 V**.

   c. Confirm that the oscilloscope does not trigger.

9. Change the DTG5000 series mainframe settings and verify the waveform:

   a. From the application menu bar of DTG5000 series mainframe, select **Settings** and then select **Time Base**.

   b. Set the **Event Input Impedance** to **1 kΩ.**

   c. Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal falling edge on the oscilloscope screen.

10. Change the DTG5000 series mainframe settings and verify that the oscilloscope untriggered:

    a. From the application menu bar of DTG5000 series mainframe, select **Settings** and then select **Time Base**.

    b. Set the **Event Input Threshold** to **–0.4 V**.

    c. Confirm that the oscilloscope does not trigger.

11. Change the DTG5000 series mainframe settings and verify the waveform:

a. From the application menu bar of DTG5000 series mainframe, select **Settings** and then select **Time Base**.

b. Set the **Event Input Threshold** to **+ 1.0 V**.

c. Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal falling edge on the oscilloscope screen.

12. Connect the cable to Jump Out2 and verify the displayed waveform:

a. Disconnect the BNC cable from the **JUMP OUT1** and then connect it to the **JUMP OUT2** on the rear panel of DTG5000 series mainframe.

b. Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal falling edge on the oscilloscope screen.

13. (DTG5078 only) Connect the cable to Jump Out3 and verify the displayed waveform:

a. Disconnect the BNC cable from the **JUMP OUT2** and then connect it to the **JUMP OUT3** on the rear panel of DTG5000 series mainframe.

b. Verify that an approximately 3.3 V_{p-p} amplitude low pulse waveform is generated from CH 2 synchronizing with CH3 signal falling edge on the oscilloscope screen.

14. Turn the function generator **Output** off.

15. Each time you push the **MANUAL EVENT** button on the front panel of DTG5000 series mainframe, the oscilloscope screen is updated with data pattern same as step **12–b**. Ignore the CH3 waveform.

All Jitter Generation

This test verifies that the all jitter generation is functional. This function is provided with the slot A CH1. While using this function, the slot A CH2 is in high impedance status.

Equipment required	One oscilloscope (TDS7154) (item 3) Two 50 Ω BNC coaxial cables (item 7) Two SMA (male)-BNC (female) adapters (item 8)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:
   a. Hook up the oscilloscope:
      - Attach an SMA (male)-BNC (female) adapter to the **CH1** connector of the output module, which is in slot A of the DTG5000 series mainframe.
      - Attach an SMA (male)-BNC (female) adapter to the **SYNC OUT** on the front panel of DTG5000 series mainframe.
      - Connect a BNC coaxial cable from the SMA-BNC adapter of output module to the **CH1 input** of oscilloscope.
      - Connect a BNC coaxial cable from the **SYNC OUT** (SMA-BNC adapter) on the front panel of DTG5000 series mainframe to the **CH2 input** of oscilloscope. See Figure 1-16.

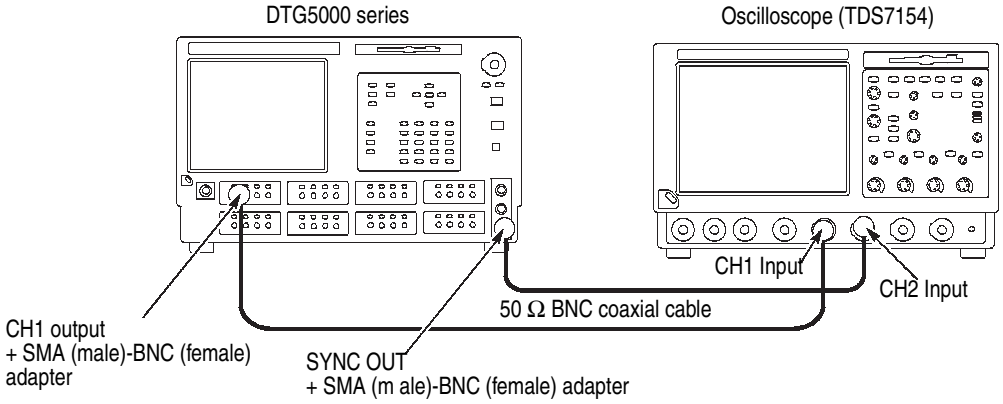


Figure 1-16: Jitter generation tests

b. Set the oscilloscope controls as follows:

Vertical
- CH1 and CH2 scale . . . . . 500 mV/div
- CH1 and CH2 impedance . . . . . 50 Ω

Horizontal
- Scale . . . . . 10 ns/div

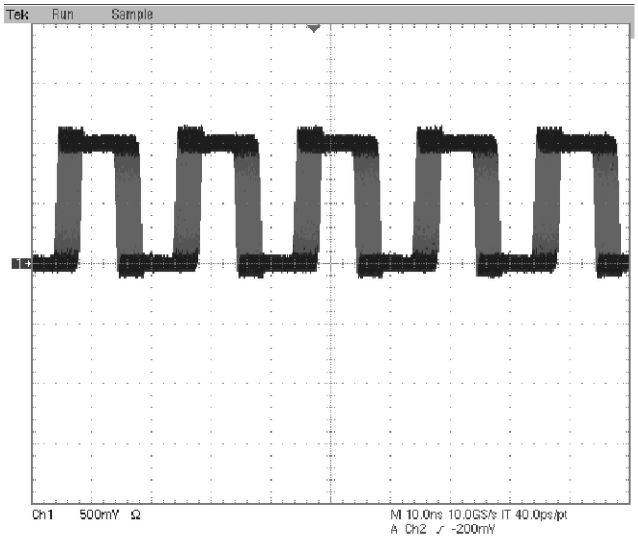
Trigger
- Source CH2
- Slope . . . . . Positive
- Level . . . . . –0.2 V

Display . . . . . Infinite Persistence

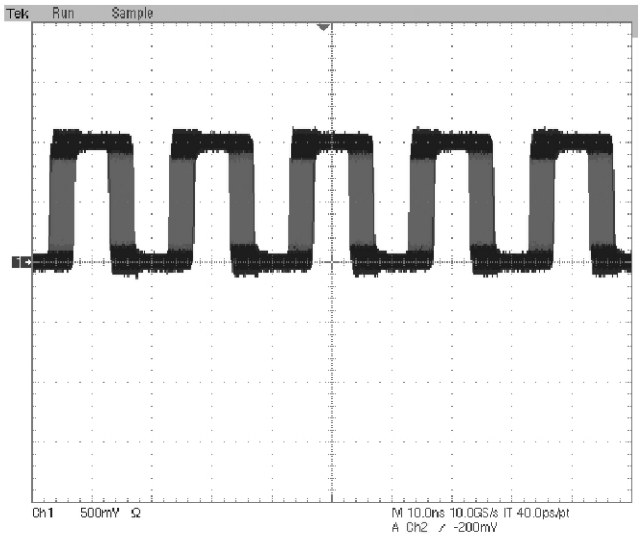
2. Load the setup file (JITGEN_INTER.dtg). Refer to *Loading Files* on page 1-13.

3. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

4. Confirm the jitter generation: In the example of Figure 1-17, a 4 ns width jitter appears on the rising and falling edges of every pulse.



DTG5078



DTG5274

Figure 1-17: Jitter generation example (all)

Partial Jitter Generation

This test verifies that the partial jitter generation is functional. This function is provided with the slot A CH1. While using this function, the slot A CH2 is in high impedance status.

Equipment required	One oscilloscope (TDS7154) (item 3) Two 50 Ω BNC coaxial cables (item 7) Two SMA (male)-BNC (female) adapters (item 8)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:

a. Hook up the oscilloscope:

- Attach an SMA (male)-BNC (female) adapter to the **CH1** connector of the output module, which is in slot A of the DTG5000 series mainframe.
- Attach an SMA (male)-BNC (female) adapter to the **SYNC OUT** on the front panel of DTG5000 series mainframe.
- Connect a BNC coaxial cable from the SMA-BNC adapter of output module to the **CH1 input** of oscilloscope.
- Connect a BNC coaxial cable from the **SYNC OUT** (SMA-BNC adapter) on the front panel of DTG5000 series mainframe to the **CH2 input** of oscilloscope. See Figure 1-16 on page 1-53.

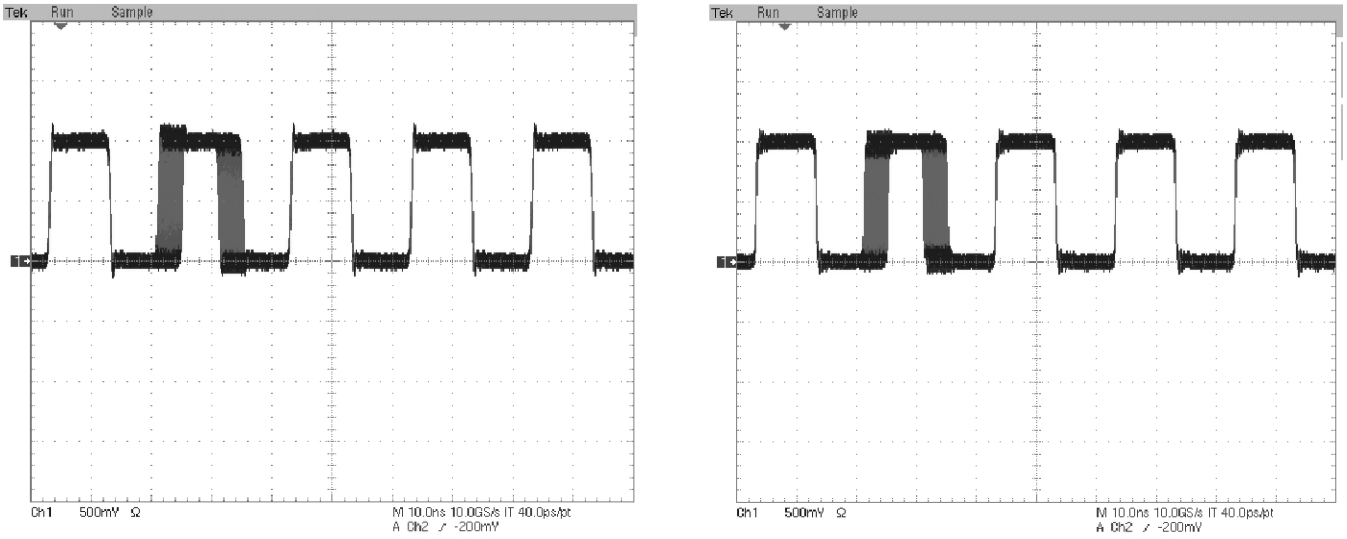
b. Set the oscilloscope controls as follows:

Vertical
- CH1 and CH2 scale . . . . . 500 mV/div
- CH1 and CH2 impedance . . . . . 50 Ω Horizontal
- Scale . . . . . 10 ns/div

Trigger
- Source CH2
- Slope . . . . . Positive
- Level . . . . . –0.2 V
- Position . . . . . Set to10%

Display . . . . . Infinite Persistence

2. Load the setup file (JITGEN_PARA.dtg). Refer to *Loading Files* on page 1-13.
3. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.
4. Press the Set Level to 50% on the oscilloscope.
5. Confirm the jitter generation: In the example of Figure 1-18, a 4 ns width jitter appears on the rising and falling edges of one pulse.



DTG5078 DTG5274

Figure 1-18: Jitter generation example (partial)

DC Output

This test verifies the DC output accuracy.

Equipment required	One digital multimeter (item 2) Lead set for DC output (item 12)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Attach the DC output lead set to the **DC output** connector at the front right side of DTG5000 series mainframe. See Figure 1-19.

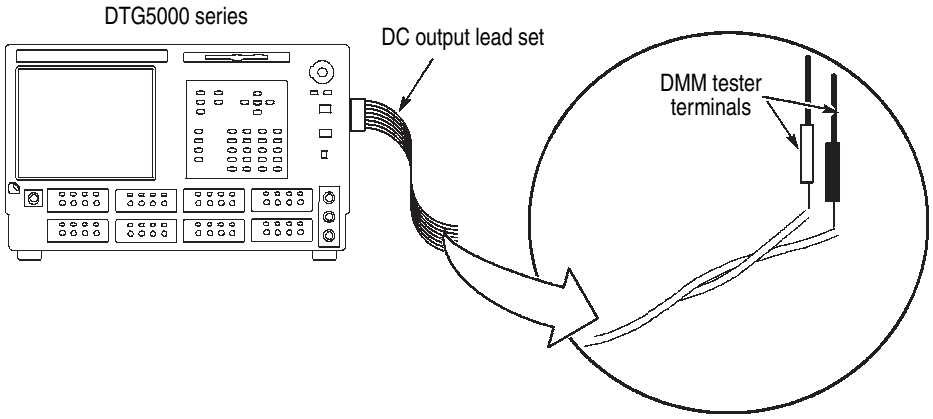


Figure 1-19: DC output tests

2. Set the digital multi meter controls:

   Mode . . . . . Direct Voltage
   Range . . . . . Auto

3. Load the setup file (DCOUT.dtg). Refer to *Loading Files* on page 1-13.
4. From the application menu bar, select **Settings**, and then select **DC Output**.
5. Move cursor to **Output On** box, and click the box to activate it.

6. Measure the potential difference for every channel:

   a. Touch the DMM tester terminal to the metallic exposed pin of DC output lead set. The lead set is composed of eight twisted lines and each line has the one pin holder at the tip.

NOTE. *Every channel is colored by its own color, for example CH1 is colored brown and CH5 is colored green. Touch the DMM tester terminal to the one channel color lead and then touch another tester terminal to the corresponding gray lead.*

   b. Verify that all the measurement results are between 0.92 V and 1.08 V.

7. Perform the same measurements as step 6–**a** while changing the Level as shown in the following table:

Level	DMM Range
–3.00 V	–3.14 V to –2.86 V
–2.00 V	–2.11 V to –1.89 V
–1.00 V	–1.08 V to –0.92 V
0.00 V	–0.05 V to 0.05 V
2.00 V	1.89 V to 2.11 V
3.00 V	2.86 V to 3.14 V
4.00 V	3.83 V to 4.17 V
5.00 V	4.80 V to 5.20 V

8. Verify that the DMM readings are within the specified range.

Skew and Delay Timing

This test verifies that the skew and delay timing of the DTG5000 series mainframe are functional.

Equipment required	One sampling oscilloscope with an 80E03 sampling module (item 4) Two 50 Ω SMA coaxial cables (item 6) One SMA termination (item 16, DTGM30 only) One attenuator (item 17)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11. You must perform both the level and skew calibration before starting this test.

1. Install the test hookup and preset the instrument controls:

a. Hook up the oscilloscope:

- Attach an attenuator to **CH1 input** of the 80E03 sampling module.
- Connect an SMA coaxial cable from the **CH1** connector of output module, which is in slot A of the DTG5000 series mainframe, to the **CH1 input** of the 80E03 sampling module.
- Connect an SMA coaxial cable from the **SYNC OUT** on the front panel of DTG5000 series mainframe to the **Trigger Direct Input** of sampling oscilloscope. See Figure 1-20.
- (DTGM30, DTGM31, and DTGM32): If your output module is DTGM30, DTGM31, or DTGM32, attach an SMA termination to the **$\overline{\text{CH1}}$** connector of output module.

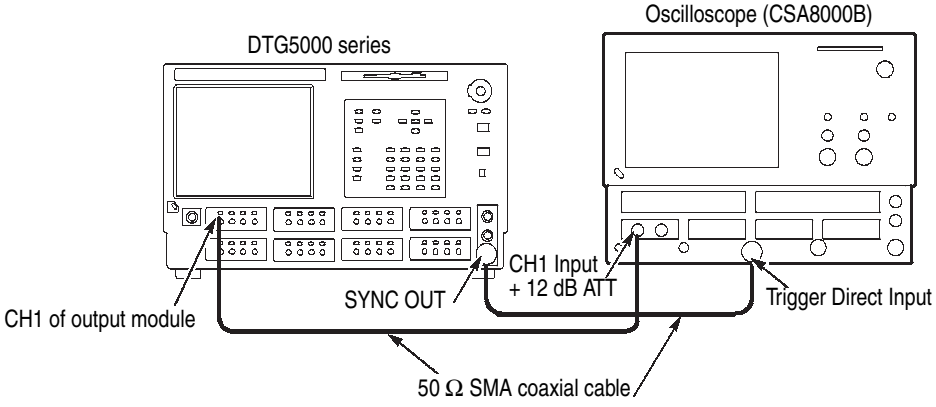


Figure 1-20: Delay timing tests

b. Set the oscilloscope controls as follows:

Vertical	
CH1 scale	200 mV/div (with a 12 dB ATT) Select **Setup** -> **Vertical** -> **External Attenuation**, then select **12 dB.**
Horizontal	
Scale	100 ps/div
Acquisition	
Mode	Average
Number of running averages	32
Trigger	
Source	External Direct
Slope	Positive
Level	Set to 50%
Measurement	
Delay Time	
Select Meas	R1 (+) to C1 (+) Delay
Reference	Absolute + 500 mV (R1, C1)

2. Load the setup file (FORMAT.dtg). Refer to *Loading Files* on page 1-13.

3. Verify that the **View by Channel** is selected in the View menu of data timing generator.

4. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** to activate the output.

5. Adjust the oscilloscope position controls so the waveform is centered on the screen.

6. Do the following substeps:

a. Save the CH1 waveform of oscilloscope to Ref 1.

b. (DTGM10, DTGM20, and DTGM21): Disconnect the SMA cable from the **CH1** connector of the output module, and then connect it to CH2, CH3, and CH4 of output module that installed in the slot A.

(DTGM30 only): Disconnect the SMA cable from the **CH1** of the output module, and then connect it to **CH2** of the module that installed in the slot A. Remove the SMA termination from the $\overline{\textbf{CH1}}$ and attach it to $\overline{\textbf{CH2}}$.

c. Record the **R1C1 Delay** measurement values.

d. Repeat substeps b and c (measurements relative to channel 1 of slot A) for all channels of all slots.

e. (DTG5078, DTG5274, and DTG5334) Calculate the difference between the maximum and minimum R1C1 values for all channels of slots A to D, including 0 ps as the value for slot A channel 1. For example, if the maximum is + 16 ps and the minimum is -34 ps, worst case skew is 50 ps.

f. Verify that the result (worst case skew between any two channels in slots A to D) is <100 ps.

g. (DTG5078 only) Calculate the difference between the maximum and minimum R1C1 values for all channels of slots A to H, including 0 ps as the value for slot A channel 1.

h. Verify that the result (worst case skew between any two channels in slots A to H) is <200 ps.

7. Push the **TIMING** button on the front panel of DTG5000 series mainframe to display the Timing Window.

8. Verify the instrument hookup: Confirm that the SMA cable is connected from the **CH1 input** of the 80E03 sampling module to the **CH1** connector of the output module which is inserted in the slot A of the mainframe. If your output module is DTGM30, DTGM31, or DTGM32, attach an SMA termination to the $\overline{\textbf{CH1}}$ connector of output module.

9. Load the setup file (DELAY.dtg). Refer to *Loading Files* on page 1-13.

10. Do the following substeps to verify the Lead Delay accuracy.

a. Save the CH1 waveform of oscilloscope to Ref 1 at the DTG delay of 0.000 ns.

b. Verify that the **View by Channel** is selected in the View menu of data timing generator.

c. Move the cursor to **1–A1 Delay** on the data timing generator screen, and then increment the value by 2 ns from 0.000 ns to 10.000 ns.

d. Adjust the oscilloscope horizontal position control so the CH1 waveform (rising edge) is centered on the screen.

e. Modify the oscilloscope setting: Set Source 2 to Ch1 and Source 1 to Ref1.

f. Verify that the **R1C1 Delay** values are within the following range.

- ± 100 ps of setup value (slot A, B, C, D of DTG5078, DTG5274, and DTG5334)
- ± 150 ps of setup value (slot E, F, G, H of DTG5078)

g. Repeat the same measurements as step **9**–**b** through step **9**–**d** for other channels (see below), and verify that the measurement results are within the specified range.

- (DTGM10, DTGM20, and DTGM21): Disconnect the SMA cable from the **CH1** connector of the output module, and then connect it to CH2, CH3 and CH4 of the output module (CH3 and CH4 are for DTG5078 only).
- (DTGM30 only): Disconnect the SMA cable from the **CH1** connector of the output module, and then connect it to **CH2** of the output module. Remove the SMA termination from the $\overline{\textbf{CH1}}$ and attach it to $\overline{\textbf{CH2}}$ connector.

h. Repeat the measurements for other modules installed in the mainframe.

11. Change the **Delay** settings of all the channels to 0.000 ns, and then set the oscilloscope measurement function to **R1(+) to C1(–) Delay**.

12. Verify the instrument hookup: Confirm that the SMA cable is connected from the **CH1 input** of the 80E03 sampling module to the **CH1** connector of the output module which is inserted in the slot A of the mainframe. If your output module is DTGM30, DTGM31, or DTGM32, attach an SMA termination to the $\overline{\textbf{CH1}}$ connector of the output module.

13. Do the following substeps to verify the Trail Delay accuracy:

a. Save the CH1 waveform of oscilloscope to Ref 1 at the delay 0.000 ns.

b. Verify that the **View by Channel** is selected in the View menu of data timing generator.

c. Move the cursor to **1–A1 PW/Duty** on the data timing generator screen, and then increment the trail delay by 0.002000 µs from 0.050000 µs to 0.060000 µs.

d. Adjust the oscilloscope horizontal position control so the CH1 waveform (falling edge) is centered on the screen.

e. Verify that the **R1C1 Delay** values are within the following range.

- ± 100 ps of setup value
  (slot A, B, C, D of DTG5078, DTG5274, and DTG5334)

f. Repeat the same measurements as step **12-b** through step **12-d** for other channels and other modules, and verify that the measurement results are within the specified range.

Clock Out Random Jitter

This test verifies the data timing generator clock out random jitter.

Equipment required	One sampling oscilloscope with an 80E03 sampling module (item 4) Two 50 Ω SMA coaxial cables (item 6) Two attenuators (item 17)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:
   a. Hook up the oscilloscope:
      - Attach the attenuator to **CH1 input** of the 80E03 sampling module and to **Direct Trigger Input** of sampling oscilloscope.
      - Connect an SMA coaxial cable from the **CLOCK OUT** on the rear panel (DTG5078, DTG5274) or the front panel (DTG5334) to the **CH1 input** of the 80E03 sampling module.
      - Connect an SMA coaxial cable from the **CLOCK $\overline{\text{OUT}}$** on the rear panel (DTG5078, DTG5274) or the front panel (DTG5334) to the **Trigger Direct Input** of sampling oscilloscope. See Figure 1-21.

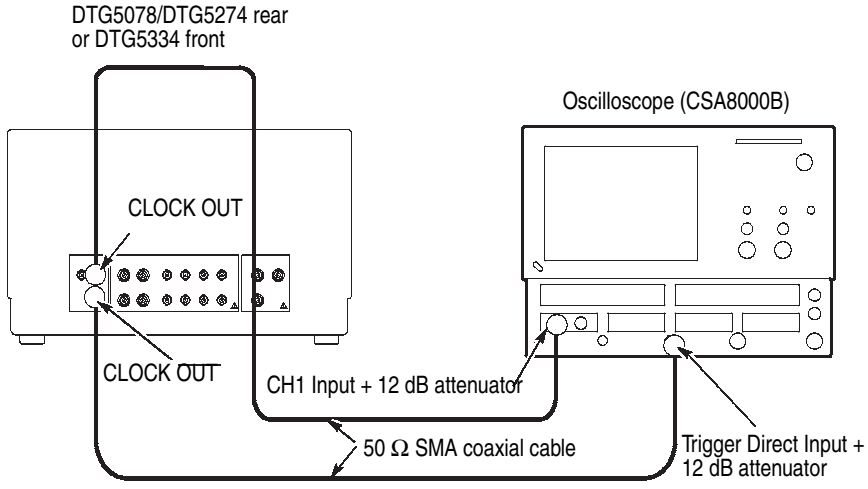


Figure 1-21: Clock out random jitter tests

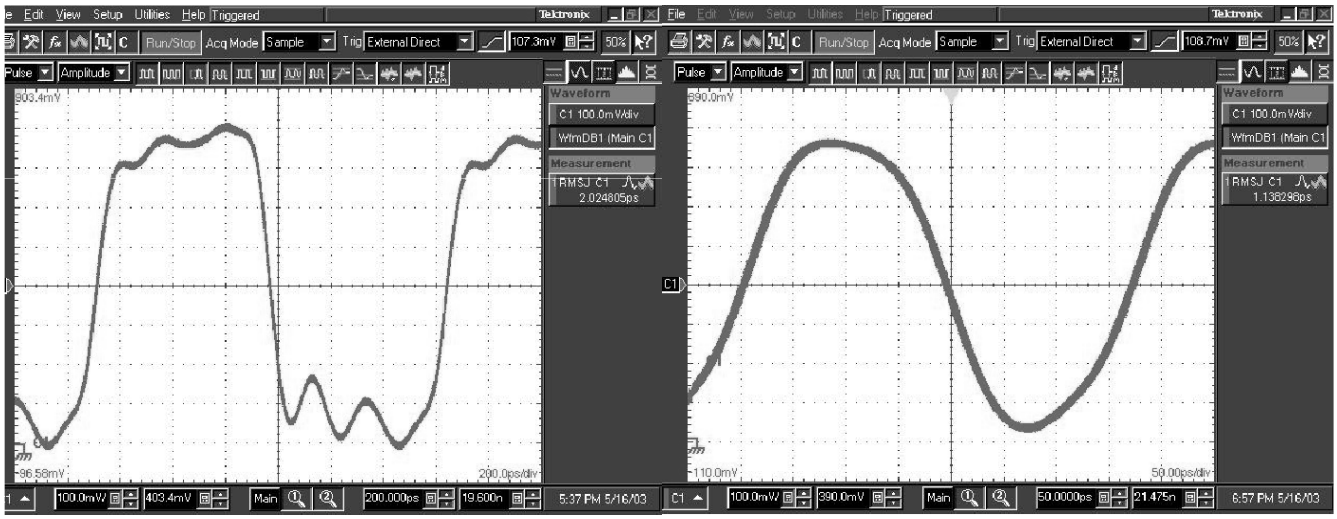
b. Set the oscilloscope controls as follows:

Vertical	
CH1 scale	100 mV/div (with a 12 dB ATT) Select **Setup** -> **Vertical** -> **External Attenuation**, then select 1**2 dB**.
Horizontal	
Scale	200 ps/div (DTG5078) 50 ps/div (DTG5274/DTG5334)
Acquisition	
Mode	Sample
Trigger	
Source	External Direct
Slope	Positive
Level	Set to 50%
Display	Infinite Persistence
Measurement	CH1 RMS Jitter Use Wfm Database Signal Type: Pulse

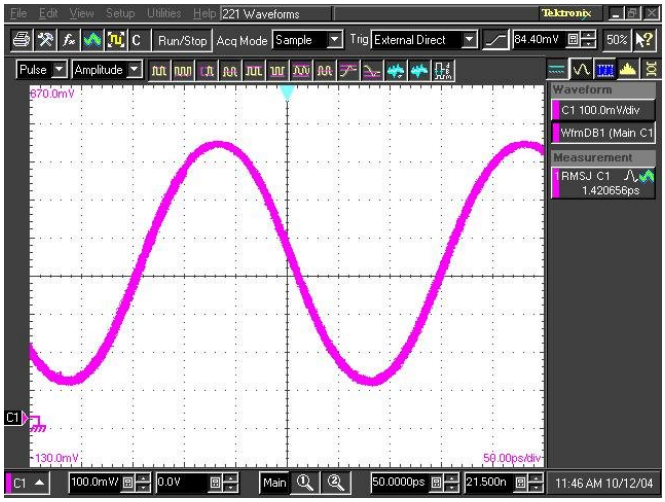
2. Load the setup file (RNDJIT.dtg). Refer to *Loading Files* on page 1-13.

3. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

4. Verify that the oscilloscope displays the waveforms as shown in Figure 1-22 while adjusting the position and offset controls.



DTG5078 DTG5274



DTG5334

Figure 1-22: Clock out random jitter samples

5. Verify that the RMS jitter is within 3 ps.

Random Jitter

This test verifies the data timing generator random jitter.

Equipment required	One sampling oscilloscope with an 80E03 sampling module (item 4) Two 50 Ω SMA coaxial cables (item 6) One SMA termination (item 16, DTG5274 and DTGM5334) One attenuator (item 17)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

NOTE. *When you perform this test, use the specified output module.*
If your mainframe is the DTG5274 or DTG5334, use the DTGM30 output module.
If your mainframe is the DTG5078, use the DTGM20 or DTGM21 output module.

1. Install the test hookup and preset the instrument controls:
   a. Hook up the oscilloscope:
      - Attach the attenuator to **CH1 input** of the 80E03 sampling module.
      - Connect an SMA coaxial cable from the **CH1** connector of the output module, which is in slot A of the DTG5000 series mainframe, to the **CH1 input** of the 80E03 sampling module.
      - Connect a second SMA coaxial cable from the **CLOCK OUT** on the rear panel (DTG5078, DTG5274) or the front panel (DTG5334) to the **Trigger Direct Input** of sampling oscilloscope. See Figure 1-23.

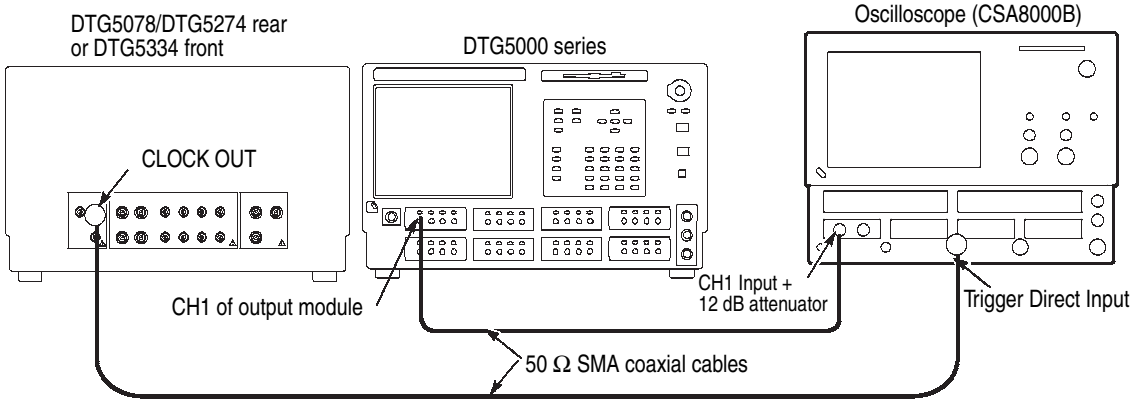


Figure 1-23: Random jitter tests

      - (DTG5274 or DTG5334): Attach an SMA termination to the $\overline{\textbf{CH1}}$ connector of the output module.

b. Set the oscilloscope controls as follows:

Vertical	
CH1 and CH2 scale	DTG5078: 150 mV/div DTG5274/DTG5334: 100 mV/div (with a 12 dB ATT) Select **Setup** -> **Vertical** -> **External Attenuation**, then select **12 dB.**
Waveform CH1	On
Horizontal	
Position	Approximately 20 ns
Scale	200 ps/div (DTG5078) 50 ps/div (DTG5274/DTG5334)
Record Length	4000 (DTG5078) 2000 (DTG5274/DTG5334)
Acquisition	
Mode	Sample
Stop After	Number of Acquisitions: 256
Trigger	
Source	External Direct
Slope	Positive
Level	Set to 50%
Display	Infinite Persistence
Measurement	
Use Wfm Database	
Signal Type	NRZ
Select Meas	NRZ-Timing -> RMS Jitter

2. Load the setup file (RNDJIT.dtg). Refer to *Loading Files* on page 1-13.

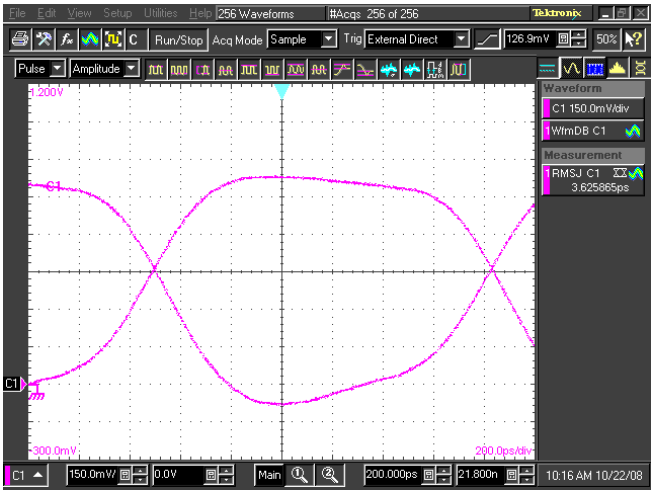
3. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

4. Verify that the oscilloscope displays the waveforms as shown in Figure 1-24 while adjusting the position and offset controls.

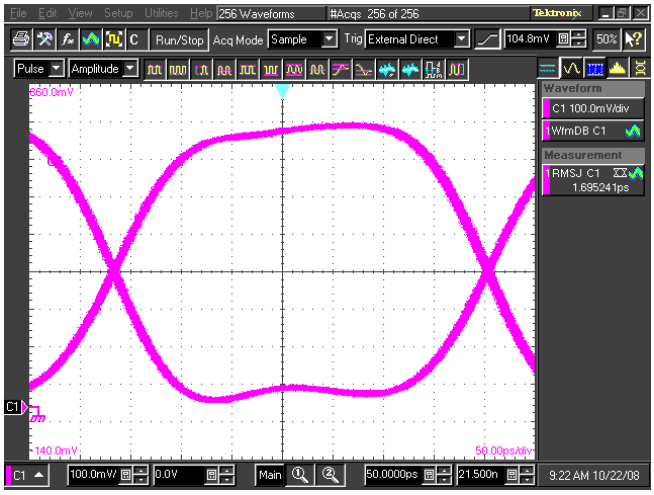
5. Center the eye pattern on screen:

a. Adjust the oscilloscope position controls to locate the eye pattern CH1 waveform on center of screen.

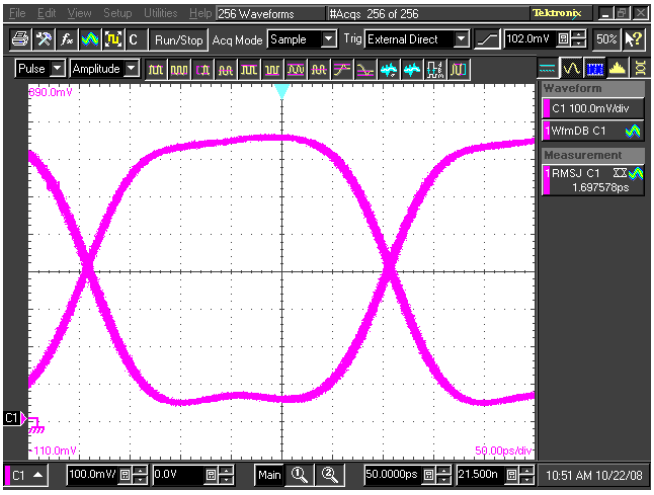
b. Adjust the vertical offset to center the waveform cross point on screen. See Figure 1-24.



DTG5078



DTG5274



DTG5334

Figure 1-24: Random jitter waveform samples

6. Verify that the RMS jitter values are within the following range:

   a. Push **CLEAR DATA**, and then push the **RUN/STOP** button.

   b. Read the **RMS Jitter** value.

   - <4 ps (DTG5078)
   - <3 ps (DTG5274)
   - <3 ps (DTG5334)

7. Repeat the same measurements for other channels.

Total Jitter

This test verifies the data timing generator total jitter.

Equipment required	One sampling oscilloscope with an 80E03 sampling module (item 4) Two 50 Ω SMA coaxial cables (item 6) One SMA termination (item 16, DTG5274 and DTG5334) Two attenuators (item 17)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

NOTE. *When you perform this test, use the specified output module. If your mainframe is the DTG5274 or DTG5334, use the DTGM30 output module. If your mainframe is the DTG5078, use the DTGM20 or DTGM21 output module.*

1. Install the test hookup and preset the instrument controls:
   a. Hook up the oscilloscope:
      - Perform the same hookup procedures as the Random Jitter test described on page 1-66.

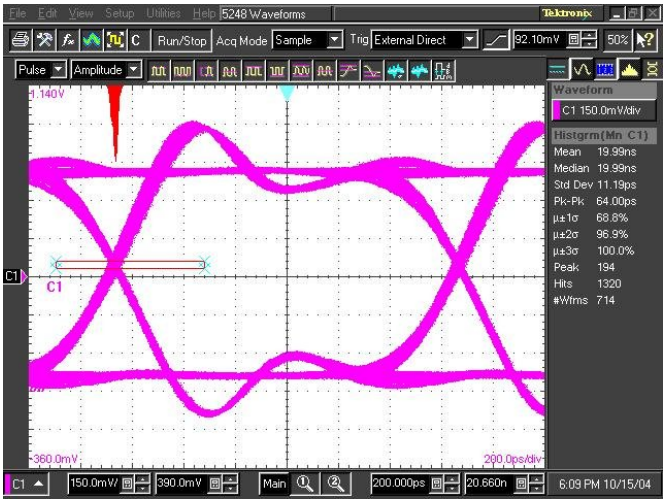
b. Set the oscilloscope controls as follows:

Vertical	
CH1 and CH2 scale	DTG5078: 150 mV/div DTG5274/DTG5334: 100 mV/div (with a 12 dB ATT) Select **Setup** -> **Vertical** -> **External Attenuation**, then select **12 dB**.
Waveform CH1	On
Horizontal	
Position	Approximately 20 ns
Scale	200 ps/div (DTG5078) 50 ps/div (DTG5274/DTG5334)
Acquisition	
Mode	Sample
Trigger	
Source	External Direct
Slope	Positive
Level	Set to 50%
Display	Infinite Persistence
Histogram	CH1 ON Turn the **Enable Histogram** check box on, select **Horizontal** radio button, select **Histogram** from Display Option, select Linear radio button, click Acq tab and select **Condition** from Stop After radio button, select **Histogram Hits**, and then input **8000** to the window.

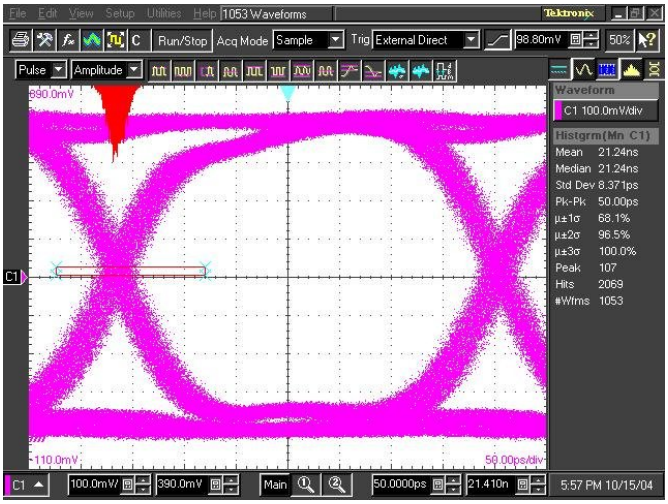
2. Load the setup file (TOTJIT.dtg). Refer to *Loading Files* on page 1-13.

3. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

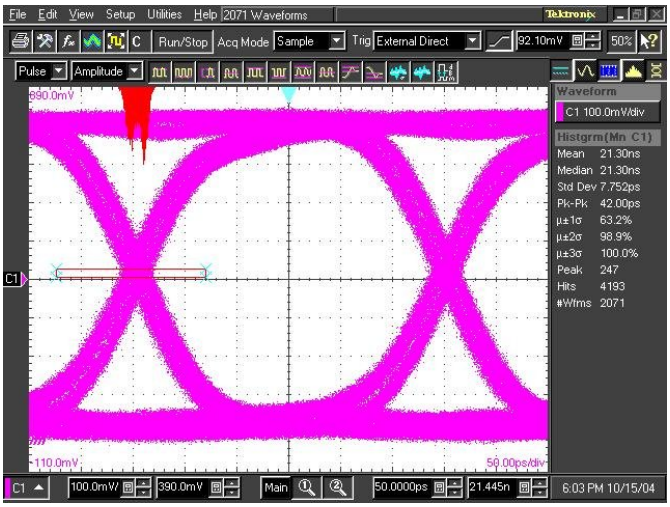
4. Verify that the oscilloscope displays the waveforms as shown in Figure 1-25 while adjusting the position and offset controls.



DTG5078



DTG5274



DTG5334

Figure 1-25: Total jitter waveform samples

5. Place the Histogram Window to the cross point of the eye pattern as shown in Figure 1-25, where vertical width of the window is set to approximately 0.2 div.
6. Change the vertical scale to 20 mV/div and horizontal scale to 20 ps/div.
7. Adjust the horizontal position, vertical offset, and Histogram Window position if the Histogram Window is out of the cross point. Set the vertical width of the window to approximately 0.2 div.
8. Stop the acquisition at the hit count 8000. Verify that the RMS jitter values are within the following range.
   a. Push **CLEAR DATA**, and then push **RUN/STOP** button.
   b. Read the **Std Dev** value.
   - <18 ps (DTG5078)
   - <16 ps (DTG5274)
   - <15 ps (DTG5334)
9. Repeat the same measurements for other channels.

PG Mode

This test verifies that the PG Mode of the DTG5000 series mainframe is functional.

Equipment required	One oscilloscope (TDS7154) (item 3) Two 50 Ω SMA coaxial cables (item 6) Two SMA (female)-BNC (male) adapters (item 9)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:
   a. Hook up the oscilloscope:
      - Attach SMA (female)-BNC (male) adapters to the oscilloscope **CH1 input** and **CH2 input** connectors.
      - Connect an SMA coaxial cable from the **CH1** connector of the output module, which is in slot A of the DTG5000 series mainframe, to the SMA-BNC adapter (CH1 input) of oscilloscope.

- Connect an SMA coaxial cable from the **CH2** connector of the output module, which is in slot A of the DTG5000 series mainframe, to the SMA-BNC adapter (CH2 input) of oscilloscope.
  See Figure 1-26.

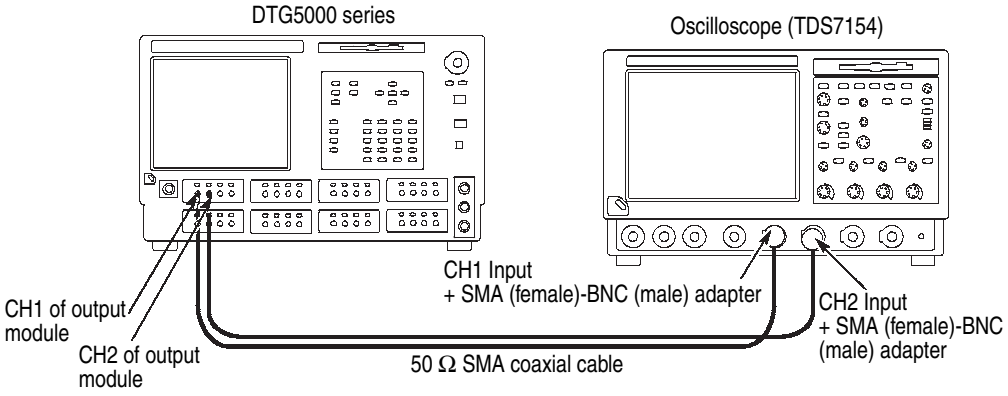


Figure 1-26: PG Mode tests

b. Set the oscilloscope controls as follows:

Vertical	
CH1 and CH2 scale	500 mV/div
CH1 and CH2 input impedance	50 Ω
Horizontal	
Scale	5 ns/div
Trigger	
Source	CH2
Slope	Positive
Level	0.5 V

2. Load the setup file (PGMODE.dtg). Refer to *Loading Files* on page 1-13.
3. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.
4. Verify that 100 MHz square waveform is displayed on the oscilloscope screen.

5. Verify the PG mode functions:

   a. Push the **TIMING** button on the front panel of DTG5000 series mainframe to display the Timing Window.

   b. Move the cursor to **Frequency** and change the frequency to 200 MHz.

   c. Verify that the frequency readout of displayed waveform is 200 MHz on the oscilloscope screen.

   d. Return the **Frequency** to 100 MHz, and then set the DTG5000 series mainframe slot A **CH1 DELAY** to 0.0020000 μs.

   e. Verify on the oscilloscope screen that the rising edge of CH1 is delayed by approximately 2 ns compared to CH2 rising edge.

6. Verify the CH1 duty:

   a. Change the slot A **CH1 Duty** to 30%.

   b. Verify on the oscilloscope screen that CH1 Duty of displayed waveform also indicates approximately 30%.

   c. Change the **CH1 Duty** to **50%**, and then change the slot A **CH1 Polarity** to **Invert**.

   d. Verify on the oscilloscope screen that the displayed waveform is inverted.

7. (DTGM10 and DTGM20 only):

   a. Push the **RUN** button of DTG5000 series mainframe to light the RUN LED.

   b. Move cursor to **Slew Rate** with the TAB key.

   c. Decrease the slew rate value by rotating the rotary encoder counterclockwise.

   d. Verify the displayed waveform: Confirm that the rising edge becomes slow on the oscilloscope screen.

Master-Slave Operation

This test verifies that the Master-Slave operation of the DTG5000 series mainframe is functional.

Equipment required	One oscilloscope (TDS7154) (item 3) Two 50 Ω SMA coaxial cables (item 6) Two 50 Ω BNC coaxial cables (item 7) Two SMA (male)-BNC (female) adapters (item 8)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:

a. Hook up the oscilloscope:

- Use an SMA coaxial cable to connect **CLK IN** and **CLK OUT1** of the Maser/Slave Connection plate on the rear panel of DTG5000 series mainframe.
- Use a second SMA coaxial cable to connect $\overline{\textbf{CLK IN}}$ and $\overline{\textbf{CLK OUT1}}$ of the Maser/Slave Connection plate on the rear panel of DTG5000 series mainframe.
- Attach an SMA (male)-BNC (female) adapter to the **CLOCK OUT** on the rear panel (DTG5078, DTG5274) or the front panel (DTG5334).
- Connect a BNC coaxial cable from the **CLOCK OUT** to the **CH1 input** of oscilloscope through an SMA-BNC adapter.
- Attach an SMA (male)-BNC (female) adapter to the **CH1** connector of the output module, which is in slot A of the DTG5000 series mainframe.
- Connect a BNC coaxial cable from the **CH1** connector of output module to the **CH2 input** of oscilloscope through an SMA-BNC adapter. See Figure 1-27.

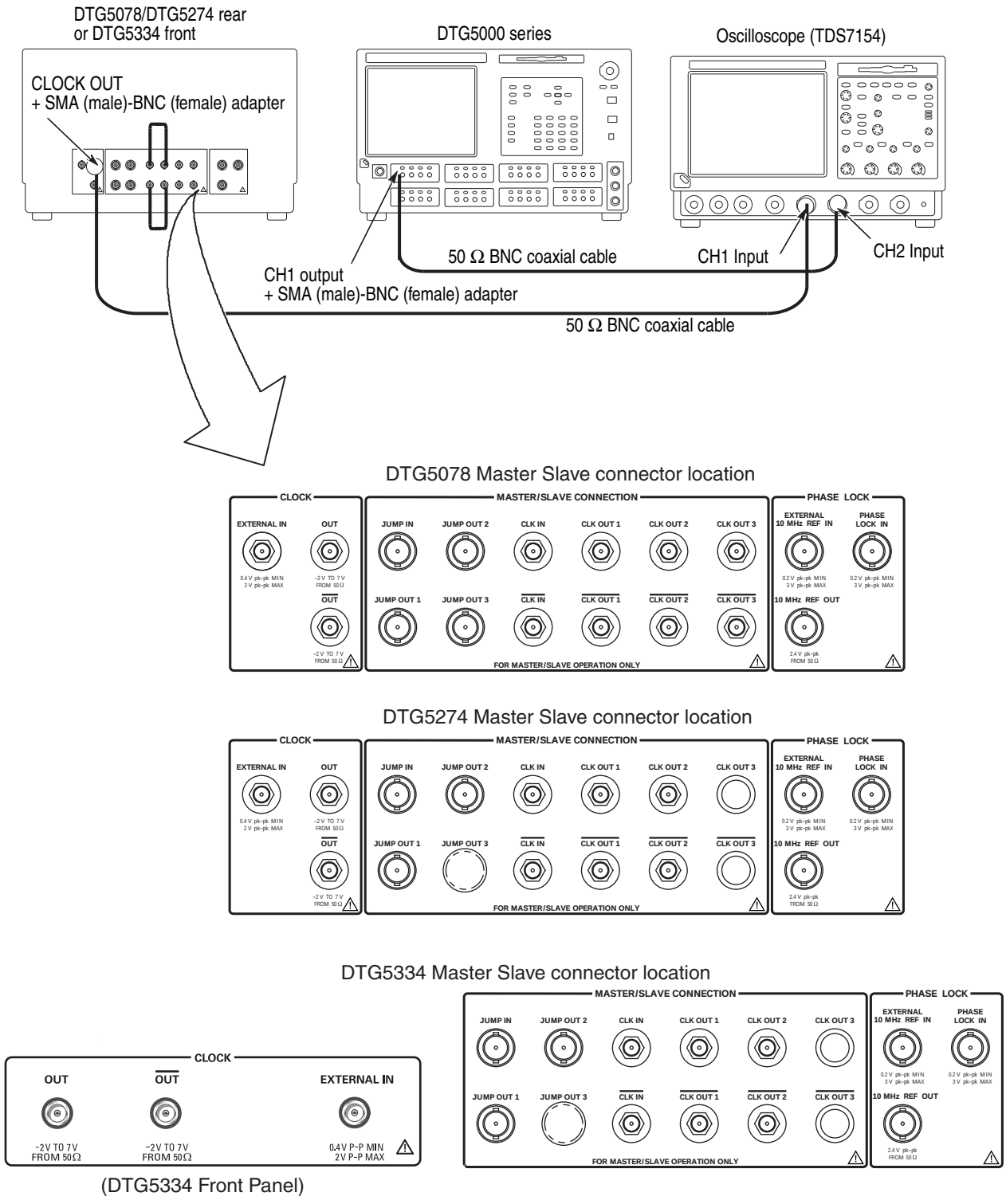


Figure 1-27: Master–Slave operation tests

b. Set the oscilloscope controls as follows:

Vertical
- CH1 and CH2 scale . . . . . 500 mV/div
- CH1 and CH2 input impedance . . . . . 50 Ω

Horizontal
- Scale . . . . . 50 ns/div

Trigger
- Source CH2
- Slope . . . . . Positive
- Level . . . . . 0.5 V

2. Set the data timing generator controls and load the setup file:

a. Exit the DTG software.

NOTE. *Move the cursor to the bottom left corner of the screen to get the Windows* ***Start*** *menu. Or, press the* ***CTRL*** *and* ***ESC*** *keys simultaneously to open the Windows* ***Start*** *menu.*

b. From the Windows **Start** menu, select **Programs**, select **Tektronix**, select **DTG5000**, and then select **DTG5000 Configuration Utility**. See Figure 1-28.

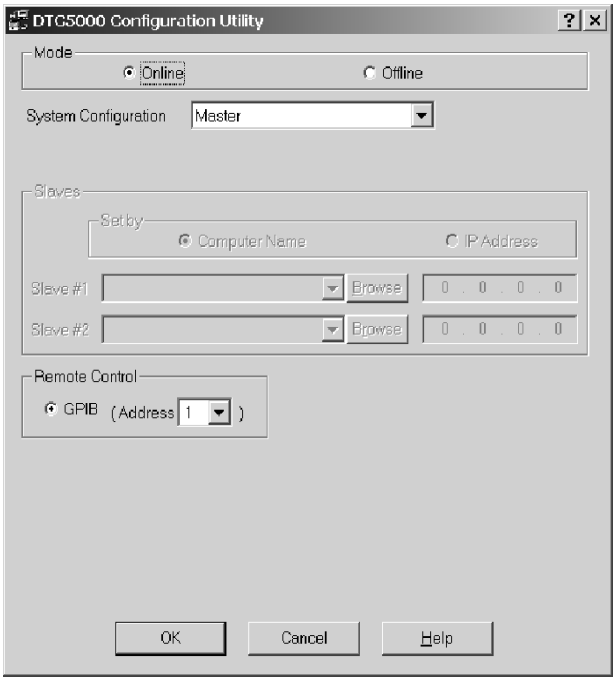


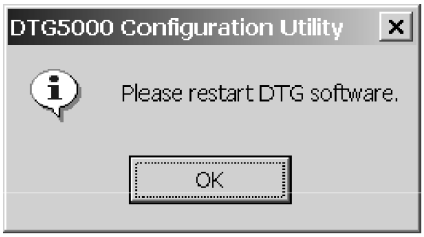
Figure 1-28: DTG5000 Configuration Utility dialog box

c. Confirm that **Online** is selected in the **Mode** box.

d. Select **Master/Slave#1** from the System Configuration pull-down menu.

e. Select **IP Address** at the **Slaves Set by** check box, and then enter **0.0.0.0** to the IP Address box.

f. Click **OK** to exit the window. The following dialog box appears and asks you to restart the DTG software.



g. Click **OK**, and then restart the DTG software.

h. Load the setup file (MASTER.dtg). Refer to *Loading Files* on page 1-13.

3. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

4. Confirm that the oscilloscope displays the waveforms such as shown in Figure 1-29.

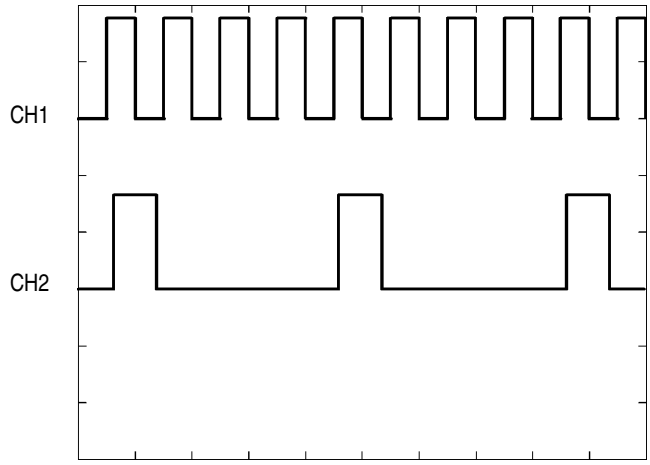


Figure 1-29: Master-Slave operation waveform sample

5. Disconnect the SMA cables from the **CLK OUT1** and **$\overline{\text{CLK OUT1}}$**. Reconnect the cables to **CLK OUT2** and **$\overline{\text{CLK OUT2}}$**, respectively.

6. Verify that the oscilloscope displays the same waveforms as step **4** on the screen.

7. (DTG5078 only): Disconnect the SMA cables from the **CLK OUT2** and **$\overline{\text{CLK OUT2}}$**. Reconnect the cables to **CLK OUT3** and **$\overline{\text{CLK OUT3}}$**, respectively. Verify that the oscilloscope displays the same waveforms as step **4** on the screen.

8. Before proceeding with the next test item, do the following substeps.

   a. Exit the DTG software.

NOTE. *Mover cursor to the button left corner of the screen to get the Windows Start menu. Or, press the* ***CTRL*** *+* ***ESC*** *keys simultaneously to open the Start menu.*

   b. From the Windows **Start** menu, select **Programs**, select **Tektronix**, select **DTG5000**, and then select **DTG5000 Configuration Utility**.
   See Figure 1-28 on page 1-77.

   c. Select **Master** from the System Configuration pull-down menu.

   d. Click **OK** to exit the window. The dialog box appears and asks you to restart the DTG software. Click **OK**, and then restart the DTG software.

Output Module

The following procedures check those characteristics that relate to the output modules that are checked under *Output Module* in *Specifications*. Refer to page 2-32.

NOTE. *When you perform the DTG5000 series output module performance tests, you can install the module to any slot of mainframe.*

There are six types of output modules: DTGM10, DTGM20, DTGM21, DTGM30, DTGM31, and DTGM32. The same performance test procedures are applied to these modules, however, each module has different specifications. If you want to check CH3 and CH4 of four channel module such as DTGM10, DTGM20, or DTGM21, you must use the DTG5078 mainframe.

Data Output DC Level

This test verifies the data output DC level accuracy of the DTG5000 series output module.

Equipment required	One digital multi meter (item 2) One 50 Ω BNC coaxial cable (item 7) One SMA (male)-BNC (female) adapter (item 8) One BNC (female)-dual banana plug (item 13) One Feed-through 50 Ω termination (item 15)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:
   a. (DTGM21 only): Set the output impedance to 50 Ω for all the four channels on the module before installing it in the mainframe and applying power.
   b. Hook up the digital multi meter:
      - Attach a BNC (female)-dual banana adapter to the digital multi meter input connector, and then attach a 50 Ω termination to the BNC–dual banana adapter.
      - Attach an SMA (male)-BNC (female) adapter to the **CH1** connector of the output module, which is in slot A of the DTG5000 series mainframe.
      - Connect a BNC coaxial cable from the SMA-BNC adapter (CH1 output of output module) to the 50 Ω termination of digital multi meter. See Figure 1-30.

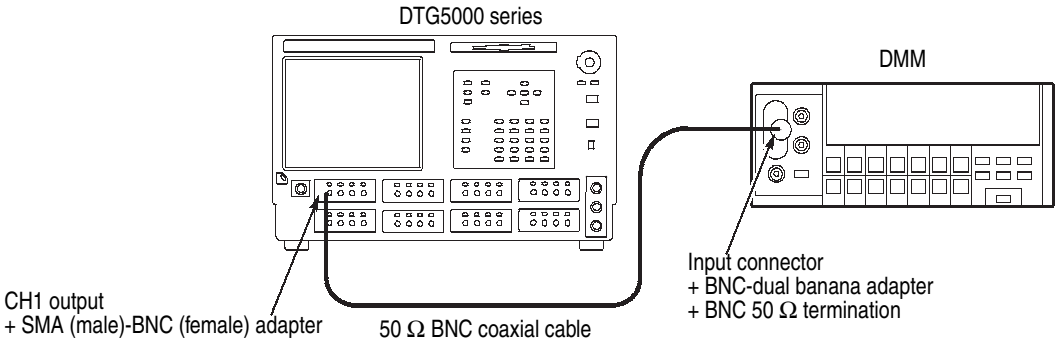


Figure 1-30: Data output DC level tests

c. Set the digital multi meter controls:

Mode	Direct Voltage
Range	Auto

2. If you want to perform the data output DC level tests for DTGM10, DTGM20, or DTGM21, continue the following steps. If your output module is DTGM30, DTGM31, or DTGM32, jump to step **5**.

3. Do the following substeps to perform the high/low level voltage measurements:

a. Load the setup file (OM_H.dtg). Refer to *Loading Files* on page 1-13.

b. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

c. Push the **LEVEL** button to set the high level and corresponding low level voltage for the CH1 output as shown in Table 1-4 (DTGM10), Table 1-6 (DTGM20), or Table 1-8 (DTGM21).

d. Verify that the DMM readings are within the voltage limits.

e. Load the setup file (OM_L.dtg). Refer to *Loading Files* on page 1-13.

f. Push the **LEVEL** button to set the low level and corresponding high level voltage for the CH1 output as shown in Table 1-5 (DTGM10), Table 1-7 (DTGM20), or Table 1-9 (DTGM21).

g. Verify that the DMM readings are within the voltage limits.

4. Change the connections and repeat the measurements:

   a. Change the connection of BNC cable from the CH1 output to CH2, CH3, and CH4 output.

   b. Perform the same measurements as step **3** for every channel.

   c. Verify that the high level and low level measurements are within the specified voltage limits.

5. (DTGM21 only):

   a. Turn off the mainframe to remove the module.

   b. Change the output impedance to 23 Ω for all the four channels on the module.

   c. Reinstall the module in the mainframe and apply power.

   d. Repeat steps 3 and 4 for the output impedance of 23 Ω using the Table 1-10 and 1-11.

Table 1-4: DTGM10 high level voltage accuracy

Setup value		
High Level Voltage	Low Level Voltage	**High Level Output Voltage Limits**
–1.0 V	–1.5 V	–1.08 V to –0.92 V
0 V	–1.5 V	–0.05 V to + 0.05 V
1 V	–1.5 V	0.92 V to 1.08 V
2 V	–1.5 V	1.89 V to 2.11 V

Table 1-5: DTGM10 low level voltage accuracy

Setup value		
Low Level Voltage	High Level Voltage	**Low Level Output Voltage Limits**
–1.0 V	2.0 V	–1.08 V to –0.92 V
0 V	2.0 V	–0.05 V to + 0.05 V
1 V	2.0 V	0.92 V to 1.08 V
1.75 V	2.0 V	1.6475 V to 1.8525 V

Table 1-6: DTGM20 high level voltage accuracy

Setup value		
High Level Voltage	Low Level Voltage	**High Level Output Voltage Limits**
–0.9 V	–1.0 V	–0.977 V to –0.823 V
0 V	–1.0 V	–0.05 V to + 0.05 V
1.0 V	–1.0 V	0.92 V to 1.08 V
2.0 V	–1.0 V	1.89 V to 2.11 V

Table 1-7: DTGM20 low level voltage accuracy

Setup value		
Low Level Voltage	High Level Voltage	**Low Level Output Voltage Limits**
–1.0 V	2.5 V	–1.08 V to –0.92 V
0 V	2.5 V	–0.05 V to + 0.05 V
1.0 V	2.5 V	0.92 V to 1.08 V
2.0 V	2.5 V	1.89 V to 2.11 V

Table 1-8: DTGM21 high level voltage accuracy (output impedance 50 ohm)

Setup value		
High Level Voltage	Low Level Voltage	**High Level Output Voltage Limits**
–1.1 V	–1.2 V	–1.183 V to –1.017 V
0 V	–1.2 V	–0.05 V to + 0.05 V
1.5 V	–1.2 V	1.405 V to 1.595 V
2.7 V	–1.2 V	2.569 V to 2.831 V

Table 1-9: DTGM21 low level voltage accuracy (output impedance 50 ohm)

Setup value		
Low Level Voltage	High Level Voltage	**Low Level Output Voltage Limits**
–1.2 V	2.7 V	–1.286 V to –1.114 V
0 V	2.7 V	–0.05 V to + 0.05 V
1.5 V	2.7 V	1.405 V to 1.595 V
2.6 V	2.7 V	2.472 V to 2.728 V

Table 1-10: DTGM21 high level voltage accuracy (output impedance 23 ohm)

Setup value		
High Level Voltage	Low Level Voltage	**High Level Output Voltage Limits**
–1.55 V	–1.65 V	–1.6465 V to –1.4535 V
0.5 V	–1.65 V	0.435 V to 0.565 V
2 V	–1.65 V	1.89 V to 2.11 V
3.7 V	–1.65 V	3.539 V to 3.861 V

Table 1-11: DTGM21 low level voltage accuracy (output impedance 23 ohm)

Setup value		
Low Level Voltage	High Level Voltage	**Low Level Output Voltage Limits**
–1.65 V	3.7 V	–1.7495 V to –1.5505 V
0.5 V	3.7 V	0.435 V to 0.565 V
2 V	3.7 V	1.89 V to 2.11 V
3.6 V	3.7 V	3.442 V to 3.758 V

6. Do the following substeps to perform the high/low level voltage measurements for the DTGM30, DTGM31, or DTGM32:

a. Load the setup file (OM_H.dtg). Refer to *Loading Files* on page 1-13.

b. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

c. Push the **LEVEL** button to set the high level and corresponding low level voltage for the CH1 output as shown in Table 1-12. Verify that the DMM reading is within the voltage limits.

d. Load the setup file (OM_L.dtg). Refer to *Loading Files* on page 1-13.

e. Push the **LEVEL** button to set the low level and corresponding high level voltage for the CH1 output as shown in Table 1-13. Verify that the DMM reading is within the voltage limits.

7. Change the connections and repeat the measurements:
   a. Change the connection of BNC cable from the CH1 output to $\overline{\text{CH1}}$ output.
   b. Perform the same measurements as step **6** for every channel.
   c. Verify that the high level and low level measurements are within the specified voltage limits.
8. Change the connections and repeat the measurements (DTGM30 only):
   a. Change the connection of the BNC cable from the $\overline{\text{CH1}}$ output to CH2 and $\overline{\text{CH2}}$ output.
   b. Perform the same measurements as step **6** for every channel.
   c. Verify that the high level and low level measurements are within the specified voltage limits.

NOTE. *When you perform the voltage measurements for $\overline{CH1}$ and $\overline{CH2}$, load the setup file OM_L.dtg for high level measurements and OM_H.dtg for low level measurements*

Table 1-12: DTGM30/DTGM31/DTGM32 high level voltage accuracy

Setup value		
High Level Voltage	Low Level Voltage	**High Level Output Voltage Limits**
–0.97 V	–1.0 V	–1.0491 V to –0.8909 V
0.5 V	–0.75 V	0.435 V to 0.565 V
2.0 V	1.50 V	1.89 V to 2.11 V
2.47 V	2.44 V	2.3459 V to 2.5941 V

Table 1-13: DTGM30/DTGM31/DTGM32 low level voltage accuracy

Setup value		
Low Level Voltage	High Level Voltage	**Low Level Output Voltage Limits**
–1.0 V	0.25 V	–1.08 V to –0.92 V
0.5 V	1.50 V	0.435 V to + 0.565 V
2.0 V	2.25 V	1.89 V to 2.11 V
2.44 V	2.47 V	2.3168 V to 2.5632 V

Data Format

This test verifies that the data format of the DTG5000 series mainframe is functional.

NOTE. *Use the DTGM10, DTGM20, DTGM21, or DTGM30 module; do not use DTGM31 and DTGM32.*

Equipment required	One oscilloscope (TDS7154) (item 3) Two 50 Ω SMA coaxial cables (item 6) Two SMA (female)-BNC (male) adapters (item 9)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:

   a. Hook up the oscilloscope:

   - Attach SMA (female)-BNC (male) adapters to the oscilloscope **CH1** and **CH2 input** connectors.
   - Connect an SMA coaxial cable from the **CH1** connector of the output module, which is in slot A of the DTG5000 series mainframe, to the SMA-BNC adapter (CH1 input) of oscilloscope.
   - Connect an SMA coaxial cable from the **CH2** connector of the output module, which is in slot A of the DTG5000 series mainframe, to the SMA-BNC adapter (CH2 input) of oscilloscope. See Figure 1-31.

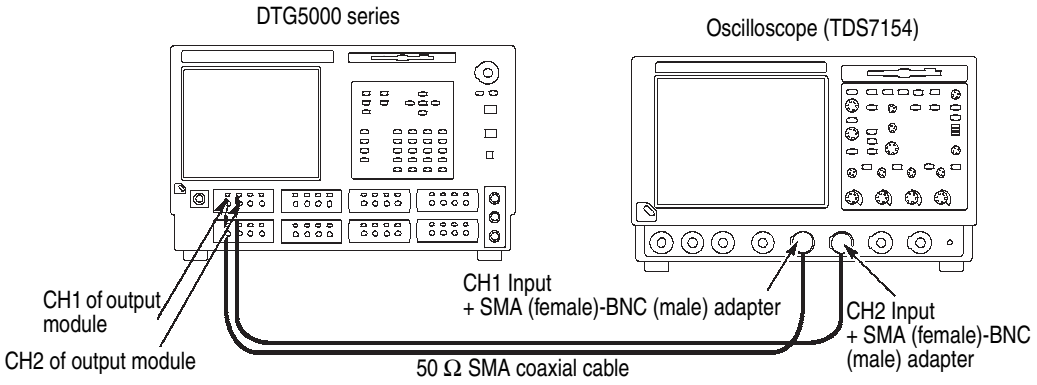


Figure 1-31: Data format tests

b. Set the oscilloscope controls as follows:

Vertical
- CH1 and CH2 scale . . . . . 500 mV/div
- CH1 and CH2 input impedance . . . . . 50 Ω

Horizontal
- Scale . . . . . 50 ns/div

Trigger
- Source CH2
- Slope . . . . . Positive
- Level . . . . . 0.5 V

2. Load the setup file (FORMAT.dtg). Refer to *Loading Files* on page 1-13.

3. Do the following substeps to verify the data format:

a. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

b. Verify that the oscilloscope displays pulse pattern such as shown in Figure 1-32.

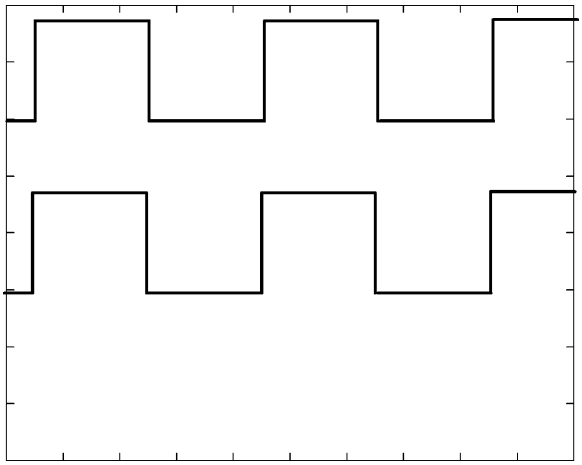


Figure 1-32: Pulse pattern example

c. Push the **TIMING** button on the front panel of DTG5000 series mainframe to display the Timing Window.

d. Change **CH1 Format** of slot A from **NRZ** to **RZ**. Verify that the displayed waveform is changed from Figure 1-32 to Figure 1-33.

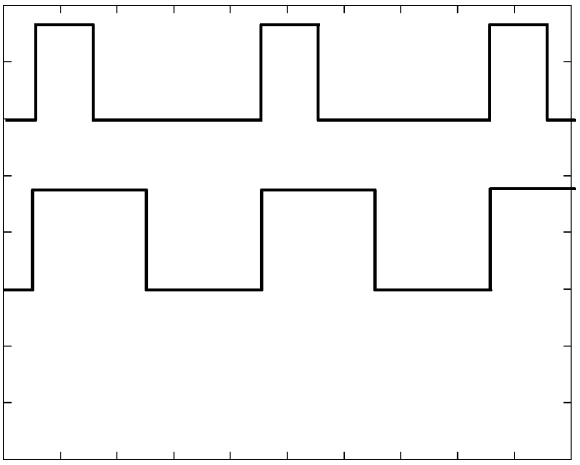


Figure 1-33: RZ waveform example

e. Change **CH1 Format** of slot A from **RZ** to **R1**. Verify that the displayed waveform is changed from Figure 1-33 to Figure 1-34.

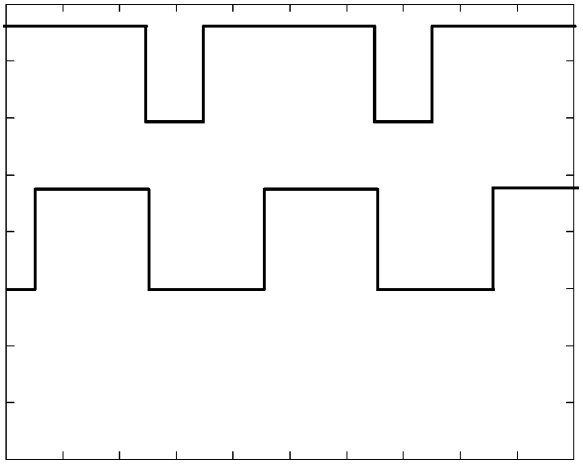


Figure 1-34: R1 waveform example

Jitter Control In

This test verifies that the external jitter input is functional. This function is supported by the DTGM31 and DTGM32. The DTGM32 has two jitter inputs, A and B.

Equipment required	One sampling oscilloscope with an 80E03 sampling module (item 4) One function generator (item 5) Three 50 Ω SMA coaxial cables (item 6) One 50 Ω BNC coaxial cable (item 7) One SMA (male)-BNC (female) adapter (item 8) Two attenuators (item 17)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:
   a. Hook up the oscilloscope and function generator:
      - Attach the attenuators to the **CH1 input** and **CH2 input** of the 80E03 sampling module.
      - Attach an SMA (male)-BNC (female) adapter to the **JITTER CONTROL IN A** connector of the output module.
      - Connect a BNC coaxial cable from the front panel **CH1 Out** of function generator to the SMA-BNC adapter (Jitter Control In A).
      - Connect an SMA coaxial cable from the **CH1** connector of the output module, which is in slot A of the DTG5000 series mainframe, to the **CH1 input** of the 80E03 sampling module through a 12 dB attenuator.
      - Connect an SMA coaxial cable from the $\overline{\textbf{CH1}}$ connector of the output module, which is in slot A of the DTG5000 series mainframe, to the **CH2 input** of the 80E03 sampling module through a 12 dB attenuator.
      - Connect an SMA coaxial cable from the **SYNC OUT** on the front panel of DTG5000 series mainframe to the **Trigger Direct Input** of the sampling oscilloscope. See Figure 1-35.

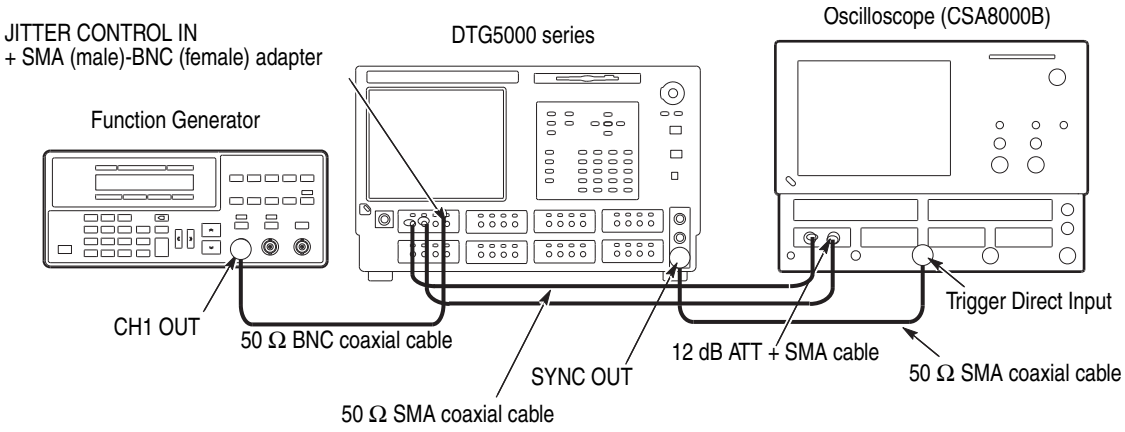


Figure 1-35: Jitter control input tests

b. Set the oscilloscope controls as follows:

Vertical	
CH1 and CH2 scale	200 mV/div (with a 12 dB ATT) Select **Setup** -> **Vertical** -> **External Attenuation**, then select **12 dB**.
CH1 and CH2 impedance	50 Ω
Horizontal	
Scale	500 ps/div (DTGM31) 5 ns/div (DTGM32)
Trigger	
Source	External Direct
Level	–0.2 V
Display	Infinite Persistence
Histogram	CH1 ON

c. Set the function generator controls:

Output channel	CH1
Function	Sine
Parameters	
Frequency	1 MHz
Amplitude	1.0 V into 50 Ω
Offset	0 mV
Output	Off

2. Load the setup file (JITIN.dtg). Refer to *Loading Files* on page 1-13.

3. Turn the function generator **Output** on.

4. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

5. Set the vertical width of histogram window to approximately 0.2 div, then adjust the vertical width to the rising edge of displayed waveform.

6. (DTGM31 only) Set the Clock Frequency to 750 MHz.

7. Confirm the jitter generation: In the examples of Figure 1-36 and Figure 1-37, a jitter appears on the rising and falling edges of every pulse. Check the jitter width.

   - 240 ps_{p-p} (DTGM31)
   - 2 ns_{p-p} (DTGM32)

8. (DTGM32 only) Change the jitter range of DTGM32 to 1 ns from 2 ns, and then check the jitter width. See Figure 1-38.

   - 1 ns_{p-p}

9. (DTGM32 only) Do the following substeps:

   a. Disconnect the SMA-BNC adapter and BNC cable from the **JITTER CONTROL IN A** connector.

   b. Connect the SMA-BNC adapter and BNC cable to **JITTER CONTROL IN B** connector.

   c. Check the jitter width. (Repeat the step 2 through step 8.)

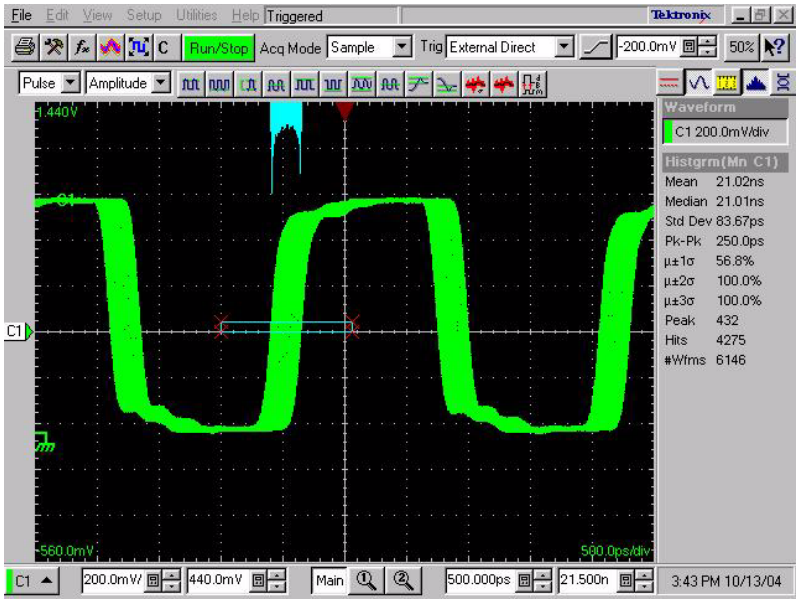


Figure 1-36: Jitter generation example (DTGM31)

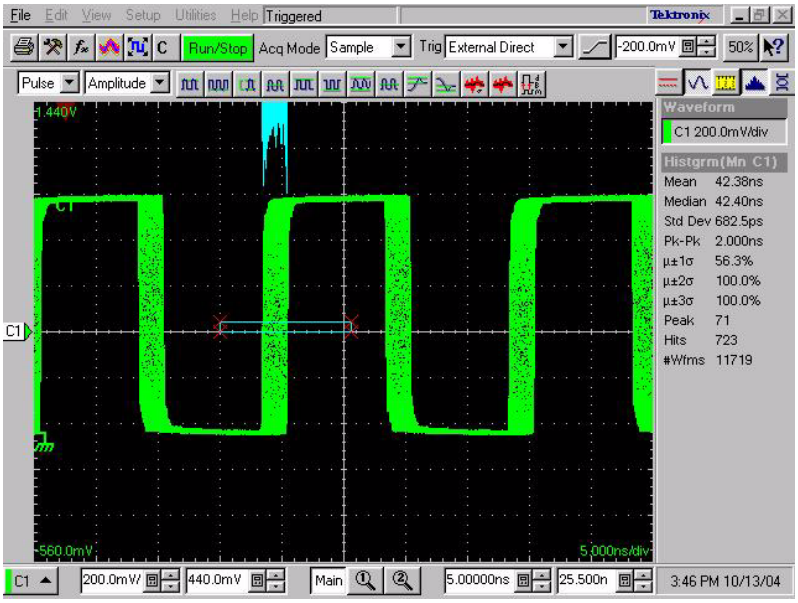


Figure 1-37: Jitter generation example (DTGM32 range 2 ns)

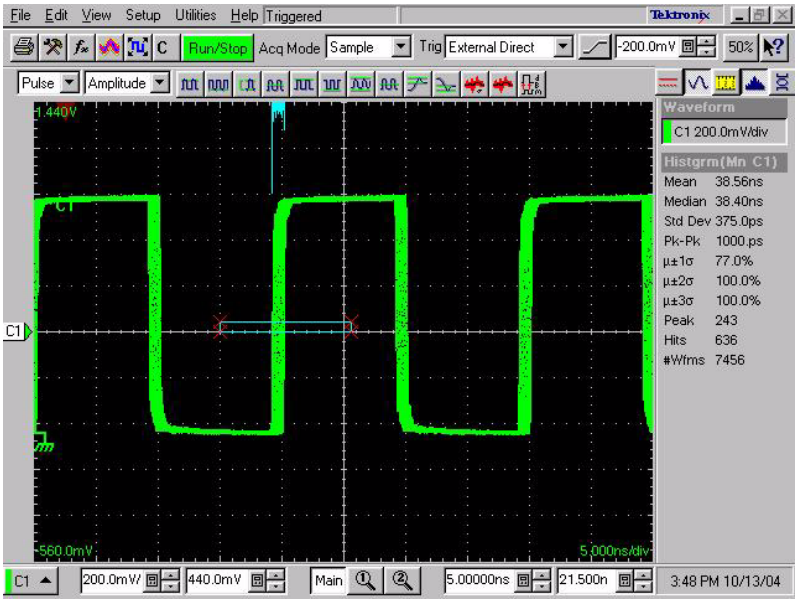


Figure 1-38: Jitter generation example (DTGM32 range 1 ns)

Inhibit Input

This test verifies that inhibit input is functional. This function is supported by the DTGM21 module.

Equipment required	One oscilloscope (TDS7104) (item 3) One function generator (item 5) One 50 Ω SMA coaxial cable (item 6) Two 50 Ω BNC coaxial cables (item 7) One SMA (female)-BNC (male) adapter (item 9) One SMB (female)-BNC (male) cable (item 18) One BNC-T connector (item 14)
Prerequisites	The DTG5000 Series Data Timing Generator must meet the prerequisites listed on page 1-11.

1. Install the test hookup and preset the instrument controls:
   a. Hook up the oscilloscope and function generator:
      - Attach a BNC-T connector to the **CH3 input** of the oscilloscope.
      - Connect a BNC coaxial cable from the **CH1 Out** of function generator to the **CH3 input** of the oscilloscope (through BNC-T connector).
      - Connect the SMB (female) side of SMB-BNC cable to the **INHIBIT IN** of the DTGM21 module, and then connect the opposite end of SMB-BNC cable to the **CH3 input** of the oscilloscope (through BNC-T connector).
      - Attach an SMA (female)-BNC (male) adapter to the oscilloscope **CH1 input** connector.
      - Connect an SMA coaxial cable from the **CH1** connector of the DTGM21 module, which is in slot A of the DTG5000 series mainframe, to the SMA-BNC adapter (CH1 input of oscilloscope). See Figure 1-39.

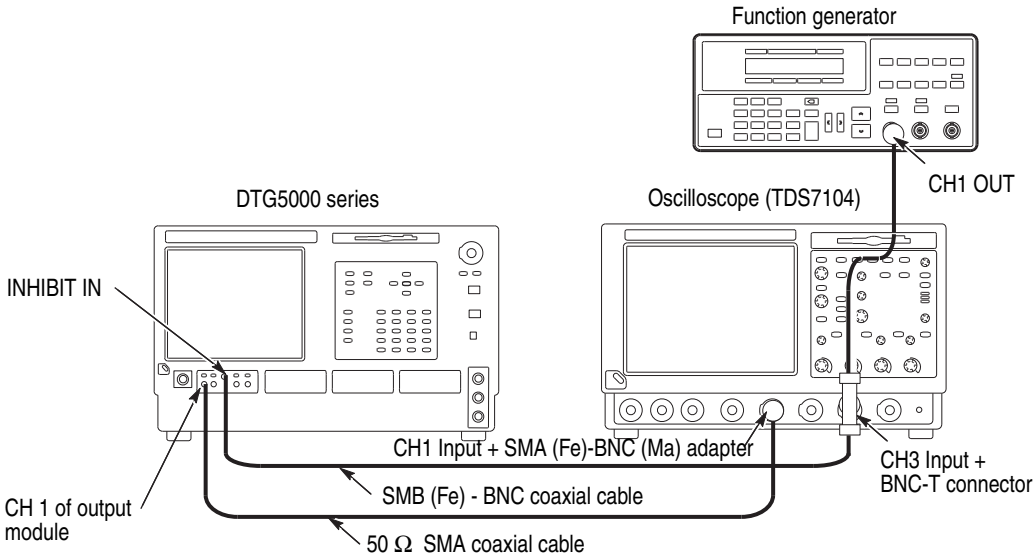


Figure 1-39: Inhibit input tests

b. Set the oscilloscope controls as follows:

Vertical
- CH1 scale . . . . . 500 mV/div
- CH3 scale . . . . . 1 V/div
- CH1 input impedance . . . . . 50 Ω
- CH3 input impedance . . . . . 1 MΩ

Horizontal
- Scale . . . . . 250 ns/div

Trigger
- Source CH3
- Mode . . . . . Normal
- Slope . . . . . Positive
- Level . . . . . +1.65 V
- Coupling . . . . . DC

Measurement
- CH1 Amplitude
- CH1 Frequency

c. Set the function generator controls:

Output channel	CH1
Function	Square
Parameters	
Frequency	1 MHz
Amplitude	1.65 V into 50 Ω
Offset	0.825 V

2. Load the setup file (INHIBIT.dtg). Refer to *Loading Files* on page 1-13.

3. Turn the function generator **Output** on.

4. Push the **RUN** button of the data timing generator to light the RUN LED, and then push the **ALL OUTPUTS ON/OFF** button to activate the output.

5. Confirm the Inhibit control.

a. Use the oscilloscope Measurement function to measure the CH1 Amplitude and CH1 Frequency.

b. Verify that the following:

- Amplitude: approximately 1 V
- Frequency: approximately 1 MHz

Specifications

Specifications

This section contains the DTG5000 Series Data Timing Generator specifications. All specifications are guaranteed unless labeled “typical”. Typical specifications are provided for your convenience but are not guaranteed.

Specifications that are check marked with the ✓ symbol are checked directly (or indirectly) in the *Performance Verification* chapter of this manual.

Performance Conditions

The performance limits in this specification are valid with these conditions:

- The instrument must have been calibrated/adjusted at an ambient temperature between +20 °C and +30 °C.
- The instrument must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The instrument must have had a warm-up period of at least 20 minutes.
- The instrument must be operating at an ambient temperature between +10 °C and +40 °C.

Product and Feature Description

The DTG5000 Series Data Timing Generator is a high speed/multichannel signal generator which creates a wide range of digital timing signals. The products are designed to generate a data pattern for standard and nonstandard pulses necessary for functional tests or characterization of legacy devices (TTL, CMOS, ECL) as well as the latest devices (PECL, LVDS, GTL, CML).

Table 2-1 and Table 2-2 show the data timing generator family.

Table 2-1: DTG5000 Series Data Timing Generators (mainframe)

	DTG5078	DTG5274/DTG5334
Maximum data rate	750 Mb/s	2.7 Gb/s (DTG5274) 3.35 Gb/s (DTG5334)
Number of slot	8 (A, B, C, D, E, F, G, and H) [1]	4 (A, B, C, and D)
Delay control	1 ps resolution (all channel)	0.2 ps resolution (all channel)
Width control	5 ps resolution (all channel in slot A, B, C, and D)	5 ps resolution (all channel)
Master-slave	Up to three (one Master, two Slaves)	Up to two (one Master, one Slave)

1. The DTG5078 mainframe has restrictions on the quantity of modules that are installed. The restriction is determined by the sum total (Pt) of the coefficient of the installed module. This sum total must be 100 or less. The coefficient of each module is shown below.

	Pt (Mxx) [1]
DTGM10	9
DTGM20	10
DTGM30	8
DTGM21	10
DTGM31	33
DTGM32	32

1. Mxx: M10/M20/M30/M21/M31/M32

Example 1: DTGM31: 3 ea
Pt=Pt(M31) x 3 = 33 x 3 = 99 <100
: Acceptable

Example 2: DTGM31: 2 ea, DTGM10: 4 ea
Pt=Pt(M31) x 2 + Pt(M10) x 4 = 33 x 2 + 9 x 4 = 102 >100
: Not acceptable

When exceeding the restrictions like above example 2, the DTG5000 series displays a warning message.
This message is displayed approximately 20 seconds and the DTG5000 series is shut down automatically.

Table 2-2: DTG5000 Series Data Timing Generators (output module)

	DTGM10	DTGM20	DTGM30	DTGM21	DTGM31	DTGM32
Number of channel	4 or 2 [1]	4 or 2 [1]	2	4 or 2 [1]	1	1
Amplitude (50 Ω)	3.5 V_{p-p} [2]	3.5 V_{p-p} [3]	1.25 V_{p-p}	5.35 V_{p-p} [4] 3.90 V_{p-p} [5]	1.25 V_{p-p}	1.25 V_{p-p}
Amplitude (1 MΩ)	10 V_{p-p}	7 V_{p-p}	2.5 V_{p-p}	7.81 V_{p-p} [6]	2.5 V_{p-p}	2.5 V_{p-p}
Source impedance	50 Ω	50 Ω	50 Ω	23 Ω or 50 Ω [7]	50 Ω	50 Ω
Maximum output current	+/– 40 mA	+/– 80 mA	+/– 80 mA	+/– 80 mA	+/– 80 mA	+/– 80 mA
Rise time/fall time at 1 V_{p-p} into 50 Ω (20% to 80%)	<540 ps (variable)	<340 ps (variable)	<110 ps	<350 ps	<110 ps	<110 ps
Inhibit Input	NA	NA	NA	Available	NA	NA
External Jitter Input	NA	NA	NA	NA	Available	Available

1. **CH3 and CH4 are not supported by DTG5274 and DTG5334.**
2. **This value is limited by Maximum Output Current (+/-40mA Max).**
3. **This value is limited by Maximum Output Current (+/-80mA Max).**
4. **Source impedance is 23 Ω.**
5. **Source impedance is 50 Ω.**
6. **Recommended source impedance is 50 Ω.**
7. **Source impedance is selectable by moving the conductor in the box.**

Additional product information is located within the User and Service manuals. See *Related Manuals and Online Documents* on page ix in the Preface.

Electrical Specification-Mainframe

Table 2-3: Operation mode

Characteristics	Description
Data Generator Mode (DG Mode)	Operates as a data generator. The output data are created through built-in pattern editor or imported files created by external simulation software tools. The output timing is defined by sample clock rate. - Timing control: Delay, Slew rate, Width - Level control: High/Low or Amplitude/Offset - Supports flexible block branching sequence function. **Note:** *Jump is not available if Long Delay is set to On.*
Pulse Generator Mode (PG Mode)	Operates as a pulse generator. The output timing is defined by signal output frequency. - Timing control: Pulse width, Delay, Duty, Slew rate - Level control: High/Low or Amplitude/Offset

Table 2-4: Sequencer

Characteristics	Description
Pattern Length	
DTG5078	
Hardware Sequence	240 to 8,000,000 words
Software Sequence	1 to 8,000,000 words
DTG5274	
Hardware Sequence	960 to 32,000,000 words
Software Sequence	1 to 32,000,000 words
DTG5334	
Hardware Sequence	960 to 64,000,000 words
Software Sequence	1 to 64,000,000 words
Pattern Length Granularity	
DTG5078	
Hardware Sequence	1 word
Software Sequence	1 word
DTG5274 and DTG5334	
Hardware Sequence	Depends on vector rate. Refer to Table 2-24 and Table 2-25.
Software Sequence	1 word
Sequence Length	1 to 8000 steps
Maximum Blocks	8000
Maximum sub-sequences	50
Sub-sequence Length	1 to 256 steps

Table 2-4: Sequencer (cont.)

Characteristics	Description
Sequence Repeat Counter	1 to 65,536 or Infinite, All channels operate the same sequence.

Table 2-5: Clock generator

Characteristics	Description	PV reference page
Clock Frequency		
DTG5078	50 kHz to 750 MHz, can be set up to 800 MHz	
DTG5274	50 kHz to 2.7 GHz, can be set up to 3.35 GHz	
DTG5334	50 kHz to 3.35 GHz, can be set up to 3.4 GHz	
Resolution	8 digits	
Internal clock[1]		
✓Accuracy	within ±1 ppm	page 1-32
Aging	within ±1 ppm/year	

1. The internal reference oscillator is used.

Table 2-6: Internal trigger generator

Characteristics	Description
Internal trigger rate[1]	
Range	1.0 µs to 10.0 s
Resolution	3 digits, minimum 0.1 µs

1. The internal reference oscillator is used.

Table 2-7: DC output

Characteristics	Description	PV reference page
Connector	2.54 mm 2 x 8 pin header (female), front right side	
Number of Channel	8	
Source Resistance	approximately 1 Ω	
Level		
Voltage Range	–3.0 V to 5.0 V	
Control	Independent	
Resolution	10 mV	
✓DC Accuracy	(±3% of the set value) ±50 mV	page 1-57
Maximum Output Current	±30 mA	
Pin Assignment	Refer to Figure 2-1.	

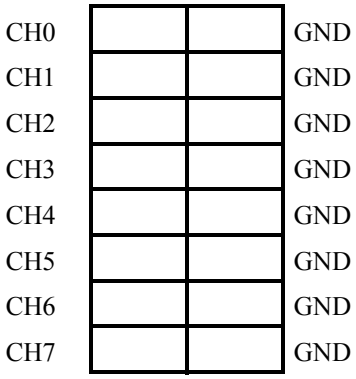


Figure 2-1: DC Output channel assignment

Table 2-8: Clock output

Characteristics	Description	PV reference page
Output connector		
DTG5078 and DTG5274	SMA rear	
DTG5334	SMA front	
Output Signal Type	Complementary	
Frequency		
DTG5078	50 kHz to 750 MHz, can be set up to 800 MHz	
DTG5274	50 kHz to 2.7 GHz, can be set up to 3.35 GHz	
DTG5334	50 kHz to 3.35 GHz, can be set up to 3.4 GHz	
Impedance	50 Ω	
Output Voltage Level [1]		
Range		
High Level (VOH) [2]	–1.00 V to 2.47 V into 50 Ω to GND –1.94 V to 7.00 V into 1 MΩ to GND	
Low Level (VOL) [3]	–2.00 V to 2.44 V into 50 Ω to GND –2.00 V to 6.94 V into 1 MΩ to GND	
Output Voltage Amplitude [4]		
Range	30 mV_{p-p} to 1.25 V_{p-p} into 50 Ω to GND 60 mV_{p-p} to 2.5 V_{p-p} into 1 MΩ to GND	
Resolution	10 mV	
Output Voltage Frequency Response	±10 dB of value shown in the curve of Figure 2-2 and Figure 2-3.	
Output Voltage Offset		
Resolution	40 mV	
Range	Depends on the limit of VOH and VOL set by the user. Refer to Output Voltage Level. Offset = (VOH + VOL) /2	
Maximum Output Current	±80 mA	
✓Rise /Fall Time (20% to 80%), typical		
DTG5078		
at 100 mV_{p-p} amplitude, 0 V offset	<85 ps into 50 Ω to GND	page 1-34
at 1.00 V_{p-p} amplitude, 0 V offset	<100 ps into 50 Ω to GND	

Table 2-8: Clock output (cont.)

Characteristics	Description	PV reference page
DTG5274		
at 100 mV_{p-p} amplitude, 0 V offset	<70 ps into 50 Ω to GND	page 1-34
at 1.00 V_{p-p} amplitude, 0 V offset	<80 ps into 50 Ω to GND	
DTG5334		
at 1.00 V_{p-p} amplitude, 0 V offset	<100 ps into 50 Ω to GND	page 1-34
✓Aberration, typical		
Positive Overshoot	<10% at 1 V_{p-p} into 50 Ω	page 1-34
Negative Overshoot	<10% at 1 V_{p-p} into 50 Ω	
✓Random Jitter, typical	Measured by RMS jitter in Measurement function of CSA8000 + 80E03.	
DTG5078	<2 ps rms, at 750 Mb/s, amplitude = 0.8 V_{p-p}	page 1-63
DTG5274	<2 ps rms, at 2.7 Gb/s, amplitude = 0.8 V_{p-p}	
DTG5334	<2 ps rms, at 3.35 Gb/s, amplitude = 0.8 V_{p-p}	

1 **When the amplitude and offset are set up, the VoH and VoL are automatically set up in DTG5000 series.**
There is no menu to set the VoH or VoL directly. Refer to Figure 2-12 on page 2-42.

2 **High level (VoH) should fulfill the following formulas simultaneously.**
R_L = Term R, Vtt = Term V

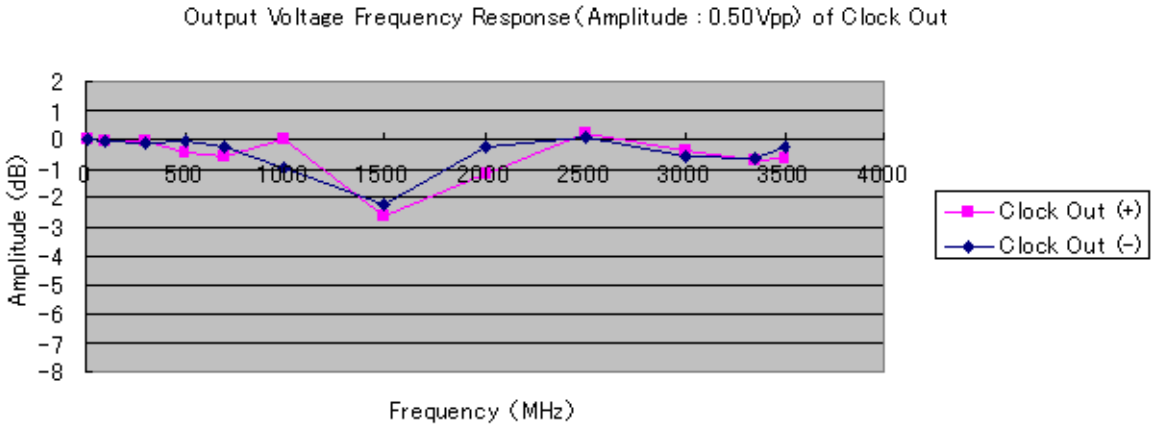
$VOH \leq 7.00$
$VOH \leq (7.00 \times RL + 50 \times Vtt) / (RL + 50)$
$VOH \leq RL / 50 \times (2.5 - 0.06 \times RL / (RL + 50)) + Vtt$
$VOH \geq (-2.00 \times RL + 50 \times Vtt) / (RL + 50)$
$VOH \geq Vtt - RL / 50$

3 **Low level (VoL) should fulfill the following formulas simultaneously.**
R_L = Term R, Vtt = Term V

$VOL \geq -2.00$
$VOL \geq (50 \times Vtt - 4.5 \times RL) / (RL + 50)$
$VOL \geq Vtt - RL\ (0.02 + 2.5 / (RL + 50))$
$VOL < ((2.5 - 0.06) \times RL / 50) + Vtt$

4 **Amplitude should fulfill the following formulas simultaneously. Amplitude = VOH - VOL**
R_L = Term R, Vtt = Term V
$VOH - VOL > 2 \times (Vtt - RL/50 - Offset)$
$VOH - VOL > 2 \times ((RL \times (-2) + 50 \times Vtt) / (RL + 50) - Offset)$
$VOH - VOL < 2 \times ((2.5 \times RL - 50 \times Offset + 50 \times Vtt) / (2 \times RL + 50))$
$VOH - VOL < 2 \times ((7 \times RL - 50 \times Vtt) / (RL + 50) - Offset)$

(1) DTG5078
DTG5274



(2) DTG5334

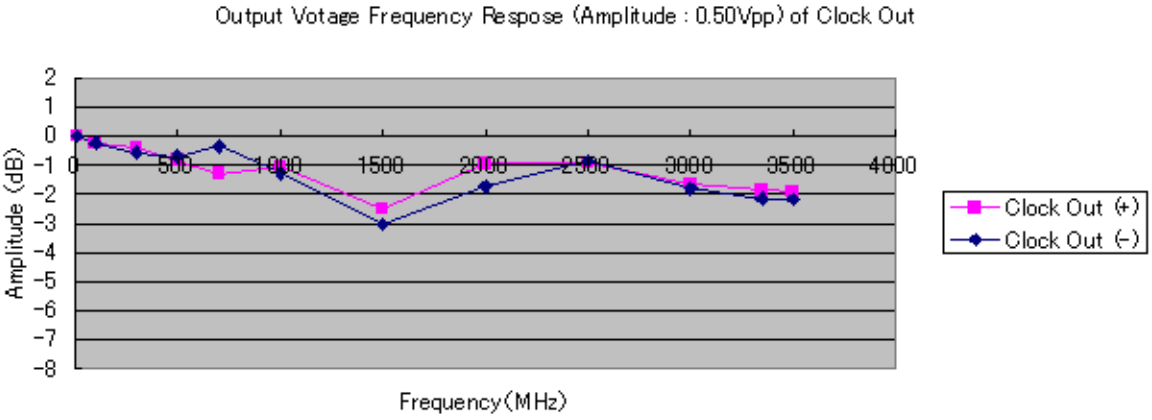
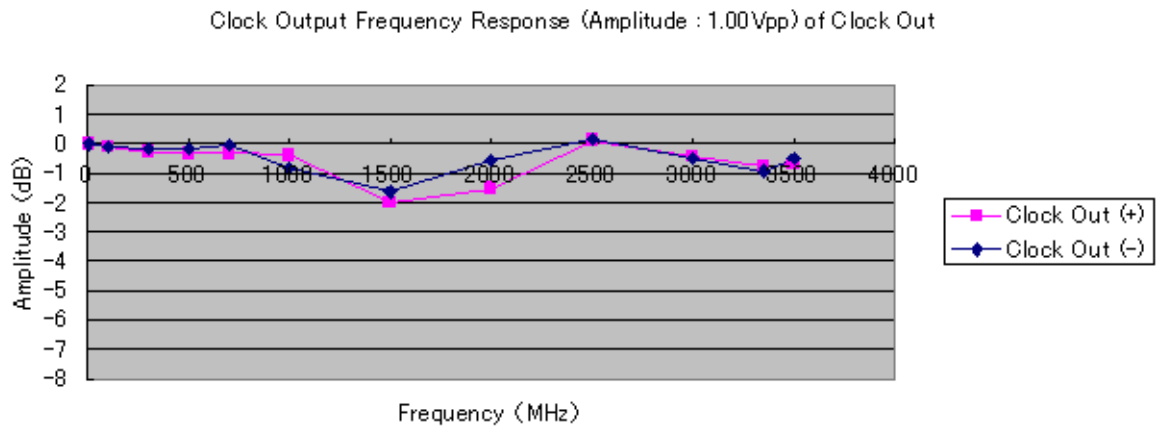


Figure 2-2: Frequency response of clock output (at 0.5 V_{p-p})

(1) DTG5078
DTG5274



(2) DTG5334

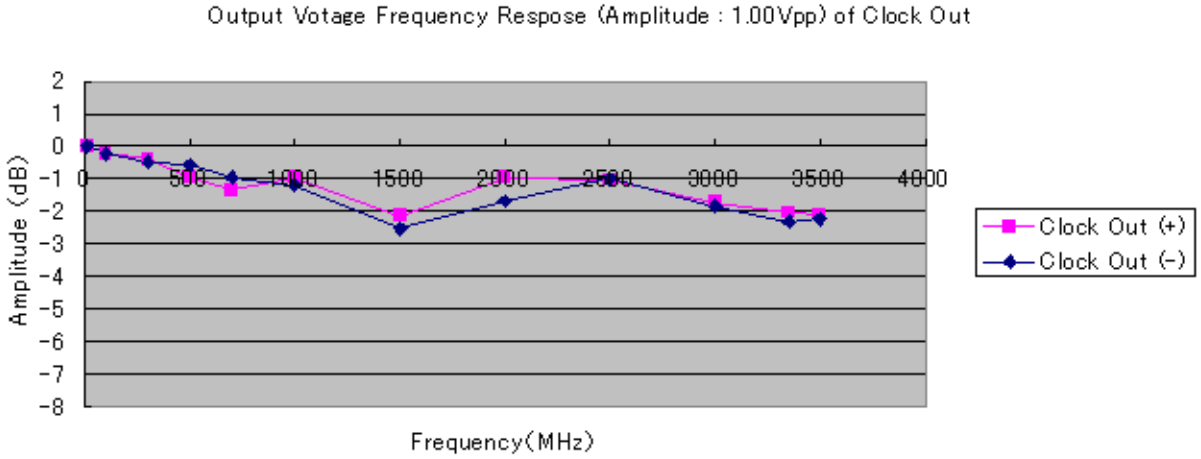


Figure 2-3: Frequency response of clock output (at 1.0 V_{p-p})

Table 2-9: External clock input

Characteristics	Description
Connector	
DTG5078 and DTG5274	SMA rear
DTG5334	SMA front
Impedance	50 Ω, AC coupled
Required Input Voltage Swing	400 mV_{p-p} to 2 V_{p-p} into 50 Ω
Required Duty Cycle	50 ±5%
Frequency Range	Slew rate should be more than 10 mV/ns.
DTG5078	1 MHz to 750 MHz
DTG5274	1 MHz to 2.7 GHz
DTG5334	1 MHz to 3.35 GHz

Table 2-10: 10 MHz reference input

Characteristics	Description	PV reference page
Connector	BNC rear	
Impedance	50 Ω, AC coupled,	
Required Input Voltage Swing	200 mV_{p-p} to 3 V_{p-p}	
✓Frequency Range	10 MHz ±0.1 MHz	page 1-39

Table 2-11: 10 MHz reference output

Characteristics	Description	PV reference page
Connector	BNC rear	
Impedance	50 Ω, AC coupled	
✓Amplitude, typical	1.2 V_{p-p} into 50 Ω to GND 2.4 V_{p-p} into 1 MΩ to GND	page 1-40

Table 2-12: Phase lock input

Characteristics	Description	PV reference page
Connector	BNC rear	
Impedance	50 Ω, AC coupled	
Required Input Voltage Swing	200 mV_{p-p} to 3 V_{p-p}	
✓Frequency Range	1 MHz to 200 MHz	page 1-42
Multiplier Rate [1]		
Long Delay, Off		
NRZ	x N, The maximum value of N is limited by the maximum data rate.	
RZ and R1	x N/2, The maximum value of N is limited by the maximum data rate.	
Long Delay, On	x N / (vector rate)	

[1] **N is an arbitrary integer.**

Table 2-13: Skew cal input

Characteristics	Description
Connector [1]	SMA front
Input Signal Type	Single end
Level	ECL into 50 Ω to –2 V

[1] **This input is used only in calibrating a skew between channels. Refer to User Manual for details. The output of a slave machine should also be input into Skew Cal In of a master machine, and then Skew Calibration should be executed.**
Skew Calibration should be executed between the same output modules. In addition, jitter amplitude also should be the same when the output module is DTGM32.

Table 2-14: Trigger input

Characteristics	Description
Connector	BNC front
Impedance	1 kΩ or 50 Ω
Slope	Positive or Negative
Input Voltage Range	–10 V to 10 V, 1 kΩ selected –5 V to 5 V, 50 Ω selected
Threshold	
Level	–5.0 V to 5.0 V
Resolution	0.1 V
Required Minimum Input Swing	1.0 V_{p-p}, 1 kΩ selected 0.5 V_{p-p}, 50 Ω selected
Required Minimum Pulse Width (Pw1)	20 ns, refer to Figure 2-4.
Maximum Delay Time to Data Out (Td1)	Refer to Figure 2-4.
DTG5078	47 H/W Clocks + 5 VCO (Ext) Clocks + 50 ns
DTG5274	201 H/W Clocks + 5 VCO (Ext) Clocks + 50 ns
DTG5334	223 H/W Clocks + 5 VCO (Ext) Clocks + 50 ns
Trigger Holdoff Time (Td 3)	Refer to Figure 2-4.
DTG5078	29 H/W Clocks + 500 ns
DTG5274	115 H/W Clocks + 500 ns
DTG5334	109 H/W Clocks + 500 ns

Table 2-15: Sync output

Characteristics	Description [1]	PV reference page
Connector	SMA front	
Output Signal Type	Single end	
✓Level, typical	CML (Current Mode Logic)	
VOH	0 V into 50 Ω to GND	page 1-29
VOL	–0.4 V into 50 Ω to GND	
Pulse Width (Pw 2)	Refer to Figure 2-4.	
DTG5078, DTG5274, and DTG5334	4 Clocks	
Rise/Fall Time (20% to 80%)	<140 ps	

[1] **DG Mode: A positive pulse is generated at the beginning of each block.**
PG Mode: A positive pulse is generated on each trigger if the Run Mode is set to Burst.
Sync Out is not available if the Run Mode is set to Continuous.

Table 2-16: Sync clock input

Characteristics	Description [1]
Connector	SMA rear
Output Signal Type	Complementary

[1] **This signal is used for only Master Slave performance test with another DTG5000 series instrument. Refer to the reference manual for details. The cable connection in Master-Slave operation in units is shown in Figure 2-5 and Figure 2-6.**

Table 2-17: Sync clock output1, output 2, and output 3

Characteristics	Description [1]
Connector	SMA rear
Output Signal Type	Complementary

[1] **This signal is used for only Master Slave performance test with another DTG5000 series instrument. Refer to the reference manual for details. Sync Clock Out 3 is equipped only with DTG5078. The cable connection in Master-Slave operation in units is shown in Figure 2-5 and Figure 2-6.**

Table 2-18: Sync jump input

Characteristics	Description [1]
Connector	BNC rear

[1] This signal is used for only Master Slave performance test with another DTG5000 series instrument. Refer to the reference manual for details. The cable connection in Master-Slave operation in units is shown in Figure 2-5 and Figure 2-6.

Table 2-19: Sync jump output 1, output 2, and output 3

Characteristics	Description [1]
Connector	BNC rear

[1] This signal is used for only Master Slave performance test with another DTG5000 series instrument. Refer to the reference manual for details. Sync Jump Out 3 is equipped only with DTG5078. The cable connection in Master-Slave operation in units is shown in Figure 2-5 and Figure 2-6.

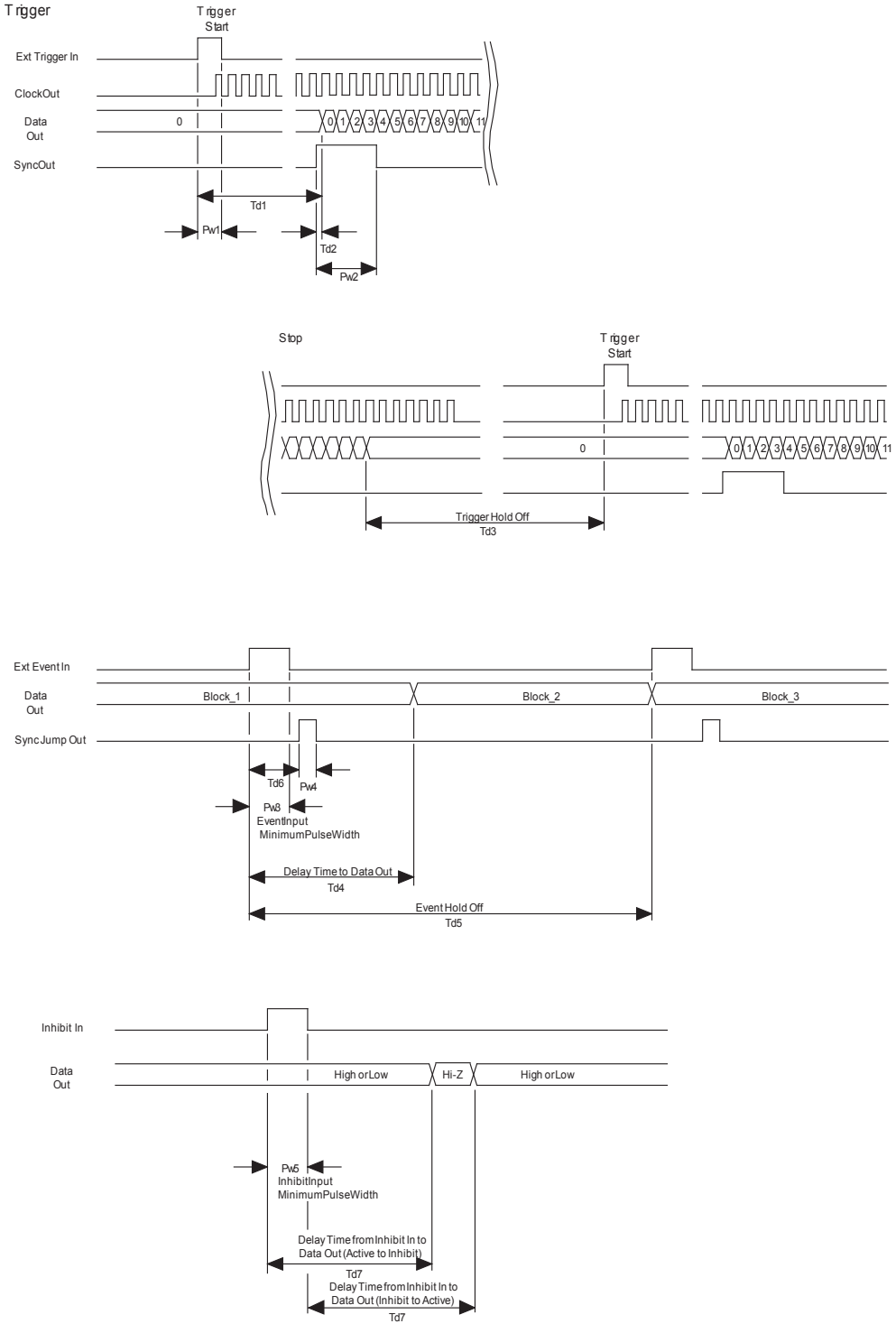


Figure 2-4: Signal timing

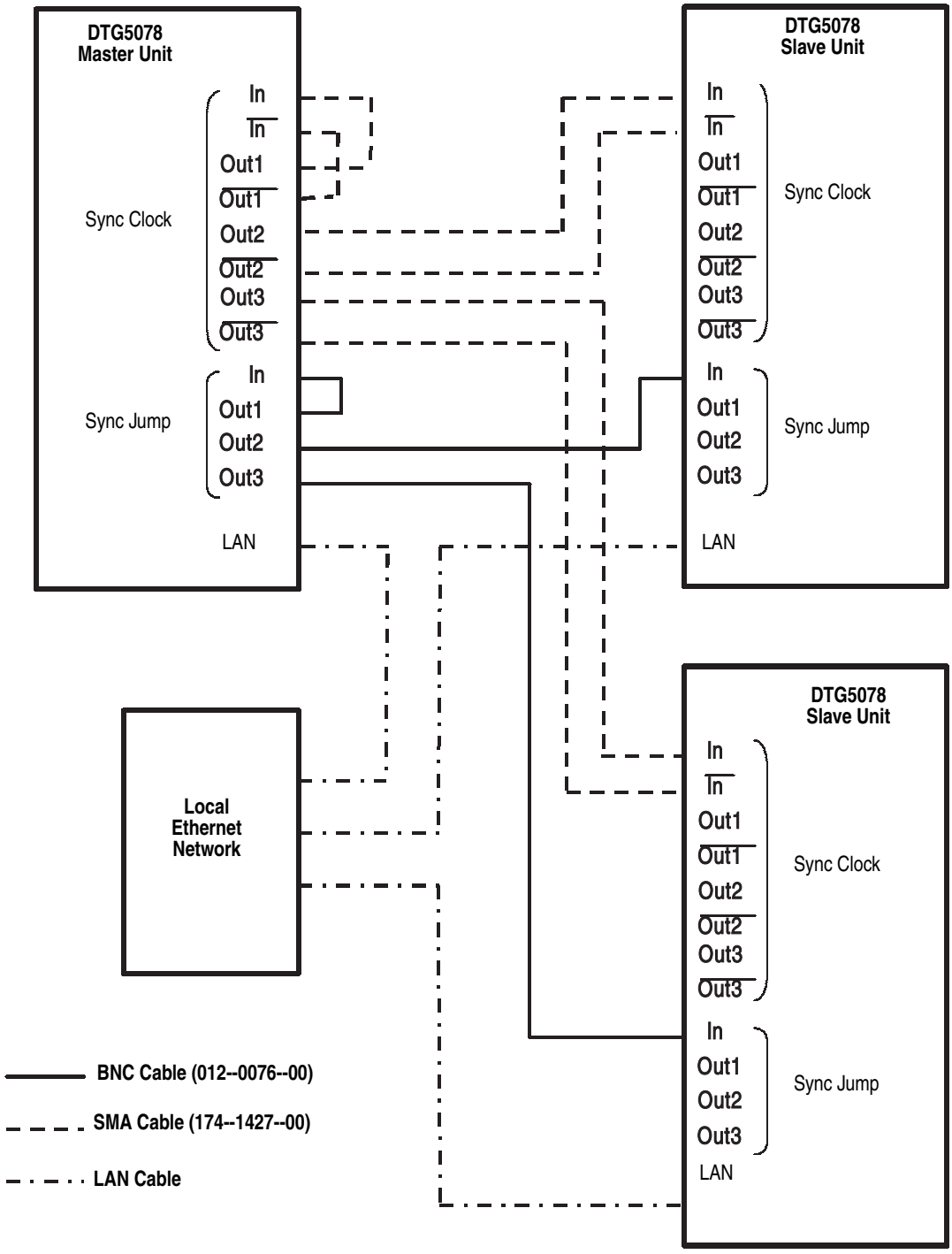


Figure 2-5: DTG5078 Master-Slave connection

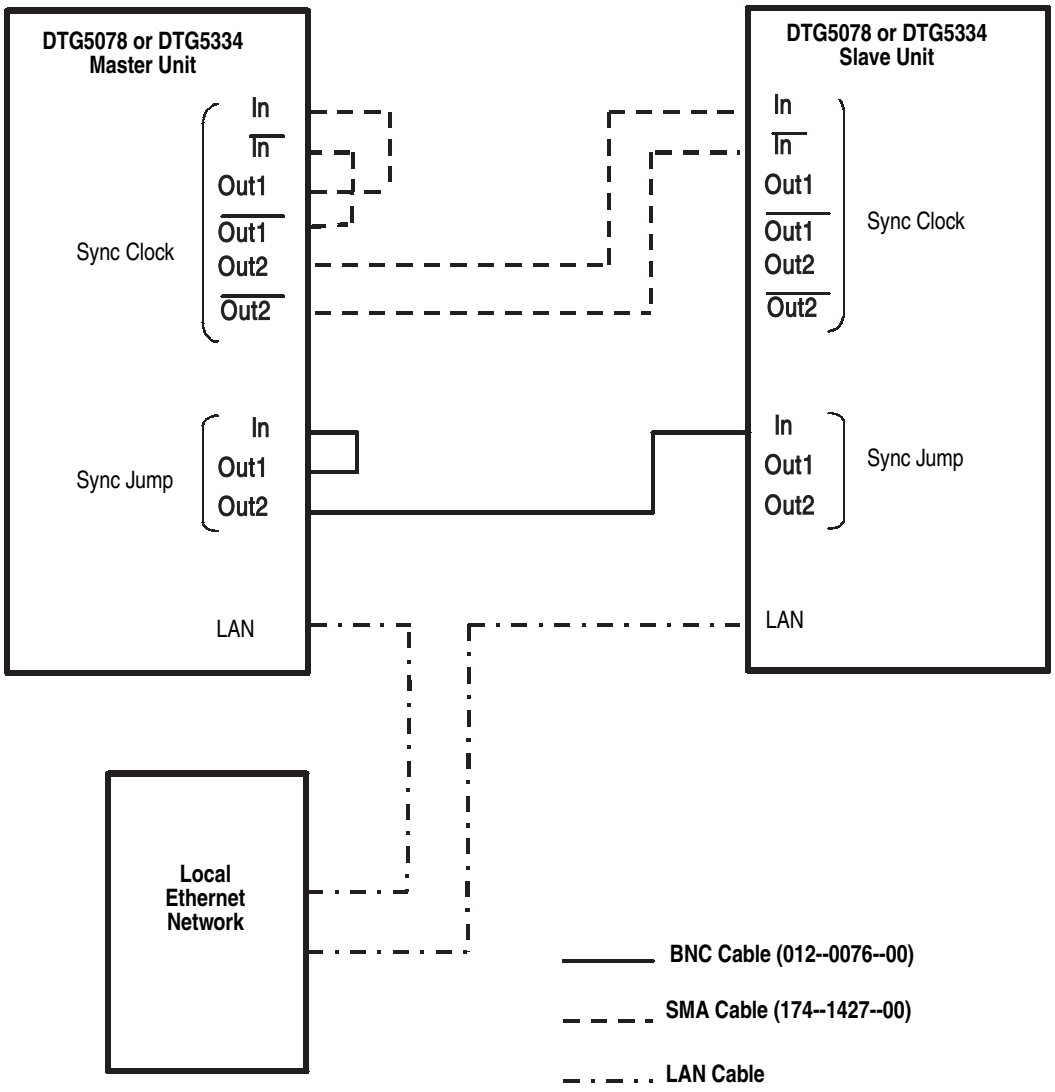


Figure 2-6: DTG5274/DTG5334 Master-Slave connection

Table 2-20: Event input

Characteristics	Description
Connector	BNC front
Impedance	1 kΩ or 50 Ω
Polarity	Normal or Invert
Input Voltage Range	–10 V to 10 V, 1 kΩ selected –5 V to 5 V, 50 Ω selected
Threshold	
Level	–5.0 V to 5.0 V
Resolution	0.1 V
Required Minimum Input Swing	1.0 V_{p-p}, 1 k Ω selected 0.5 V_{p-p}, 50 Ω selected
Required Minimum Pulse Width	
DTG5078	32 H/W Clocks + 10 ns
DTG5274 and DTG5334	128 H/W Clocks + 10 ns
Maximum Delay Time to Data Output (Td4)	at Asynchronous Jump Mode, refer to Figure 2-4.
DTG5078	402 H/W Clocks
DTG5274	1621 H/W Clocks
DTG5334	1643 H/W Clocks
Event Holdoff Time (Td5)	at Asynchronous Jump Mode, refer to Figure 2-4.
DTG5078	320 H/W Clocks
DTG5274 and DTG5334	1280 H/W Clocks

Table 2-21: CPU module and peripheral devices

Characteristics	Description
CPU	Celeron 566 MHz
Core Chip	Intel 815E (815GMCH + ICH12)
DRAM	128 MB SDRAM
Storage	
Hard Disk	≥20 GB, User usable area is about 90%
USB	USB 1.1 Series A 2ch Receptacle, rear Series A 1ch Receptacle, front right side
Ethernet	10BASE-T, 100BASE-TX, rear
Video Output	

Table 2-21: CPU module and peripheral devices (cont.)

Characteristics	Description
Connector	15 pin Dsub, rear
Format	VGA (640 X 480), SVGA (800 X 600), XGA (1024 X 768), SXGA (1280 X 1024), UXGA (1600 X 1200)
GPIB	24 pin, IEEE488.2, rear
Drive	Floppy disk 1.44 MB, front CD-ROM, rear
Keyboard Connector	PS/2 type connector (6-pin mini-DIN), rear
Mouse Connector	PS/2 type connector (6-pin mini-DIN), rear
Serial Port	RS232C, 9 pin Dsub, rear
Physical Specifications	Comply with IEEE1101.10 233.4 mm (W) x 160 mm (D) x 40 mm (H)
Real Time Clock	
Lifetime	>5 years
Type	Coin type lithium battery, CR2032 (Li 3 V 220 mAh)

Table 2-22: Display

Characteristics	Description
Display Area	Horizontal: 170.4 mm (6.71 in) Vertical: 127.8 mm (5.03 in)
Resolution	800 (H) x 600 (V) pixels (SVGA)

Output Pattern

Table 2-23: DG mode

Characteristics	Description	PV reference page
Data Format		
Slot A to D	NRZ, RZ, R1	
Slot E to H	NRZ	

Table 2-23: DG mode (cont.)

Characteristics	Description	PV reference page
Data Rate		
DTG5078		
NRZ only	50 kb/s to 750 Mb/s, can be set up to 800 Mb/s	
with RZ/R1	50 kb/s to 375 Mb/s, can be set up to 400 Mb/s	
DTG5274		
NRZ only	50 kb/s to 2.7 Gb/s, can be set up to 3.35 Gb/s	
with RZ/R1	50 kb/s to 1.35 Gb/s, can be set up to 1.675 Gb/s	
DTG5334		
NRZ only	50 kb/s to 3.35 Gb/s, can be set up to 3.40 Gb/s	
with RZ/R1	50 kb/s to 1.675 Gb/s, can be set up to 1.70 Gb/s	
Data Rate Resolution		
Internal Clock	8 digits	
External Clock	4 digits	
External Phase Lock In	4 digits	
Clock Range	Refer to Table 2-24 and Table 2-25.	
Channel Addition	Slot E, F, G and H are not available in DTG5078. Refer to Figure 2-7 on page 2-25.	
Slot	A, B, C and D.	
Function	AND or XOR.	
Delay Offset		
Range	Refer to Table 2-26.	
Resolution		
DTG5078	1 ps	
DTG5274 and DTG5334	0.2 ps	
Lead Delay	Refer to Figure 2-8 for definition and Figure 2-9 for maximum lead delay.	
Range	Refer to Table 2-27.	
Resolution		
DTG5078	1 ps	
DTG5274 and DTG5334	0.2 ps	
✓Accuracy	The timing reference is the lead edge which lead delay of each channel set to 0 ns. Skew calibration includes temperature calibration.	
DTG5078	±100 ps, after skew calibration at + 20 °C to + 30 °C ambient temperature. (Slot A, B, C, D) ±150 ps, after skew calibration at + 20 °C to + 30 °C ambient temperature. (Slot E, F, G, H)	page 1-59
DTG5274 and DTG5334	±100 ps, after skew calibration at + 20 °C to + 30 °C ambient temperature.	

Table 2-23: DG mode (cont.)

Characteristics	Description	PV reference page
Trail Delay	Refer to Figure 2-8 for definition, available in RZ/R1.	
Slot	A, B, C and D.	
Range	Refer to Table 2-28.	
Resolution	5 ps	
✓Accuracy	±100 ps, after skew calibration at + 20 °C to + 30 °C ambient temperature.	page 1-59
	The timing reference is the lead edge which lead delay of each channel set to 0 ns. Skew calibration includes temperature calibration.	
Duty Cycle	Refer to Figure 2-8 for definition, available in RZ/R1.	
Slot	A, B, C and D.	
Range	(Trail Delay – Lead Delay) / Period x 100	
Resolution	0.1%	
Pulse Width	Refer to Figure 2-8 for definition, available in RZ/R1.	
Slot	A, B, C and D.	
Range	Duty x Period / 100 or Trail Delay – Lead Delay	
Resolution	5 ps	
Phase	Phase = Lead Delay / Period x 100 (%)	
Resolution	0.1%	
Differential Timing Offset [1]		
Range	–1.0 ns to 1.0 ns	
Resolution		
DTG5078	1 ps	
DTG5274 and DTG5334	0.2 ps	
Skew Calibration	Only the skew between channels of same type output module is calibrated.	
Range	500 ps	
✓Accuracy		
DTG5078	100 ps, after skew calibration (Slot A, B, C, D) 200 ps, after skew calibration (Slot E, F, H, G)	page 1-59
DTG5274 and DTG5334	100 ps, after skew calibration	
✓Random Jitter	Measured by RMS jitter in Measurement function of CSA8000 + 80E03.	
DTG5078 (using DTGM20 or DTGM21)	<4 ps rms, at 750 Mb/s, delay = 0.0 ns, amplitude = 0.8 V_{p-p}, data format = NRZ, slew rate = 2.25 V/ns, jitter mode = off	page 1-66
DTG5274 (using DTGM30)	<3 ps rms, at 2.7 Gb/s, delay = 0.0 ns, amplitude = 0.8 V_{p-p}, data format = NRZ, jitter mode = off	
DTG5334 (using DTGM30)	<3 ps rms, at 3.35 Gb/s, delay = 0.0 ns, amplitude = 0.8 V_{p-p}, data format = NRZ, jitter mode = off	

Table 2-23: DG mode (cont.)

Characteristics	Description	PV reference page
✓Total Jitter	Measured with PRBS2^15–1 pattern. Measured by RMS Jitter and Pk-Pk Jitter in Measurement function of CSA8000 + 80E03.	
DTG5078 (using DTGM20 or DTGM21)	<18 ps rms, (<85 ps $_{p-p}$, typical), at 750 Mb/s, delay = 0.0 ns, amplitude = 0.8 V, Data Format = NRZ, and Jitter mode off	page 1-69
DTG5274 (using DTGM30)	<16 ps rms, (<60 ps $_{p-p}$, typical), at 2.7 Gb/s, delay = 0.0 ns, amplitude = 0.8 V, Data Format = NRZ, and Jitter mode off	
DTG5334 (using DTGM30)	<15 ps rms, (<60 ps $_{p-p}$, typical), at 3.35 Gb/s, delay = 0.0 ns, amplitude = 0.8 V, Data Format = NRZ, and Jitter mode off	
Total Jitter[2]	Measured with the DTGM30 (serial numbers B010627-B010629, B020630-B020634, and B020652 and above)	
DTG5334 (serial numbers B020296 and above only)	<44 ps $_{p-p}$ at 3.35 Gb/s, delay = 0.0 ns, amplitude = 0.4 V $_{p-p}$, offset = 0.0 V, Data Format = NRZ, and Jitter mode off, at an ambient temperature of 20 °C to 30 °C	
Cross Point [3]		
Slot	A, B, C, and D	
Range	30% to 70%	
Resolution	1%	
Jitter Performance [4]		
Mode	All Pattern Jitter, Partial Pattern Jitter	
All Pattern Jitter		
Jitter Profile	Sine, Gaussian Noise, Square, and Triangle.	page 1-53
Jitter Frequency	0.015 Hz to 1.56 MHz	
Jitter Frequency Resolution	4 digits or 1 mHz	
Jitter Amplitude	Refer to Table 2-29.	
Resolution	10 ps or 0.01 UI	
Partial Pattern Jitter		
Jitter Profile	Sine, Gaussian Noise, Square, and Triangle.	page 1-55
Jitter Frequency	0.015 Hz to 1.56 MHz	
Jitter Frequency Resolution	4 digits or 1 mHz	
Jitter Amplitude	Refer to Table 2-29.	
Resolution	10 ps or 0.01 UI	

1 Lead Delay + Differential Timing Offset have to be within the range of Lead Delay. Trail Delay + Differential Timing Offset have to be within the range of Trail Delay.

2 This specification is adapted only to the combination of the DTG5334 with serial numbers B020296 and above, and the DTGM30 with serial numbers B010627-B010629, B020630-B020634, and B020652 and above. Applies only to slot B, channels 1 and 2, and slot C, channel 1. Measured per HDMI CTS Version 1.3, using PRBS 2^15-1 pattern. May be measured using a DSA70804 with two P7313SMA probes and HT3 HDMI application software, or may be measured using a CSA8200 with 80E03 or 80E04 in accordance with the performance verification procedure.

3 This function is available when the DTGM30, DTGM31, or DTGM32 output module is used and the data format is set to NRZ.

4 Jitter Performance is available only for Ch1 in slot A. When this function is activated, Ch2 in slot A output is disabled.

Table 2-24: Clock range in NRZ

Clock		Period		Hardware Clock	Vector Rate	Minimum Block Length in Hardware Sequence (DTG5334/ DTG5274/ DTG5078)	Block Size Granularity (DTG5334/ DTG5274/ DTG5078)
From	To	From	To				
Max Freq.	200 Mb/s	Min Period	5 ns	<200 MHz	1	960/960/240	4/4/1
250 Mb/s	100 Mb/s	4 ns	10 ns	500 MHz to 200 MHz	2	480/480/120	2/2/1
125 Mb/s	50 Mb/s	8 ns	20 ns		4	240/240/60	1/1/1
62.5 Mb/s	25 Mb/s	16 ns	40 ns		8	120/120/30	
50 Mb/s	20 Mb/s	20 ns	50 ns		10	96/96/24	2/2/1
25 Mb/s	10 Mb/s	40 ns	100 ns		20	48/48/12	1/1/1
12.5 Mb/s	5 Mb/s	80 ns	200 ns		40	24/24/6	
6.25 Mb/s	2.5 Mb/s	160 ns	400 ns		80	12/12/3	
5 Mb/s	2 Mb/s	200 ns	500 ns		100	10/10/3	
2.5 Mb/s	1 Mb/s	400 ns	1 µs		200	5/5/2	
1.25 Mb/s	500 kb/s	800 ns	2 µs		400	3/3/1	
625 kb/s	250 kb/s	1.6 µs	4 µs		800	2/2/1	
500 kb/s	200 kb/s	2 µs	5 µs		1000	1/1/1	
250 kb/s	100 kb/s	4 µs	10 µs		2000		
125 kb/s	50 kb/s	8 µs	20 µs		4000		

Table 2-25: Clock range in RZ/R1

Clock		Period		Hardware Clock	Vector Rate	Minimum Block Length in Hardware Sequence (DTG5334/ DTG5274/ DTG5078)	Block Size Granularity (DTG5334/ DTG5274/ DTG5078)
From	To	From	To				
Max Freq.	100 Mb/s	–	10 ns	<200 MHz	2	480/480/120	2/2/1
125 Mb/s	50 Mb/s	8 ns	20 ns	500 MHz to 200 MHz	4	240/240/60	1/1/1
62.5 Mb/s	25 Mb/s	16 ns	40 ns		8	120/120/30	
50 Mb/s	20 Mb/s	20 ns	50 ns		10	96/96/24	2/2/1
25 Mb/s	10 Mb/s	40 ns	100 ns		20	48/48/12	1/1/1
12.5 Mb/s	5 Mb/s	80 ns	200 ns		40	24/24/6	
6.25 Mb/s	2.5 Mb/s	160 ns	400 ns		80	12/12/3	
5 Mb/s	2 Mb/s	200 ns	500 ns		100	10/10/3	
2.5 Mb/s	1 Mb/s	400 ns	1 µs		200	5/5/2	
1.25 Mb/s	500 kb/s	800 ns	2 µs		400	3/3/1	
625 kb/s	250 kb/s	1.6 µs	4 µs		800	2/2/1	
500 kb/s	200 kb/s	2 µs	5 µs		1000	1/1/1	
250 kb/s	100 kb/s	4 µs	10 µs		2000		
125 kb/s	50 kb/s	8 µs	20 µs		4000		

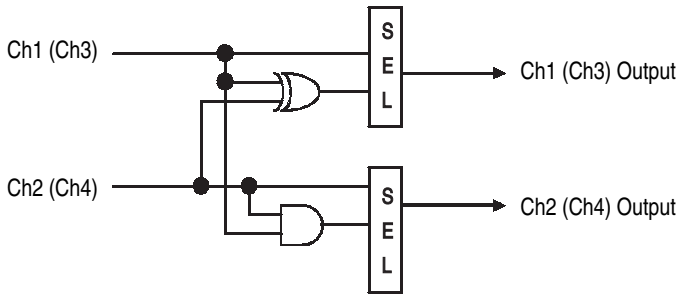
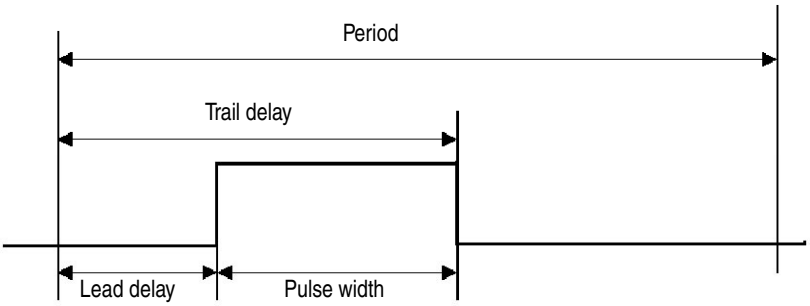


Figure 2-7: Channel addition function

Table 2-26: Delay offset

Long Delay	Format	Period	Delay Offset
Off	---	---	0 to 5 ns
On	NRZ	≥1.25 ns	SW Sequence: 0 to 600 ns HW Sequence: 0 to 300 ns
		<1.25 ns	SW Sequence: 0 to 480 x Period HW Sequence: 0 to 240 x Period
	RZ/R1	≥2.5 ns	SW Sequence: 0 to 600 ns HW Sequence: 0 to 300 ns
		<2.5 ns	SW Sequence: 0 to 240 x Period HW Sequence: 0 to 120 x Period



Phase = Lead delay / Period x 100 (%)
Duty = Pulse width / Period x 100 (%)

Figure 2-8: The definitions of lead/trail delay and pulse width

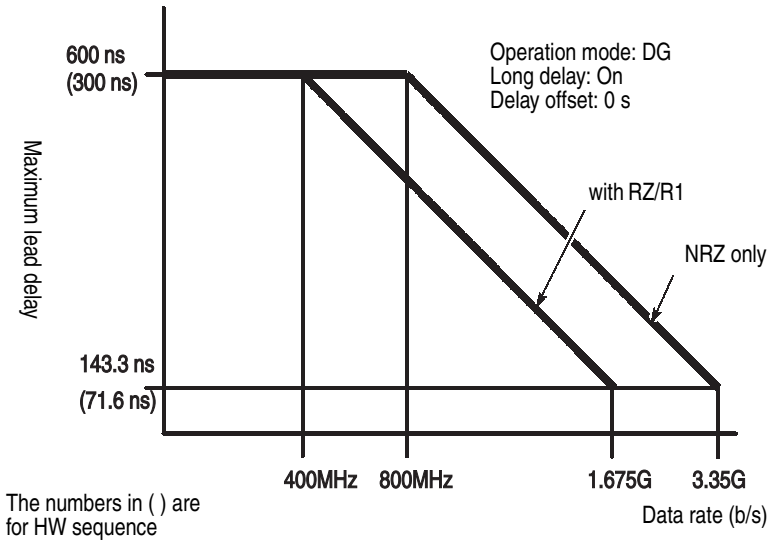


Figure 2-9: Maximum lead delay

Table 2-27: Lead delay

Long Delay	Format	Period	Lead Delay[1]
Off	---	---	0 (–Delay Offset) to 5 ns (–Delay Offset)
On	NRZ	≥1.25 ns	SW Sequence: 0 (–Delay Offset) to 600 ns (–Delay Offset) HW Sequence: 0 (–Delay Offset) to 300 ns (–Delay Offset)
		<1.25 ns	SW Sequence: 0 (–Delay Offset) to 480 x Period (–Delay Offset) HW Sequence: 0 (–Delay Offset) to 280 x Period (–Delay Offset)
	RZ/R1	≥2.5 ns	SW Sequence: 0 (–Delay Offset) to 600 ns (–Delay Offset) HW Sequence: 0 (–Delay Offset) to 300 ns (–Delay Offset)
		<2.5 ns	SW Sequence: 0 (–Delay Offset) to 240 x Period (–Delay Offset) HW Sequence: 0 (–Delay Offset) to 120 x Period (–Delay Offset)

[1] **Lead delay should be between 0% and 100% in Duty conversion and Pulse Width is from 290 ps to (Period – 290 ps).**

Table 2-28: Trail delay

Long Delay	Period	Trail Delay
Off	<10 ns	290 ps (–Delay Offset) to 5 ns + Period / 2(–Delay Offset) [1, 2]
	≥10 ns	Period / 2 – Delay Offset to 5 ns + Period / 2 (–Delay Offset)[2]
On	---	See footnote 2

1 **When the jitter generation is enabled, the range of trail delay for mainframe 1, slot A, CH1 is set as follows:**
290 ps (–Delay Offset) to 5 ns + 290 ps (–Delay Offset)

2 **Trail delay should be between 0% and 100% in Duty conversion and Pulse Width is from 290 ps to (Period – 290 ps).**

Table 2-29: Jitter amplitude

Jitter Edge	Data Format	Jitter Mode	Jitter Profile	Maximum Jitter Amplitude (UI p-p)
Both	NRZ	All Pattern Jitter	Sine	The larger of the numerical values derived by the formula below. (1 – Minimum Pulse Width / Period) * 9.9e5 / Fj or 1 – Minimum Pulse Width / Period *Note: Condition 1 should be fulfilled. See Condition 1 below.*
			Others	1 – 290 ps / Period
		Partial Pattern Jitter	Any	*Note: Condition 1 should be fulfilled.*
	RZ/R1	All Pattern Jitter	Sine	(Period – Pulse Width - 290 ps) / Period * 9.9e5 / Fj *Note: Condition 1 should be fulfilled.*
			Others	(Period – Pulse Width - 290 ps) / Period
		Partial Pattern Jitter	Any	*Note: Condition 1 should be fulfilled.*
Rise/ Fall	NRZ	Any	Any	(Period – 290 ps) / Period * 2 *Note: Condition 1 should be fulfilled.*
	RZ/R1	Any	Any	(min (Pulse Width, Period – Pulse Width) – 290 ps) / Period * 2 *Note: Condition 1 should be fulfilled.*

Fj: Jitter Frequency
Ajui_pp: Jitter Amplitude expressed with UIpk–pk
Ajui_rms: Jitter Amplitude expressed with UIrms
Ajs_pp: Jitter Amplitude expressed with s pk–pk
Ajs_rms: Jitter Amplitude expressed with s rms
Ajui_pp * Period = Ajs_pp
Ajui_rms * Period = Ajs_rms

Condition 1
Lead Delay + Ajs_pp/2 ≤ Maximum of Lead Delay and
Lead Delay – Ajs_pp/2 ≥ Minimum of Lead Delay

If Ch1 of Slot A is set to RZ/R1, the following condition 2 should be also fulfilled.

Condition 2
Trail Delay + Ajs_pp/2 ≤ Maximum of Trail Delay and
Trail Delay – Ajs_pp/2 ≥ Minimum of Trail Delay

Table 2-30: PG mode

Characteristics	Description	PV reference page
Slot	A, B, C and D. ***Note:*** *Slot E, F, G and H are not available in PG Mode.*	
Frequency		
DTG5078	50 kHz to 375 MHz, can be set up to 400 MHz	
DTG5274	50 kHz to 1.35 GHz, can be set up to 1.675 GHz	
DTG5334	50 kHz to 1.675 GHz, can be set up to 1.70 GHz	
Frequency Resolution		
Internal Clock	8 digits	
External Clock	4 digits	
External Phase Lock In	4 digits	
Run Mode	Continuous or Burst	
Burst Count	1 to 65,536	
Pulse Rate	Off, 1/1, 1/2, 1/4, 1/8, or 1/16	
Channel Addition	Refer to Figure 2-7 on page 2-25.	
Slot	A, B, C, and D ***Note:*** *Slot E, F, G and H are not available in DTG5078.*	
Function	AND or XOR	
Delay Offset		
Range	0 to 3 µs	
DTG5078	1 ps	
DTG5274 and DTG5334	0.2 ps	
Lead Delay	Refer to Figure 2-8 for definition.	
Range [1]		
>3 µs	0 (–Delay Offset) to Period (–Delay Offset)	
<3 µs	0 (–Delay Offset) to 3µs (–Delay Offset)	
Resolution [1]		
DTG5078	1 ps	
DTG5274 and DTG5334	0.2 ps	
✓Accuracy [2]		
DTG5078, DTG5274 and DTG5334	±100 ps, after skew calibration at + 20 °C to + 30 °C ambient temperature.	page 1-59
Trail Delay	Refer to Figure 2-8 for definition.	
Resolution[3]	5 ps	
✓Accuracy [2]	±100 ps, after skew calibration at + 20 °C to + 30 °C ambient temperature.	page 1-59

Table 2-30: PG mode (cont.)

Characteristics	Description	PV reference page
Duty Cycle	Refer to Figure 2-8 for definition.	
Range	(Trail Delay – Lead Delay) / Period x Pulse Rate x 100	
Resolution	0.1%	
Pulse Width	Refer to Figure 2-8 for definition.	
Range	Duty x Period x Pulse Rate / 100 or Trail Delay – Lead Delay	
Resolution	5 ps	
Phase	Phase = Lead Delay / Period x Pulse Rate x 100 (%)	
Resolution	0.1%	
Differential Timing Offset [4]		
Range	–1.0 ns to 1.0 ns	
Resolution		
DTG5078	1 ps	
DTG5274 and DTG5334	0.2 ps	
Skew Calibration	Only the skew between channels of same type output module is calibrated.	
Range	500 ps	
✓Accuracy		
DTG5078, DTG5274 and DTG5334	100 ps, after skew calibration	page 1-59
✓Random Jitter	Measured by RMS jitter in Measurement function of CSA8000 + 80E03.	
DTG5078 (using DTGM20 or DTGM21)	<4 ps_{rms}, at 375 MHz, delay = 0.0 ns, amplitude = 0.8 V_{p-p}, slew rate = 2.25 V/ns, jitter mode = off	page 1-66
DTG5274 (using DTGM30)	<4 ps_{rms}, at 1.35 GHz, delay = 0.0 ns, amplitude = 0.8 V_{p-p}, jitter mode = off	
DTG5334 (using DTGM30)	<4 ps_{rms}, at 1.675 GHz, delay = 0.0 ns, amplitude = 0.8 V_{p-p}, jitter mode = off	

1 Lead delay should be between 0% and 100% in Duty conversion and Pulse Width is from 290 ps to (Period – 290 ps).

2 The timing reference is the lead edge which lead delay of each channel set to 0 ns.
Skew calibration includes temperature calibration.

3 Trail delay should be between 0% and 100% in Duty conversion and Pulse Width is from 290 ps to (Period x Pulse Rate – 290 ps).

4 Lead Delay + Differential Timing Offset have to be within the range of Lead Delay.
Trail Delay + Differential Timing Offset have to be within the range of Trail Delay.

Electrical Specification-Output Module

Table 2-31: DTGM10

Characteristics	Description	PV reference page
Connector	SMA (4 ea)	
Output Signal Type	Single-ended	
Number of channels	4 channels when used in DTG5078 2 channels when used in DTG5274 or DTG5334	
Source Impedance	50 Ω	
Polarity	Normal or Inverted	
Output Voltage[1]		
High Level (VOH) range	–1.25 V to + 2.00 V into 50 Ω to GND –2.50 V to + 7.00 V into 1 MΩ to GND	
Low Level (VOL) range	–1.50 V to + 1.75 V into 50 Ω to GND –3.00 V to + 6.50 V into 1 MΩ to GND	
Amplitude (VOH - VOL) range	0.25 V_{p-p} to 3.50 V_{p-p} into 50 Ω to GND 0.50 V_{p-p} to 10.00 V_{p-p} into 1 MΩ to GND	
Offset ((VOH + VOL) / 2) range	Depends on the limit of VOH and VOL set by the user.	
Resolution	5 mV	
Maximum Output Voltage	+ 7.0 V	
Minimum Output Voltage	–3.0 V	
✓DC Accuracy	(±3% of the set value) ±50 mV into 50 Ω to GND, after level calibration at + 20 °C to + 30 °C ambient temperature.	page 1-80
Maximum Output Current	±40 mA Refer to Figure 2-11 for the equivalent circuit.	
Rise /Fall Time (20% to 80%), typical		
at high 1.0 V, low 0 V	<540 ps, into 50 Ω to GND	
at high 2.0 V, low –1.0 V	<1.5 ns, into 50 Ω to GND	
Slew Rate Control		
Range	0.65 V/ns to 1.30 V/ns, into 50 Ω to GND	
Resolution	10 mV/ns	
Aberration, typical		
Positive Overshoot	<16% at High = 1.0 V, Low = 0 V	
Negative Overshoot	<16% at High = 1.0 V, Low = 0 V	
Delay Time from Sync Out to Data Output (Td2), typical		
DTG5078 (after Skew Calibration)	4.2 ns	
DTG5274 (after Skew Calibration)	3.3 ns	
DTG5334 (after Skew Calibration)	3.4 ns	

[1] **Output voltage (Vout) should fulfill the following two conditions.**

R_L = Term R, Vtt = Term V

1) $-0.04 \times R_L + Vtt \leq Vout \leq 0.04 \times R_L + Vtt$

2) $-3.00 \leq Vout \leq 7.00$

Note. *These conditions are automatically fulfilled, when setup.*

Table 2-32: DTGM20

Characteristics	Description	PV reference page
Connector	SMA (4 ea)	
Output Signal Type	Single-ended	
Number of channels	4 channels when used in DTG5078 2 channels when used in DTG5274 and DTG5334	
Source Impedance	50 Ω	
Polarity	Normal or Inverted	
Output Voltage[2]		
High Level (VOH)	–0.90 V to + 2.5 V into 50 Ω to GND –1.80 V to + 5.0 V into 1 MΩ to GND	
Low Level (VOL)	–1.00 V to +2.40 V into 50 Ω to GND –2.00 V to + 4.80 V into 1 MΩ to GND	
Amplitude (VOH _ VOL)	0.10 V_{p-p} to 3.50 V_{p-p} into 50 Ω to GND 0.20 V_{p-p} to 7.00 V_{p-p} into 1 MΩ to GND	
Offset ((VOH + VOL) / 2)	Depends on the limit of VOH and VOL set by the user.	
Maximum Output Voltage	+ 5.0 V	
Minimum Output Voltage	–2.0 V	
Resolution	5 mV	
✓DC Accuracy	(±3% of the set value) ±50mV into 50 Ω to GND, after level calibration at + 20 °C to + 30 °C ambient temperature.	page 1-80
Maximum Output Current	±80 mA, refer to Figure 2-11 for the equivalent circuit.	
Rise /Fall Time (20% to 80%), typical		
at high 1.0 V, low 0 V	<340 ps, into 50 Ω to GND	
at high 2.0 V, low -1.0 V	<760 ps, into 50 Ω to GND	
Slew Rate Control		
Range	0.63 V/ns to 2.25 V/ns, into 50 Ω to GND	
Resolution	10 mV/ns	
Aberration, typical		
Positive Overshoot	<15% at High = 1.0 V, Low = 0 V	
Negative Overshoot	<15% at High = 1.0 V, Low = 0 V	
Delay Time from Sync Out to Data Output (Td2), typical		
DTG5078 (after Skew Calibration)	4.2 ns	
DTG5274 (after Skew Calibration)	3.3 ns	
DTG5334 (after Skew Calibration)	3.3 ns	

[2] **Output voltage (Vout) should fulfill the following two conditions.**
R_L = Term R, Vtt = Term V
1) $-0.08 \times R_L + Vtt \leq Vout \leq 0.08 \times R_L + Vtt$
2) $-2.00 \leq Vout \leq 5.00$

Note. *These conditions are automatically fulfilled, when setup.*

Table 2-33: DTGM30

Characteristics	Description	PV reference page
Connector	SMA (4 ea)	
Output Signal Type	Complementary	
Number of channels	2	
Source Impedance	50 Ω	
Polarity	Normal or Inverted	
Output Voltage	Refer to Figure 2-10 on page 2-41.	
High Level (VOH)[1]	–1.00 V to + 2.47 V into 50 Ω to GND –1.94 V to + 7.00 V into 1 MΩ to GND	
Low Level (VOL)[2]	–2.00 V to + 2.44 V into 50 Ω to GND –2.00 V to + 6.94 V into 1 MΩ to GND	
Amplitude (VOH - VOL) [3]	30 mV_{p-p} to 1.25 V_{p-p} into 50 Ω to GND 60 mV_{p-p} to 2.50 V_{p-p} into 1 MΩ to GND	
Offset ((VOH + VOL) / 2)	Depends on the limit of VOH and VOL set by the user.	
Maximum Output Voltage	+ 7.0 V	
Minimum Output Voltage	–2.0 V	
Resolution	5 mV	
✓DC Accuracy	(±3% of the set value) ±50mV into 50 Ω to GND, after level calibration at + 20 °C to + 30 °C ambient temperature.	page 1-80
Maximum Output Current	±80 mA Refer to Figure 2-12 for the equivalent circuit.	
Rise /Fall Time (20% to 80%), typical		
at high 0.1 V, low 0 V	<95 ps into 50 Ω to GND	
at high 1.0 V, low 0 V	<110 ps into 50 Ω to GND	
Aberration, typical		
Positive Overshoot	<10% at High = 1.0 V, Low = 0 V	
Negative Overshoot	<10% at High = 1.0 V, Low = 0 V	
Total Jitter[4]		
DTG5078	<16 ps_{rms} (typical 60 ps_{p-p}) at 750 Mb/s Delay = 0.0 ns, Amplitude = 0.8 V_{p-p}, Data format = NRZ, Jitter mode = off	
DTG5274	<16 ps_{rms} (typical 60 ps_{p-p}) at 2.7 Gb/s Delay = 0.0 ns, Amplitude = 0.8 V_{p-p}, Data format = NRZ, Jitter mode = off	
DTG5334	<15 ps_{rms} (typical 50 ps_{p-p}) at 3.35 Gb/s Delay = 0.0 ns, Amplitude = 0.8 V_{p-p}, Data format = NRZ, Jitter mode = off	
Delay Time from Sync Out to Data Output (Td2), typical		
DTG5078 (after Skew Calibration)	3.5 ns	
DTG5274 (after Skew Calibration)	2.7 ns	
DTG5334 (after Skew Calibration)	2.6 ns	

1 **High level (VoH) should fulfill the following formulas simultaneously.**
R_L = Term R, Vtt = Term V
VOH ≤ 7.00
VOH ≤ (7.00 x RL + 50 x Vtt) / (RL + 50)
VOH ≤ RL / 50 x (2.5 – 0.06 x RL / (RL + 50)) + Vtt
VOH ≥ (–2.00 x RL + 50 x Vtt) / (RL + 50)
VOH ≥ Vtt – RL / 50

2 **Low level (VoL) should fulfill the following formulas simultaneously.**
R_L = Term R, Vtt = Term V
VOL ≥ –2.00
VOL ≥ (50 x Vtt – 4.5 x RL) / (RL + 50)
VOL ≥ Vtt – RL (0.02 + 2.5 / (RL + 50))
VOL < ((2.5 – 0.06) x RL / 50) + Vtt

3 **Amplitude should fulfill the following formulas simultaneously.**
R_L = Term R, Vtt = Term V
VOH – VOL > 2 x (Vtt – RL/50 - Offset)
VOH – VOL > 2 x ((RL x (–2) + 50 x Vtt) / ((RL + 50) – Offset))
VOH – VOL < 2 x ((2.5 x RL – 50 x Offset + 50 x Vtt) / (2 x RL + 50))
VOH – VOL < 2 x ((7 x RL – 50 x Vtt) / (RL + 50) – Offset)

4 **Total Jitter is measured with PRBS2^15-1 pattern. Measured by "Histogram WIndow" of CSA8000 + 80E03.**

Table 2-34: DTGM21

Characteristics	Description	PV reference page
Connector	SMA (4 ea)	
Output Signal Type	Single-ended	
Number of channels	4 channels when used in DTG5078 2 channels when used in DTG5274 or DTG5334	
Source Impedance[1]	23 Ω or 50 Ω	
Polarity	Normal or Inverted	
Output Voltage[2, 3]		
High Level (VOH) range	–1.55 V to + 3.70 V into 50 Ω to GND at 23 Ω source impedance –1.10 V to + 2.70 V into 50 Ω to GND at 50 Ω source impedance –2.20 V to + 5.40 V into 1 MΩ to GND at 50 Ω source impedance	
Low Level (VOL) range	–1.65 V to + 3.60 V into 50 Ω to GND at 23 Ω source impedance –1.20 V to + 2.60 V into 50 Ω to GND at 50 Ω source impedance –2.40 V to + 5.20 V into 1 MΩ to GND at 50 Ω source impedance	
Amplitude (VOH - VOL) range	0.10 V_{p-p} to 5.35 V_{p-p} into 50 Ω to GND at 23 Ω source impedance 0.10 V_{p-p} to 3.90 V_{p-p} into 50 Ω to GND at 50 Ω source impedance 0.20 V_{p-p} to 5.20 V_{p-p} into 1 MΩ to GND at 50 Ω source impedance	
Offset ((VOH + VOL) / 2) range	Depends on the limit of VOH and VOL set by the user.	
Resolution	5 mV	
Maximum Output Voltage	+ 5.4 V	
Minimum Output Voltage	–2.4 V	

Table 2-34: DTGM21 (cont.)

Characteristics	Description	PV reference page
✓DC Accuracy[4]	(±3% of the set value) ±50 mV into 50 Ω to GND, after level calibration at + 20 °C to + 30 °C ambient temperature.	page 1-80
Maximum Output Current	±80 mA Refer to Figure 2-11 on page 2-41 for the equivalent circuit.	
Rise /Fall Time (20% to 80%), typical		
at high 1.0 V, low 0 V	<350 ps, into 50 Ω to GND	
at high 2.7 V, low 0 V	<780 ps, into 50 Ω to GND	
at high 3.7 V, low –1.65 V	<1 ns, into 50 Ω to GND	
Aberration, typical		
Positive Overshoot	<15% at High = 1.0 V, Low = 0 V	
Negative Overshoot	<15% at High = 1.0 V, Low = 0 V	
Output Leakage in Inhibit	<±1.5 μA	
Delay Time from Sync Out to Data Output (Td2), typical		
DTG5078 (after Skew Calibration)	4.9 ns	
DTG5274 (after Skew Calibration)	3.5 ns	
DTG5334 (after Skew Calibration)	3.6 ns	
Inhibit Input		
Connector	SMB front	
Impedance	1 kΩ, DC coupled	
Level	3.3 V LVCOMS (High: 3.3 V, Low: 0 V)	
Maximum Input Voltage	+3.5 V	
Output State	High: Inhibit Low: Active	
Required Minimum Pulse Width (Pw5)	>8 ns, refer to Figure 2-4.	
Delay Time from Inhibit In to Data Output (Td7)	Active to Inhibit: approximately 13 ns at 50 Ω load Inhibit to Active: approximately 12 ns at 50 Ω load Refer to Figure 2-4.	

1 **Source impedance is selected by internal bus conductor per channel.**
CH1: P540, CH2:P542, CH3:P544, CH4:P546
1 – 2 -> 50 Ω
2 – 3 -> 23 Ω

2 **Output voltage (Vout) should fulfill the following two conditions.**
R_L = Term R, Vtt = Term V
1) $-0.04 \times R_L + Vtt \leq Vout \leq 0.04 \times R_L + Vtt$
2) $-3.00 \leq Vout \leq 7.00$
Note. *These conditions are automatically fulfilled, when setup.*

3 **Recommended source impedance is 50 Ω for 1 MΩ external output load.**

4 **DC accuracy is specified for only 50 Ω load.**

Table 2-35: DTGM31

Characteristics	Description	PV reference page
Connector	SMA (2 ea)	
Output Signal Type	Complementary	
Number of channels	1 channel	
Source Impedance	50 Ω	
Polarity	Normal or Invert	
Output Voltage		
High Level (VOH)[1]	–1.00 V to + 2.47 V into 50 Ω to GND –1.94 V to + 7.0 V into 1 MΩ to GND	
Low Level (VOL)[2]	–2.00 V to +2.44 V into 50 Ω to GND –2.00 V to + 6.94 V into 1 MΩ to GND	
Amplitude (VOH _ VOL)[3]	0.03 V_{p-p} to 1.25 V_{p-p} into 50 Ω to GND 0.06 V_{p-p} to 2.50 V_{p-p} into 1 MΩ to GND	
Offset ((VOH + VOL) / 2)	Depends on the limit of VOH and VOL set by the user.	
Maximum Output Voltage	+ 7.0 V	
Minimum Output Voltage	–2.0 V	
Resolution	5 mV	
✓DC Accuracy	(±3% of the set value) ±50 mV into 50 Ω to GND, after level calibration at + 20 °C to + 30 °C ambient temperature.	page 1-80
Maximum Output Current	±80 mA, refer to Figure 2-11 on page 2-41 for the equivalent circuit.	
Rise /Fall Time (20% to 80%), typical		
at high 1.0 V, low 0 V	<95 ps, into 50 Ω to GND	
at high 2.0 V, low -1.0 V	<110 ps, into 50 Ω to GND	
Aberration, typical		
Positive Overshoot	<10% at High = 1.0 V, Low = 0 V	
Negative Overshoot	<10% at High = 1.0 V, Low = 0 V	
Total Jitter[4]		
DTG5078	<16 ps_{rms} (typical 65 ps_{p-p}) at 750 Mb/s, after Dj adjustment Delay = 0.0 ns, Amplitude = 0.8 V_{p-p}, Data format = NRZ, Jitter mode = off	
DTG5274	<14 ps_{rms} (typical 60 ps_{p-p}) at 2.7 Gb/s, after Dj adjustment Delay = 0.0 ns, Amplitude = 0.8 V_{p-p}, Data format = NRZ, Jitter mode = off	
DTG5334	<13 ps_{rms} (typical 50 ps_{p-p}) at 3.35 Gb/s, after Dj adjustment Delay = 0.0 ns, Amplitude = 0.8 V_{p-p}, Data format = NRZ, Jitter mode = off	
Delay Time from Sync Out to Data Output (Td2), typical		
DTG5078 (after Skew Calibration)	5.4 ns	
DTG5274 (after Skew Calibration)	4.4 ns	
DTG5334 (after Skew Calibration)	4.2 ns	

Table 2-35: DTGM31 (cont.)

Characteristics	Description	PV reference page
Jitter Control In		
Connector	SMA front	
Impedance	50 Ω (DC coupled)	
Input Amplitude Range	0 V_{p-p} to 1 V_{p-p} (DC coupled) Input impedance may exceed 1 V_{p-p} when jitter amplitude is set to the maximum jitter amplitude value. Refer to Figure 2-13 on page 2-42.	
Maximum Input Voltage	±1.0 V	
Maximum Jitter Amplitude	240 ps_{p-p}, at Data Rage ≤2.7 Gb/s {240 – 61.5 x (Data Rate – 2.7)} ps_{p-p}, at Data Rate >2.7 Gb/s Cross point should be around 50%. Refer to Figure 2-14 on page 2-43.	
Jitter Frequency Response	Refer to Figure 2-15 on page 2-43.	

1 **High level (VoH) should fulfill the following formulas simultaneously.**

R_L = Term R, Vtt = Term V

VOH ≤ 7.00

VOH ≤ (7.00 x RL + 50 x Vtt) / (RL + 50)

VOH ≤ RL / 50 x (2.5 – 0.06 x RL / (RL + 50)) + Vtt

VOH ≥ (– 2.00 x RL + 50 x Vtt) / (RL + 50)

VOH ≥ Vtt – RL / 50

2 **Low level (VoL) should fulfill the following formulas simultaneously.**

R_L = Term R, Vtt = Term V

VOL ≥ –2.00

VOL ≥ (50 x Vtt – 4.5 x RL) / (RL + 50)

VOL ≥ Vtt – RL (0.02 + 2.5 / (RL + 50))

VOL < ((2.5 – 0.06) x RL / 50) + Vtt

3 **Amplitude should fulfill the following formulas simultaneously.**

R_L = Term R, Vtt = Term V

VOH – VOL > 2 x (Vtt - RL/50 – Offset)

VOH – VOL > 2 x ((RL x (– 2) + 50 x Vtt) / ((RL + 50) – Offset))

VOH – VOL < 2 x ((2.5 x RL – 50 x Offset + 50 x Vtt) / (2 x RL + 50))

VOH – VOL < 2 x ((7 x RL – 50 x Vtt) / (RL + 50) – Offset)

4 **Total Jitter is measured with PRBS2^15-1 pattern. Measured by "Histogram WIndow" of CSA8000 + 80E03.**

Table 2-36: DTGM32

Characteristics	Description	PV reference page
Connector	SMA (2 ea)	
Output Signal Type	Complementary	
Number of channels	1 channel	
Required Minimum Pulse Width	>2.86 ns [1]	
Source Impedance	50 Ω	
Polarity	Normal or Invert	
Output Voltage		
High Level (VOH) [2]	–1.00 V to + 2.47 V into 50 Ω to GND –1.94 V to + 7.0 V into 1 MΩ to GND	
Low Level (VOL) [3]	–2.00 V to +2.44 V into 50 Ω to GND –2.00 V to + 6.94 V into 1 MΩ to GND	
Amplitude (VOH _ VOL) [4]	0.03 V_{p-p} to 1.25 V_{p-p} into 50 Ω to GND 0.06 V_{p-p} to 2.50 V_{p-p} into 1 MΩ to GND	
Offset ((VOH + VOL) / 2)	Depends on the limit of VOH and VOL set by the user.	
Maximum Output Voltage	+ 7.0 V	
Minimum Output Voltage	–2.0 V	
Resolution	5 mV	
✓DC Accuracy	(±3% of the set value) ±50 mV into 50 Ω to GND, after level calibration at + 20 °C to + 30 °C ambient temperature.	page 1-80
Maximum Output Current	±80 mA, refer to Figure 2-11 for the equivalent circuit.	
Rise /Fall Time (20% to 80%), typical		
at high 1.0 V, low 0 V	<95 ps, into 50 Ω to GND	
at high 2.0 V, low -1.0 V	<110 ps, into 50 Ω to GND	
Aberration, typical		
Positive Overshoot	<10% at High = 1.0 V, Low = 0 V	
Negative Overshoot	<10% at High = 1.0 V, Low = 0 V	
Total Jitter [5]		
Jitter Amplitude Range 1	<23 ps_{rms} (typical 100 ps_{p-p}) at 350 Mb/s Delay = 0.0 ns, Amplitude = 0.8 V_{p-p}, Data format = NRZ, Jitter mode = off	
Jitter Amplitude Range 2	<30 ps_{rms} (typical 130 ps_{p-p}) at 350 Mb/s Delay = 0.0 ns, Amplitude = 0.8 V_{p-p}, Data format = NRZ, Jitter mode = off	
Delay Time from Sync Out to Data Output (Td2), at Range 1, typical		
DTG5078 (after Skew Calibration)	8.0 ns	
DTG5274 (after Skew Calibration)	6.6 ns	
DTG5334 (after Skew Calibration)	6.6 ns	

Table 2-36: DTGM32 (cont.)

Characteristics	Description	PV reference page
Delay Time from Sync Out to Data Output (Td2), at Range 2, typical		
DTG5078 (after Skew Calibration)	11.7 ns	
DTG5274 (after Skew Calibration)	10.4 ns	
DTG5334 (after Skew Calibration)	10.3 ns	
Jitter Control In		
Connector	SMA front (2 ea), Input A and Input B. Input A and Input B are interchangeable. Jitter profile is the composite signal of Input A and Input B.	
Impedance	50 Ω (DC coupled)	
Input Amplitude Range	0 V_{p-p} to 1 V_{p-p} (DC coupled) Input impedance may exceed 1 V_{p-p} when jitter amplitude is set to the maximum jitter amplitude value. Refer to Figure 2-16.	
Maximum Input Voltage	±1.0 V	
Maximum Jitter Amplitude		
Range 1	1 ns_{p-p}	
Range 2	2 ns_{p-p}	
Jitter Frequency Response, typical	Refer to Figure 2-17 on page 2-44.	

1. When the following conditions are satisfied, the value of the Required Minimum Pulse becomes "> 1.34 ns":

- Data pattern is the clock pattern (1,0,1,0,.....) or a pattern like (1,1,1,0,0,0,1,1,1,0,0,0,.....) equivalent to a clock pattern.
- Jitter profile must be a sine waveform of 10 MHz or less.

2. High level (VoH) should fulfill the following formulas simultaneously.

R_L = Term R, Vtt = Term V

$VOH \leq 7.00$

$VOH \leq (7.00 \times RL + 50 \times Vtt) / (RL + 50)$

$VOH \leq RL / 50 \times (2.5 - 0.06 \times RL / (RL + 50)) + Vtt$

$VOH \geq (-2.00 \times RL + 50 \times Vtt) / (RL + 50)$

$VOH \geq Vtt - RL / 50$

3. Low level (VoL) should fulfill the following formulas simultaneously.

R_L = Term R, Vtt = Term V

$VOL \geq -2.00$

$VOL \geq (50 \times Vtt - 4.5 \times RL) / (RL + 50)$

$VOL \geq Vtt - RL\ (0.02 + 2.5 / (RL + 50))$

$VOL < ((2.5 - 0.06) \times RL / 50) + Vtt$

4. Amplitude should fulfill the following formulas simultaneously.

R_L = Term R, Vtt = Term V

$VOH - VOL > 2 \times (Vtt - RL/50 - Offset)$

$VOH - VOL > 2 \times ((RL \times (-2) + 50 \times Vtt) / ((RL + 50) - Offset))$

$VOH - VOL < 2 \times ((2.5 \times RL - 50 \times Offset + 50 \times Vtt) / (2 \times RL + 50))$

$VOH - VOL < 2 \times ((7 \times RL - 50 \times Vtt) / (RL + 50) - Offset)$

5. Total Jitter is measured with PRBS2^15-1 pattern. Measured by "Histogram WIndow" of CSA8000 + 80E03.

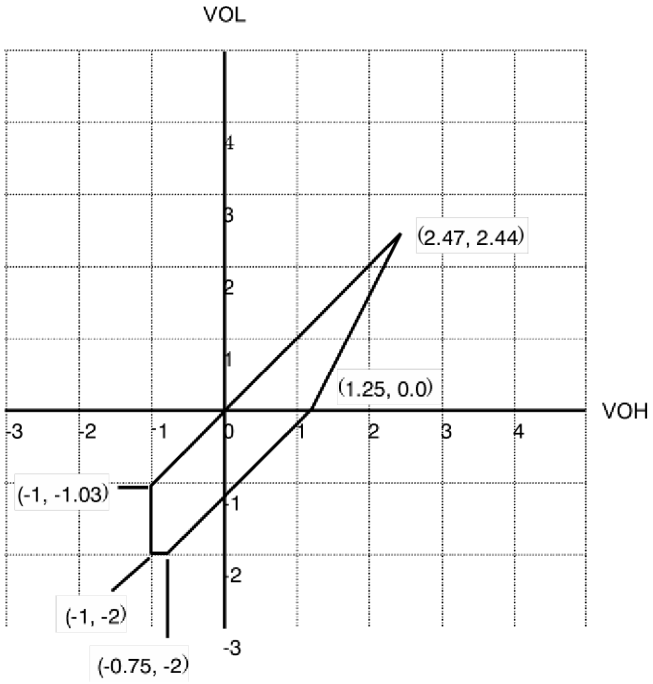


Figure 2-10: Output voltage window and clock out (DTGM30, DTGM31, DTGM32)

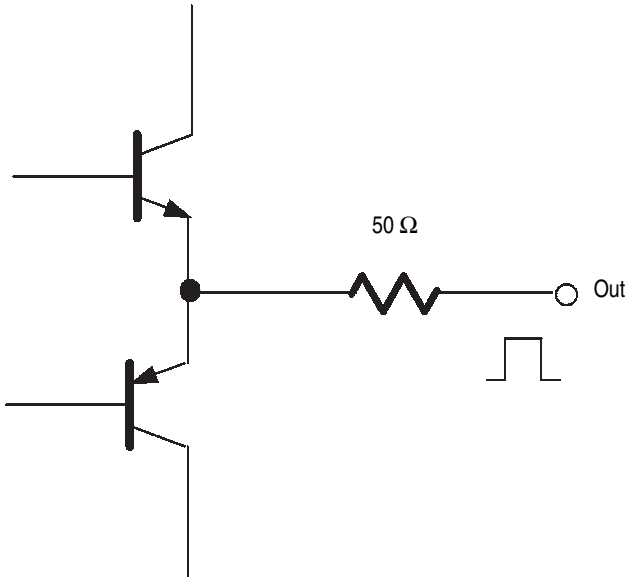


Figure 2-11: Equivalent circuit (DTGM10, DTGM20, DTGM21 outputs)

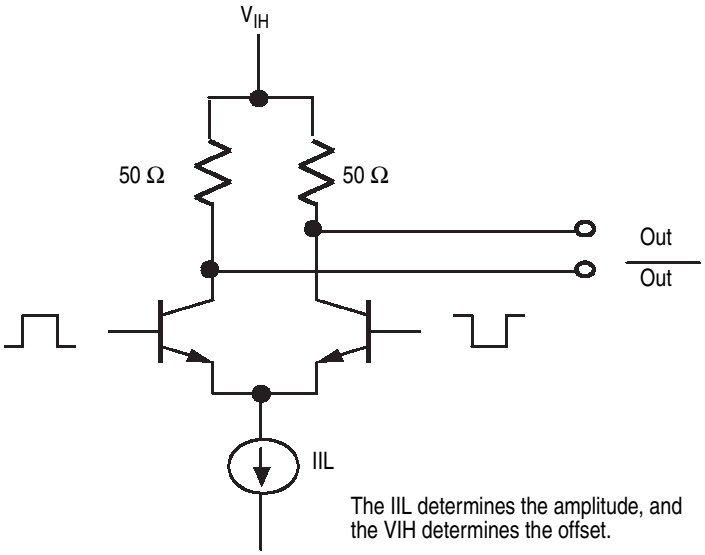


Figure 2-12: Equivalent circuit (DTGM30, DTGM31, DTGM32 outputs)

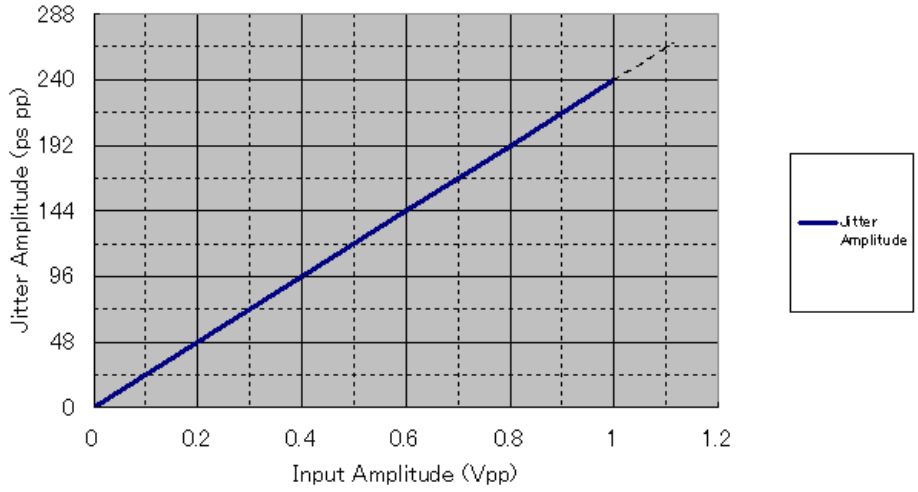


Figure 2-13: Input amplitude vs Jitter amplitude (DTGM31)

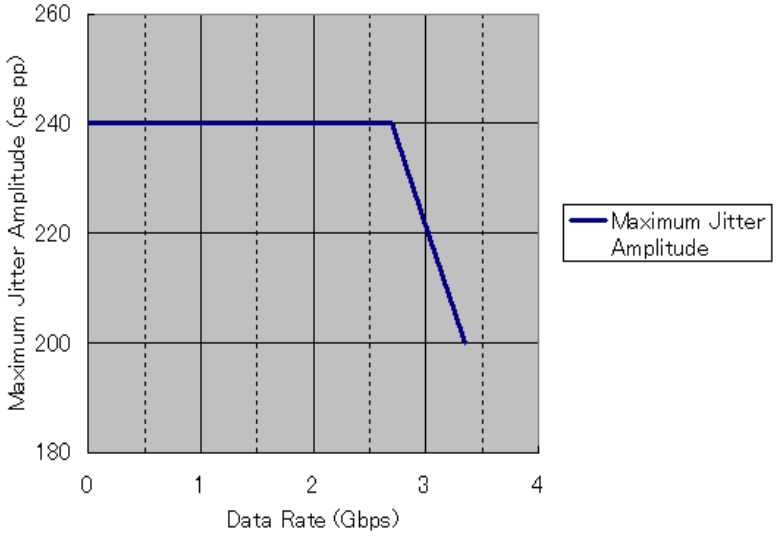


Figure 2-14: Data rate vs Maximum jitter amplitude (DTGM31)

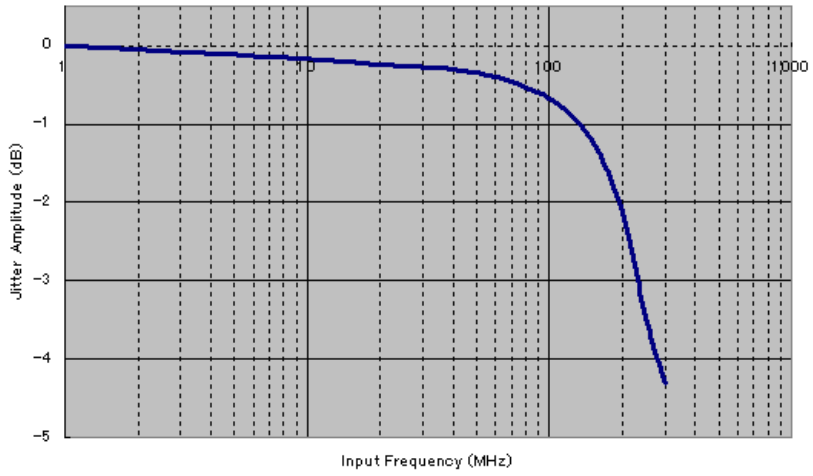


Figure 2-15: Input frequency vs Jitter amplitude (DTGM31)

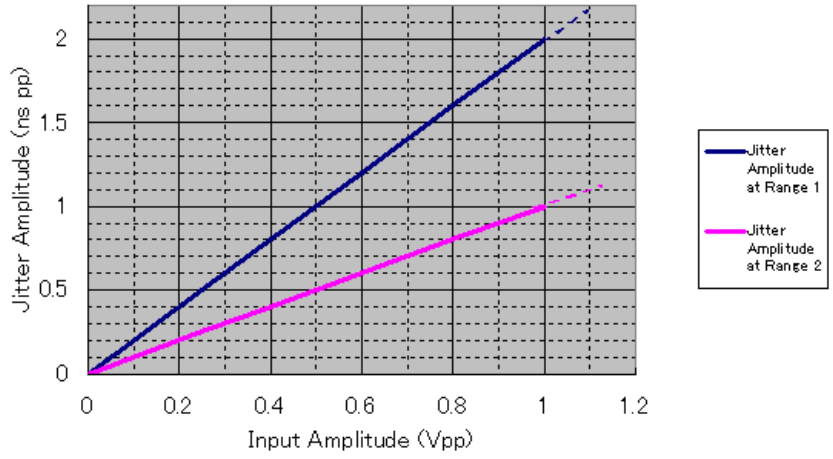


Figure 2-16: Input amplitude vs Jitter amplitude (DTGM32)

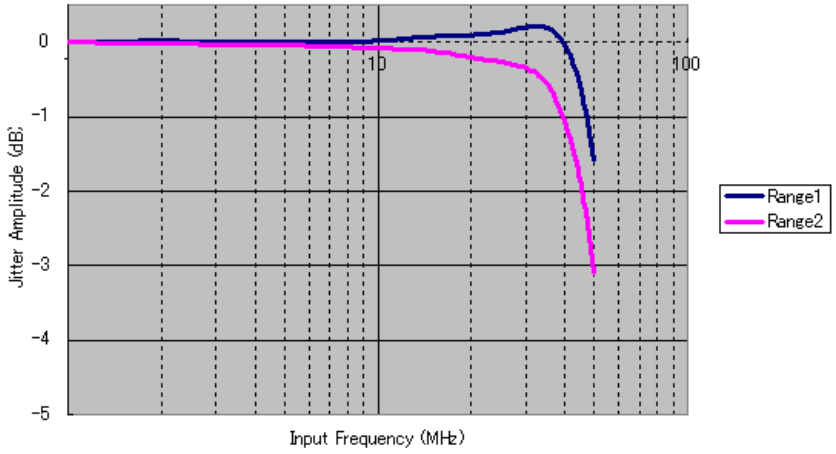


Figure 2-17: Input frequency vs Jitter amplitude (DTGM32)

Miscellaneous

Table 2-37: Mechanical

Characteristics	Description	
Net weight		
DTG5078	approx. 17.5 kg (38.6 lb)	
DTG5274	approx. 17.0 kg (37.5 lb)	
DTG5334	approx. 17.6 kg (38.8 lb)	
DTGM10	approx. 0.25 kg (0.55 lb)	
DTGM20	approx. 0.26 kg (0.57 lb)	
DTGM30	approx. 0.27 kg (0.60 lb)	
DTGM21	approx. 0.27 kg (0.60 lb)	
DTGM31	approx. 0.27 kg (0.60 lb)	
DTGM32	approx. 0.27 kg (0.60 lb)	
Net weight with package		
DTG5078	approx. 24.0 kg (52.9 lb)	
DTG5274	approx. 23.5 kg (51.8 lb)	
DTG5334	approx. 24.1 kg (53.1 lb)	
Dimensions		
DTG5078/DTG5274/DTG5334	Height	266 mm (10.5 in) 284 mm (11.3 in) with bottom feet
	Width	445 mm (17.5 in) 459 mm (18.1 in) with side handle
	Length	462 mm (18.2 in) 502 mm (19.8 in) with rear feet
DTGM10/DTGM20/DTGM30/DTGM21/ DTGM31/DTGM32	Height	33 mm (1.3 in)
	Width	84 mm (3.3 in)
	Length	133 mm (5.2 in)
Dimensions with package		
DTG5078/DTG5274/DTG5334	Height	500 mm (19.7 in)
	Width	600 mm (23.6 in)
	Length	790 mm (31.1 in)
DTGM10/DTGM20/DTGM30/DTGM21/ DTGM31/DTGM32	Height	83 mm (3.3 in)
	Width	238 mm (9.4 in)
	Length	227 mm (8.9 in)

Table 2-38: Installation requirement

Characteristics	Description
Heat dissipation	
Maximum power	600 VA
Dissipation (fully loaded)	Maximum line current is 5.5 Arms at 50 Hz, 90 V line.
Surge current	30 A (25 °C) peak for ≤ 5 line cycles, after the instrument has been turned off for at least 30 seconds.
Cooling clearance	Top: 2 cm (0.8 in) Bottom: 2 cm (0.8 in) ***NOTE:*** *The feet on the bottom provide the required clearance when set on a flat surface.*
	Sides 15 cm (6 in)
	Rear 7.5 cm (3 in)

Table 2-39: Environmental

Characteristics	Description
Atmospherics	
Temperature	
Operating [1]	+10 °C to +40 °C
Nonoperating	–20 °C to +60 °C
Temperature Gradient	
Operating	≤15 °C per hour (No condensation)
Nonoperating	≤30 °C per hour (No condensation)
Relative humidity	
Operating	20% to 80% (no condensation) Maximum wet-bulb temperature 29.4 °C
Nonoperating	5% to 90% (no condensation) Maximum wet-bulb temperature 40.0 °C
Altitude	(Hard disk drive restriction)
Operating	Up to 3,000 m (10,000 ft) Maximum operating temperature decreases 1 °C each 300 m (1,000 ft) above 1,500 m (5,000 ft)
Nonoperating	Up to 12,000 m (40,000 ft)

Table 2-39: Environmental (cont.)

Characteristics	Description
Dynamics	
Random Vibration	
Operating	2.65 m/s^2_{rms} (0.27 Grm), from 5 Hz to 500 Hz, 10 minutes
Nonoperating	22.36 m/s^2_{rms} (2.28 Grm), from 5 Hz to 500 Hz, 10 minutes
Shock	
Nonoperating	294 m/s^2 (30 G), half-sine, 11 ms duration Three shocks per axis in each direction (18 shocks total)

[1] **May not meet all performance specifications outside this range.**

Table 2-40: Power supply

Characteristics	Description
Rating voltage	100 VAC to 240 VAC
Voltage range	90 VAC to 250 VAC
Frequency	47 Hz to 63 Hz
Maximum Power	560 W (600 VA maximum)
Surge Current	30 A peak (25 °C) for ≤ 5 line cycles, after the instrument has been turned off at least 30 seconds.