TLA7S08 & TLA7S16 Series
Product Specifications & Performance Verification

Technical Reference Manual

077-0114-01

Tektronix

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Technical Reference Manual

This document applies to TLA System Software Version 5.5 or higher

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077-0114-01

Tektronix

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- Worldwide, visit www.tektronix.com to find contacts in your area.

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Preface

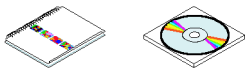
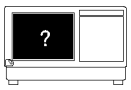
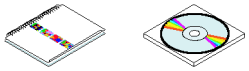
This document provides the specifications for the TLA7S08 and TLA7S16 PCI Express Serial Analyzer modules and high-level procedures to verify that the product is functioning correctly.

Related Documentation

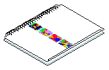
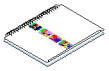
The following table lists related documentation that is available for your Tektronix logic analyzer family product. The documentation is available on the TLA Documentation CD included with your instrument and on the Tektronix Web site (www.tektronix.com). Refer to the Tektronix Web site for the most current documentation.

To obtain documentation that is not specified in the table, contact your local Tektronix representative.

Related Documentation

Item	Purpose	Location
TLA Quick Start User Manuals	High-level operational overview	
Online Help	In-depth operation and UI help	
Installation Quick Reference Cards	High-level installation information	
Installation Manuals	Detailed first-time installation information	
XYZs of Logic Analyzers	Logic analyzer basics	 www.Tektronix.com
Declassification and Securities instructions	Data security concerns specific to sanitizing or removing memory devices from Tektronix products	 www.Tektronix.com
Application notes	Collection of logic analyzer application specific notes	
Product Specifications & Performance Verification Procedures	TLA Product specifications and performance verification procedures	
TPI.NET Documentation	Detailed information for controlling the logic analyzer using .NET	

Related Documentation (cont.)

Item	Purpose	Location
Field upgrade kits	Upgrade information for your logic analyzer	 
Optional Service Manuals	Self-service documentation for modules and mainframes	 

Specifications and Characteristics

All specifications in this document are guaranteed unless noted *Typical*. Typical characteristics describe typical or average performance and provide useful reference information.

Specifications that are marked with the ✓ symbol are checked directly (or indirectly) at your nearest Tektronix location.

The performance limits in this specification are valid with these conditions:

- The instrument must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The instrument must have had a warm-up period of at least 30 minutes.

For modules, the performance limits in this specification are valid with these conditions:

- The serial analyzer modules must be installed in a Logic Analyzer Mainframe.
- The module must have been calibrated/adjusted at an ambient temperature between +20 °C and +30 °C.

Atmospheric Characteristics

The following table lists the Atmospheric characteristics of the Tektronix serial analyzers.

Table 1: Atmospheric characteristics

Characteristic	Description
Temperature	*Operating (no media in CD or DVD drive of the mainframe)*
	+5 °C to +45 °C, 15 °C/hr maximum gradient, noncondensing (derated 1 °C per 305 m (1000 ft) above 1524 m (5000 ft) altitude)
	Nonoperating (no media)
	-20 °C to +60 °C, 15 °C/hr maximum gradient, noncondensing
Relative Humidity	*Operating (no media)*
	20% to 80% relative humidity, noncondensing. Maximum wet bulb temperature: +29 °C (derates relative humidity to approximately 22% at +50 °C).
	Nonoperating (no media)
	8% to 80% relative humidity, noncondensing. Maximum wet bulb temperature: +29 °C (derates relative humidity to approximately 22% at +50 °C).
Altitude	*Operating*
	To 3000 m (9843 ft), (derated 1 °C per 305 m (1000 ft) above 1524 m (5000 ft) altitude.
	Nonoperating
	12,190 m (40,000 ft)

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Table 2: Data input for differential probes

Characteristic	Description
Data rate	2.5 Gb/s, 5 Gb/s [1]
Minimum differential input amplitude, peak-to-peak	120 mV
Maximum nondestructive input signal to probe	±7.5 V
Input common mode range	±7.5 V
Minimum input eye height	60 mV for continuous data streams
Input eye width	0 UI for jitter at frequencies below 10 MHZ and without jitter above 10 MHz 0.7 UI for jitter at frequencies above 10 MHz (Measured with random jitter of 5 ps RMS)
Random jitter tolerance *(Typical)*	5 ps RMS
Sinusoidal jitter tolerance *(Typical)*	1 ns for frequencies below 1 MHz 100 ps for frequencies between 1 MHz and 10 MHz 20 ps for frequencies above 10 MHz
Location of transition detect inputs	Channels A3, A0, B3, B0, C3, C0, D3, D0
Minimum time to detect loss of signal at the input	8 ns
Number of FTS packets required to resynchronize following the L0s exit	12 for Gen1 17 for Gen2

[1] The data rate can be modulated from 0% to –0.5% fo the nominal data rate frequency at a modulation rate not exceeding the range of 30 kHz to 33 kHz.

Table 3: Channel width and depth

Characteristic		Description
Number of data channels	TLA7S08	8
	TLA7S16	16
Acquisition memory depth		32 M samples

Table 4: Clocking

Characteristic	Description
External reference clock	
Minimum peak-to-peak differential input voltage *(Typical)*	150 mV
Absolute differential input voltage limit *(Typical)*	2.5 V
Clock frequency *(Typical)*	100 MHz ±10% or 125 MHz with or without SSC (Spread Spectrum Clocking) [1]
Frequency tolerance *(Typical)*	±350 ppm

Table 4: Clocking (cont.)

Characteristic	Description
Rise time *(Typical)*	55 ps
Fall time *(Typical)*	55 ps
Duty cycle*(Typical)*	40% to 60%
Total jitter, peak-to-peak*(Typical)*	25 ps below 1 MHz 200 ps above 1 MHz

1 The data rate can be modulated from 0% to –0.5% fo the nominal data rate frequency at a modulation rate not exceeding the range of 30 kHz to 33 kHz.

Table 5: SerDes

Characteristic	Description
Trigger resources	
Clock encoding standard	Supports 8b10b encoded serial data

Table 6: Lane processing

Characteristic	Description
Time required to dynamically change the data rate*(Typical)*	2.3 µs Gen1 to Gen2 transitions 3.0 µs Gen1 to Gen2 transitions
Polarity inversion	Available on all input channels
Descrambling polynomial	Descrambles data using the polynomial defined in PCI Express Specification Revision 1.1:x^16=x^5+x^4+x^3+x^1
Autoset lane number	Each lane has a training sequence recognizer that stores the last known lane number assignment. The SUT must provide TS1 training sequences for the Autoset to work. Changes are not applied automatically. The software polls the lane number registers and then prompts the user to use Autoset when changes are detected.
Autoset lane polarity	Each lane has a training sequence recognizer that stores the last known lane polarity. The SUT must provide TS1 training sequences for the Autoset to work. Changes are not applied automatically. The software polls the lane number registers and then prompts the user to use Autoset when changes are detected.
Auto-track lane rate	When the auto-track feature is enabled, data will be aligned at the current data rate. Training sequences must be acquired for the module to change rates. EIOS packets must be acquired to initiate the speed change. The signalling levels (specified above) must be met.
Force lane rate	When forced, data will be acquired at the specified rate of 2.5 Gbps and 5 Gbps.

Table 6: Lane processing (cont.)

Characteristic	Description
Lane data groups	Reports the 8b 10b symbol information acquired from each lane or internal module status symbols if no data is available.
	The following information is available when 8b 10b symbols are acquired Disparity error indicator Running disparity error indicator K-code/D-code indicator 8-bit code value Full 10b value if an 8b 10b code error is encountered
	Internal module status symbols: NC: the lane is not required for the chosen link width No_Ref: the SERDES is unable to recover the data from the lane EIDLE: the lane is presently in electrical idle Realign: one of the lanes in the link woke up from electrical idle or an alignment exit condition was encountered Deskew: the lane has encountered an alignment entry condition and is waiting for the other lanes to find theirs

Table 7: Link processing

Characteristic	Description
Channel cross-point switch	Any-to-any channel mapping
Lane alignment entrance	If the link is not currently in the aligned state, the hardware will automatically attempt lane-to-lane alignment (deskew) on any of the following conditions: ■ Skip ordered set ■ Electrical idle exit ordered set ■ Beginning of a TS2 training sequence ■ Last occurance fo a TS2 training sequence The alignment to the beginning of TS2 training sequences is disabled after a Gen1-to-Gen2 data rate transition and re-enabled by the first skipped ordered set.
Lane alignment exit	If the link is currently in the aligned state, the hardware will abandon the current alignment (deskew) settings on any of the following conditions: ■ Electrical idle ordered set ■ Misaligned COM symbol across the active lanes ■ Lane 0 goes into electrical idle ■ Data rate mismatch occurs on the lanes within the link ■ Any lane wakes up from electrical idle
Lane alignment exit recovery	32 symbol times

Table 7: Link processing (cont.)

Characteristic	Description	
Maximum skew between lanes	32 symbol times This defines the maximum skew between lanes of a link that the lane alignment module can deskew	
Link support	TLA7S08	One uni-directional x8, x4,x2, or x1 link
		One bi-directional x4, x2, or x1 link
	TLA7S16	One uni-directional x16, x8, x4, x2, or x1 link
		One bi-directional x8, x4, x2, or x1 link
Auto-track link width	Link-width changes are automatically tracked; this feature is always enabled. Real-time resources that depend on link width (such as packet recognizers) remain unusable through any change in link width.	
Link Status group	Reports the current state of the link ■ –: TLP or DLLP packet data is present on the link ■ Rates_Vary: the data rates of the active lanes in the link do not match ■ Aligning: at least one lane encounted an alignment entry condition which resulted in the start of an alignment cycle ■ Aligned: the alignment logic has not seen an alignment entry condition since the last alignment exit condition ■ 10b_mode: the symbols being acquired are 10b encoded therefore further link processing is not performed ■ Logic_Idle: the link is aligned and is logically idle (all active lanes have 0x00 data) ■ FTS: the link is aligned and a fast training sequence ordered set is present on Lane 0 ■ TS1: the link is aligned and a TS1 training sequence is present on Lane 0 ■ TS2: the link is aligned and a TS2 training sequence is present on Lane 0 ■ SKP: the link is aligned and a skip ordered set is present on Lane 0 ■ EIOS: the link is aligned and an electrical idle ordered set is present on Lane 0 ■ EIEOS: the link is aligned and an electrical idle exit ordered set is present on Lane 0 ■ Forced: the module is being used in bidirectional mode with timestamp averaging disabled and the other link direction needed to store data even though this link direction had nothing to store. A sample must be acquired in this case even though only half of the data is valid.	
Link Width group	Reports the current number of active lanes in the link ■ x1, x2, x4, x8, x16: active lane count ■ Unknown: the link is currently not aligned so the an accurate lane count cannot be established Each link direction has its own version of this group.	

Table 7: Link processing (cont.)

Characteristic	Description
Link Rate group	2.5G or 5.0G Reports the current rate of the link; to report 5.0G, all active lanes must be at 5.0G.
Link Violation group	Reports protocol violations on the link ■ –: no violations currently detected ■ Bad_Frame: an SDP or STP symbol was detected in a non-modulo-4 lane number ■ Bad_LIDLE: non-zero data was detected on an active lane outside of packet, ordered set, or training sequence ■ Bad_Symbol: an 8b10b disparity or lookup error was detected on one of the active lanes in the link ■ Bad_CRC: a DLLP CRC error was detected The violations are priority encoded such that when multiple errors occur, the one with the highest priority is reported. The order from highest to lowest is as follows: Bad_Frame, Bad_LIDLE, Bad_Symbol, Bad_CRC
TLP Type group	Reports the type of the active TLP packet The type remains asserted for the duration of the packet. When an old packet ends in the same symbol time that a new packet begins, the newest packet type is reported.
DLLP Type group	Reports the type of the active DLLP packet The type remains asserted for the duration of the packet. When an old packet ends in the same symbol time that a new packet begins, the newest packet type is reported.
SDP group	Asserts for each sample that contains a valid DLLP packet start
STP group	Asserts for each sample that contains a valid TLP packet start

Table 8: Event recognizer resources

Characteristic	Description
DLLP packet recognizers	4 per link direction Each recognizer supports full 32-bit mask and match on the DLLP packet excluding the CRC and framing bytes. Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned.
TLP packet recognizers	4 per link direction Each recognizer supports full 32-bit mask and match for the first 4 dwords of the TLP packet excluding the framing and sequence number. Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned.
Symbol sequence recognizers	4 shared between link directions Each recognizer supports full mask and match on each symbol in a sequence up to 16 symbols deep. Any position in the sequence can be marked with a NOT in which case the recognition process will only continue if the current symbol does not satisfy the mask and match logic.
Link event recognizers	4 per link direction Each recognizer is a unique logical OR of the selected link events.

Table 8: Event recognizer resources (cont.)

Characteristic		Description
Link event:	Disparity error	Asserts when an 8b10b disparity error is detected on any of the selected lanes. Each lane of the link can be individually included or excluded.
	Code error	Asserts when an 8b10b table lookup error is detected on any of the selected lanes. Each lane of the link can be individually included or excluded.
	Electrical idle	Asserts when electrical idle is detected on any of the selected lanes. Each lane of the link can be individually included or excluded.
	DLLP frame error	Asserts when an SDP start symbol is detected in a non-modulo-4 lane number Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned
	TLP frame error	Asserts when an STP start symbol is detected in a non-modulo-4 lane number. Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned
	DLLP CRC error	Asserts when the calculated CRC does not match the CRC value in the packet payload. Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned
	Logical idle error	Asserts when packet and ordered set traffic is not active and a non-zero data symbol is detected in any of the active lanes in the link. Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned
	Data rate change	Can be programmed to assert when the link data rate changes: ■ To Gen1 (2.5G) ■ To Gen2 (5.0G) ■ To any rate different than the last known rate Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned.
	Lane width change	Can be programmed to assert when the link width changes: ■ Downtrain (to any width less than the last known width) ■ Uptrain (to any width more than the last known width) ■ x1, x2, x4, x8, or x16 ■ Not x1, Not x2, Not x4, Not x8, or Not x16 ■ To any width different than the last known width Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned

Table 9: Filtering

Characteristic	Description
Bidirectional filtering control	Each direction of a link has independent filter control settings.
Idle filtering	Logical idle and electrical idle conditions can be filtered from storage.
Ordered set filtering	The following ordered sets can be selected for filtering from storage: TS1, TS2, SKP, EIOS, FTS, EIEOS

Table 9: Filtering (cont.)

Characteristic	Description
DLLP packet filtering	The following DLLP packet types can be selected for filtering from storage: Ack, Nack, PM, FC1, FC2, UpdateFC, Vendor Specific
TLP packet filtering	The following TLP packet types can be selected for filtering from storage: MRd, MRdLk, MWr, IORd, IOWr, CfgRd0, CfgWr0, CfgRd1, CfgWr1, Msg, MsgD, Cpl, CplD, CplLk, CplDLk

Table 10: Trigger state machine

Characteristic	Description
Sequencer states	8
Sequencer rate	The trigger state machine evaluates it logic and can advance one state every other symbol time.
Event recognizer inputs per state	10 total, eight programmable event recognizer inputs and two dedicated event counter results
Event occurrence counters	two 16-bit event occurrence counters per state Each counter can be independently programmed to monitor any event recognizer output. The counter actions are automatic. They automatically increment at the rate of the selected event recognizer output (which can be faster than the sequencer rate). And they automatically reset when their host state is exited
Global counter-timers	There are four 48-bit signed global counter/timers that are actionable at the rate of the sequencer. Maximum count value = 2^47 – 1 Maximum time value = (2^47 – 1) * 3.6ns = ~141 hours
Backplane trigger	The backplane trigger signal can be recognized as the trigger for the acquisition.
Backplane signal inputs	Up to four backplane signals can be used as events.
Arm hold-off	The execution of the trigger state machine can be held-off by using the Arm input. The Arm input can be controlled by any other module in the system. If Arm is not explicitly assigned, then the module will automatically arm itself immediately at the beginning of each acquisition.
Main trigger position	The trigger position is programmable to any data sample.

Table 11: Trigger machine actions

Characteristic	Description
Trigger	Triggers the main acquisition memory
Increment and decrement global counter	Counters can be incremented or decremented.
Reset global counter	Counters can be reset.
Start or stop global timer	Timers can be started or stopped. When stopped they hold their present value.
Reset global timer	Timers can be reset. When reset, it continues in the state it was in prior to the reset action – either running or stopped.

Table 11: Trigger machine actions (cont.)

Characteristic	Description
Reset and start or stop global timer	Timer resources may be simultaneously reset and started or reset and stopped in a single action.
Set or clear backplane signal	Any of the four signals may be driven onto the backplane to be used by another module. All four backplane signals can be used. If ARM is used then Signal-4 is not available.
Trigger Out	A Trigger Out signal can be driven to the backplane to trigger other modules.
Goto state	Jump to any state from any state.
Start or stop storage	Turns storage on or off. Once turned off, no samples will be stored until another start storage action is encountered. The data sample containing the condition that stops storage is not stored. The data sample containing the condition that starts storage is stored.

Table 12: Module input/trigger/backplane delay relation ships

Characteristic	Description
Real-time signal uncertainty *(Typical)*	±30 ns + data rate offset
External trigger in to probe tip *(Typical)*	958 ns + real-time signal uncertainty
External signal in to probe tip *(Typical)*	950 ns + real-time signal uncertainty
Probe tip to external trigger out *(Typical)*	1170 ns + real-time signal uncertainty
Probe tip to external signal out *(Typical)*	1150 ns + real-time signal uncertainty
Internal TLA7Sxx module to module signal delay *(Typical)*	
TLA7Sxx to TLA7Sxx	130 ns + real-time signal uncertainty
TLA7Sxx to TLA7Axx	470 ns + real-time signal uncertainty
TLA7Sxx to TLA7Bxx	–100 ns + real-time signal uncertainty
Internal TLA7Sxx module to module trigger delay *(Typical)*	
TLA7Sxx to TLA7Sxx	105 ns + real-time signal uncertainty
TLA7Sxx to TLA7Axx	490 ns + real-time signal uncertainty
TLA7Sxx to TLA7Bxx	–100 ns + real-time signal uncertainty
Internal TLA7Sxx module to module arm delay *(Typical)*	
TLA7Sxx to TLA7Sxx	85 ns + real-time signal uncertainty
TLA7Sxx to TLA7Axx	460 ns + real-time signal uncertainty
TLA7Sxx to TLA7Bxx	–100 ns + real-time signal uncertainty
Internal module toTLA7Sxx module signal delay *(Typical)*	
TLA7Axx to TLA7Sxx	–220 ns + real-time signal uncertainty
TLA7Bxx to TLA7Sxx	320 ns + real-time signal uncertainty
Internal module toTLA7Sxx module trigger delay *(Typical)*	
TLA7Axx to TLA7Sxx	–265 ns + real-time signal uncertainty
TLA7Bxx to TLA7Sxx	270 ns + real-time signal uncertainty
Internal module toTLA7Sxx module arm delay *(Typical)*	

Table 12: Module input/trigger/backplane delay relation ships (cont.)

Characteristic	Description
TLA7Axx to TLA7Sxx	–270 ns + real-time signal uncertainty
TLA7Bxx to TLA7Sxx	280 ns + real-time signal uncertainty

Table 13: Storage control

Characteristic	Description
Initial storage state	The initial storage state can be set to store all or store none at the beginning of each acquisition. The start/stop storage trigger machine actions can be used to change the storage state during the acquisition.

Table 14: Data placement

Characteristic	Description
System time zero placement error *(Typical)*	±3.6 ns + 10 MHz backplane skew
Timestamp accuracy *(Typical)*	±9 ns
Data rate offset *(Typical)*	(unit interval – 4 ns) × 68
Data correlation error *(Typical)*	Timestamp Accuracy + System Time Zero Placement Error + Data Rate Offset
Timestamp counter	
Resolution	25 ps
Duration	62.5 hours (2.6 days)

Table 15: Mechanical

Characteristic		Description
Material		Chassis parts are constructed of aluminum alloy. The front panel is constructed of plastic laminated to steel front panel. Circuit boards are constructed of glass laminate.
Weight	TLA7S08	5.17 lbs (2.345 kg)
	TLA7S16	5.40 lbs (2.45 kg)
Shipping weight		Includes packaging
	TLA7S08	14.21 lbs (6.445 kg)
	TLA7S16	14.34 (6.505)
Overall dimensions	Height	10.32 in (262 mm)
	Width	2.39 in (61 mm)
	Length	14.7 in (373 mm)
Mainframe interlock		1.4 ECL keying is implemented

Performance Verification Procedures

There are no customer self-service performance verification procedures for the TLA7S08 or TLAS716 Serial Analyzer modules. If you want to verify the performance of your serial analyzer module, you must return the module to your local Tektronix office. However you can perform a functional check. (See page 14, *Functional Verification*.)

Functional Check Procedures

Functional Verification

Functional verification procedures consist of running the Power-on diagnostics, Extended diagnostics, and acquiring a signal from the SUT.

Power-on and Extended Diagnostics

Do the following steps to run the power-on and extended diagnostics:

NOTE. *Running the extended diagnostics will invalidate any acquired data. If you want to save any of the acquired data, do so before running the extended diagnostics.*

You will need a mainframe with a serial analyzer module installed in the mainframe.

NOTE. *If you control your logic analyzer from a remote location, make sure that you select Run Power-on Diagnostics in the TLA Connection dialog box. Otherwise the instrument will bypass the power-on diagnostics.*

Perform the following tests to complete the functional verification procedure:

1. If you have not already done so, power on the instrument.

   The instrument runs the power-on diagnostics each time that you power-on the instrument. If any failures occur, the diagnostic window will appear.

2. Go to the System menu and select Calibration and Diagnostics.

3. Scroll through the list of tests and verify that all power-on diagnostics pass.

NOTE. *Allow the instrument to warm up for 30 minutes before continuing with the Extended diagnostics.*

4. Click the Extended Diagnostics tab.

5. Select the top-most selection for your module in the list of tests. For example, if your serial analyzer module is installed in Slot 3 of your mainframe, select Slot 3:TLA7S08 - SA.

6. Select the type of test that you want to run (One Time, Continuous, or Until Fail).

7. Click Run to start the tests.

   All tests that displayed an "Unknown" status will change to a Pass or Fail status depending on the outcome of the tests.

8. After the tests have completed, scroll through the list and verify that the instrument passes all tests.

NOTE. *Installing a module in the mainframe provides a means of verifying connectivity and communication between the module and the mainframe. If the instrument fails any test, try using a different module and repeat the tests to isolate the problem to the mainframe or to the module.*

Acquire a Signal

To verify that the serial analyzer module can acquire signals, connect the serial analyzer to a known good signal source through one of the serial analyzer probes.

Power on the serial analyzer and the SUT.

Go to the serial analyzer Setup window and verify that the channel activity connectors show activity for any channels connected to the SUT. If necessary, refer to the Status Area near the top of the Setup window to decode the channel status colors. The serial analyzer always acquires signals. If the channel activity indicators show the correct activity for the SUT, you have verified that the serial analyzer acquired a signal from the SUT and displayed the information in the Setup window.