

# BERTScope™

## CRJ 125A-PCIE

### PLL-PCIE

## Getting Started Guide

Part Number 0130-711-00.01



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**Part Number 0130-711-00.01**

**6 May 2008**



## **Warranty**

SyntheSys Research warrants that this product will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If a product proves defective during this period, SyntheSys Research will either repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product, at its option.

In order to obtain warranty service, you must notify SyntheSys Research of the defect before the warranty period expires and make appropriate arrangements for service. You shall be responsible for packaging and shipping the defective product to the service center designated by SyntheSys Research, with shipping charges prepaid. SyntheSys Research shall pay for the return shipment of the product to you if the shipment is to a location within the country where the service center resides. You shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other location.

This warranty shall not apply to any defect, failure, or damage caused by using this product improperly or by inadequate maintenance or care. SyntheSys Research shall not be obliged to furnish warranty service to repair damage resulting from connection to incompatible equipment or improper use. SyntheSys Research shall not be obliged to furnish warranty service to repair damage resulting from attempts by non-SyntheSys Research representatives or designees to install, repair, or service the product. SyntheSys Research shall not be obliged to furnish warranty service to repair any damage or malfunction caused by the use of non-SyntheSys Research supplies. SyntheSys Research shall not be obliged to furnish service under this warranty to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

SyntheSys Research disclaims any implied warranties of merchantability or fitness for a particular purpose. SyntheSys Research's responsibility to replace or repair the defective products is the sole and exclusive remedy for breach of this warranty. SyntheSys Research will not be liable for any indirect, incidental, special, or consequential damages irrespective of whether SyntheSys Research has advance notice of the possibility of such damages. This warranty is given by SyntheSys Research in lieu of any other warranties, express or implied.

## **Technical Support**

If you have not already purchased extended warranty options for this product, you may do so at any time during the product's warranty period. This extended warranty provides continued warranty coverage for up to two additional years, supplementing the normal one-year warranty period.

For service or questions, please contact us at:

Service Department  
SyntheSys Research Inc.  
3475-D Edison Way  
Menlo Park, CA 94025-1821 U.S.A.  
Voice: +1 (650) 364-1853  
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Email: [tech\\_support@bertscope.com](mailto:tech_support@bertscope.com)  
Website: [www.bertscope.com](http://www.bertscope.com)

When you contact SyntheSys Research for service, please have your product model number, serial number, and purchase date information available. Our service department is available from 9:00 a.m. to 5:00 p.m. (Pacific Time), Monday through Friday.

## **Calibration**

The recommended calibration interval is one year. Calibration requires return to the factory. For calibration service, please contact the Service Department as listed above.



## Product Safety Summary

To avoid personal injury or damage to this product or devices connected to it, please review and abide by the following safety guidelines.

**Use the product only as specified.**

**Do not remove covers.** There are no user serviceable components within the instrument.

**Use only the proper power cable.** Be sure the power cable is certified for the country in which the product will be used.

**Connect to proper power mains.** The line voltage and frequency must be within the values specified for the product.

**Replace only with the proper fuse.**

**Ground the product.** The chassis of this product is intended to be connected to earth ground through the protective conductor in the power cable. Failure to ground the product potentially exposes the user to shock hazard, may result in radiated or conducted emissions beyond the certified limits, or result in electro-static discharge (ESD) damage to the product itself, or other devices connected to it.

**Do not exceed input voltage or power ratings on any connector.**

**Do not operate product in an ambient environment beyond specifications.**

**Provide proper cooling.** Make sure the instrument cooling vents are not blocked. Vacuum excess dust from ventilation openings when required.

**Do not operate in a flammable or explosive environment.**

**Do not operate with suspected failure or physical damage.**

Power for this device is controlled through a low voltage power switch located on the front panel. A "keep alive" portion of the power supply circuit provides the small amount of power required to operate the switch and main power control circuit. The product does not contain a principal power switch which disconnects the supply from the power mains. In the unlikely event of a fire or other emergency, power can be disconnected by removing the line cable from the power input connector located on the rear panel.

## Terminology and Symbols

The following terminology may appear in this manual:

**WARNING.** A warning statement identifies conditions which may result in personal injury or death.

**CAUTION.** A caution statement identifies conditions which may result in damage to the instrument or devices connected to it.

**NOTICE.** A notice statement identifies conditions which may result in unintended operating modes, incorrect measurement results, or require resetting the instrument or personal computers operating software interacting with it.

The following symbols may appear on the product:



WARNING or CAUTION - Refer to Manual



WARNING – High Voltage



Protective Earth Ground connection.

## Environmental Considerations

### *Product End of Life*

Abide by the following guidelines when recycling this product at end of life:

**Product Recycling:** Producing this product required the use of natural resources. The product may contain materials which could be harmful to the environment or health if disposed of improperly at end of useful life. To avoid the potential for environmental contamination and reduce the demand for additional natural resources, we recommend that you recycle this product.



This product complies with the European Union's requirements stated in Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

**Restriction on Hazardous Substances:** This product has been classified as Monitoring and Control equipment, and is outside the scope of the 2002/95/EC RoHS Directive. This product may contain lead, cadmium, or hexavalent chromium.

## Installation

This product is intended to be operated in a controlled laboratory environment.

It is intended to operate on a bench top, or on top of another instrument such as the BERTScope. There are four shock absorbing feet located on the bottom of the instrument. Operate the instrument only when positioned with the feet facing downward. Do not operate the instrument with the long axis vertical, standing on its side, as this will block the path of air required for cooling.

# Table of Contents

Product Safety Summary .....	v
Terminology and Symbols.....	v
Environmental Considerations .....	vi
Product End of Life .....	vi
Installation .....	vi
Introduction.....	1
Test Equipment Required.....	2
Test Preparation.....	2
Control Software Installation.....	2
Installing the USB driver .....	6
Completing the PLL Analyzer test set-up .....	9
Configuring the Compliance Base Board (CBB) .....	9
Hardware Test Setup.....	10
Testing PLL Loop Response .....	12
Specifications .....	15



## Introduction

The CRJ 125A-PCIE and PLL-PCIE analyze the loop response of the Phase Locked Loop (PLL) used to generate the Tx clock in PCI Express® Add-In cards. The transmit clock is generated locally on the card and synchronized with the systems by phase locking it to a 100 MHz reference clock (REF-CLK) which is distributed through the motherboard or backplane. The loop response characteristics (bandwidth and peaking) determine the jitter transfer function from the REF-CLK to the Tx clock. The PCI Express CEM specification requires the tight control of the PLL Response to manage the entire system jitter budget, assuring reliable operation. To assure compliance, the Tx clock generation PLL response will be verified during compliance workshops.

The CRJ 125A-PCIE and PLL-PCIE measure the PLL response by substituting a test clock for the locally generated REF\_CLK which contains a calibrated level of sinusoidal jitter. The PLL analyzer measures the transferred jitter by applying the transmitted compliance pattern output from the Add-In card under test into a reference PLL. The phase deviation is digitized and analyzed within the instrument to determine its spectral components. The frequency of the modulating sinusoidal jitter is incrementally swept, with measurement data taken at each frequency step. The instrument computes the PLL magnitude and phase, along with jitter transfer function automatically.

In addition to measuring the loop response, the PLL analyzer contains the synthesizer used to generate the jitter modulated REF\_CLK. The jitter appears as true phase modulation in the REF\_CLK output, maintaining a 50% duty factor at all times. This allows the PLL analyzer to be used with all types of clock generation PLLs, including those which incorporate dual edge phase detectors.

Incorporating the synthesizer within the instrument facilitates internal self calibration, eliminating the need for the user to manually normalize the test setup calibration. Once the cabling to the Compliance Base Board is connected, the user can begin testing immediately.

An external PC is used to host system control and report generation software. This program plots the PLL Loop Response, compares the measured bandwidth and peaking against the specification limits, and can generate a test report in hard copy or HTML file format. The instruments communicate with the host PC through a USB interface.

Both the CRJ 125A-PCIE and PLL-PCIE have identical capabilities and specifications for measuring PCIe Tx clock generation PLL response. The PLL-PCIE instrument is dedicated to performing these measurements. The CRJ 125A-PCIE adds the PCIe PLL analysis capability to the CRJ 12500A Clock Recovery Instrument with Jitter Analysis. All of the base functionality and performance of the CRJ 12500A is retained. For information on use of the CRJ 12500A clock recovery, SSC modulation monitoring function, or jitter spectral analysis, refer to the instrument's online help guide.

## Test Equipment Required

The following equipment is required for PLL Loop Response testing to revision 2.0 requirements:

- PLL Analyzer model CRJ 125A-PCIE or PLL-PCIE.
- PLL Analysis control software – supplied with PLL Analyzer.
- Compliance Base Board V 2.0, jumpers configured to source the **REF\_CLK** from external input. If the CBB is purchased from SyntheSys Research, the jumpers will be properly configured. Information for reconfiguring a standard CBB is found in section 3.3.
- SMP-M 50Ω terminators for unused lanes. See note below.
- SMA-M to SMP-M interconnect cables for Tx data out. Low loss, ≈40 cm length. Two required. Astrolab Minibend s-16, p/n: 32081-29094C-29473C-16 or equivalent.
- SMA-M to SMP-M interconnect cables for REF\_CLK in. ≈0.5 m length. Two required. Loss characteristics are not critical as frequency content is ≈100 MHz. Rosenberger p/n 101462-4205 or equivalent.
- Host PC to operate application software. Windows 2000 or XP operating system. One free USB1.1 or 2.0 port. While not required to perform a PLL Loop Response test, a printer (either local or networked to the host PC) is required if the user desires hard copy output of the test reports. Results can also be stored as HTML files for printing at a later time.
- USB cable, type A to Type B. Supplied with PLA Analyzer.
- ATX type PC Power supply, with outputs as required to power Add-In card to be tested through the CBB. A higher quality, low noise supply may be required for some Add-In cards.
- The use of ESD dissipating mats for the work surface and wrist straps for the operator are good practice and suggested to avoid damage to the Add-In card under test and other test equipment.

Note: As allowed in the PCI Express standard, some Add-In cards require termination of unused lanes in order to initiate generation of the compliance test pattern. The CBB may be configured with various combinations of connectors installed to access the Tx lanes. Lanes without access connectors will be properly terminated. PLL Loop response testing is performed by measuring the Tx output on lane 0 only. If the Add-In card under test requires termination of unused Tx lanes to initiate compliance pattern generation, the user will need to terminate the required lanes which have access connectors on the CBB.

## Test Preparation

### ***Control Software Installation***

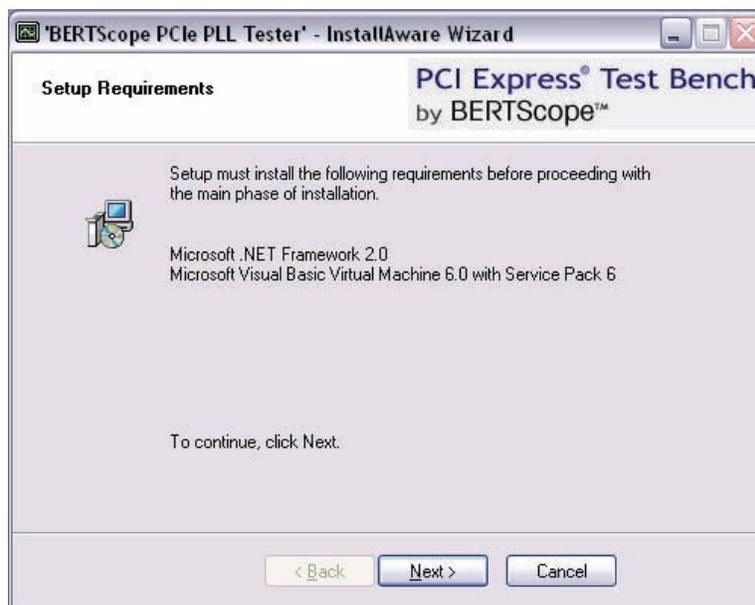
Install the control software on the host PC before connecting the PLA Analyzer. The software only needs to be installed once on the host PC. It is installed from the CD-ROM supplied with the PLL Analyzer.

Turn on the power on the host PC and wait for the operating system to fully boot. Insert the CD-ROM into the drive. The installer should autostart. Select CR\_PCIE\_PLL-Tester from the install menu choices. If the CD-ROM does not autostart, explore the CD-ROM root directory using My Computer or Explorer, locate the Setup\_CR\_PCIE\_PLL.EXE file, and double-click to start installation.

The InstallAware Wizard with a progress indicator will appear.

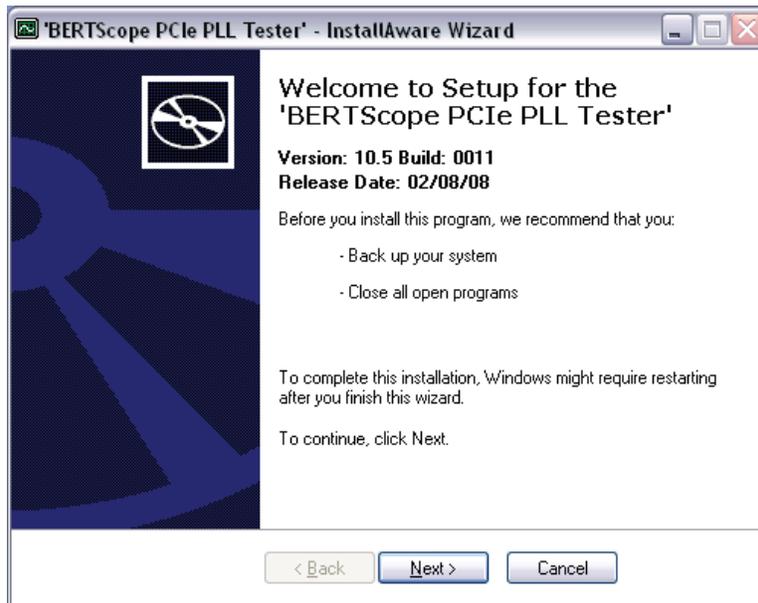


The screen showing the system requirements will then appear:



If the required add-ins are not installed, they can be downloaded for no charge from the Microsoft web site: [www.microsoft.com](http://www.microsoft.com).

When the following screen appears:

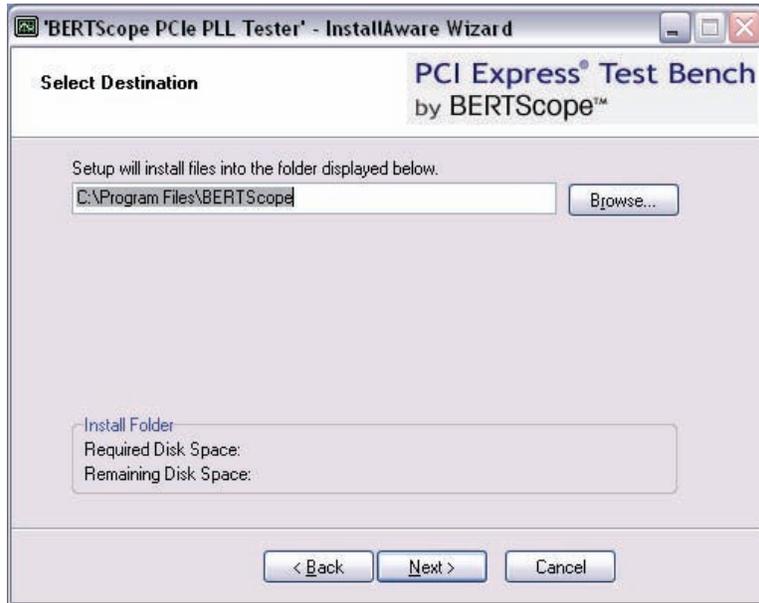


Click Next to continue.

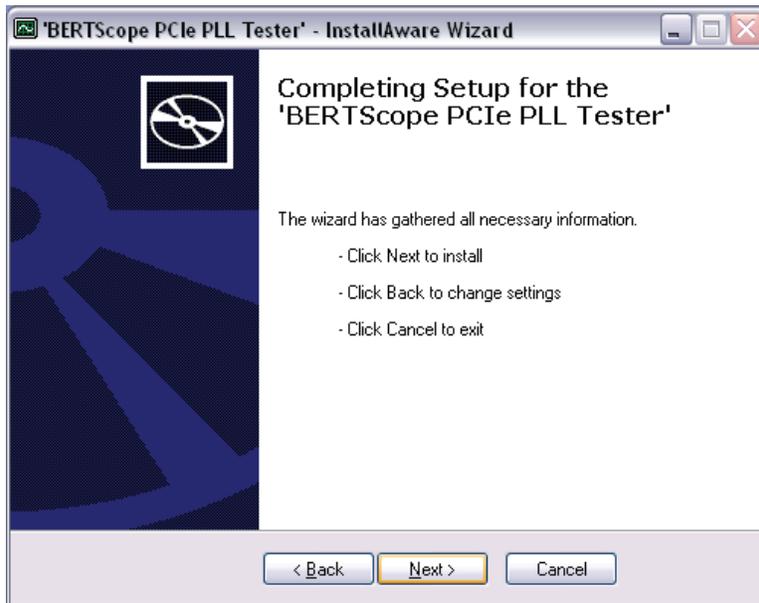
Select 'Typical Setup' on the next screen, then click Next.



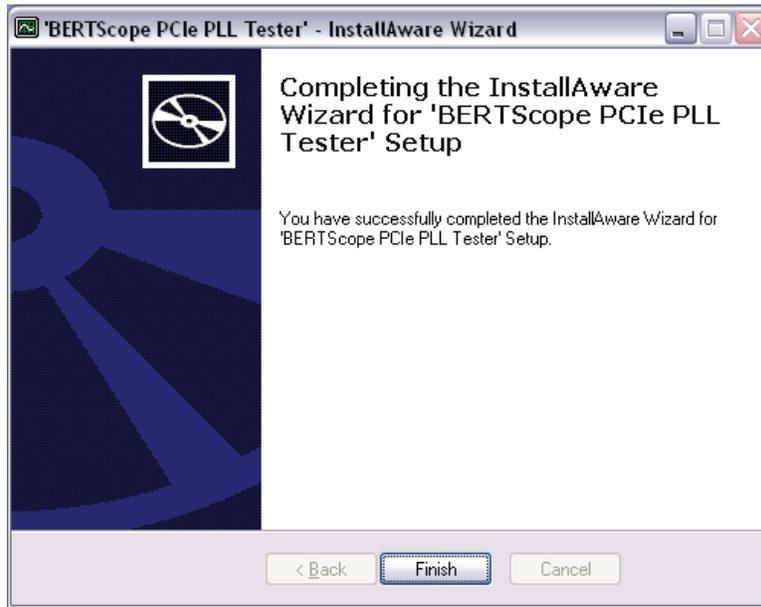
Select the default path on the next screen. Click Next



On the following screen, click Next to install.



A window with a progress bar will appear, showing the installation status. At completion, the following window will appear:



Click Finish.

### ***Installing the USB driver***

The software installer has installed the control software and loaded, but did not install the USB driver for the PLL Analyzer. The user will be prompted to install the driver the first time the PLL Analyzer is connected to the host computer. The driver only needs to be installed once.

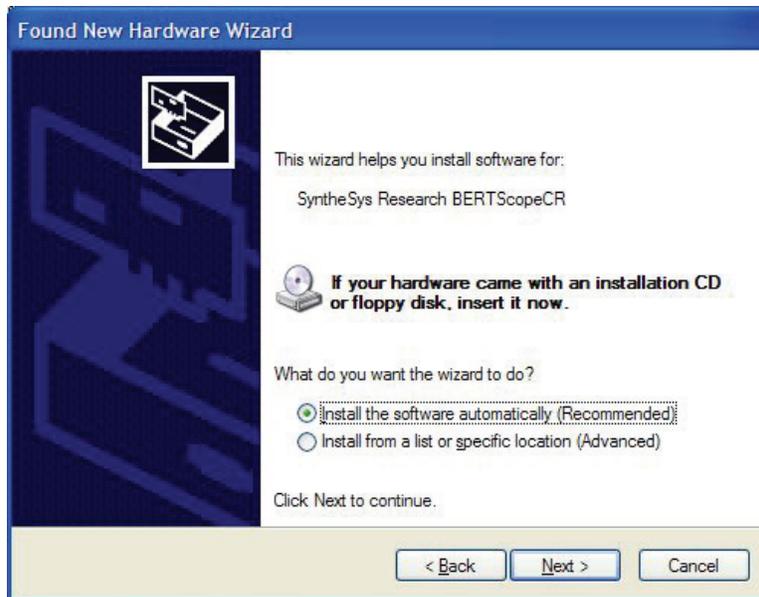
- Be sure the control software has been loaded from the CD-ROM as described in step 2.1 above.
- Power up the host PC and wait for the operating system to fully boot, if not already done. Do not start the PLL Analyzer application at this time.
- Connect the power cable of the PLL Analyzer to a live power outlet and push the power button.
- Using the supplied USB cable, connect the end with the type B connector to the receptacle labeled USB IN on the rear panel of the instrument.



- Connect the other end with the type A connector to an open USB port on the host PC.
- The “Found New Hardware” wizard notice will appear in the lower right side of the Windows Desktop screen. After the operating system detects the type of device, the installation wizard will start.
- The opening window will appear:



- Select the ‘No, not this time’ radio button and then click Next. The Wizard identifies the device as a “SyntheSys Research BERTScope CR”.

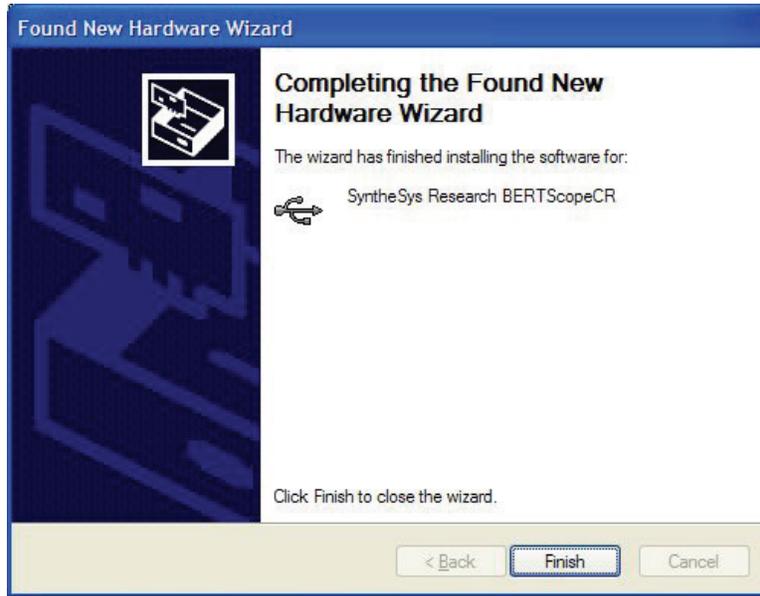


- Use the default 'Install the software automatically (Recommended)' radio button option, then click Next.
- If the Hardware Installation dialog box stating that the driver has not been tested for "Windows XP compatibility" message pops up, press the Continue Anyway button.



*(Continued on next page)*

- After the Completion dialog window appears, click Finish to complete installation.



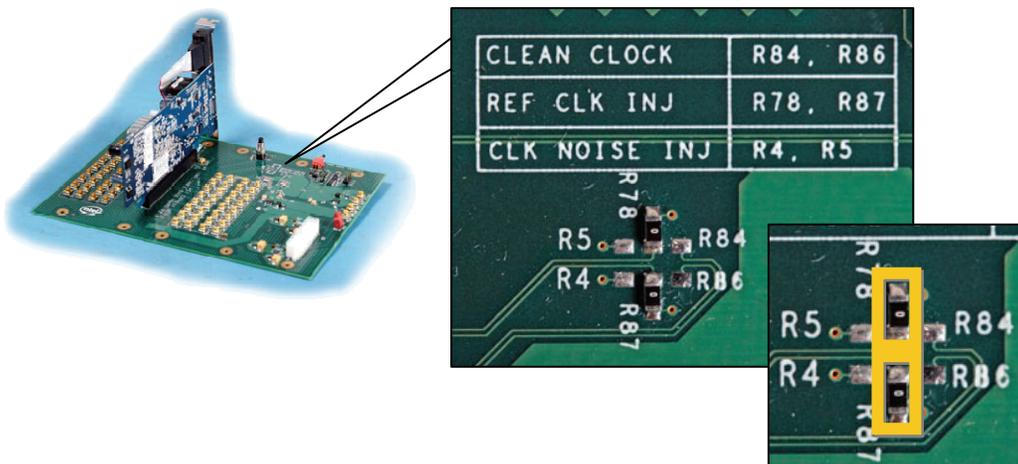
The instrument is now ready to operate.

## ***Completing the PLL Analyzer test setup***

### **Configuring the Compliance Base Board (CBB)**

The Compliance Base Board (CBB) jumpers must be configured to source the distributed REF\_CLK from the input connectors. The CBB fixtures supplied from SyntheSys Research in the PCIE TEST KIT are already properly configured, and can be used immediately for PLL Loop Response testing.

The default configuration of the board as supplied by the PCI-SIG is with the REF\_CLK signal supplied from an on-board clock generator. The configuration change to “REF CLK INJ” is performed by relocating jumpers on the CBB. The jumpers are surface mount devices (0  $\Omega$  resistors), and require a soldering iron to reposition. The jumpers are located near the COMP-MODE-TRIGGER button, SW3. The proper jumper locations are R78 and R87, are shown below.



## Hardware Test Setup

Prior to configuring the test set-up, prepare the area for testing. It is suggested that an ESD dissipating mat be applied to the work surface. A grounding connection is located on the PLL Analyzer instrument.

Configure the instrument and cabling as described below:

1. Connect the supplied USB cable between the USB port on the host PC and the USB IN connector on the rear panel of the PLL Analyzer.

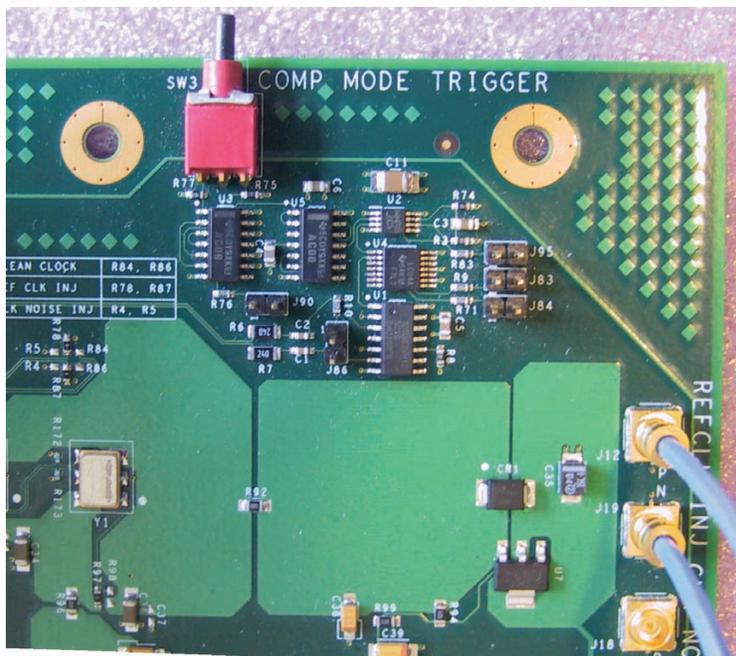


2. Connect the ATX PC Power Supply to the power connector on the Compliance Base Board (CBB)
3. Connect the longer SMA cables between the PCIe CLK+ output on the PLL Analyzer to the REF CLK P input connector on the CBB. Using the second cable, connect the PCIe CLK- output to the REF CLK- input of the CBB. Be sure to observe the proper polarity.

The PCIe CLK output connectors are located on the rear of the model CRJ 125A-PCIE instrument:



The PCIe CLK+ and PCIe CLK- connectors are located on the front panel of the model PLL-PCIE analyzer. The REF\_CLK input connector locations on the CBB are shown below.



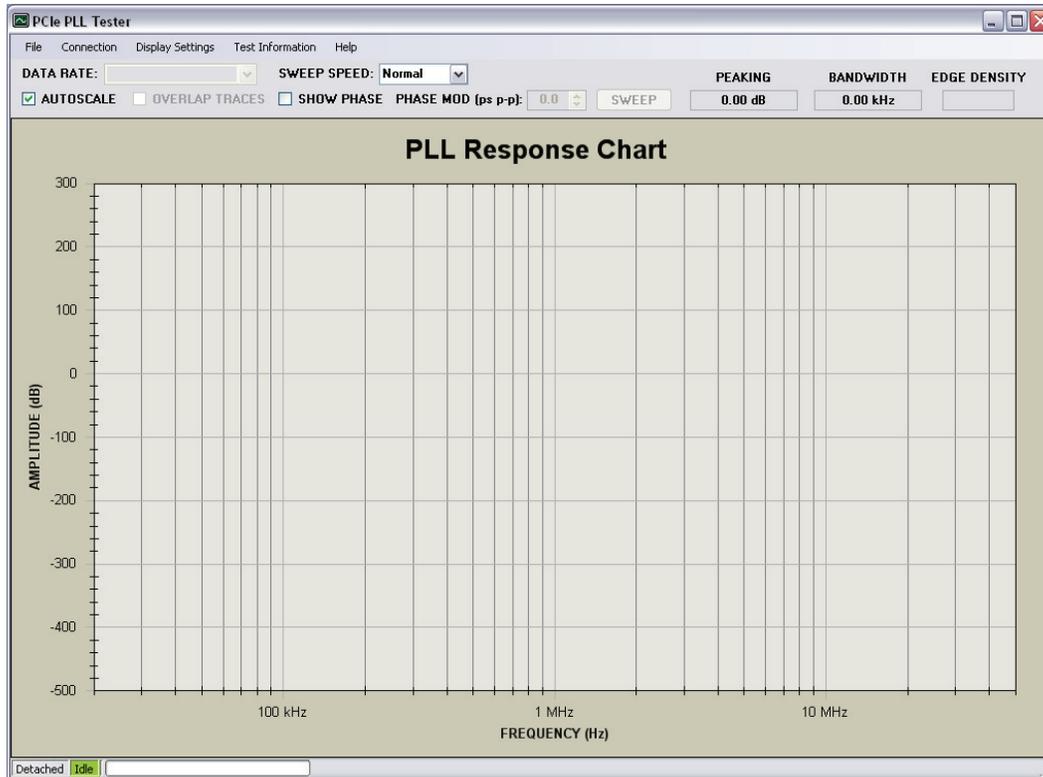
4. Using the short, low loss SMA-M to SMA-M connectors, connect Tx LANE 0 P on the CBB to DATA INPUT+ on the PLL Analyzer.

Connect Tx LANE 0 N on the CBB to DATA INPUT- on the PLL Analyzer. The Data Input connectors are located on the front panel of the instrument. Be sure to observe correct polarity

NOTE: If a model CRJ 125A-PCIE analyzer is being used, the DATA OUTPUT connectors must be terminated into 50  $\Omega$ . Use the terminators supplied with the instrument for this purpose.







In the DATA RATE pull down menu, select either 2.5 GT/s or 5 GT/s, depending on your testing rate.

The phase modulation defaults to 43.4 ps, the maximum allowed by the compliance spec. This setting should be used for a normal compliance test. Higher modulation levels can be entered to characterize sensitivity to modulation level, and observe test margin of this parameter.

Perform the test using the following procedure.

1. Install the Add-In card to be tested into the socket on the CBB. Connect any required auxiliary power connectors to the ATX PC Power supply.
2. Turn on the power supply.
3. Turn on the device power using the PWR switch on the CBB.

Note: The response characteristics in the Tx clock generation PLL in some devices have been known to drift during warm up. When this occurs, the drift appears to have a relatively fast time constant. If the card being tested demonstrates this effect, wait approximately 10 seconds before initiating the test.

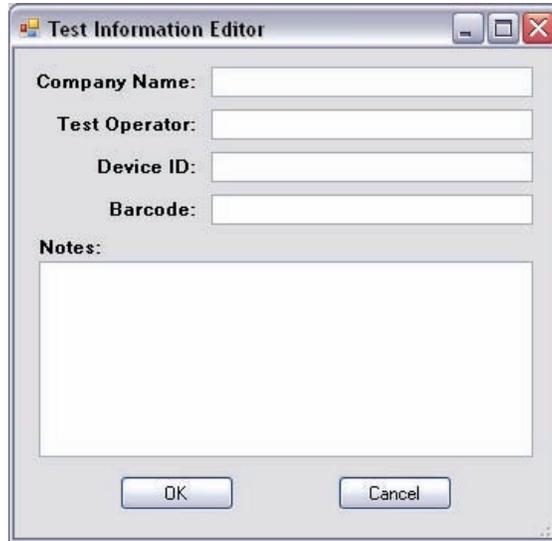
4. Using the COMP MODE TRIGGER button (SW3) on the CBB, cycle through to the proper mode for testing. The power up mode is 2.5 GT/s. Pressing the button once changes the device to 5.0 GT/s, with -3.5 dB pre-emphasis. A second push advances the device to 5.0 GT/s with -6 dB pre-emphasis.

NOTE: the PLA Analyzer will generate correct results while operating at a 5 GT/s data rate with a 2.5 GT/s pattern from the Add-In card. However, the software will apply the incorrect test limits for pass-fail testing. The card operating mode can be easily verified by observing the measured edge density during the test, as described in the next step.

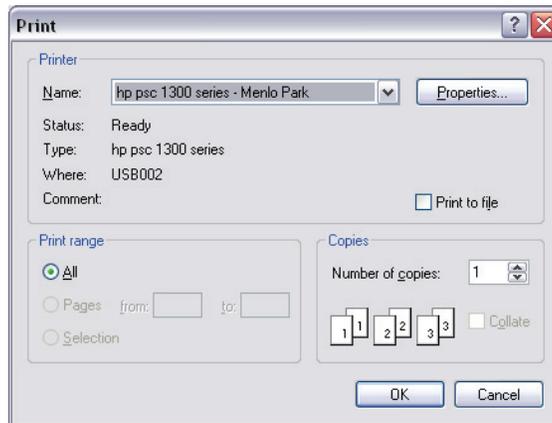
5. Click SWEEP to begin the test. The test will take approximately 15 seconds to complete. Prior to stepping the S<sub>j</sub> modulation, the analyzer initiates the test by generating a clean REF\_CLK signal, and measures the edge density of the Tx output. The measured edge density is displayed continuously in real time in the upper right corner of the application software window.

NOTE: If the device is generating a normal compliance pattern without gaps, the transition density measurement should read approximately 73.4%. A reading of approximately 37% indicates the Add-In card is operating at the 2.5 GT/s rate, while the software is configured to test at 5 GT/s.

- At the completion of the test sweep, the measured loop bandwidth and peaking will be displayed. The software also compares these results against the compliance limits for a generation 2.0 device at the data rate selected, and displays TEST PASSED or TEST FAILED at the top banner of the window.
- To generate a test report hard copy, click FILE-PRINT from the top menu area in the software. A Test Information dialog box will first appear to allow the user to record information which will appear on the test report.



After entering the appropriate information, click OK. This brings up the standard Windows Print dialog box.



Select the printer of choice and click OK to generate a test report hard copy. To generate the test report and save as an HTML file for later printing, select the FILE-PRINT TO FILE option from the top menu in the application.

This completes the PLL Loop Response test.

# Specifications

The following specifications apply to both the CRJ 125A-PCIE and PLL-PCIE instruments:

Parameter	Value
<b>Ref. Clock Output</b>	
Configuration	True differential, compatible with PCIe electrical specifications
Base Frequency	100 MHz
Duty Cycle	50 % $\pm$ 0.1 %
Phase Modulation Frequency	30 kHz – 80 MHz
Modulation amplitude at 100 MHz	0.15 – 1.5 % UI
Residual Phase Jitter	$\ll$ 43.4 ps integrated from 5 to 15 MHz
<b>Measurement Input</b>	
Configuration	True Differential. 50 $\Omega$ , DC Coupled
Connector	APC 3.5 (SMA compatible). User replaceable Winchel Planar Crown
Input Sensitivity	Complies with PCIe specification
Data Rate	2.5, 5.0 and 8.0 GT/s
Transition Density	62.5 – 75 %
Measured Amplitude Resolution	0.01 dB
Frequency Resolution	10 kHz
Relative Amplitude Accuracy	0.05 dB
<b>Measurement Results</b>	
Configuration	PLL loop response magnitude with jitter transfer function and optional loop response phase. Optional cursor at -3 dB point
Plot modes	Last scan only, or overlaid traces from previous scans.
Parameters	PLL bandwidth and peaking' data output transition density. Loop BW and peaking tested against CEM Gen 2 specification limits at 5.0 and 2.5 GT/s data rates.
Hard Copy	Test report including results plot and user entered test data can be printed to local or networked printer, or saved in either HTML or .PDF formats.
<b>General</b>	
Dimensions (W x H x D)	39.4 x 9.5 x 33.6 cm (15.5 x 3/375 x 13.25 in)
Weight	4 kg (9 lbs)
Power Consumption	150 W, max
Power Requirements	90 – 265 VAC rms 47 – 63 Hz

## Environmental

Temperature, Operating	+10 – +40 °C	Tested per MIL-PRF 28800F
Temperature, non-operating	-22 – +60 °C	Tested per MIL-PRF 28800F
Humidity	20 – 80 %, non- condensing	

The following additional specifications apply to the CRJ 125A:

Parameter	Value
<b>Data Inputs/Outputs</b>	
Configuration	True differential, Passive DC coupled through path
Impedance	50 $\Omega$ , Unused outputs must be terminated into 50 $\Omega$
Connector	APC 3.5 (SMA compatible). User replaceable Winchel Planar Crown
Insertion Loss	$\approx$ 1 dB at minimum data rate, increasing linearly to $\approx$ 2 dB at 12.5 Gbps
Input Sensitivity	< 100 mV single ended, < 50 mV differential
Max. Input Voltage	$\pm$ 5 V p-p
<b>Clock Output</b>	
Configuration	Single Ended
Connector	APC 3.5 (SMA compatible). User replaceable Winchel Planar Crown
Amplitude	250 mV – 1.5 mV p-p
Amplitude Accuracy	10% for amplitudes > 300 mV; 30 mV for amplitudes < 300 mV
Transition Time, 20-80 %	30 ps max, 25 ps typical
Return loss	15 dB typical
Intrinsic Jitter	70 fs typical. 250 fs rms max, measured at 800 mV p-p input, 10 Gbps, 1010 pattern.
Sub-rate output divider ratios:	1, 2, 4, 5, 6, 7, 8, 9,10, 12, 14, 16, 18, 20, 24, 25, 28, 30, 32, 35, 36, 40, 42, 45, 48, 49, 50, 54, 56, 60, 63, 64, 70, 72, 80, 81, 90, 100, 108, 112, 120, 126, 128, 140, 144, 160, 162, 168, 180, 192, 196, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 336, 360, 384, 392, 432, 448, 504, 512, 576, 648
<b>Clock Recovery</b>	
Output Clock Range	150 MHz – 12.5 GHz, continuous with no range gaps
Loop Bandwidth	100 kHz – 12 MHz, variable
Loop Bandwidth Accuracy	$\pm$ 5 %
Loop Frequency Response	-20 dB/decade to -40 dB/decade
Loop Peaking	0 – 6.0 dB for BW $\geq$ 500 kHz. 0 dB for BW < 500 kHz
Loop Peaking Accuracy	10 % for peaking $\geq$ 2.0 dB, 0.2 dB for peaking < 2.0 dB
Loop Locking Range	$\pm$ 50 MHz default, adjustable from 10 – 500 MHz
Loop Tracking Range	SSC +500 to -5500 ppm (+0.05 to -0.55 %) deviation, 30-33 kHz triangle modulation

Lock Modes	Auto and Manual
Edge Density compensation	Auto – uses the first measured edge density after lock or manually entered. Displays error message when measured edge density greatly differs from setting.
Clock Recovery Measurements	Input Edge Density, Phase deviation in pk-pk and rms. displayed on instrument front panel. Actual PLL Response and jitter transfer function displayed through control software.

### Trigger Output

Signal	TTL Compatible, from 50Ω, available on rear panel SMA connector
Latency	≈ 300 ms

### Trigger Input

Signal	TTL Compatible, DC coupled into from 50Ω, available on rear panel SMA connector.
Min. pulse width	50 ns

### Jitter Spectrum Measurements

Display	Plot of jitter spectrum versus component frequency. Peak or Envelop (Peak Hold) modes. User positionable cursors allow integrated jitter spectrum to be measured between selected frequency range.
Jitter Component Frequency Range	200 Hz – 90 MHz
Minimum Frequency Resolution	200 Hz
Vertical Units	ps or % UI
Vertical Scale	Linear or Log
Intrinsic Noise Floor	≈70 fs for component frequency > 1 MHz, 250 fs rms max.

### Other Measurements

Duty Cycle Distortion	0 – 50 % UI, displayed in % UI or ps.
SSC Modulation	Display of SSC modulation waveform (period deviation versus time). Vertical units of PPM deviation or ps. Horizontal fixed for 30–33 kHz modulation frequency.