PIM2
PULSE INPUT MODULE 2

The Pulse Input Module 2 (PIM2) provides four channels of 16 bit or two channels of 32 bit event counting with channel-to-channel independent totalizing capability. All counters (one per channel) are independently readable and resettable.

Each input channel is provided with a separate gate input. These gates allow the event inputs to be configured as four dual input channels to allow the input events to be gated by other external sources.

Input events can be counted at speeds of up to one million pulses per second. Concatenation of counters allows for counting of over four billion (4×10^9) events.

Anti-coincidence circuitry ensures that the counters are not read in an undefined state.

Software control selects input channel and channel to be reset.

Signals are connected directly to the module via on-card quick disconnect terminals.

Installation

Series 500 system:

The PIM2 module may be placed in any available slot in the Series 500; however, digital modules should generally be placed in the high-numbered slots if any analog modules are present in the system.

To install the module, remove the baseboard top cover and insert the module into the desired slot with the component side facing the power supply.

CAUTION: Always turn off the baseboard power before installing or removing modules. Replace the top cover and secure it with screws. To avoid the possibility of EMI radiation, never operate the system with the top cover removed.

System 570:

The System 570 can accept one PIM2 module in its option slot. To install the module, position it so that the cable strain relief is towards the rear of the unit; insert the card edge into the guide and carefully slide the card into the option slot.

CAUTION: Always turn off the power to the 570 mother board before installing or removing modules in/from the option slot. To avoid the possibility of EMI radiation, never operate the system with the top cover open.

For either system, update the software configuration table to show the location of the PIM2.

User-Configured Components

See Table 1 and Figure 1 for a list of user-configured components and their locations on the PIM2 module.

Switch 1 (S1) selects between separate 16 bit operation of counters 0 and 1, or concatenation of these two counters (32 bits). Switch 2 (S2) selects between separate 16 bit operation of counters 2 and 3, or concatenation of these two counters (32 bits).

Each of the four segments of switch set 3 either connects or disconnects the gate input signal at the terminal connector to or from the gate input circuit.

Table 1. User-Configured Components on the PIM2

Name	Designation	Function
Switch 1	S1	Channels 0 and 1 16 bits each (0,1) or both concatenated (0→1) 32 bits.
Switch 2	S2	Channels 2 and 3 16 bits each (2,3) or both concatenated (2→3) 32 bits.
Switch set 3	S3	Connect/disconnect gate input signal at the terminal connector to/from gate input circuit. (One switch/channel).

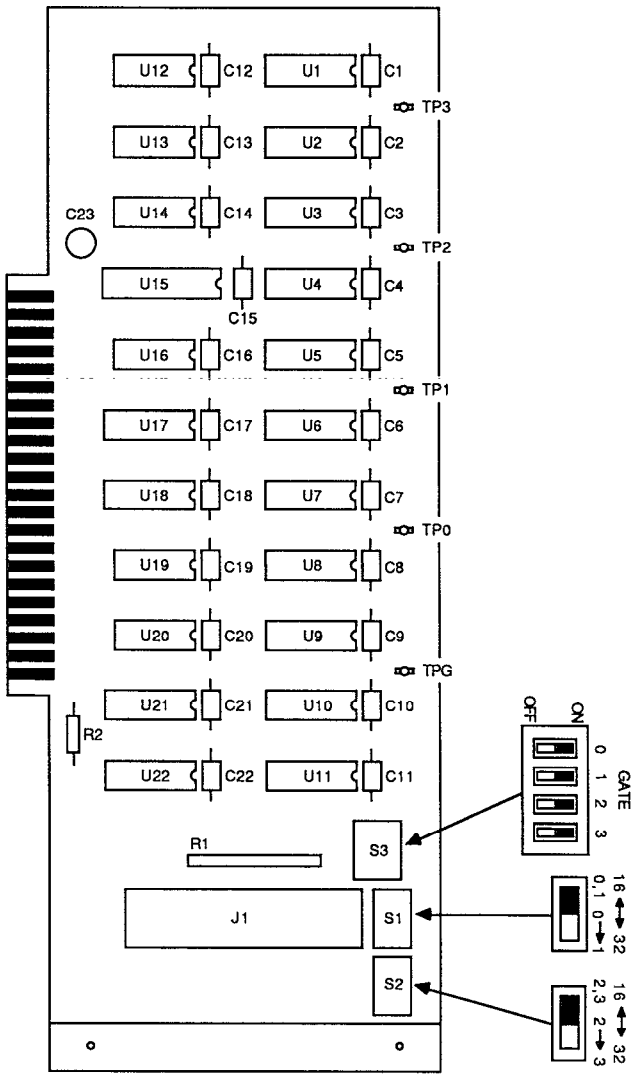


Figure 1. PIM2 Module

Connections

All connections to the PIM2 are made to screw terminal J1. This terminal accepts 16-24 gauge wire stripped to 3/16 of an inch.

The connecting terminal for the PIM2 is shown in Figure 2 which illustrates a typical connection. Figure 3 shows a possible connect-ing scheme in which the module is hardware configured to accept a gated input signal.

When making any connections to the PIM2, keep in mind that all input channels are TTL compatible. Also, though not necessary for operation, the use of shielded cable is recommended to minimize the possibility of EMI (Electro-Magnetic Interference) radiation. In this case the cable would contain the typical two leads for signal and ground plus an outside shield. Connect the signal and ground leads as shown in Figure 2, connect one end of the shield to a rear chassis ground post and leave the other end disconnected. Never use the shield as a signal carrying lead.

CAUTION: PIM2 inputs are non-isolated, meaning that circuit ground is connected to power line ground. Any circuits connected to the module must also be referenced to power line ground and must not be floating.

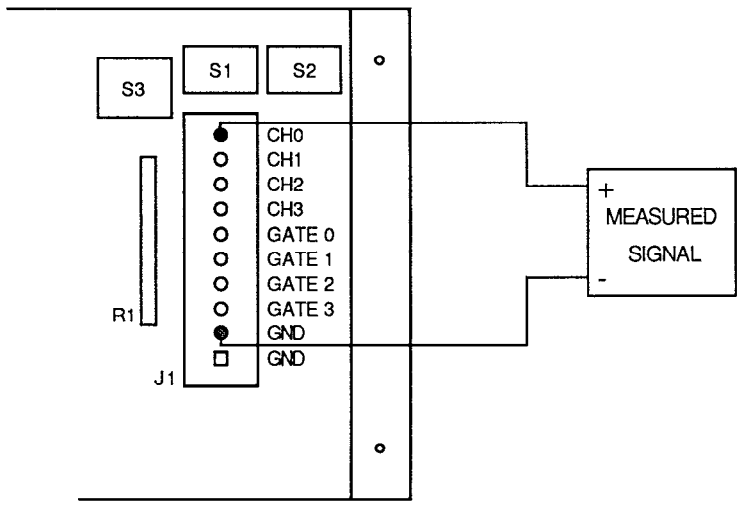


Figure 2. Typical PIM2 Connection

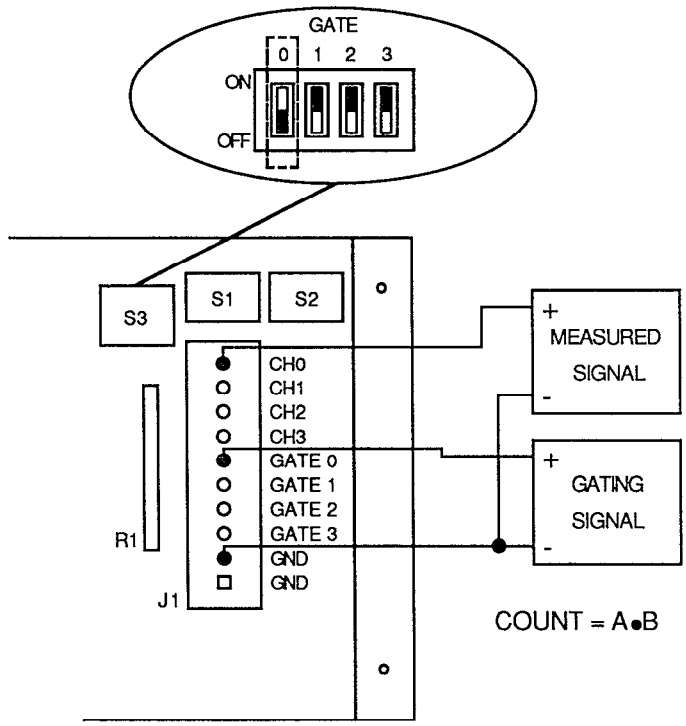


Figure 3. Typical Gated Input Connection

Computer Memory Locations

The memory locations of the computer can hold only 8 bits of information (more commonly referred to as a BYTE). To store a 16 bit number in memory, that number must be broken into two bytes - high byte and low byte - and stored in two consecutive memory locations. The same reasoning applies to a 32 bit number. Here, 4 memory locations are to hold the needed number (4 locations × 8 bits/location = 32 bits).

Commands

PIM2 peek/poke memory locations provide software control of the channel to be selected and the channel to be reset. These memory locations are also used to read the low and high byte of event data from the selected counter.

PIM2 commands are summarized in Table 2. Table 3 lists the memory locations for the slot-dependent commands.

Table 2. Commands used with the PIM2 module

Command	Location	
CHANNEL SELECT	Slot-dependent CMDA	(Write) *
CHANNEL RESET	Slot-dependent CMDB	(Write) *
READ LOW DATA	Slot-dependent CMDA	(Read)
READ HIGH DATA	Slot-dependent CMDB	(Read)

*Legal values written to either CMDA or CMDB locations are 0,1,2 or 3, for channels 0-3 respectively.

Table 3. Memory locations for slot-dependent commands

SLOT	CMDA	CMDB
Slot 1	CFF80	CFF81
Slot 2	CFF82	CFF83
Slot 3	CFF84	CFF85
Slot 4	CFF86	CFF87
Slot 5	CFF88	CFF89
Slot 6	CFF8A	CFF8B
Slot 7	CFF8C	CFF8D
Slot 8*	CFF8E	CFF8F
Slot 9	CFF90	CFF91
Slot 10	CFF92	CFF93

*Locations of slot dependent commands for the option slot of System 570.

CHANNEL SELECT

Location: Slot-dependent CMDA - Write only.

Legal values written to the Channel Select register are 0-3. Writing any of these values to the channel select location will determine which of the four input channels (0-3) on the PIM2 is to be read.

CHANNEL RESET

Location: Slot-dependent CMDB - Write only.

Legal values written to Channel Reset are 0-3. Writing any of these values to the channel reset location will immediately reset the respective hardware counter (0-3) to zero.

In 32 bit mode, it is only necessary to issue a CHANNEL RESET to the lower order 16 bit counter. The upper 16 bit counter is reset automatically.

An important point to remember here is that CHANNEL RESET only clears the counters to zero and not the data (count) that we actually read. It is this feature of the module that allows for two different modes of operation when reading the data from

the counters. In one mode, CHANNEL RESET is issued at the begin-ning only, just to ensure that the counters are initialized to zero.

In the second mode, CHANNEL RESET is issued every time after the first read (the first read latches the entire count whether in 16 or 32 bit mode). This mode allows the counters to start counting again while we are still reading the last count they supplied. This allows for maximum throughput.

Note that powering-on will not automatically reset the counters to zero. The CHANNEL RESET command must be issued to ensure that the desired counter is properly reset.

LOW DATA

Location: Slot-dependent CMDA

Reading the LOW DATA location provides the low byte of the current count from the counter previously selected with CHANNEL SELECT. To obtain the complete count, the HIGH DATA location should be read immediately after reading LOW DATA, and the two bytes combined as described below:

COUNT 16 = LOBYTE + (256 * HIBYTE)

The actual count from any given counter is latched at the time the LOW DATA location is read. This ensures that the low byte does not overflow before the high byte is access-ed with the HIGH DATA command.

In 32 bit mode, the functionality just described still applies, the only difference being that 32 bits of data must be read and combined instead of 16.

To read the count from a 32 bit counter, follow these steps:

1. Issue a CHANNEL RESET to the lower order 16 bit counter. The upper order 16 bit counter is automatically reset.
2. Issue a CHANNEL SELECT for the low order 16 bit counter.
3. Read the LOW DATA location for the counter just selected. This action supplies the lowest order 8 bits and most importantly it latches the entire 32 bit count.
4. Read the HIGH DATA location.
5. Issue a CHANNEL SELECT for the higher order 16 bit counter.
6. Read the LOW DATA location.
7. Read the HIGH DATA location.

To obtain the complete count, the four bytes from the two 16 bit counters must be com-bined as described below:

COUNT 32 = COUNT16L + (65536 * COUNT16H)

Where

COUNT16L = 16 bit count from the lower order counter and COUNT16H = 16 bit count from the higher order counter.

HIGH DATA

Location: Slot-dependent CMDB

Reading the HIGH DATA location provides the high byte of the current count. The LOW DATA location should always be read before reading HIGH DATA. This ensures that the current count is latched, preventing the low byte from overflowing before the high byte is read.

Theory of Operation

Circuitry on the PIM2 module, which is shown on schematic drawing number 501-146, may be divided into six groups:

1. Input/Gating circuitry
2. Anti-Coincidence detection
3. Command development and function decoding
4. 16/32 bit selection
5. Counters circuitry
6. Data buffering

From the terminal connector, input signals are routed through four sections of a hex-Schmitt trigger inverter (U19-74LS14). These elements add hysteresis to the input signals to provide the counters with clean-jitter-free square waves regardless of the shape of the original input signal. The gating circuitry is made up of a quad NAND gate (U20-74LS00), one section of R1, and switch S3.

The anti-coincidence detection circuitry is made up of two transparent data latches (U11 and U22-74LS75). These circuits assure that the counters are never read in an undefined state.

The command development circuitry is made up of a quad OR gate (U16-74LS32), two dual four line decoders (U17 and U18-74LS139), a transparent data latch (U21-74LS75), and two sections of a hex inverter (U13-74LS04). This circuitry decodes the baseboard command signals CMDA and CMDB, the READ/WRITE signal, and two data lines (D0 and D1) to produce the necessary read/write functions for each counter.

The circuitry to select between 16 or 32 bit operation is made up two-quad data selectors (U9 and U10-74LS157), and switches S1 and S2.

The counters are made up of U1-U8, which are 8 bit binary counters (74LS590). Two of these units are used per each 16 bit counter. Counter circuitry is also supported by U12 (74LS00), U13 (74LS04), and U14 (74LS32).

All counters are connected to a common data bus. Buffering beween this internal data bus and the baseboard data bus is proided by U15, an octal data buffer (74LS244).

Specifications

Input Characteristics:

All inputs non-isolated and TTL compatible

Absolute maximum input voltage = +5.5/−0.3V

High level input current = 20μA

Low level input current = −400μA.

Maximum Count:

1. No concatenation (16 bits/counter): 65536 events.
2. With concatenation (32 bits/counter): over 4 billion events (4,294,967,295) per set of concatenated counters.

Resolution: 16/32 bits (normal/concatenated).

Maximum Counting Speed:

1. Real-time totalizing (read-only mode, no reset): 250,000 pulses/second, or 250kHz.
2. Sampled input count (read and reset counter mode): 1,000,000 pulses/second, or 1MHz.

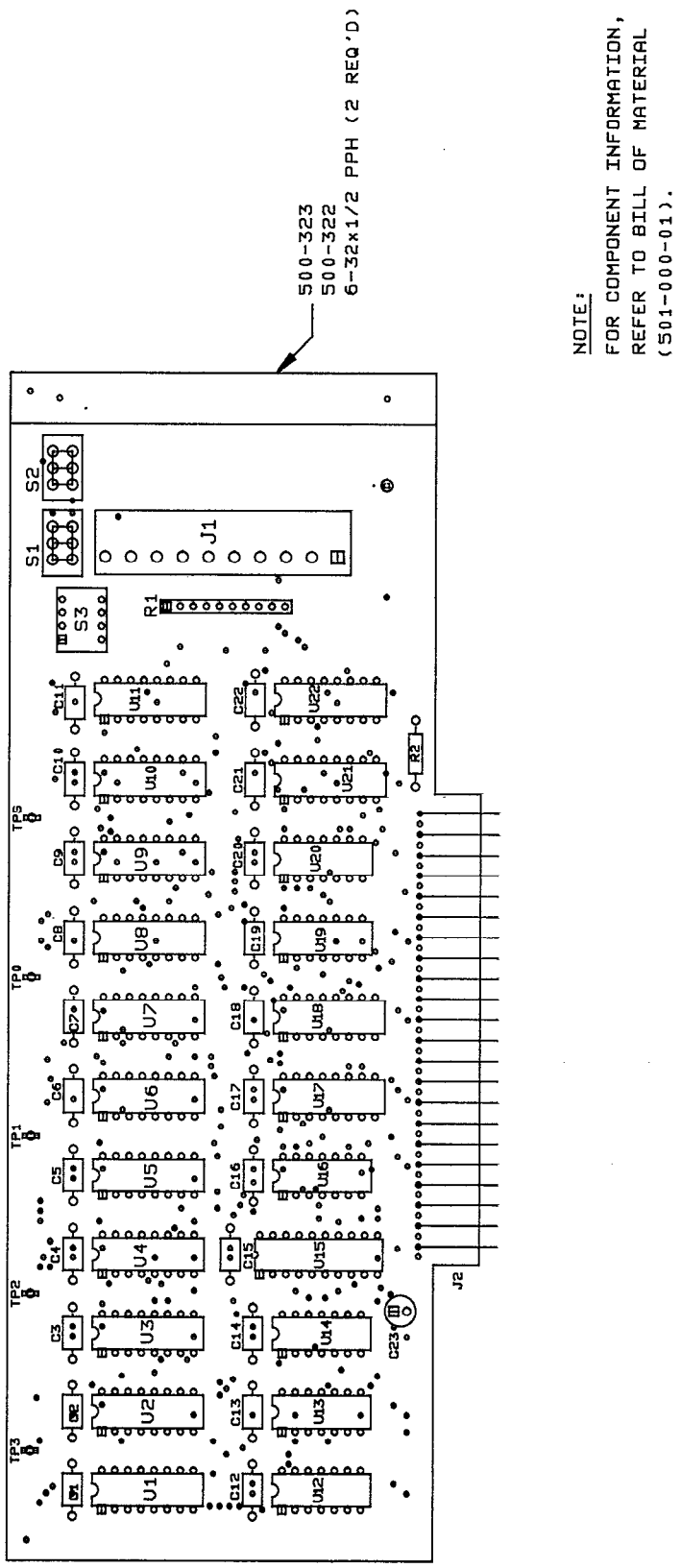
Gated Input Non-coherence: ±1 count.

Minimum Input Pulse Width: 50nsec.

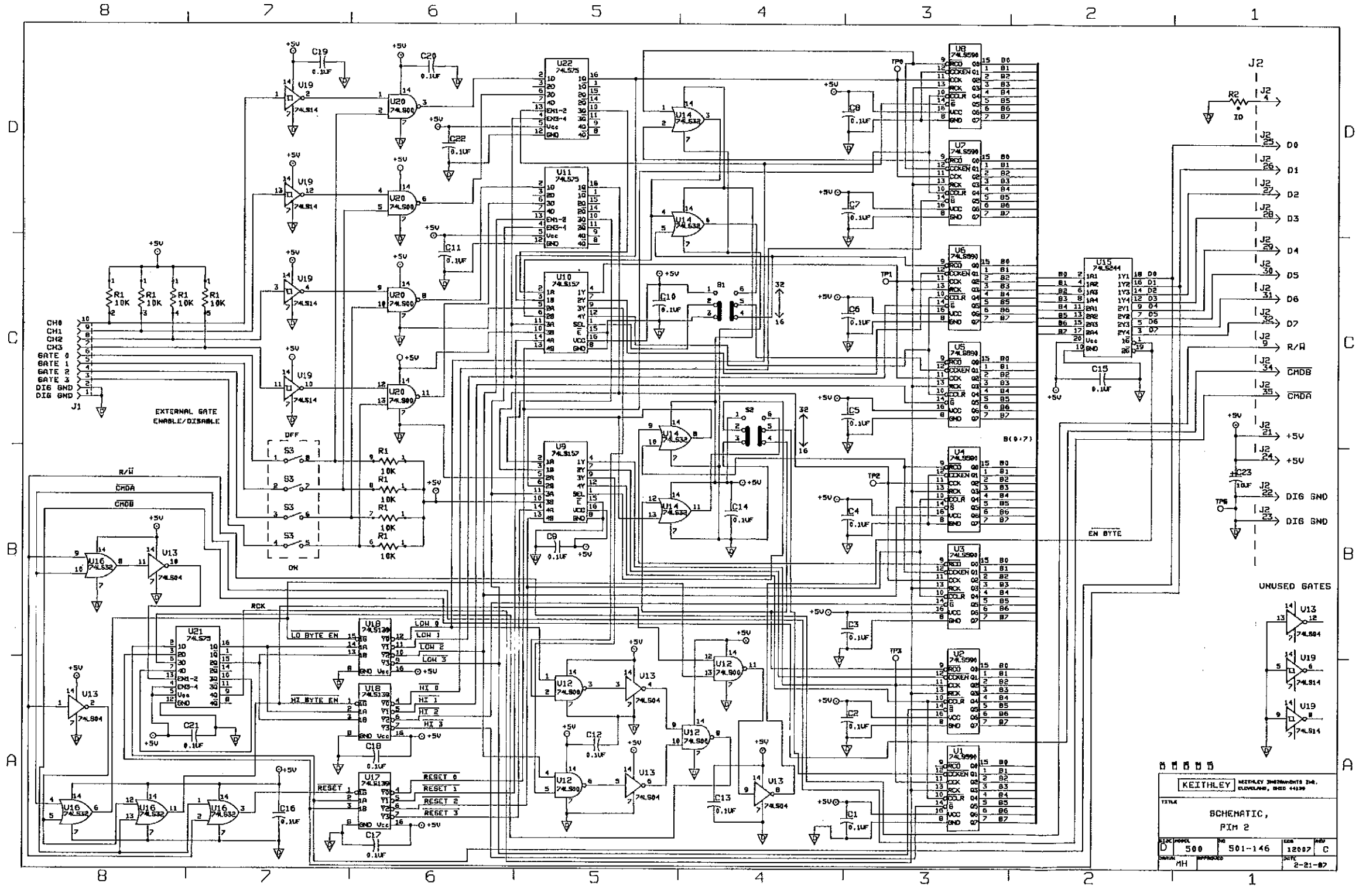
Power Requirements: +5V 475mA.

Key Features:

* Four channel, fully synchronous event counter with channel to channel independent totalizing capability.
* All counters independently readable and resettable.
* Four separate gates allow the inputs to be configured as four dual input channels to allow the input events to be gated by external sources.
* Concatenation of counters is available by means of user-selectable switches to obtain two fully-independent, fully synchronous 32 bit counters.



PIM2 COMPONENT LAYOUT



PIM2 SCHEMATIC DIAGRAM