Tektronix®

AWG5200 Series
Arbitrary Waveform Generators
Specifications and Performance Verification

Technical Reference

Revision B

Warning

The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries before performing service.

www.tek.com

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- In North America, call 1-800-833-9200.
- Worldwide, visit www.tek.com to find contacts in your area.

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General safety summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

To avoid fire or personal injury

Use proper power cord. Use only the power cord specified for this product and certified for the country of use.

Ground the product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe all terminal ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Power disconnect. The power cord disconnects the product from the power source. Do not block the power cord; it must remain accessible to the user at all times.

Do not operate without covers. Do not operate this product with covers or panels removed.

Do not operate with suspected failures. If you suspect that there is damage to this product, have it inspected by qualified service personnel.

Avoid exposed circuitry. Do not touch exposed connections and components when power is present.

Do not operate in wet/damp conditions.

Do not operate in an explosive atmosphere.

Keep product surfaces clean and dry.

Provide proper ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Terms in this manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

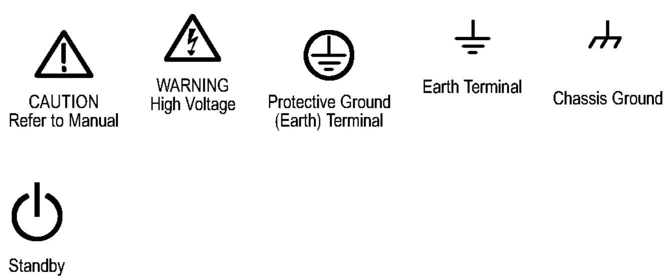
CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Symbols and terms on the product

These terms may appear on the product:

- DANGER indicates an injury hazard immediately accessible as you read the marking.
- WARNING indicates an injury hazard not immediately accessible as you read the marking.
- CAUTION indicates a hazard to property including the product.

The following symbol(s) may appear on the product:



Service safety summary

Only qualified personnel should perform service procedures. Read this *Service safety summary* and the *General safety summary* before performing any service procedures.

Do not service alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use care when servicing with power on. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This manual contains specifications and performance verification procedures for the AWG5200 Series Arbitrary Waveform Generators.

Related documents

The following documents are also available for this product and can be downloaded from the Tektronix website www.tek.com/manual/downloads.

- *AWG5200 Series Installation and Safety Manual*. This document provides safety information and how to install the generator. Tektronix part number: 071-3529-xx.
- *AWG5200 Series Programmer Manual*. This document provides the programming commands to remotely control the generator. Tektronix part number: 077-1337-xx.
- *AWG5200 User Manual*. This document is a printable version of the AWG5200 help system. Tektronix part number: 077-1334-xx.

Specifications

This section contains the specifications for the AWG5200 series Arbitrary Waveform Generators.

All specifications are typical unless noted as warranted. Warranted specifications that are marked with the ✓ symbol are checked in this manual.

Performance conditions

To meet specifications, the following conditions must be met:

- The instrument must have been calibrated/adjusted at an ambient temperature between +20 °C and +30 °C.
- The instrument must be operating within the environmental limits. (See Table 38 on page 26.)
- The instrument must be powered from a source that meets the specifications. (See Table 36 on page 23.)
- The instrument must have been operating continuously for at least 20 minutes within the specified operating temperature range.

Electrical specifications

Table 1: Run mode

Characteristics	Description
Continuous mode	An arbitrary waveform is output continuously.
Triggered mode	An arbitrary waveform is output only once when a trigger signal is applied. After the waveform is output, the instrument waits for the next trigger signal.
Triggered continuous mode	An arbitrary waveform is output continuously after a trigger signal is applied.

Table 2: Arbitrary waveform

Characteristics	Description
Waveform memory	Real Waveforms: 2 Gs/channel Complex waveforms: 1 Gs/channel
Minimum waveform size	
Continuous run mode	1 sample
Triggered run modes or sequence	Real waveform: 2400 samples Complex waveform: 1200 samples Real waveforms are waveforms that have a single input value for each sample point. IQ waveforms, referred to as “Complex waveforms”, use 2 values for each sample point.
Waveform granularity	
Continuous run mode	1 sample
Triggered run modes	1 sample
IQ (Complex) waveform support	IQ waveforms, referred to as “Complex waveforms”, are supported for use with real time digital up-conversion and play out. The carrier signal is generated independently of the waveform with an NCO (Numerically Controlled Oscillator). The waveform requires 2 values for each sample point. In the IQ waveform, I and Q samples alternate in pairs or groups depending on the interpolation selection. The format depends on the interpolation rate selected (2x or 4x)

Table 3: Real time digital signal processing

Characteristics	Description
Double Data Rate Interpolation (DDR Mode)	Enabling DDR mode increases the output sample rate to 5 to 10 GS/s (2*fclk) and interpolates the input sample data by 2X to match the output rate. 2X interpolation is required for sample rates above 5.0 GS/s. With DDR enabled, the output image moves from (fclk - fout) to (2*fclk - fout). Because the input data rate does not increase, the output bandwidth remains (fclk/2). DDR is most useful when combined with digital up-conversion which allows the user to specify the output center frequency up to the DDR Nyquist frequency. When the waveform is a traditional, real valued, waveform (not IQ), enabling DDR applies a low pass filter at a frequency just below (fclk/2) so that no signal is generate between (fclk/2) and (2*fclk - fclk/2).
Digital Up-conversion (DIGUP license required)	The DAC system in each channel includes a digital IQ modulator and numerically controlled oscillator (NCO) that provides digital up-conversion to a specified carrier frequency Digital up-conversion requires an IQ input waveform. In the IQ waveform I and Q samples alternate in pairs or groups depending on the interpolation selection. Digital up-conversion can only be used with sample rates between 2.5 and 5 GS/s. Use interpolation when a lower waveform sample rate is needed.
Waveform interpolation	Real time interpolation of IQ (complex) waveforms is supported independently on each channel during play out. Supported interpolation rates are 2x and 4x. Only IQ (complex) waveforms can be interpolated. The interpolation factor refers to the sample rate of the complex pair of points relative to the global instrument sample rate set by the clock. For example if the sample rate is set to 5 GS/s and the interpolation factor is 2, then the waveform sample rate of both I and Q samples is 2.5 GS/s. DDR interpolation offers an additional doubling of the sample rate.
Inverse SINC filter	Real time correction of the sinx/x frequency roll off can be enabled or disabled independently on each channel.

Table 4: Sequencer

Characteristics	Description
Number of steps	16,384 (maximum) 14 address bits
Maximum repeat count	1048576 (2^{20})

Table 5: Sample clock generator

Characteristics	Description
Sample rate	The sample clock frequency is a global parameter that applies to all channels. DDR can be enabled on a per channel basis allowing the sample rate to be doubled on selected channels. The sample clock frequency is always between 2.5 GHz and 5 GHz. To achieve sample rates lower than 2.5 GS/s, the system replicates points. The number of replicated points increases by powers of 2, therefore the clock frequency is $SR \times 2^n$,. where n is an integer that results in a frequency between 2.5 GHz and 5 GHz. When using complex waveforms digital up conversion, the sample rate is limited to 2.5 GS/s to 5 GS/s. To achieve lower sample rates, use waveform interpolation.
DDR enabled:	Real waveforms: 596 S/s to 10 GS/s Complex (IQ) waveforms: 5 GS/s to 10 GS/s
DDR disabled	Real waveforms: 298 S/s to 5 GS/s Complex (IQ) waveforms: 2.5 GS/s to 5 GS/s
Sample rate resolution	
Jitter Reduction Mode (PLL integer mode)	3 digits with jitter reduction (50 MHz sample clock frequency steps from 2.5 GHz to 5 GHz). With DDR enabled, the resolution is 100 MHz Sample rates below the clock range are a power of 2 division of the clock frequency so Low Jitter sample rates are a power of 2 divisions of the 50 MHz stepped frequencies.
Without Jitter Reduction (PLL FracN mode)	8 digits
✓ Sample rate frequency accuracy	Sample Rate * 10 MHz Ref Accuracy/10 MHz Example: 5 GS/s * (±20 Hz)/10 MHz = ±10 kHz
✓ 10 MHz reference accuracy	10 MHz ± 20 Hz (Temperature between 0 to 50 °C; includes aging within 1 year of calibration.)

Table 6: Analog output skew

Characteristics	Description
Skew between (+) and (–) outputs	±15 ps
Skew between channels	±25 ps Skew is calibrated using the (+) outputs of the DC High BW output path for each channel. Channel delay will change when a different path is selected or when various DAC features are enabled.
Delay change from DC High BW output path to other output paths	
DC High Volt (Option HV)	1.2 ns
AC Direct	340 ps
AC Amplified (Option AC)	740 ps
Skew adjustment range	±2 ns Used to adjust skew between channels in a single instrument.

Table 6: Analog output skew (cont.)

Characteristics	Description
Skew adjustment resolution	250 fs
Skew stability between channels	
Sync out to channel	< ±0.5 ps/ °C
Channel to channel	< ±0.5 ps/ °C (±0.18 ps/ °C @ 1 GHz)
Phase adjustment	Used to adjust skew between all channels in an instrument relative to another instrument.
Range	-8,640° to +8,640° of the DAC clock.
Resolution	0.1° of the DAC clock.

Table 7: Signal output characteristics

Characteristics	Description
Connector type	2 SMA connectors per channel.
Number of outputs	AWG5202: 2. AWG5204: 4. AWG5208: 8.
DAC resolution	16, 15, 14, 13 or 12 bits. Enabling markers degrades resolution. 16-bit mode: 0 markers available. 15-bit mode: 1 marker, M1. 14-bit mode: 2 markers, M1, M2. 13-bit mode: 3 markers, M1, M2, M3. 12-bit mode: 4 markers, M1, M2, M3, M4.
Type of outputs	
Output path	
DC High BW	(+) and (–) complementary (differential). Includes a variable gain, high bandwidth, DC coupled amplifier in the signal path.
DC High Volt (Option HV)	(+) and (–) complementary (differential). An additional amplifier adds high amplitude with reduced bandwidth.
AC Direct	Single ended output from the (+) connector. A direct connection to the DAC output including a balun to reduce common mode distortion. The AC Direct path offers the lowest noise and distortion performance.
AC Amplified (Option AC)	Single ended output from the (+) connector. Includes an amplified path and a passive variable attenuator path to provide a large output amplitude range.
ON/OFF control	Independent control for each analog output channel.
Output impedance	50 Ω

Table 7: Signal output characteristics (cont.)

Characteristics	Description
VSWR	
Output path	
DC High BW (Includes option DC Amplified)	DC to 1 GHz < 1.25:1 1 GHz to 3 GHz < 1.9:1 3 GHz to 4 GHz < 2.3:1
DC High Voltage (Option HV)	DC to 400 MHz < 1.6:1 400 MHz to 1 GHz < 1.75:1 1 GHz to 2 GHz < 2.3:1
AC Direct	10 MHz to 300 MHz < 2.0:1 300 MHz to 1.4 GHz <1.6:1 1.4 GHz to 3 GHz < 2.2:1 3 GHz to 4 GHz < 2.5:1
AC Amplified (Option AC)	10 MHz to 500 MHz < 2.4:1 500 MHz to 1.5 GHz < 1.75:1 1.5 GHz to 4 GHz < 1.9:1
Output Modes	
NRZ	In NRZ mode, each sample is held for the entire sample period (1/sample rate). This results in the familiar sin(x)/x frequency response. With DDR mode enabled, the sin(x)/x bandwidth doubles.
RZ	In RZ mode, each sample is held for half of the sample period. This doubles the sin(x)/x bandwidth, but reduces the amplitude by half. This may be useful when playing a real waveform with the signal in the second Nyquist zone. For real waveforms, DDR mode filters the signal in the 2nd and 3rd Nyquist zones and is not useful in this case.
MIX Mode	In Mix mode, each sample is inverted for the second half of the sample period. This is effectively like mixing the output waveform with the sample clock. This boosts the signal in the second Nyquist zone, but zeros the DC component of the waveform and reduces low frequency components. This may be useful when playing a real waveform with the signal in the second Nyquist zone. For real waveforms, DDR mode filters the signal in the 2nd and 3rd Nyquist zones and is not useful in this case.
Amplitude control	Independent amplitude control for all channels. Units of dBm or V can be selected.
Amplitude range	
Output path	
DC High BW	25 mV_{p-p} to 750 mV_{p-p} into 50 Ω single-ended. 50 mV_{p-p} to 1.5 V_{p-p} into 100 Ω differential.
DC High BW (with Option DC Amplified)	25 mV_{p-p} to 1.5 V_{p-p} into 50 Ω single-ended. 50 mV_{p-p} to 3.0 V_{p-p} into 100 Ω differential.
DC High Volt (Option HV)	10 mV_{p-p} to 5 V_{p-p} into 50 Ω single-ended. 20 mV_{p-p} to 10.0 V_{p-p} into 100 Ω differential.

Table 7: Signal output characteristics (cont.)

Characteristics	Description
AC Direct	–17 dBm to –5 dBm. 10 MHz to 3.5 GHz.
AC Amplified (Option AC)	–85 dBm to 10 dBm (10 MHz to 3.5 GHz.) –50 dBm to 10 dBm (3.5 GHz to 4 GHz.) Amplitude accuracy and flatness degrades at frequencies beyond 3.5 GHz and below –50 dBm output amplitude. It is not recommended to operate in this region.
Amplitude adjustment resolution	
Output paths	
DC High BW	1 mVpp or 0.01 dB.
DC High Volt (Option HV)	1 mVpp or 0.01 dB.
AC Direct	0.1 dB
AC Amplified (Option AC)	0.1 dB
✓ DC amplitude accuracy	Within ±5 °C of internal self calibration temperature.
Output path	
DC High BW	Amplitude < 100 mV: ±5% of amplitude Amplitude 100 mV to 1.5 V: ±2% of amplitude
DC High Volt (Option HV)	Amplitude < 160 mV: ±5% of amplitude Amplitude 160 mV to 5 V: ±2% of amplitude
AC amplitude accuracy	
Output path	
AC Direct	0.5 dB at 100 MHz (0 °C to 45 °C) 1 dB at 100 MHz (45 °C to 50 °C)
AC Amplified (Option AC)	0.5 dB at 100 MHz (0 °C to 45 °C) 1 dB at 100 MHz (45 °C to 50 °C)
DC Offset range	
Output path	
DC High BW	± 2 V into 50 Ω to ground termination. ± 4 V into high resistance or matching voltage termination.
DC High Volt (Option HV)	± 2 V into 50 Ω to ground termination. ± 4 V into high resistance or matching voltage termination.
DC Offset resolution	
Output path	(AC-path outputs use a different output bias circuit.)
DC High BW	1 mV
DC High Volt (Option HV)	1 mV

Table 7: Signal output characteristics (cont.)

Characteristics	Description
DC Offset accuracy	Differential offset is sensitive to output amplitude setting. Within ±5 °C of internal self calibration temperature. Common mode = ((OutP + OutN)/2). Differential Mode = (OutP - OutN).
Output path	
DC High BW	
✓ Common mode (Warranted)	±(2% of |offset| + 10 mV); into 50 Ω to ground termination.
Differential mode	±25 mV; into 100 Ω differential.
DC High Volt (Option HV)	
✓ Common mode (warranted)	±(2% of |offset| + 1% of amplitude + 20 mV).
Differential mode	± 88 mV; Into 100 Ω differential.
AC output DC bias range	
Output path	
AC Direct	± 5 V at 150 mA.
AC Amplified (Option AC)	± 5 V at 150 mA.
AC output DC bias resistance	
Output path	
AC Direct	1 Ω
AC Amplified (Option AC)	1 Ω
✓ AC output DC bias accuracy (warranted)	
Output path	
AC Direct	±(2% of bias + 20 mV); into an open circuit (zero load current).
AC Amplified (Option AC)	±(2% of bias + 20 mV); into an open circuit (zero load current).

Table 7: Signal output characteristics (cont.)

Characteristics	Description
Analog bandwidth	Analog bandwidth is measured with the ideal sin(x)/x response curve of the DAC mathematically removed from the measured data.
Output path	
DC High BW	At 750 mV_{pp} single ended: DC - 2 GHz (–3 dB bandwidth). DC - 4 GHz (–6 dB bandwidth).
DC High BW (Option DC)	At 1.5 V_{pp} single ended: DC - 1.3 GHz (–3 dB bandwidth). The analog bandwidth degrades as the amplitude is increased beyond 750 mV.
DC High Volt (Option HV)	At 2 V_{pp} single-ended: DC – 370 MHz (–3 dB bandwidth). At 4 V_{pp} single-ended: DC – 200 MHz (–3 dB bandwidth).
AC Direct	10 MHz - 2 GHz (–3 dB bandwidth). 10 MHz - 4 GHz (–6 dB bandwidth).
AC Amplified (Option AC)	10 MHz - 2 GHz (–3 dB bandwidth). 10 MHz - 4 GHz (–6 dB bandwidth).
Sin(x)/x Bandwidth	4.44 GHz * fsample ÷ 10 GS/s (DDR Mode) fsample = sample rate The sin(x)/x bandwidth can be solved by using the following equation: 20 * log (sin(x)/x) = –3 x = π * fout ÷ fsample fsample = sample rate fout = sin(x)/x bandwidth
Rise/fall time	Rise and fall times only apply to DC output paths.
Output path	
DC High BW	< 115 ps at 750 mV_{pp} single ended.
DC High BW (Option DC)	< 180 ps at 1.5 V_{pp} single ended.
DC High Volt (Option HV)	< 1.3 ns, at 5 V_{pp} single-ended. < 1.1 ns, at 4 V_{pp} single-ended. < 0.8 ns, at 3 V_{pp} single-ended. < 0.6 ns, at 2 V_{pp} single-ended.

Table 7: Signal output characteristics (cont.)

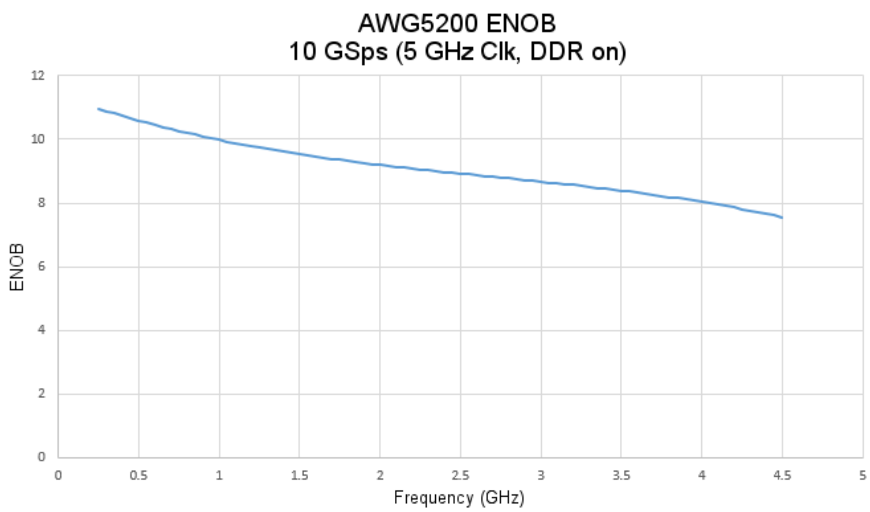
Characteristics	Description
Step response aberrations	Step response aberrations only apply to DC output paths.
Output path	
DC High BW	< 16% $_{pp}$, at 750 mV_{pp} single ended.
DC High BW (Option DC)	< 16% $_{pp}$, at 1.5 V_{pp} single ended.
DC High Volt (Option HV)	< 10% $_{pp}$, at 5 V_{pp} single ended.
Harmonic distortion	
Output path	
DC High BW	(See Table 8 on page 11.) (See Table 9 on page 12.)
DC High Voltage	(See Table 10 on page 12.) (See Table 11 on page 12.)
AC Direct	(See Table 12 on page 12.)
AC Amplified (Option AC)	(See Table 14 on page 13.) (See Table 15 on page 14.) (See Table 13 on page 13.)
ENOB	

Table 7: Signal output characteristics (cont.)

Characteristics	Description
SFDR	SFDR is the difference in dB between a CW carrier signal and the largest spur, excluding harmonics, within a defined frequency range around the carrier. Measured with a balun and with output amplitude set to 500 mV.
Operating at 2.5 GS/s (DC High BW)	(See Table 16 on page 14.)
Operating at 2.5 GS/s (AC Direct Out)	(See Table 19 on page 15.)
Operating at 5 GS/s (DC High BW)	(See Table 17 on page 14.)
Operating at 5 GS/s (AC Direct Out)	(See Table 20 on page 15.)
Operating at 10 GS/s (DC High BW)	(See Table 18 on page 15.)
Operating at 10 GS/s (AC Direct Out)	(See Table 21 on page 16.)
Phase noise	
Operating at 2.5 GS/s	(See Table 22 on page 16.)
Operating at 5 GS/s or 10 GS/s with DDR enabled	(See Table 23 on page 16.)

Table 8: Harmonic distortion (DC High BW 500 mVpp)

Fo (MHz)	2nd harmonic, 2Fo (MHz)	3rd harmonic, 3Fo (MHz)	2nd harmonic distortion max (dBc)	3rd harmonic distortion max (dBc)
100	200	300	–70	–76
300	600	900	–76	–67
500	1000	1500	–70	–64
1000	2000	3000	–65	–59
1200	2400	3600	–62	–51
1300	2600	3900	–56	–48
2000	4000	6000	–47	–40
2400	4800	7200	–51	–40
2600	5200	7800	–50	–38
3000	6000	9000	–51	–41
3500	7000	10500	–50	–53
4000	8000	12000	–49	–76

Table 9: Harmonic distortion (DC High BW 1.5 Vpp)

Fo (MHz)	2nd harmonic, 2Fo (MHz)	3rd harmonic, 3Fo (MHz)	2nd harmonic distortion max (dBc)	3rd harmonic distortion max (dBc)
100	200	300	–72	–55
300	600	900	–59	–40
500	1000	1500	–54	–34
1000	2000	3000	–36	–20
1200	2400	3600	–39	–18
1300	2600	3900	–40	–18
2000	4000	6000	–37	–20
2400	4800	7200	–36	–24

Table 10: Harmonic distortion (DC High Voltage 1.0 Vpp)

Fo (MHz)	2nd harmonic, 2Fo (MHz)	3rd harmonic, 3Fo (MHz)	2nd harmonic distortion max (dBc)	3rd harmonic distortion max (dBc)
100	200	300	–66	–60
300	600	900	–53	–36
500	1000	1500	–49	–32

Table 11: Harmonic distortion (DC High Voltage 5.0 Vpp)

Fo (MHz)	2nd harmonic, 2Fo (MHz)	3rd harmonic, 3Fo (MHz)	2nd harmonic distortion max (dBc)	3rd harmonic distortion max (dBc)
100	200	300	–58	–43
300	600	900	–53	–30
400	1000	1500	–42	–22

Table 12: Harmonic distortion (AC Direct –5 dBm)

Fo (MHz)	2nd harmonic, 2Fo (MHz)	3rd harmonic, 3Fo (MHz)	2nd harmonic distortion max (dBc)	3rd harmonic distortion max (dBc)
100	200	300	–67	–77
300	600	900	–67	–70
500	1000	1500	–66	–66
1000	2000	3000	–69	–63
1200	2400	3600	–69	–60
1300	2600	3900	–67	–59
2000	4000	6000	–60	–71
2400	4800	7200	–54	–69
2600	5200	7800	–60	–82
3000	6000	9000	–67	–85

Table 12: Harmonic distortion (AC Direct –5 dBm) (cont.)

Fo (MHz)	2nd harmonic, 2Fo (MHz)	3rd harmonic, 3Fo (MHz)	2nd harmonic distortion max (dBc)	3rd harmonic distortion max (dBc)
3500	7000	10500	–70	–86
4000	8000	12000	–72	–84

Table 13: Harmonic distortion (AC Amplified –15 dBm)

Fo (MHz)	2nd harmonic, 2Fo (MHz)	3rd harmonic, 3Fo (MHz)	2nd harmonic distortion max (dBc)	3rd harmonic distortion max (dBc)
100	200	300	–48	–49
300	600	900	–52	–50
500	1000	1500	–53	–51
1000	2000	3000	–51	–49
1200	2400	3600	–47	–50
1300	2600	3900	–49	–48
2000	4000	6000	–50	–53
2400	4800	7200	–50	–59
2600	5200	7800	–52	–67
3000	6000	9000	–50	–68
3500	7000	10500	–50	–67
4000	8000	12000	–58	–75

Table 14: Harmonic distortion (AC Amplified 0 dBm)

Fo (MHz)	2nd harmonic, 2Fo (MHz)	3rd harmonic, 3Fo (MHz)	2nd harmonic distortion max (dBc)	3rd harmonic distortion max (dBc)
100	200	300	–49	–49
300	600	900	–53	–50
500	1000	1500	–53	–51
1000	2000	3000	–50	–48
1200	2400	3600	–47	–49
1300	2600	3900	–49	–48
2000	4000	6000	–51	–43
2400	4800	7200	–51	–57
2600	5200	7800	–50	–67
3000	6000	9000	–47	–64
3500	7000	10500	–47	–66
4000	8000	12000	–57	–75

Table 15: Harmonic distortion (AC Amplified +10 dBm)

Fo (MHz)	2nd harmonic, 2Fo (MHz)	3rd harmonic, 3Fo (MHz)	2nd harmonic distortion max (dBc)	3rd harmonic distortion max (dBc)
100	200	300	–30	–28
300	600	900	–29	–29
500	1000	1500	–27	–29
1000	2000	3000	–28	–29
1200	2400	3600	–30	–29
1300	2600	3900	–30	–29
2000	4000	6000	–27	–36
2400	4800	7200	–31	–42
2600	5200	7800	–31	–51
3000	6000	9000	–29	–50
3500	7000	10500	–29	–51
4000	8000	12000	–40	–58

Table 16: SFDR operating at 2.5 GS/s (DC High Bandwidth, 500 mV_{pp})

2.5 GS/s		In band performance		Adjacent band performance	
	Analog channel output frequency	Measured across	Specification	Measured across	Specification
	100 MHz	10 to <1250 MHz	–80 dBc	–	–
	10 to <155 MHz	10 to <1250 MHz	–80 dBc	–	–
	155 to <1000 MHz	10 to <1000 MHz	–53 dBc	1000 to <1250 MHz	–60 dBc
	1000 to <1250 MHz	1000 to <1250 MHz	–51 dBc	10 to <1000 MHz	–50 dBc

Table 17: SFDR operating at 5 GS/s (DC High Bandwidth, 500 mV_{pp})

5 GS/s		In band performance		Adjacent band performance	
	Analog channel output frequency	Measured across	Specification	Measured across	Specification
	100 MHz	10 to <1250 MHz	–80 dBc	1250 to <2500 MHz	–75 dBc
	10 to <310 MHz	10 to <1250 MHz	–80 dBc	1250 to <2500 MHz	–70 dBc
	310 to <1250 MHz	10 to <1250 MHz	–67 dBc	1250 to <2500 MHz	–64 dBc
	1250 to <2000 MHz	1250 to <2000 MHz	–53 dBc	10 to <1250 MHz	–38 dBc
				1250 to <2000 MHz	–58 dBc
	2000 to <2500 MHz	2000 to <2500 MHz	–33 dBc	10 to <2000 MHz	–31 dBc

Table 18: SFDR operating at 10 GS/s (DC High Bandwidth, 500 mV_{pp})

10 GS/s		In band performance		Adjacent band performance	
	Analog channel output frequency	Measured across	Specification	Measured across	Specification
	100 MHz	10 to <1250 MHz	–80 dBc	1250 to <5000 MHz	–69 dBc
	10 to <625 MHz	10 to <1250 MHz	–74 dBc	1250 to <5000 MHz	–63 dBc
	625 to <1250 MHz	10 to <1250 MHz	–69 dBc	1250 to <5000 MHz	–59 dBc
	1250 to <2000 MHz	1250 to <2000 MHz	–63 dBc	10 to <1250 MHz	–60 dBc
				2000 to <5000 MHz	–54 dBc
	2000 to <3500 MHz	2000 to <3500 MHz	–50 dBc	10 to <2000 MHz	–47 dBc
				3500 to <5000 MHz	–50 dBc
	3500 to <4000 MHz	3500 to <4000 MHz	–53 dBc	10 to <3500 MHz	–43 dBc
				4000 to <5000 MHz	–54 dBc

Table 19: SFDR operating at 2.5 GS/s (AC Direct Out)

(–5.0 dBm. Harmonics not included. Measured at the maximum output amplitude.)

2.5 GS/s		In band performance		Adjacent band performance	
	Analog channel output frequency	Measured across	Specification	Measured across	Specification
	100 MHz	10 to <1250 MHz	–80 dBc	–	–
	10 to <155 MHz	10 to <1250 MHz	–80 dBc	–	–
	155 to <1000 MHz	10 to <1000 MHz	–62 dBc	1000 to <1250 MHz	–66 dBc
	1000 to <1250 MHz	1000 to <1250 MHz	–60 dBc	10 to <1000 MHz	–62 dBc

Table 20: SFDR operating at 5 GS/s (AC Direct Out)

(–5.0 dBm. Harmonics not included. Measured at the maximum output amplitude.)

5 GS/s		In band performance		Adjacent band performance	
	Analog channel output frequency	Measured across	Specification	Measured across	Specification
	100 MHz	10 to <1250 MHz	–80 dBc	1250 to <2500 MHz	–75 dBc
	10 to <310 MHz	10 to <1250 MHz	–80 dBc	1250 to <2500 MHz	–70 dBc
	310 to <1250 MHz	10 to <1250 MHz	–67 dBc	1250 to <2500 MHz	–60 dBc
	1250 to <2000 MHz	1250 to <2000 MHz	–58 dBc	10 to <1250 MHz	–55 dBc
				2000 to <2500 MHz	–60 dBc
	2000 to <2500 MHz	2000 to <2500 MHz	–62 dBc	10 to <2000 MHz	–51 dBc

Table 21: SFDR operating at 10 GS/s (AC Direct Out)

(–5.0 dBm. Harmonics not included. Measured at the maximum output amplitude.)

10 GS/s		In band performance		Adjacent band performance	
	Analog channel output frequency	Measured across	Specification	Measured across	Specification
	100 MHz	10 to <1250 MHz	–80 dBc	1250 to <5000 MHz	–64 dBc
	10 to <625 MHz	10 to <1250 MHz	–78 dBc	1250 to <5000 MHz	–59 dBc
	625 to <1250 MHz	10 to <1250 MHz	–71 dBc	1250 to <5000 MHz	–57 dBc
	1250 to <2000 MHz	1250 to <2000 MHz	–67 dBc	10 to <1250 MHz	–60 dBc
				2000 to <5000 MHz	–55 dBc
	2000 to <3500 MHz	2000 to <3500 MHz	–52 dBc	10 to <2000 MHz	–48 dBc
				3500 to <5000 MHz	–56 dBc
	3500 to <4000 MHz	3500 to <4000 MHz	–55 dBc	10 to <3500 MHz	–41 dBc
				4000 to <5000 MHz	–58 dBc

Table 22: Phase noise operating at 2.5 GS/s

	Analog output frequency	
Offset frequency	100 MHz	1 GHz
100 Hz	–112 dBc/Hz	–92 dBc/Hz
1 kHz	–132 dBc/Hz	–110 dBc/Hz
10 kHz	–136 dBc/Hz	–117 dBc/Hz
100 kHz	–134 dBc/Hz	–114 dBc/Hz
1 MHz	–144 dBc/Hz	–124 dBc/Hz
10 MHz	–160 dBc/Hz	–150 dBc/Hz

Table 23: Phase noise operating at 5.0 GS/s; or 10 GS/s with DDR enabled

	Analog output frequency			
Offset	100 MHz	1 GHz	2 GHz	4 GHz
100 Hz	–112 dBc/Hz	–92 dBc/Hz	–86 dBc/Hz	–80 dBc/Hz
1 kHz	–132 dBc/Hz	–110 dBc/Hz	–105 dBc/Hz	–99 dBc/Hz
10 kHz	–138 dBc/Hz	–118 dBc/Hz	–112 dBc/Hz	–106 dBc/Hz
100 kHz	–138 dBc/Hz	–118 dBc/Hz	–112 dBc/Hz	–106 dBc/Hz
1 MHz	–148 dBc/Hz	–128 dBc/Hz	–122 dBc/Hz	–116 dBc/Hz
10 MHz	–160 dBc/Hz	–150 dBc/Hz	–140 dBc/Hz	–140 dBc/Hz

Table 24: Marker outputs

Characteristics	Description
Connector type	SMA on rear panel.
Number of outputs	4 per channel.

Table 24: Marker outputs (cont.)

Characteristics	Description
Type of output	Single ended.
ON/OFF Control	Independent control for each marker.
Output impedance	50 Ω
Output voltage	Independent control for each marker. Output voltage into RLOAD [Ω] to GND is approximately (2 * RLOAD / (50 + RLOAD)) times of voltage setting.
Amplitude range	0.2 V_{p-p} to 1.75 V_{p-p} into 50 Ω.
Window	–0.5 V to 1.75 V into 50 Ω.
Resolution	0.1 mV
External termination voltage	–1.0 V to +3.5 V.
Maximum output current	60 mA
✓ DC accuracy (warranted)	±(10% of |output high or low setting| + 25 mV) into 50 Ω.
Rise/fall time	< 150 ps (20% to 80% of swing when High = 0.4 V, Low = –0.4 V).
Aberrations	< 20% $_{p-p}$ for the first 1 ns following the step transition with 100% reference at 10 ns.
Random jitter	≤ 5 ps rms
Sample rate	2.5 GS/s to 5 GS/s.
Minimum pulse width	400 ps 2 Samples at 5 GS/s.
Maximum data rate	2.5 Gb/s. Minimum pulse width does not support data output at maximum sample rate.
Skew between markers (From the same channel)	±25 ps
Variable delay control	Independent control for each marker.
Range	±2 ns
Resolution	1 ps
Accuracy	< ±25 ps from delay value.

Table 25: 10 MHz Ref Out (reference output)

Characteristics	Description
Connector type	SMA on rear panel.
Output impedance	50 Ω (AC coupled).
Amplitude	+4 dBm, ±2 dBm. Sine wave output.
✓ Frequency (warranted)	Within ±(1 ppm + Aging), Aging: ±1 ppm per year. (Temperature between 0 °C to 50 °C.)

Table 26: Ref In (reference input)

Characteristics	Description
Connector type	SMA on rear panel.
Input impedance	50 Ω (AC coupled).
Input amplitude	–5 dBm to +5 dBm.
Fixed frequency range	10 MHz, ±40 Hz.
Variable frequency range	35 MHz to 240 MHz. Acceptable frequency drift while the instrument is operating is ± 0.1%.

Table 27: Clock Out

Characteristics	Description
	The external clock output is a copy of an internal clock generator that is used to create the DAC sample clock. This clock always operates in the octave range specified below. It is multiplied and divided to create the effective DAC sampling rate.
Connector type	SMA on rear panel.
Output impedance	50 Ω AC coupled.
Output amplitude	+3 dBm to +10 dBm.
Frequency range	2.5 GHz to 5 GHz. For sample rates lower than 2.5 GS/s the output frequency is: Fout = SR * 2n ; where n is an integer that gives Fout between 2.5 GHz and 5 GHz.
Frequency resolution	
Internal and fixed reference clock operation	With jitter reduction: 50 MHz. Without jitter reduction: 100 MHz ÷ 2^{20}.
External variable reference clock operation	With jitter reduction: Fref ÷ R. Without jitter reduction: Fref ÷ R ÷ 2^{20}
	Fref = reference clock frequency R = 4 when 140 MHz < Fref ≤ 240 MHz R = 2 when 70 MHz < Fref ≤ 140 MHz R = 1 when 35 MHz ≤ Fref ≤ 70 MHz

Table 28: Clock In

Characteristics	Description
	The external clock input can be used to create the DAC sample clock. This clock must always operate in the octave range specified below. It is multiplied and divided to create the actual DAC sample clock.
Connector type	SMA on rear panel.
Input impedance	50 Ω (AC coupled).
Input amplitude	0 dBm to +10 dBm.
Frequency range	2.5 GHz to 5 GHz. Acceptable frequency drift while the instrument is operating is ±0.1%.

Table 29: Sync In

Characteristics	Description
Connector type	SMA on rear panel.
Input impedance	500 Ω (AC coupled)
Input amplitude	2.5 V_{p-p} Max
Frequency	Clock output ÷ 32.

Table 30: Sync Out

Characteristics	Description
Connector type	SMA on rear panel.
Output impedance	50 Ω (AC coupled).
Output amplitude	1 V_{p-p}, ±20% into 50 Ω.
Frequency	Clock output ÷ 32.

Table 31: Trigger Inputs

Characteristics	Description
Number of inputs	2 (A and B)
Connector	SMA on rear panel.
Trigger modes	Synchronous Synchronous mode is when the trigger signal becomes internally synchronized with a frame clock. After a valid trigger event is processed, waveform playback will start at the rising edge of the internal frame clock (also called sync clock). This clock runs at FCLK/32 since there are 32 waveform samples per frame. Because of this, there is 32 samples of timing uncertainty for a random trigger signal. (FCLK is the sample clock.) The trigger signal of a synchronous mode trigger does not need to be synchronous with the sample clock, reference, or any internal clock. A trigger may have random timing as expected. If the trigger signal can be synchronized to the frame rate, as is done in multi-instrument synchronization, then trigger jitter will be very small.
Input impedance	1 kΩ or 50 Ω selectable, DC coupled.
Slope / Polarity	Positive or negative, selectable
Input voltage range	
1 kΩ selected	–10 V to 10 V.
50 Ω selected	< 5 V_{RMS}
Input voltage minimum amplitude	0.5 V_{p-p}
Threshold control	
Range	–5.0 V to 5.0 V.
Resolution	0.1 V
Accuracy	± 5% of setting + 0.1 V.
Minimum pulse width	20 ns
Delay to analog output	The DAC sampling clock frequency is displayed on the clock settings tab when the external clock output is enabled.

Table 31: Trigger Inputs (cont.)

Characteristics	Description
Synchronous trigger mode	
PERF-50, real waveform Synchronous mode, DC High Bandwidth	$8064/F_{CLK}$ + (0 to 70 ns) Typical: 3225.6 to 3295.6 ns at 2.5 GS/s Typical: 1612.8 to 1688.8 ns at 5 GS/s
PERF-50, Digital Up-converter (DUC) IQ waveform Synchronous mode, DC High Bandwidth	$8280/F_{CLK}$ + (0 to 70 ns) Typical: 3312 to 3382 ns at 2.5 GS/s Typical: 1656 to 1726 ns at 5 GS/s
X25 (low sample-rate range), real waveform Synchronous mode, DC High Bandwidth	($8320/F_{CLK}$ + 128/(Sample Rate) ± 100 ns) ± 0.2%
X25 (low sample-rate range), Digital Up-converter (DUC) IQ waveform Synchronous mode, DC High Bandwidth	3382 ± 40 ns The only F_{CLK} and Sample rate available in X25 low-sample-rate range, DUC with IQ waveform is: Sample rate = 2.5 GS/s, and F_{CLK} = 2.5 GHz)
Hold off	Trigger hold off is the amount of delay required at the end of a waveform before another trigger event can be processed. Minimum time between trigger events is the sum of hold off plus the waveform duration. Note that “Delay to Analog Output” is not included in this sum.
PERF-50, real waveform, Synchronous-mode	Typical: $2368/F_{CLK}$ 473.6 ns at 5 GS/s 947.2 ns at 2.5 GS/s Maximum: $2432/F_{CLK}$ + 20 ns 506.4 ns at 5 GS/s 992.8 ns at 2.5 GS/s
PERF-50, Digital Up-converter (DUC) IQ waveform, Synchronous-mode	Typical: $4576/F_{CLK}$ 915.2 ns at 5 GS/s 1830.4 ns at 2.5 GS/s
X25 (low sample-rate range), real waveform, Synchronous mode	Typical: $2180/F_{CLK}$

Table 31: Trigger Inputs (cont.)

Characteristics	Description
Jitter, synchronous mode	50 Ω or 1kΩ
Random trigger (not synchronized)	32 F_{CLK} periods + 100 ps peak-to-peak 2.5 GS/s: 12.9 ns 5.0 GS/s: 6.5 ns
Frame-synchronized trigger	< 100 ps peak-to-peak A frame-synchronized trigger is used in multi-instrument synchronization, but could be used for any triggering condition.

Table 32: Pattern Jump In connector

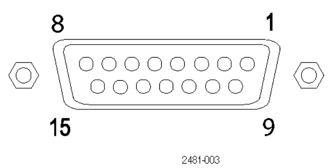
Characteristics	Description	
Connector type	15-pin D-sub female connector on rear panel.	
Input signal pin assignment		
	Pin assignments	
	1	GND
	2	Data bit 0, input
	3	Data bit 1, input
	4	Data bit 2, input
	5	Data bit 3, input
	6	GND
	7	Strobe, input
	8	GND
	9	GND
	10	Data bit 4, input
	11	Data bit 5, input
	12	Data bit 6, input
	13	Data bit 7, input
	14	GND
	15	GND
Input levels	3.3 V LVCMOS compliant. 5 V TTL compliant.	
Input impedance	1 kΩ resistor pull up to +5 V.	
Number of jump destinations	256	

Table 32: Pattern Jump In connector (cont.)

Characteristics	Description
Strobe	
Polarity	Default: Data is clocked in on negative edge. You can select negative or positive.
Minimum pulse width	20 ns
Setup and hold	Setup: 20 ns. Hold: 20 ns.
Holdoff time	48000/F_{CLK} where F_{CLK} is the DAC clock. 9.6 us at 5 GS/s 19.2 us at 2.5 GS/s Strobe hold off is the amount of delay required at the end of a waveform before another strobe pulse can be processed.

Table 33: Auxiliary Outputs (Flags)

Characteristics	Description
Connector type	SMB on rear panel.
Number of outputs	AWG5202 and AWG5204: 4 AWG5208: 8
Output impedance	AC nominal impedance: 50 Ω DC source resistance: 28.3 Ω
Output amplitude, typical	High: 4.97 V into open circuit (no load) High: 3.17 V into 50 Ω Low: 0.001 V into open circuit
Maximum toggle frequency	Same as inverse of waveform duration 2400 samples minimum waveform size in a sequence
Skew between outputs	460 ps, typical 2 ns, maximum
Delay from analog out	PERF-50: (2.5 GS/s ≤ Sample rate ≤ 5.0 GS/s) Delay < –3800*FCLK (Sample clock cycles) 5 GHz sample clock (5 GS/s): Delay < –760 ns 2.5 GHz sample clock (2.5 GS/s): Delay < –1520 ns X25: (Sample rate ≤2.5 GS/s) Delay < –(3720 × F_{CLK} + 128 ×(Sample Rate)) Flags precede analog output.

Table 34: Computer system

Characteristics	Description
CPU	Intel core I7-4700EQ, 4 core, 2.4 GHz, 6M cache.
Memory	16 GB (2 x 8 GB), DDR3-1600 or faster SODIMM.

Table 34: Computer system (cont.)

Characteristics	Description
Hard disk drive	Solid state, ≥1 TB, removable.
Video output	1 VGA port on rear panel.
ESATA	1 port on rear panel, 1.5 Gb/s. Instrument must be powered down to make connection.
USB	4 ports, USB 3.0, rear panel, type A connector. 2 ports, USB 2.0, front panel, type A connector.
GPIB	Available as an optional accessory that connects to the USB Device and USB Host ports with the TEK-USB-488 GPIB to USB Adapter The control interface is incorporated into the instrument user interface.
Video output	1 VGA port on rear-panel.
LAN	RJ-45 LAN connector supporting 10/100/1000 Ethernet on rear panel.

Table 35: Display

Characteristics	Description
Display area	132 mm X 99 mm (5.2 in X 3.9 in, 6.5 in diagonal)
Resolution	1024 X 768 pixels
Touch screen	Built-in touch screen

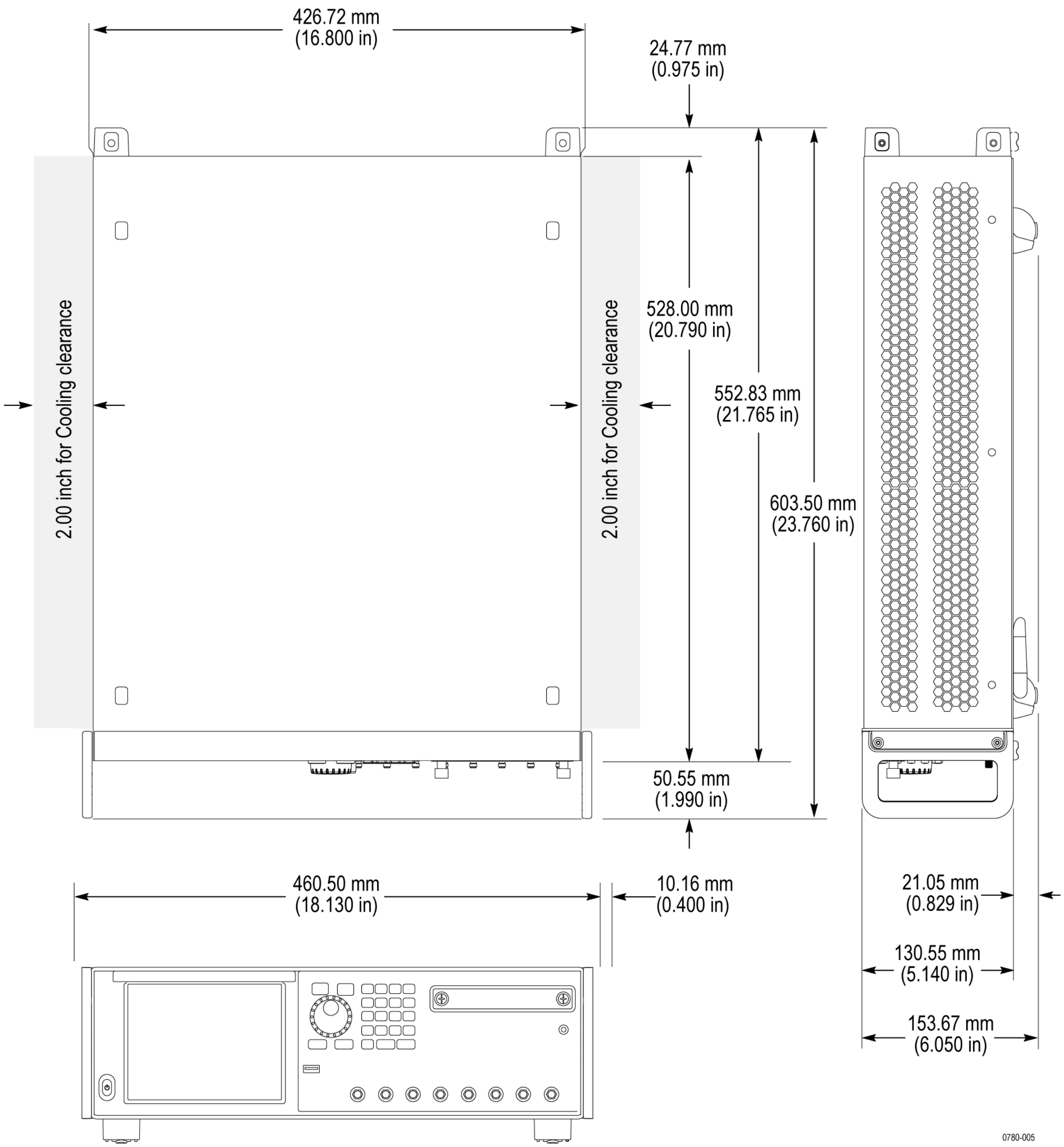
Table 36: Power supply

Characteristics	Description
Source voltage and frequency	⚠ ***WARNING.*** *To reduce the risk of fire and shock, ensure that the mains supply voltage fluctuations do not exceed 10% of the operating voltage range.*
Rating voltage	100 V_{AC} to 240 V_{AC}.
Frequency range	50 Hz to 60 Hz.
Power consumption	750 W maximum <500 W typical

Mechanical characteristics

Table 37: Mechanical characteristics

Characteristics	Description		
Net weight			
	AWG5202	AWG5204	AWG5208
Without package	44 lb (19.96 kg)	45.45 lb (20.62 kg),	50.7 lb (23 kg),
With package	46.35 lb (21.02 kg)	47.75 lb (21.66 kg)	53 lb (24.04 kg)
Dimensions, with feet and handles			
Height	153.6 mm (6.05 in)		
Width	460.5 mm (18.13 in)		
Length	603 mm (23.76 in)		
Cooling method	Forced-air circulation with no air filter.		
Cooling clearance			
Top	0 in		
Bottom	0 in		
Left side	50 mm (2 in)		
Right side	50 mm (2 in)		
Rear	0 in		


426.72 mm
(16.800 in)
24.77 mm
(0.975 in)
2.00 inch for Cooling clearance
2.00 inch for Cooling clearance
528.00 mm
(20.790 in)
552.83 mm
(21.765 in)
603.50 mm
(23.760 in)
50.55 mm
(1.990 in)
460.50 mm
(18.130 in)
10.16 mm
(0.400 in)
21.05 mm
(0.829 in)
130.55 mm
(5.140 in)
153.67 mm
(6.050 in)
0780-005

Environmental characteristics

Table 38: Environmental characteristics

Characteristics	Description
Temperature	
Operating	0 °C to +50 °C (+32 °F to 122 °F)
Nonoperating	–20 °C to +60 °C (-4 °F to 140 °F) with 30 °C/hour (86 °F/hour) maximum gradient, with no media installed in disc drives.
Relative humidity	
Operating	5% to 90% relative humidity at up to +30 °C (+86 °F). 5% to 45% relative humidity above +30 °C (+86 °F) up to +50 °C (122 °F) noncondensing.
Nonoperating	5% to 90% relative humidity at up to 30 °C. 5% to 45% relative humidity above +30 °C (+86 °F) up to +60 °C (140 °F) noncondensing.
Altitude	
Operating	Up to 3,000 m (approximately 10,000 feet). Maximum operating temperature decreases 1 °C (34 °F) each 300 m (984 ft) above 1.5 km (4921 ft).
Nonoperating	Up to 12,000 m (approximately 40,000 feet).

Performance verification procedures

Two types of performance verification procedures can be performed on the instrument: *Brief Procedures* and *Performance Tests*. You may not need to perform all of these procedures, depending on what you want to accomplish.

- To rapidly confirm that the instrument functions and was adjusted properly, perform *Diagnostics* and *Calibration*.

Advantages: These procedures are quick to do and require no external equipment or signal sources. These procedures perform extensive functional and accuracy testing to provide high confidence that the instrument will perform properly.

- To further check functionality, first perform Diagnostics and Calibration, and then perform *Functional Test*.

Advantages: The procedure requires minimal additional time to perform, and requires minimal equipment. The procedure can be used when the instrument is first received.

- If more extensive confirmation of performance is desired, complete the self tests and functional test, and then do the *Performance Tests*.

Advantages: These procedures add direct checking of warranted specifications. These procedures require specific test equipment. (See page 43, *Required equipment*.)

If you are not familiar with operating this instrument, refer to the online help or the user information supplied with the instrument.

Input and output options

The instrument has two USB ports on the front panel, and four USB ports on the rear panel. (See Figure 1.) These ports can be used for an external mouse and/or keyboard. Additionally, an external video display can be connected to the VGA display port on the rear panel.

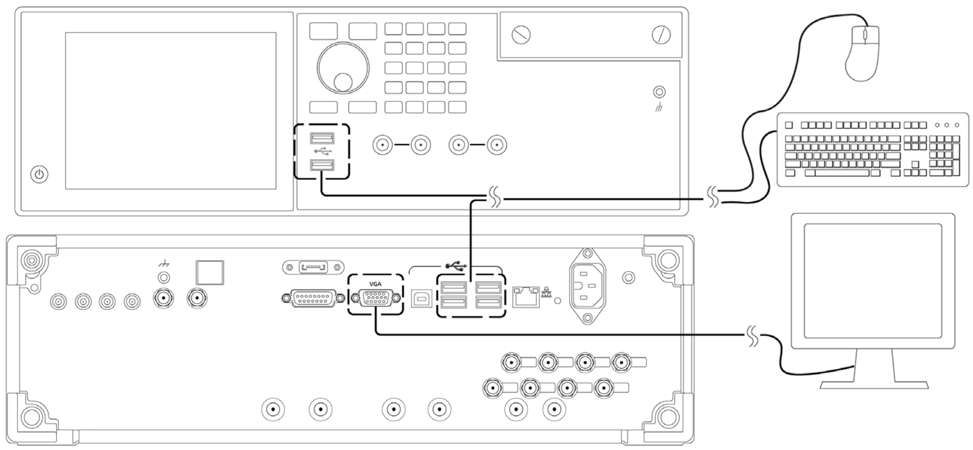


Figure 1: Peripheral connections

Brief procedures

There are three procedures in this section that provide a quick way to confirm basic functionality and proper adjustment:

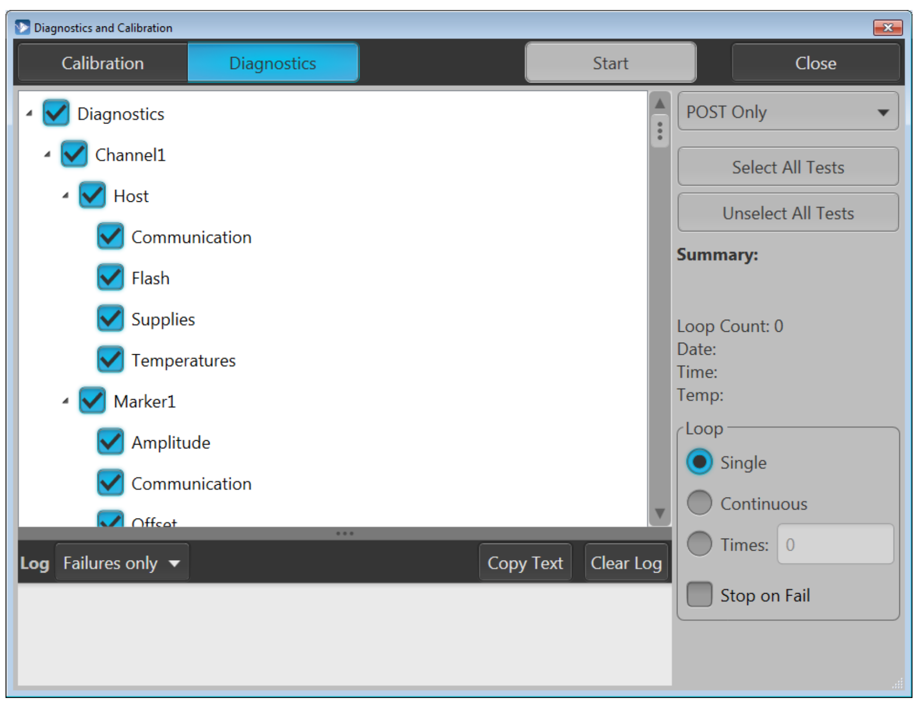
- *Diagnostics*
- *Calibration*
- *Functional test*

Diagnostics

The following steps run the internal routines that confirm basic functionality and proper adjustment.

Equipment	Prerequisites
None	None

1. Disconnect all the cables from the output channels.
2. From the **Utilities** tab, select **Diag & Cal**.
3. Click the **Diagnostics & Calibration** button and then select **Diagnostics**.



4. In the Diagnostics dialog box, confirm that all the check boxes are selected. If they are not all selected, click the **Select all tests** button.

5. Click the **Start** button to execute the diagnostics.

   The internal diagnostics perform an exhaustive verification of proper instrument function. This verification may take several minutes. When the verification is completed, the resulting status will appear in the dialog box.

6. Verify that **Pass** appears as Status in the dialog box when the diagnostics complete.

7. Click the **Close** button.

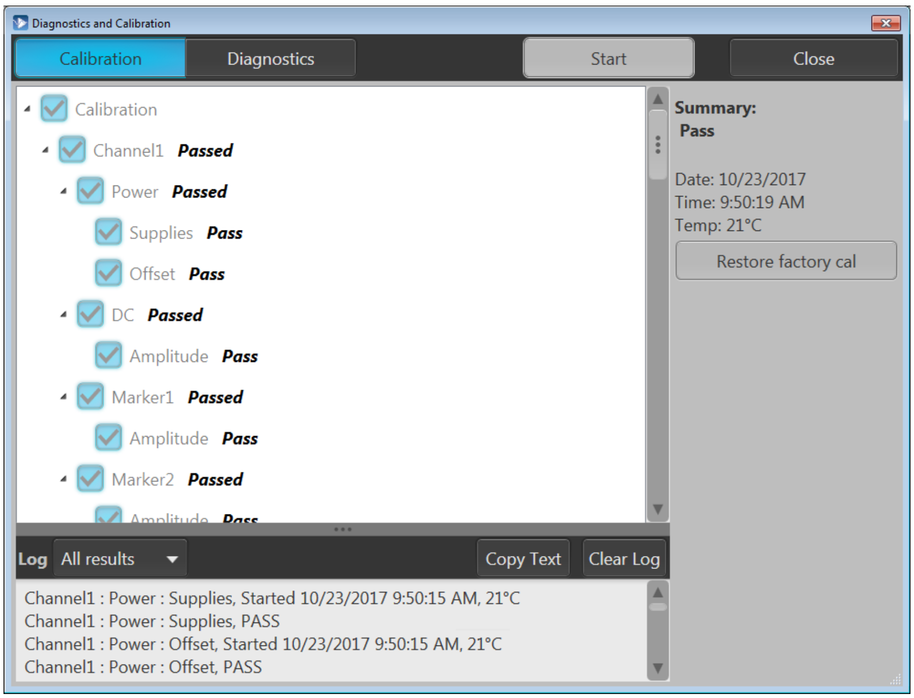
Calibration

Equipment	Prerequisites
None	Power on the instrument and allow a 20 minute warm-up before doing this procedure.

1. From the **Utilities** tab, select **System**.

2. From the **Utilities** tab, select **Diag & Cal**.

   Click the **Diagnostics & Calibration** button and then select **Calibration**.



3. Click the **Start** button to start the routine.

4. Verify that **Pass** appears in the Summary column for all items when the calibration completes.
5. Click the **Close** button.

Functional test

The purpose of the procedure is to confirm that the instrument functions properly.

The procedures use “AWG” when referring to the AWG5200 series instruments.

The required equipment is listed below.

Table 39: Required equipment for the functional test

Item	Qty.	Minimum requirements	Recommended equipment
Oscilloscope	1 ea.	Bandwidth: 4 GHz or higher 4 channels	Tektronix DPO70404C
Function generator	1 ea.	1 kHz, square wave, 5 V_{p-p} output	Tektronix AFG3021C
Signal analyzer	1 ea.	Bandwidth: 14 GHz or higher	Tektronix RSA5126B
Adapter	4 ea	TekConnect oscilloscope input to SMA input	Tektronix TCA-SMA
50 Ω SMA cable	4 ea.	DC to 20 GHz	Tensolite 1-3636-465-5236
50 Ω SMA terminator	3 ea.	DC to 18 GHz	Tektronix part number 136-7162-xx (supplied with AWG).
50 Ω BNC cable	1 ea.	Male connectors both ends	Tektronix part number 012-0057-01
SMA-BNC adapter	3 ea.	SMA female to BNC male connector	Tektronix part number 015-0572-00
Planar Crown RF Input Connector – 7005A-1 SMA Female	1 ea.	Planar Crown RF Input Connector – Type N to SMA Female For use with Tektronix RSA5126B signal analyzer	Tektronix part number 131-8689-00

Functional check prerequisites

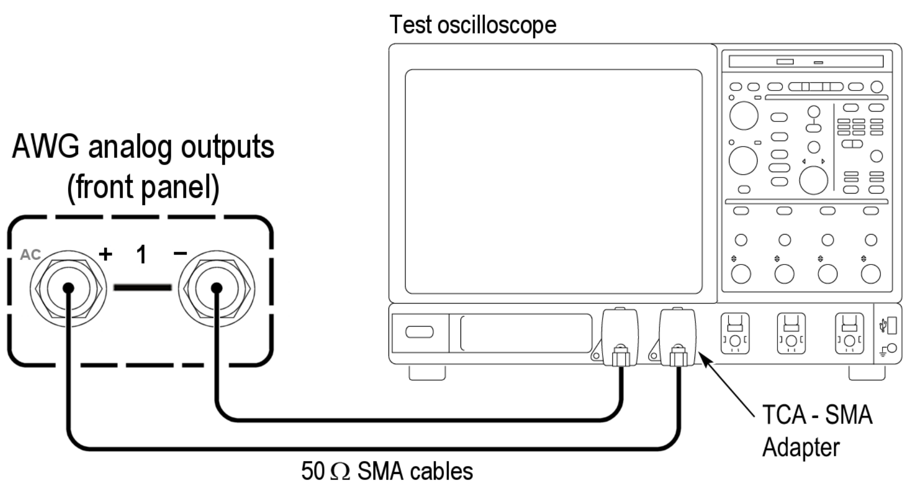
1. Click the **Reset to Default Setup** button in the toolbar .
2. Load the test waveform **PV_Square.wfmx** into the Waveform List.

   Test waveforms are located at **C:\Program Files\Tektronix\AWG5200\Samples\PV**.

Checking the analog channel outputs

Required equipment	Prerequisites
Oscilloscope	None
One TCA-SMA adapter	
One 50 Ω SMA cable	
One 50 Ω SMA terminator	

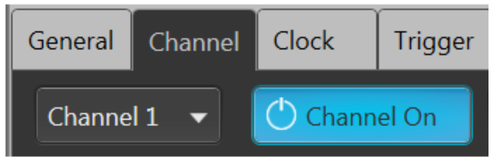
1. Set the test oscilloscope as follows:
   - **a.** Vertical scale: 200 mV/div (CH 1 and CH 2)
   - **b.** Horizontal scale: 100 ns/div
   - **c.** Input coupling: DC (CH 1 and CH 2)
   - **d.** Input impedance: 50 Ω (CH 1 and CH 2)
   - **e.** Position: +2 div (CH 1 and CH 2, if necessary)
   - **f.** Trigger source: CH 1
   - **g.** Trigger level: 0 mV
   - **h.** Trigger slope: Positive
   - **i.** Trigger mode: Auto
2. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
3. Connect CH 1 (+) of the AWG to channel 1 of the test oscilloscope using a 50 Ω SMA cable and a TCA-SMA adapter.
4. Connect CH 1 (–) of the AWG to channel 2 of the test oscilloscope using a 50 Ω SMA cable and a TCA-SMA adapter.



5. Click the **Home** tab on the display.

6. From the Waveform List window, assign the waveform **PV_Square.wfmx** to Channel 1.

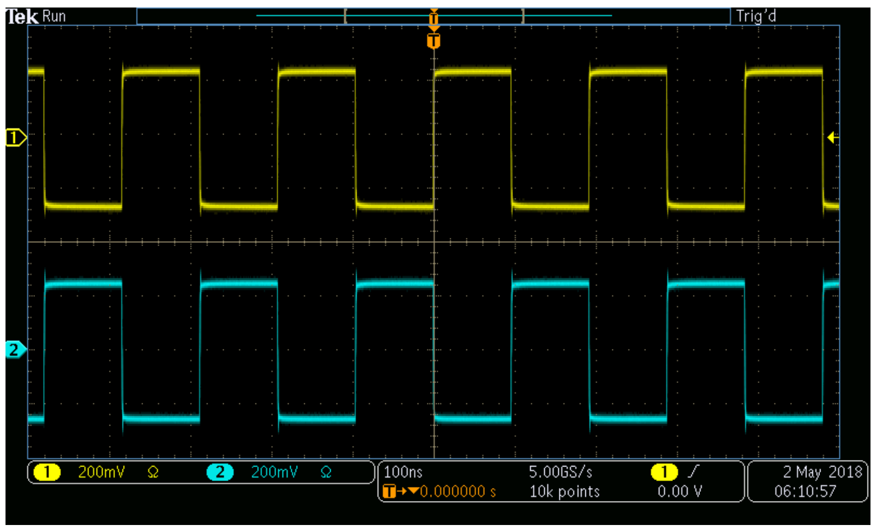
7. Click the **Setup -> Channel** tab and enable Channel 1.



8. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *enable* the outputs (front panel light off).

9. Click the **Play** button on-screen or press the button on the front panel of the AWG.

10. Check that the channel's waveform is properly displayed on the test oscilloscope screen.



11. Press AWG the front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).

12. Repeat steps 3 through 11 until all channels are checked, modifying the instructions with the channel number under test.

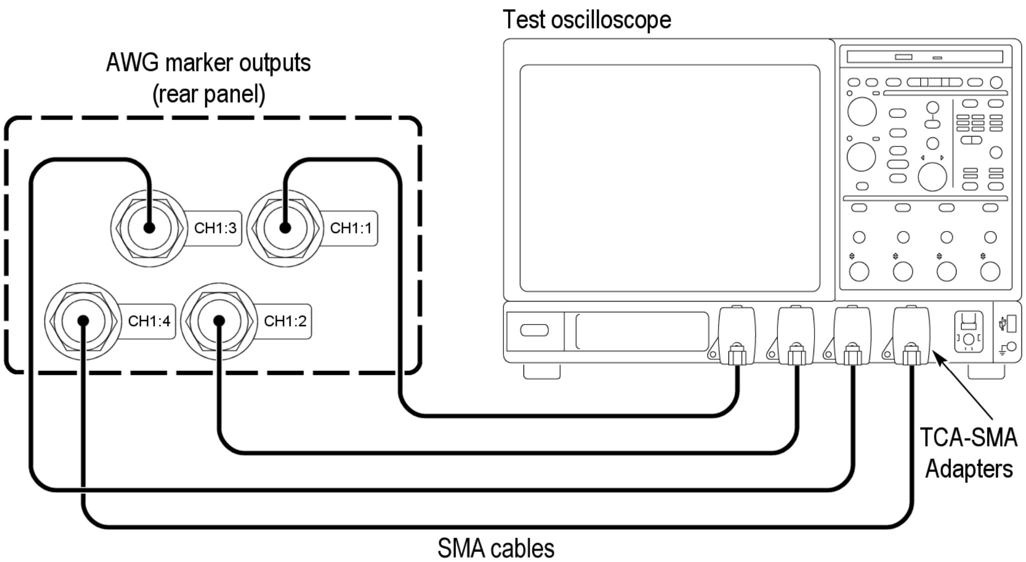
13. Disconnect the test setup.

Checking the marker outputs

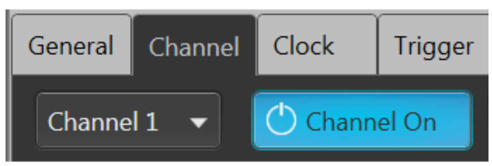
Required equipment	Prerequisites
Oscilloscope	None
Four TCA-SMA adapters	
Four 50 Ω SMA cables	

1. Set the test oscilloscope as follows:
   a. Vertical scale: 1 V/div (CH 1 through CH 4)
   b. Horizontal scale: 100 ns/div
   c. Input coupling: DC
   d. Input impedance: 50 Ω
   e. CH 1 through CH 4 position: adjust as necessary to display all four traces
   f. Trigger source: CH1
   g. Trigger level: 0 mV
   h. Trigger slope: Positive
   i. Trigger mode: Auto
2. If needed, press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
3. Connect the AWG's Channel 1 markers to the test oscilloscope using a 50 Ω SMA cable and a TCA-SMA adapter.
   - Connect marker CH1:1 to channel 1 of the test oscilloscope.
   - Connect marker CH1:2 to channel 2 of the test oscilloscope.
   - Connect marker CH1:3 to channel 3 of the test oscilloscope.
   - Connect marker CH1:4 to channel 4 of the test oscilloscope.

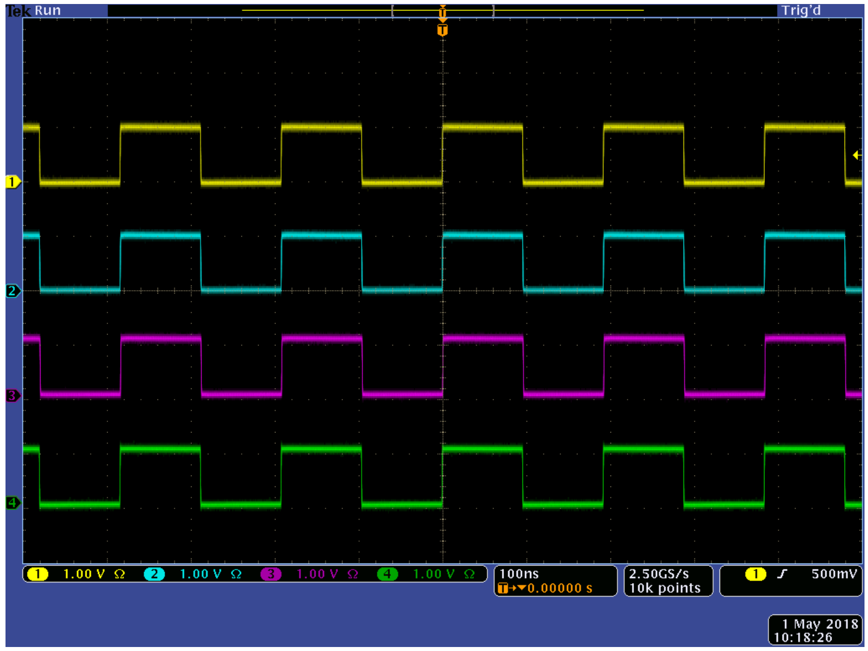
NOTE. *If a channel's marker is not connected to the test oscilloscope, it must be terminated with a 50 Ω SMA terminator.*



4. Click the **Home** tab on the display.
5. From the Waveform List window, assign the waveform **PV_Square.wfmx** to Channel 1.
6. Click the **Setup -> Channel** tab and enable the select Channel 1 output.



7. In the **Setup -> Channel** tab, select **Output Settings** and set the Channel 1 **Resolution** to **12+4 Mkrs**.
8. Click the **Play** button on-screen or on the front panel.
9. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *enable* the outputs (front panel light off).
10. Check that the CH1:1 through CH1:4 waveforms are properly displayed on the test oscilloscope screen.



11. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).

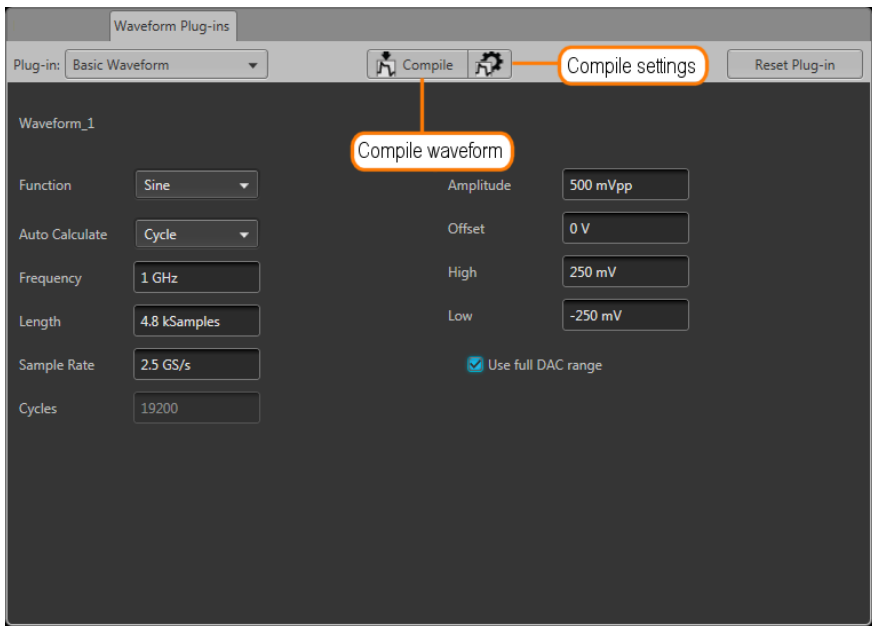
12. Repeat steps 3 through 11 until all channels are checked, modifying the instructions with the channel number under test.

Disconnect the test setup.

Checking the AC output

Required equipment	Prerequisites
Signal analyzer	None
One 50 Ω SMA cable	
Planar Crown RF Input Connector – Type N to SMA Female	
Two 50 Ω SMA terminators	

1. If needed, press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
2. Create a 1 GHz test waveform from the AWG using the Basic Waveform plug-in.
   a. Click the **Waveform Plug-in** tab on the display.
   b. Select **Basic Waveform** from the Waveform Plug-ins drop down list.



   c. Click the **Reset Plug-in** button.
   d. Set the Function to Sine.
   e. Set the Frequency to 1 GHz.

NOTE. *Leave all other settings at their default settings.*

   f. Click the Compile Settings icon to open the compile settings dialog screen.
   g. In the Name field, change the name to Waveform_1 GHz.

h. Close the compile settings dialog screen.

i. Click Compile.

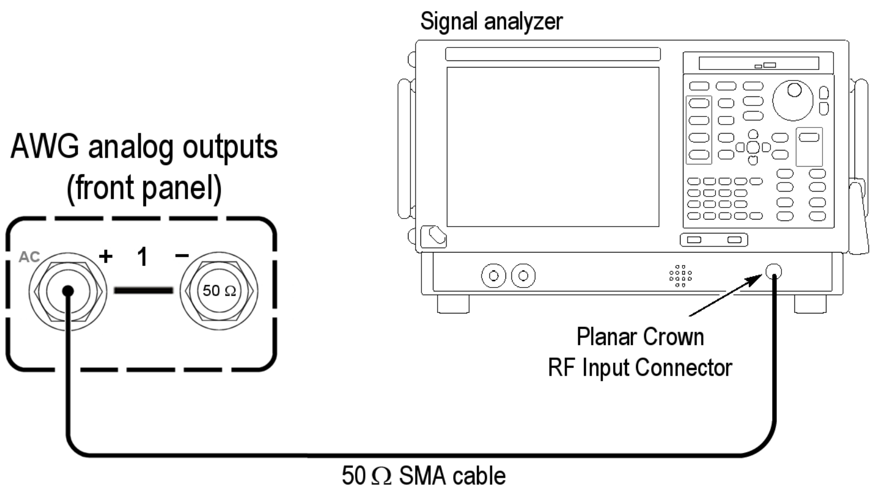
3. Set the spectrum analyzer as follows:

   a. Press the Preset button to set the analyzer to its default settings.

   b. Display the Spectrum measurement.

   c. Set Center Frequency to 1 GHz.

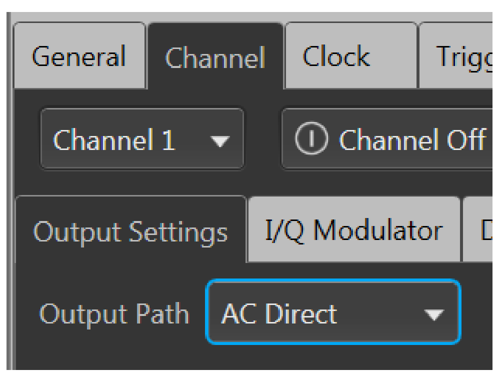
4. Use a 50 Ω SMA cable to connect the CH 1 AC connector (+) on the AWG to the RF input of the signal analyzer.



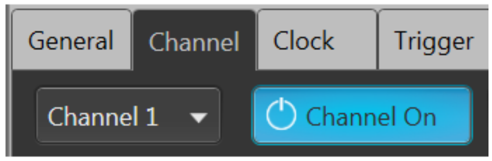
5. Click the **Setup -> Channel** tab and click the **Output Settings** tab.

   a. Select Channel 1.

   b. Set the **Output Path** to **AC Direct**.



   c. Enable the Channel 1 output.



6. Click the **Home** tab on the display.
7. In the Waveform List window, assign the **Waveform_1 GHz** waveform to the Channel 1.
8. Press the **Play** button, or click Play on the display.
9. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *enable* the outputs (front panel light off).
10. Check that the waveform is properly displayed on the signal analyzer screen.

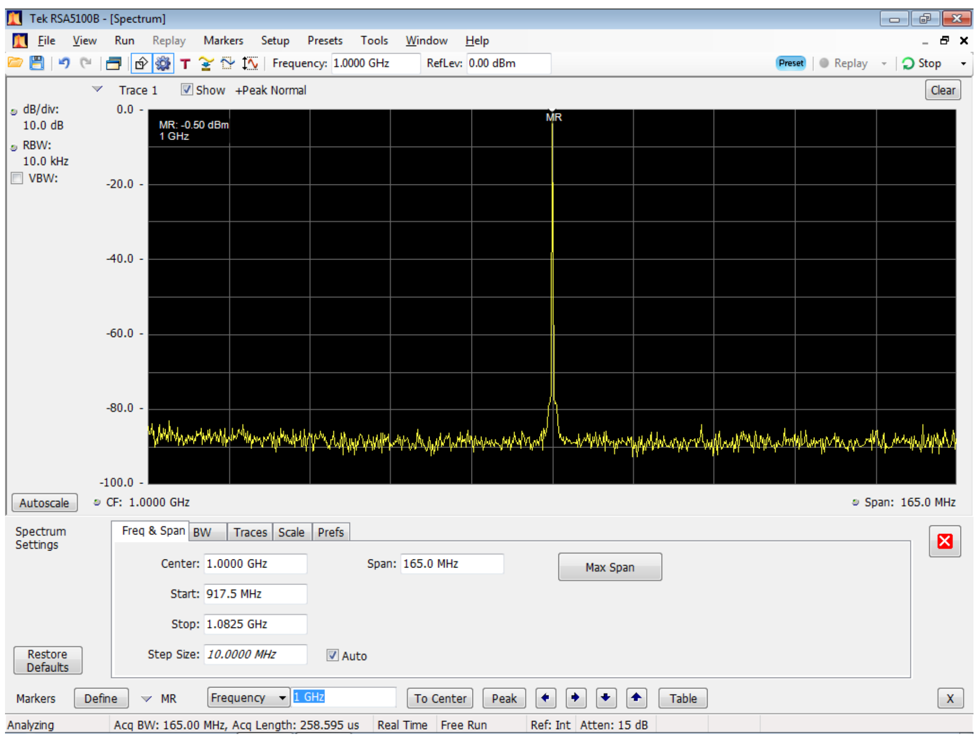


Figure 2: 1 GHz output waveform

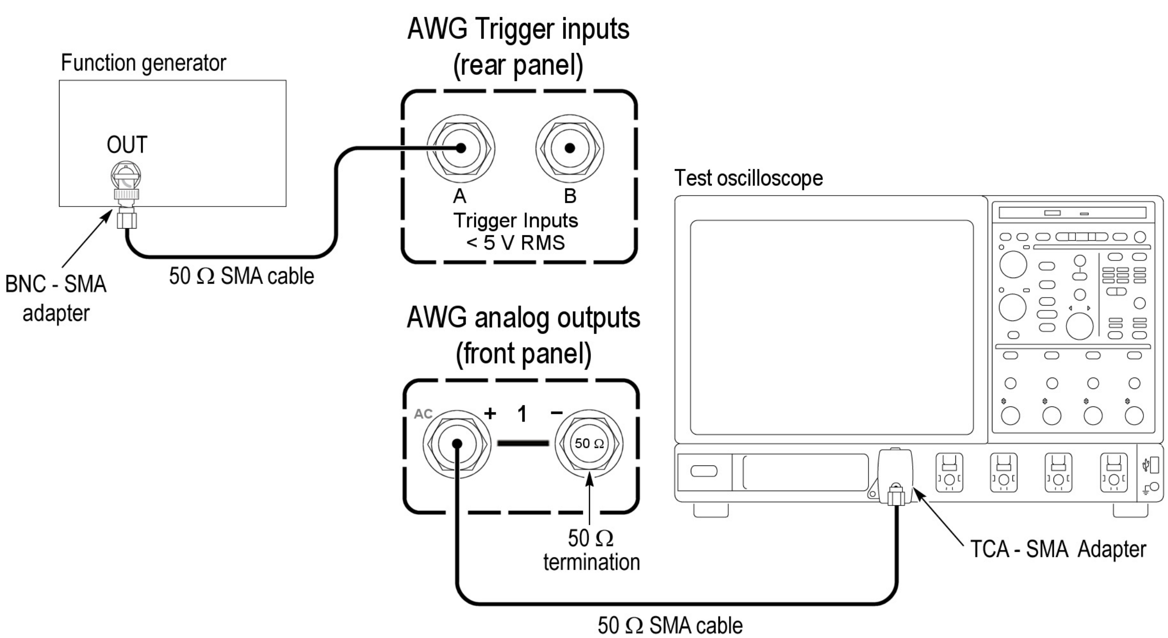
11. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
12. Repeat steps 4 through 11 until all channels are checked, modifying the instructions with the channel number under test.

Disconnect the test setup.

Checking the triggered outputs

Required equipment	Prerequisites
Oscilloscope	None
Function Generator (AFG3021C or equivalent)	
One TCA-SMA adapter	
Two 50 Ω SMA cables	
One SMA female to BNC male adapter	

1. Set the oscilloscope as follows:
   a. Vertical scale: 200 mV/div (CH 1)
   b. Horizontal scale: 20 ns/div
   c. Trigger source: CH 1
   d. Trigger level: 100 mV
2. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
3. Connect a BNC to SMA adapter to the output of the function generator.
4. Connect an SMA cable between the output of the function generator and the Trigger A input on the rear panel of the AWG.
5. Connect CH 1 (+) of the AWG to channel 1 of the test oscilloscope using a 50 Ω SMA cable and a TCA-SMA adapter.



7. Click the **Home** tab on the display.

8. Click the **Reset to Default Setup** button in the toolbar .
9. Set the Function Generator to output a 1 kHz square wave at 5 $V_{p\text{-}p}$.
10. Turn on the output of the Function Generator.
11. Load the test waveform **PV_Square.wfmx** into the Waveform List.

    Test waveforms are located at **C:\Program Files\Tektronix\AWG5200\Samples\PV**.
12. From the Waveform List window, assign the waveform **PV_Square.wfmx** to Channel 1.
13. Click the **Home** tab and set the AWG's Channel 1 as follows:
    - Run Mode to **Triggered**
    - Trigger Input to **A**
    - Enable the Channel
14. In the **Setup -> Trigger** tab, set the **External Trigger Level** to 1.0 V (A and B). Leave all other settings to their default settings.
15. Click the **Play** button on-screen or on the front panel of the AWG.
16. Click the **Home** tab and verify that the squarewave output is displayed on the AWG.
17. Verify that the squarewave output is displayed on the test oscilloscope.
18. Move the cable from the Trigger A input to the Trigger B input.
19. Click the **Home** tab and set the trigger input to **B**.
20. Verify that the output is displayed on the test oscilloscope (as in step 17).
21. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
22. Disconnect the test setup.

Performance tests

This section contains performance verification procedures for the specifications listed below.

- 10 MHz reference frequency accuracy
- Analog amplitude accuracy
- Marker high and low level accuracy

Prerequisites

The tests in this section provide confirmation of performance and functionality

The following requirements and conditions must be met:

- The cabinet must be installed.
- The AWG must have been last adjusted at an ambient temperature between +20 °C and +30 °C, must have been operating for a warm-up period of at least 20 minutes, and must be operating at an ambient temperatures between +10 °C and +40 °C.
- You must have performed and passed the procedure *Diagnostics* and *Calibration*, and the procedure *Functional Tests*.

Required equipment

The following table lists the test equipment required to perform the performance verification procedures. The table identifies examples of recommended equipment and lists the required precision where applicable. If you substitute other test equipment for the listed examples, the equipment must meet or exceed the listed tolerances.

Table 40: Required equipment for performance tests

Item	Qty.	Minimum requirements	Recommended equipment
Frequency counter	1 ea.	Frequency accuracy: within ± 0.01 ppm	Tektronix MCA3040
Digital multimeter	1 ea.	DC accuracy: within ± 0.01%	Keithley 2000 DMM or Tektronix DMM4040/4050
Adapter	3 ea.	TekConnect oscilloscope input to SMA input	Tektronix TCA-SMA
50 Ω SMA cable	1 ea.	DC to 20 GHz	Tensolite 1-3636-465-5236
50 Ω SMA terminator	3 ea.	DC to 18 GHz	Tektronix part number 136-7162-xx (supplied with AWG).
50 Ω BNC feed-through terminator	1 ea.	DC to 1 GHz, feedthrough	Tektronix part number 011-0049-02

Table 40: Required equipment for performance tests (cont.)

Item	Qty.	Minimum requirements	Recommended equipment
SMA-BNC adapter	3 ea.	SMA female to BNC male connector	Tektronix part number 015-0572-00
SMA-BNC adapter	1 ea.	SMA male to BNC female connector	Tektronix part number 015-0554-00
BNC-dual banana adapter	1 ea.	BNC to dual banana plugs	Tektronix part number 103-0090-00

Test record

Photocopy the test records and use them to record the performance test results. (See page 65, *Test record*.)

Termination resistance measurement

Many of the performance tests use a BNC-dual banana adapter and 50 Ω BNC feed-through terminator connected to a DMM.

For accuracy, the termination resistance of this connection is used in the calculations.

Use this procedure and note the measured value for use in these procedures.

1. Connect the BNC-dual banana adapter and 50 Ω BNC feed-through terminator to the HI and LO inputs of the digital multimeter.

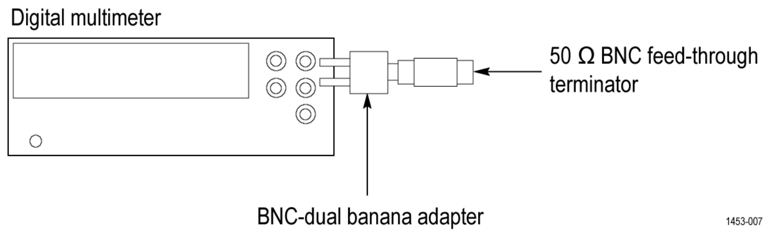


Figure 3: Equipment connection to measure terminator resistance

2. Set the digital multimeter to the **Ω 2 wires** mode.
3. Measure the resistance and note the value as **Term_R**.

   Keep this value available for use in several performance check calculations.
4. Set the digital multimeter to the **DCV** mode.

NOTE. *Lead resistance is not included in the measurement results when using four wire ohms. The accuracy is higher especially for small resistances. Use a four wire method if necessary.*

Analog amplitude accuracy

Required equipment	Prerequisites
Digital multimeter	AWG preparation and load test waveforms (See page 43.)
BNC-dual banana adapter	
50 Ω BNC feed-through terminator	Termination resistance measurement procedure (Term R) (See page 45.)
SMA female-BNC male adapter	
50 Ω SMA terminator	

Before starting this procedure, ensure you have the "**Term R**" value used in the calculations. (See page 45, *Termination resistance measurement*.)

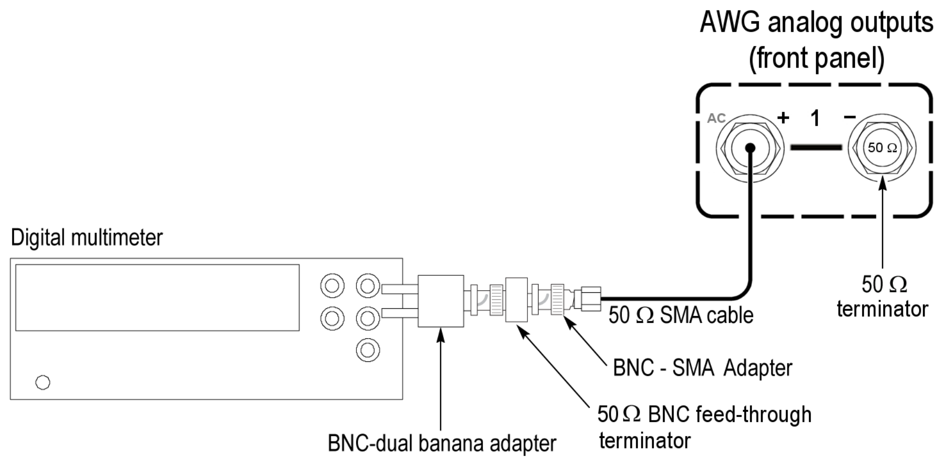
DC High BW output path

1. Click the **Reset to Default Setup** button in the toolbar .
2. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
3. Load the test waveforms **PV_DC_Plus.wfmx** and **PV_DC_Minus.wfmx** into the Waveform List.

NOTE. *Test waveforms are located at* ***C:\Program Files\Tektronix\AWG5200\Samples\PV***.

4. From the Waveform List window, assign the test waveform **PV_DC_Plus.wfmx** to Channel 1.
5. Connect the CH 1 (+) connector from the AWG to the HI and LO inputs of the digital multimeter.

   Use a 50 Ω SMA cable, a BNC-SMA adapter, a 50 Ω BNC feed-through terminator, and a BNC dual banana adapter.
6. Terminate the CH 1 (–) connector on the AWG with a 50 Ω SMA terminator.

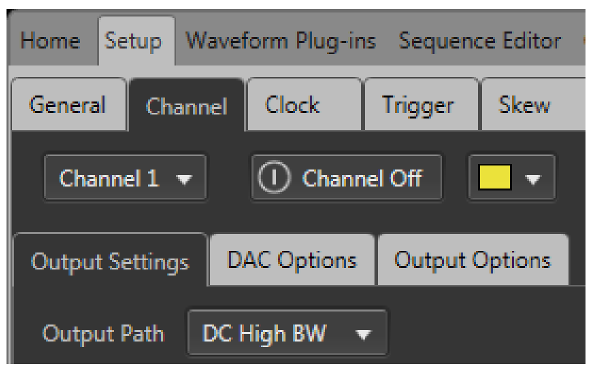


7. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *enable* the outputs (front panel light off).

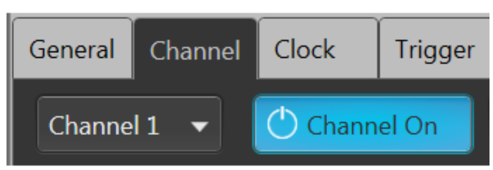
8. Click the **Setup -> Channel** tab and click the **Output Settings** tab.

    a. Select Channel 1.

    b. Set the **Output Path** to **DC High BW**.



    c. Enable the Channel 1 output.



9. Set the **Amplitude** of the AWG as shown in the following table. (See Table 41.)

Table 41: Analog amplitude accuracy (DC High BW output path)

Amplitude settings	Accuracy limits
25 mV_{p-p}	23.75 mV to 26.25 mV
100 mV_{p-p}	98 mV to 102 mV

Table 41: Analog amplitude accuracy (DC High BW output path) (cont.)

Amplitude settings	Accuracy limits
200 mV_{p-p}	196 mV to 204 mV
500 mV_{p-p}	480 mV to 520 mV
1 V_{p-p} **(Requires option DC)**	980 mV to 1.02 V
1.5 V_{p-p} **(Requires option DC)**	1.47 V to 1.53 V

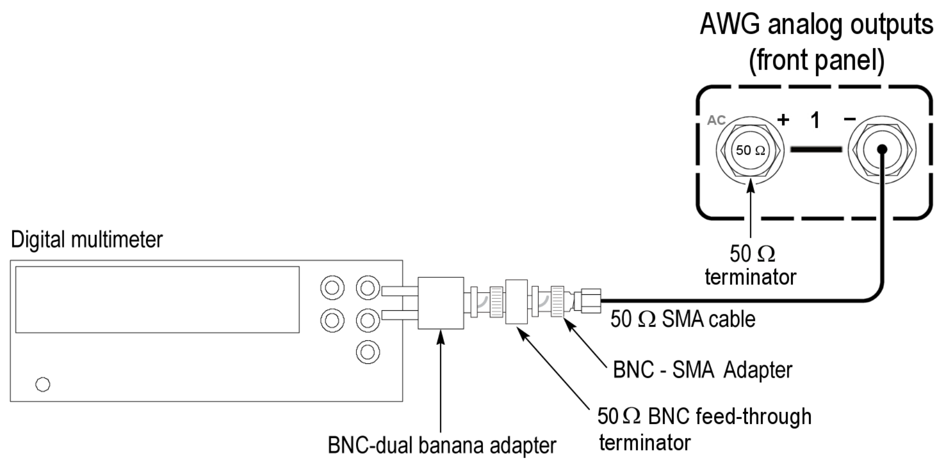
10. Press the **Play** button, or click Play on the display.
11. Measure the output voltage on the digital multimeter and note the value as **Measured_voltage_1**.
12. Use the following formula to compensate the voltage for the 50 Ω BNC feed-through terminator:

    V_high = [(Term_R + 50) / (2 Term_R)] Measured_voltage_1

    Where Term_R is the resistance of the 50 Ω BNC feed-through terminator. (See page 45, *Termination resistance measurement*.) procedure.
13. From the Waveform List window, assign the waveform **PV_DC_Minus.wfmx** to Channel 1.
14. Measure the output voltage on the digital multimeter and note the value as **Measured_voltage_2**.
15. Use the following formula to compensate the voltage for the 50 Ω BNC feed-through terminator:

    V_low = [(Term_R + 50) / (2 Term_R)] Measured_voltage_2

    Where Term_R is the resistance of the 50 Ω BNC feed-through terminator. (See page 45, *Termination resistance measurement*.) procedure.
16. Verify that the voltage difference |(V_high – V_low)| falls within the limits given in the table. (See Table 41 on page 47.)
17. Repeat steps 9 through 16 for each Amplitude setting in the table. (See Table 41 on page 47.)
18. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
19. Move the SMA cable from the CH 1 (+) connector to the CH 1 (–) connector and move the 50 Ω SMA terminator from the CH 1 (–) connector to the CH 1 (+) connector.



20. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *enable* the outputs (front panel light off).
21. Repeat steps 9 through 17 for the CH1 (–) connector.
22. Repeat steps 4 through 21 until all channels are checked, modifying the instructions for the channel under test.
23. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
24. Disconnect the test setup.

DC High Volt output path

NOTE. ***This is the start of testing the optional DC High Volt output path (Option HV).***

If option HV is not licensed, skip this procedure.

1. Click the **Reset to Default Setup** button in the toolbar .
2. Load the test waveforms **PV_DC_Plus.wfmx** and **PV_DC_Minus.wfmx** into the Waveform List.

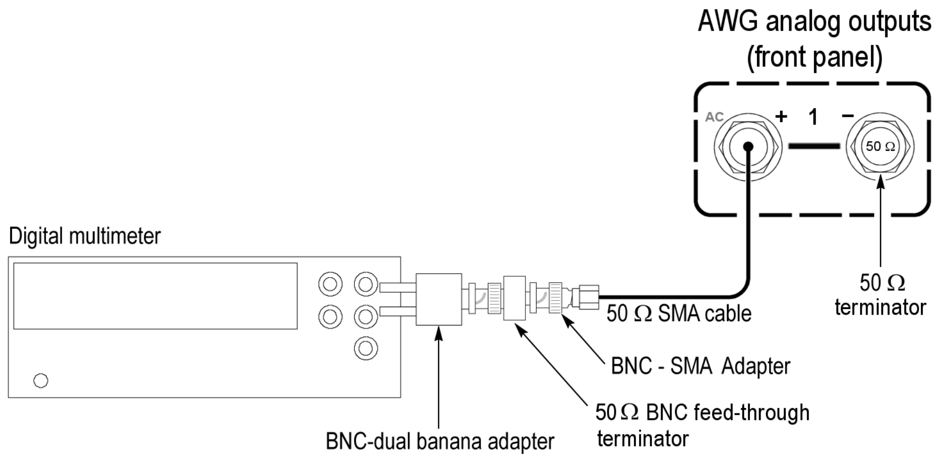
NOTE. *Test waveforms are located at* ***C:\Program Files\Tektronix\AWG5200\Samples\PV****.*

3. From the Waveform List window, assign the waveform **PV_DC_Plus.wfmx** to Channel 1.
4. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).

5. Connect the CH 1 (+) connector from the AWG to the HI and LO inputs of the digital multimeter.

   Use a 50 Ω SMA cable, a BNC-SMA adapter, a 50 Ω BNC feed-through terminator, and a BNC dual banana adapter.

6. Terminate the CH 1 (–) connector on the AWG with a 50 Ω SMA terminator.

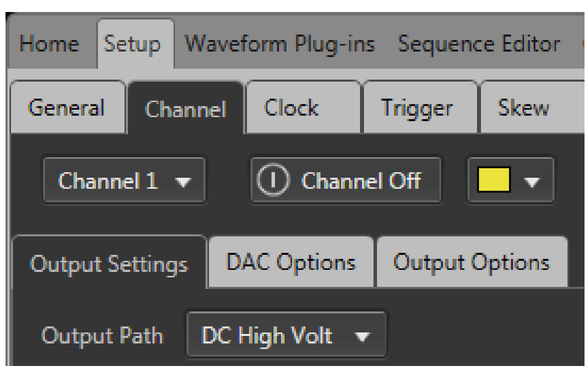


7. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *enable* the outputs (front panel light off).

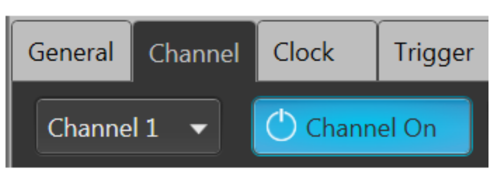
8. Click the **Setup -> Channel** tab and click the **Output Settings** tab.

   a. Select Channel 1.

   b. Set the **Output Path** to **DC High Volt**.



   c. Enable the Channel 1 output.



9. Set the **Amplitude** of the AWG as shown in the following table. (See Table 42.)

Table 42: Analog amplitude accuracy (DC High Volt output path)

Amplitude settings	Accuracy limits
10 mV_{p-p}	9.5 mV to 10.5 mV
100 mV_{p-p}	98 mV to 102 mV
500 mV_{p-p}	480 mV to 520 mV
5 V	4.92 V to 5.08 V

10. Press the **Play** button, or click Play on the display.

11. Measure the output voltage on the digital multimeter and note the value as **Measured_voltage_1**.

12. Use the following formula to compensate the voltage for the 50 Ω BNC feed-through terminator:

    V_high = [(Term_R + 50) / (2 Term_R)] Measured_voltage_1

    Where Term_R is the resistance of the 50 Ω BNC feed-through terminator. (See page 45, *Termination resistance measurement*.) procedure.

13. From the Waveform List window, assign the waveform **PV_DC_Minus.wfmx** to Channel 1.

14. Measure the output voltage on the digital multimeter and note the value as **Measured_voltage_2**.

15. Use the following formula to compensate the voltage for the 50 Ω BNC feed-through terminator:

    V_low = [(Term_R + 50) / (2 Term_R)] Measured_voltage_2

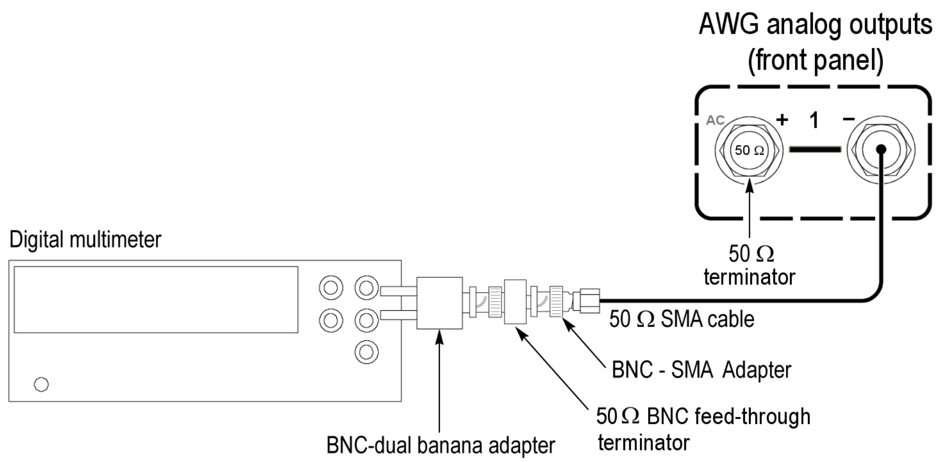
    Where Term_R is the resistance of the 50 Ω BNC feed-through terminator. (See page 45, *Termination resistance measurement*.) procedure.

16. Verify that the voltage difference |(V_high – V_low)| falls within the limits given in the table. (See Table 42 on page 51.)

17. Repeat steps 9 through 16 for each amplitude setting in the table. (See Table 42 on page 51.)

18. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).

19. Move the SMA cable from the CH 1 (+) connector to the CH 1 (–) connector and move the 50 Ω SMA terminator from the CH 1 (–) connector to the CH 1 (+) connector.



20. Repeat steps 9 through 17 for the CH1 (–) connector.

21. Repeat steps 3 through 20 until all channels are checked, modifying the instructions for the channel under test.

22. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).

23. Disconnect the test setup.

Analog offset accuracy (DC output paths)

Required equipment	Prerequisites
Digital multimeter	AWG preparation and load test waveforms(See page 43, *Prerequisites*.)
BNC-dual banana adapter	
50 Ω BNC feed-through terminator	Termination resistance measurement procedure
SMA female-BNC male adapter	
50 Ω SMA terminator	

Before starting this procedure, ensure you have the "**Term R**" value used in the calculations. (See page 45, *Termination resistance measurement*.)

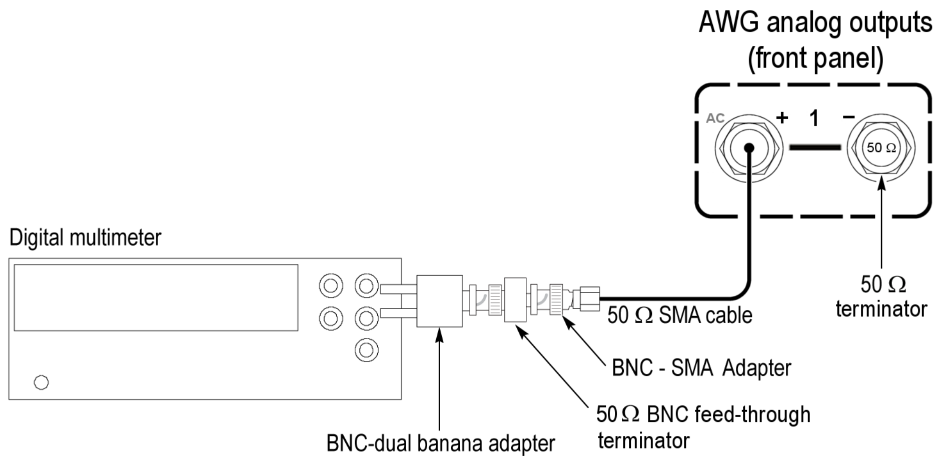
1. Click the **Reset to Default Setup** button in the toolbar .

2. Load the test waveform **PV_DC_Zero.wfmx** into the Waveform List.

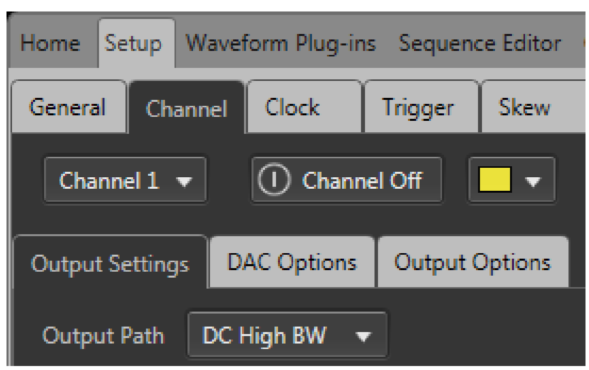
NOTE. *Test waveforms are located at* ***C:\Program Files\Tektronix\AWG5200\Samples\PV****.*

3. From the Waveform List window, assign the waveform **PV_DC_Zero.wfmx** to Channel 1.

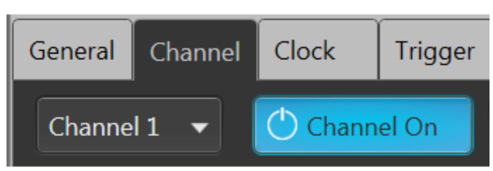
4. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
5. Connect the CH 1 (+) connector from the AWG to the HI and LO inputs of the digital multimeter. Use a 50 Ω SMA cable, a BNC-SMA adapter, a 50 Ω BNC feed-through terminator, and a BNC dual banana adapter.
6. Terminate the CH 1 (–) connector on the AWG using a 50 Ω SMA terminator.



7. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *enable* the outputs (front panel light off).
8. Click the **Setup -> Channel** tab and click the **Output Settings** tab.
   a. Select Channel 1.
   b. Set the **Output Path** to **DC High BW**.



   c. Enable the Channel 1 output.



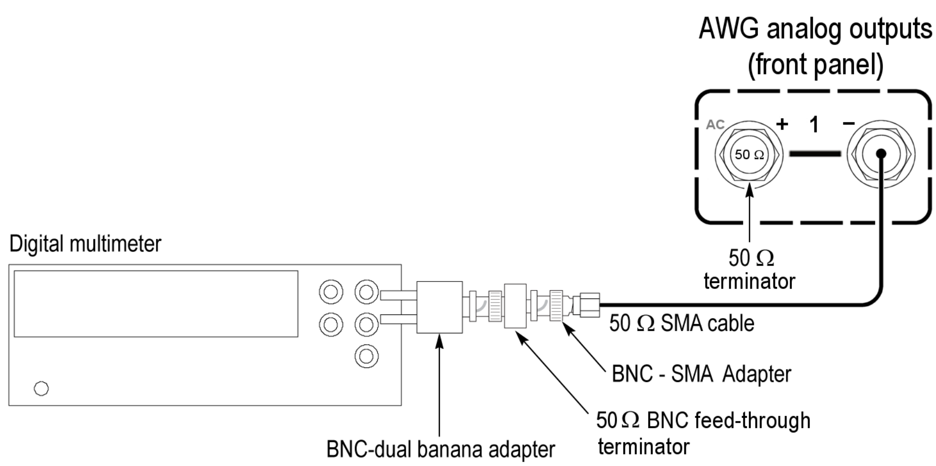
9. Set the **Offset** of the AWG as shown in the first row of the following table. (See Table 43.)

Table 43: Offset accuracy

Offset settings	Accuracy limits
2 V	1.95 V to 2.05 V
0 V	–10 mV to 10 mV
–2 V	–2.05 V to –1.95 V

10. Press the **Play** button, or click Play on the display.
11. Measure the output voltage on the digital multimeter and note the value as **Measured_voltage**.
12. Use the following formula to compensate the voltage for the 50 Ω BNC feed-through terminator:
    V = [(Term_R + 50) / (2×Term_R)] × Measured_voltage

    Where Term_R is the resistance of the 50 Ω BNC feed-through terminator. (See page 45, *Termination resistance measurement*.) procedure.
13. Verify that the voltage *V* falls within the limits given in the table. (See Table 43 on page 54.)
14. Repeat steps 9 through 13 for each offset setting in the table. (See Table 43 on page 54.)
15. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
16. Move the SMA cable from the CH 1 (+) connector to the CH 1 (–) connector and move the 50 Ω SMA terminator from the CH 1 (–) connector to the CH 1 (+) connector.



17. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *enable* the outputs (front panel light off).

18. Repeat steps 9 through 14 for the (–) output.

19. Repeat steps 3 through 18 until all channels are checked, modifying the instructions for the channel under test.

---

*NOTE. **This is the start of testing the optional DC High Volt output path.***

If option HV is licensed, continue with this procedure. If not, skip to step 22.

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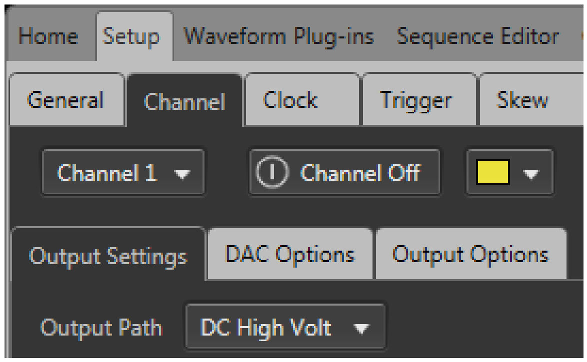
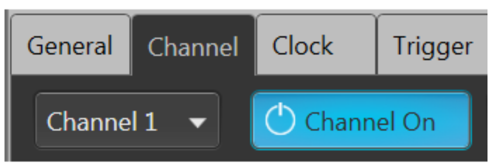
20. Click the **Setup -> Channel** tab and click the **Output Settings** tab.

    a. Select Channel 1.

    b. Set the **Output Path** to **DC High Volt**.



    c. Enable the Channel 1 output.



21. Repeat steps 9 through 19 for the DC High Volt path.

22. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).

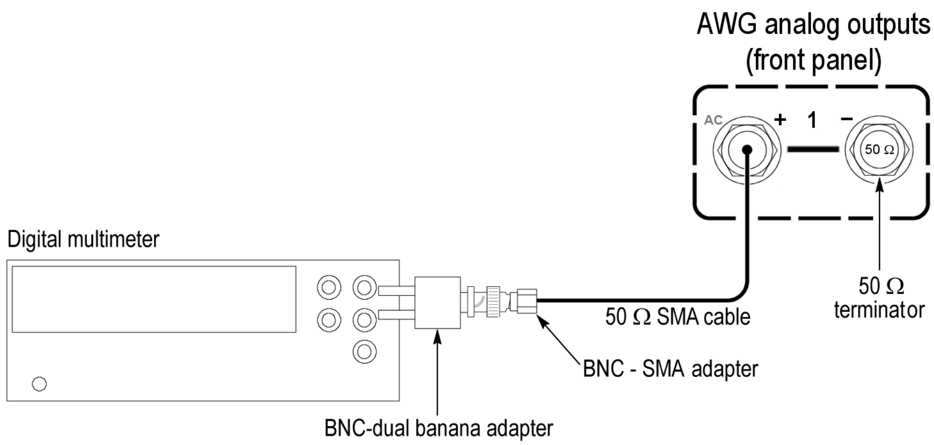
23. Disconnect the test setup.

Analog output DC Bias accuracy (AC output paths)

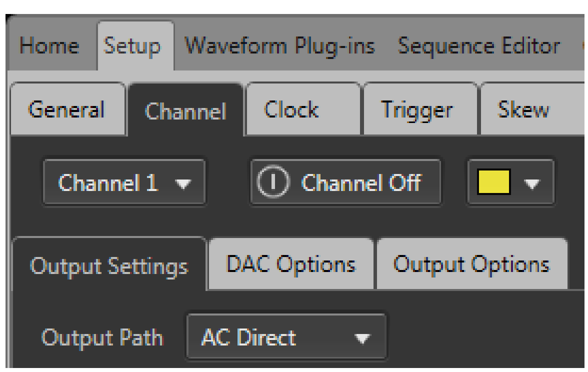
Required equipment	Prerequisites
Digital multimeter	AWG preparation and load test waveforms(See page 43, *Prerequisites*.)
BNC-dual banana adapter	Termination resistance measurement procedure
SMA female-BNC male adapter	
50 Ω SMA terminator	

Before starting this procedure, ensure you have the "**Term R**" value used in the calculations. (See page 45, *Termination resistance measurement*.)

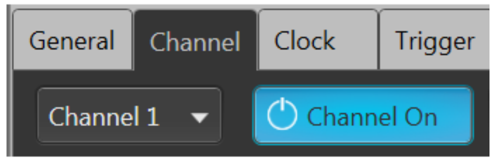
1. Click the **Reset to Default Setup** button in the toolbar .
2. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
3. Connect the CH 1 (+) connector from the AWG to the HI and LO inputs of the digital multimeter. Use a 50 Ω SMA cable, a BNC-SMA adapter, and a BNC dual banana adapter.
4. Terminate the CH 1 (–) connector on the AWG using a 50 Ω SMA terminator.



5. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *enable* the outputs (front panel light off).
6. Click the **Setup -> Channel** tab and click the **Output Settings** tab.
   a. Select Channel 1.
   b. Set the **Output Path** to **AC Direct**.



   c. Enable the Channel 1 output.



7. Set the **DC Bias** of the AWG as shown in the first row of the following table. (See Table 44.)

Table 44: Analog DC bias accuracy

Bias settings	Accuracy limits
5 V	4.88 V to 5.12 V
0 V	–20 mV to 20 mV
–5 V	–5.12 V to –4.88 V

8. Measure the output voltage on the digital multimeter and note the value as **V_1**.
9. Press the front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
10. Measure the output voltage on the digital multimeter and note the value as **V_2** (DMM residual voltage).
11. Verify that the voltage difference (V_1 – V_2) falls within the limits given in the table. (See Table 44 on page 57.)
12. Repeat steps 7 through 11 for each bias setting in the table. (See Table 44 on page 57.)
13. Repeat steps 3 through 12 until all channels are checked, modifying the instructions for the channel number under test.

NOTE. ***This is the start of testing the optional AC Amplified output path.***

If option AC is licensed, continue with this procedure. If not, skip to step 17.

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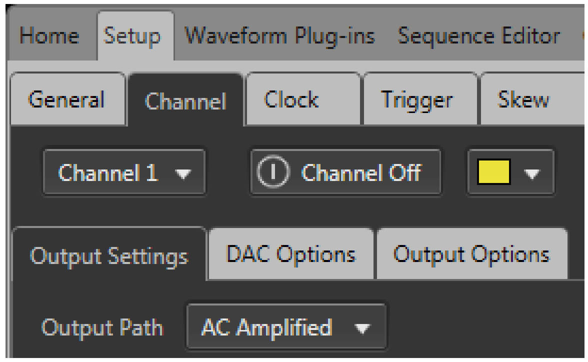
14. Click the **Setup -> Channel** tab and click the **Output Settings** tab.
    a. Select Channel 1.
    b. Set the **Output Path** to **AC Amplified**.



15. Repeat steps 7 through 13 until all channels are checked, modifying the instructions for the channel number under test.

16. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).

17. Disconnect the test setup.

Marker high and low level accuracy

Required equipment	Prerequisites
Digital multimeter	(See page 43, *Prerequisites*.)
BNC-dual banana adapter	Termination resistance measurement procedure
50 Ω BNC cable	
50 Ω BNC feed-through terminator	
SMA male-BNC female adapter	
50 Ω SMA terminator (three)	

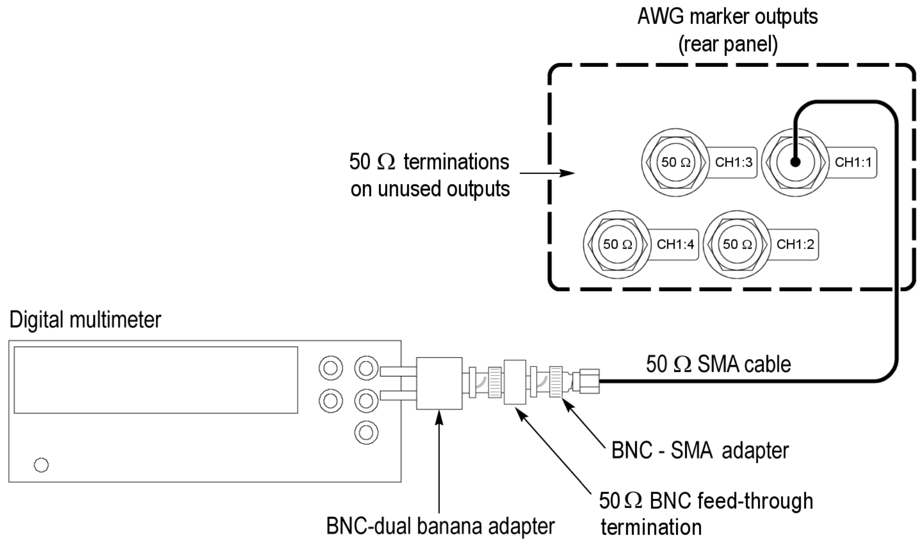
Marker high level accuracy

Before starting this procedure, ensure you have the "**Term R**" value used in the calculations. (See page 45, *Termination resistance measurement*.)

1. Click the **Reset to Default Setup** button in the toolbar .
2. Load the test waveform **PV_DC_Plus.wfmx** into the Waveform List.

NOTE. *Test waveforms are located at* ***C:\Program Files\Tektronix\AWG5200\Samples\PV***.

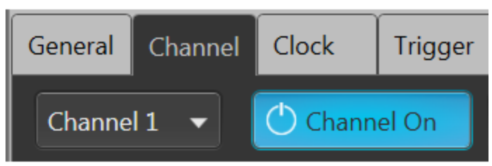
3. From the Waveform List window, assign the waveform **PV_DC_Plus.wfmx** to Channel 1.
4. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).
5. Connect the AWG's CH1:1 marker connector to the HI and LO inputs on the digital multimeter. Use a 50 Ω SMA cable, a BNC-SMA adapter, a 50 Ω BNC feed-through terminator, and a BNC-Banana adapter.
6. Terminate the AWG's CH1:2 through CH1:4 markers using 50 Ω SMA terminators.



7. In the **Setup -> Channel** tab, select **Output Settings** and set the Channel 1 **Resolution** to **12+4 Mkrs**.

8. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *enable* the outputs (front panel light off).

9. Enable the Channel 1 output.



10. In the **Setup -> Channel** tab, select **Output Settings** and set the Channel 1 Marker High Level setting as shown in the first row of the following table. (See Table 45.)

Table 45: Marker high level accuracy

High level settings	Accuracy limits
+ 1.75 V	1.55 V to 1.95 V
0.0 V	–25 mV to +25 mV
–0.3 V	–0.305 V to –0.295 V

11. Measure the output voltage on the digital multimeter and note the value as **Measured_voltage_1**.

12. Use the following formula to compensate the voltage for the 50 Ω BNC feed-through terminator:

Marker_High = (Term_R + 50) / (2 Term_R) Measured_voltage_1

Where Term_R is the resistance of the 50 Ω BNC feed-thought terminator. (See page 45, *Termination resistance measurement*.) procedure.

13. Verify that the Marker_High level falls within the limits given in the table. (See Table 45 on page 60.)

14. Repeat steps 10 through 13 for the remaining rows in the table. (See Table 45 on page 60.)

15. Repeat steps 5 through 13 for each CH1 marker (markers CH1:2 through CH1:4), always terminating the unused markers for the channel under test.

16. Repeat steps 5 through 15 until all channels are checked, modifying the instructions with the channel number under test.

17. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).

NOTE. *This is a continuation of the procedure Marker high level accuracy check.*

Marker low level accuracy

18. Load the test waveform **PV_DC_Minus.wfmx** into the Waveform List.

NOTE. *Test waveforms are located at* ***C:\Program Files\Tektronix\AWG5200\Samples\PV****.*

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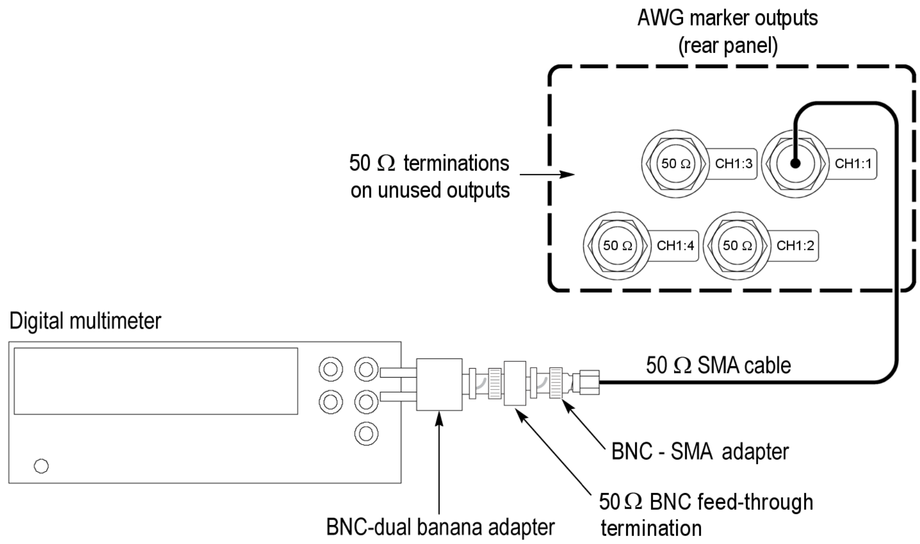
19. From the Waveform List window, assign the waveform **PV_DC_Minus.wfmx** to Channel 1.

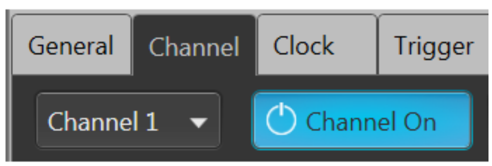
20. Connect the AWG's CH1:1 marker connector to the HI and LO inputs on the digital multimeter. Use a 50 Ω SMA cable, a BNC-SMA adapter, a 50 Ω BNC feed-through terminator, and a BNC-Banana adapter.

21. Terminate the AWG's CH1:2 through CH1:4 markers using 50 Ω SMA terminators.



22. Press the front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *enable* the outputs (front panel light off).

23. Enable the Channel 1 output.



24. In the **Setup -> Channel** tab, select **Output Settings** and set the Channel 1 Marker Low Level setting as shown in the first row of the following table. (See Table 46.)

Table 46: Marker low level accuracy

Low level settings	Accuracy limits
+ 1.55 V	1.37 V to 1.73 V
0.0 V	–25 mV to +25 mV
–0.5 V	–0.525 V to –0.475 V

25. Measure the output voltage on the digital multimeter and note the value as **Measured_voltage_2**.

26. Use the following formula to compensate the voltage for the 50 Ω BNC feed-through terminator:

Marker_Low = (Term_R + 50) / (2 Term_R) Measured_voltage_2

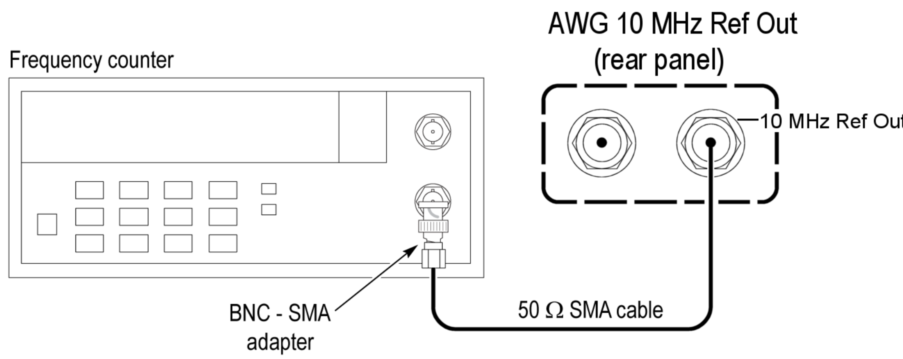
Where Term_R is the resistance of the 50 Ω BNC feed-through terminator. (See page 45, *Termination resistance measurement*.) procedure.

27. Verify that the Marker Low level falls within the limits given in the table. (See Table 46 on page 62.)
28. Repeat steps 24 through 27 for the remaining rows in the table. (See Table 46 on page 62.)
29. Repeat steps 20 through 28 for each CH1 marker (markers CH1:2 through CH1:4), always terminating the unused markers for the channel under test.
30. Repeat steps 20 through 29 until all channels are checked, modifying the instructions with the channel number under test.
31. Press the AWG front panel **All Outputs Off** button (or click All Outputs Off on the Home screen) to *disable* the outputs (front panel light on).

10 MHz reference frequency accuracy

Required equipment	Prerequisites
Frequency counter	(See page 43, *Prerequisites*.)
SMA female-to-BNC male adapter	
50 Ω SMA cable	

1. Click the **Reset to Default Setup** button in the toolbar .
2. Connect the 10 MHz Reference Output on the rear of the AWG to the input of the Frequency Counter. Use a 50 Ω SMA cable and a BNC-SMA adapter.



3. On the Frequency Counter, press the Meas and the Freq buttons.
4. Verify that the frequency counter reading falls within the range of 9.99998 MHz to 10.00002 MHz.
5. Disconnect the test setup.

Test record

Photocopy the test record pages and use them to record the performance test results for your AWG.

AWG5200 series performance test record

AWG Model:	
AWG Serial Number:	Certificate Number:
Temperature:	RH %:
Date of Calibration:	Technician:

Performance test			Minimum	Test result	Maximum
Analog Amplitude Accuracy					
DC High BW Output Path					
AWG5202, AWG5204, AWG5208					
	Ch 1 +	Amplitude			
		25 mV_{p-p}	23.75 mV		26.25 mV
		100 mV_{p-p}	98 mV		102 mV
		200 mV_{p-p}	196 mV		204 mV
		500 mV_{p-p}	480 mV		520 mV
		1 V_{p-p}	980 mV		1.02 V
		1.5 V_{p-p}	1.47 V		1.53 V
	Ch 2 +	Amplitude			
		25 mV_{p-p}	23.75 mV		26.25 mV
		100 mV_{p-p}	98 mV		102 mV
		200 mV_{p-p}	196 mV		204 mV
		500 mV_{p-p}	480 mV		520 mV
		1 V_{p-p}	980 mV		1.02 V
		1.5 V_{p-p}	1.47 V		1.53 V
AWG5204, AWG5208					
	Ch 3 +	Amplitude			
		25 mV_{p-p}	23.75 mV		26.25 mV
		100 mV_{p-p}	98 mV		102 mV
		200 mV_{p-p}	196 mV		204 mV
		500 mV_{p-p}	480 mV		520 mV
		1 V_{p-p}	980 mV		1.02 V
		1.5 V_{p-p}	1.47 V		1.53 V

Performance test		Minimum	Test result	Maximum
Ch 4 +	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V
AWG5208				
Ch 5 +	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V
Ch 6 +	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V
Ch 7+	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V
Ch 8 +	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V

Performance test		Minimum	Test result	Maximum
AWG5202, AWG5204, AWG5208				
Ch 1 –	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V
Ch 2 –	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V
AWG5204, AWG5208				
Ch 3 –	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V
Ch 4 –	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V
AWG5208				
Ch 5 –	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V

Performance test		Minimum	Test result	Maximum
Ch 6 –	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V
Ch 7–	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V
Ch 8 –	Amplitude			
	25 mV_{p-p}	23.75 mV		26.25 mV
	100 mV_{p-p}	98 mV		102 mV
	200 mV_{p-p}	196 mV		204 mV
	500 mV_{p-p}	480 mV		520 mV
	1 V_{p-p}	980 mV		1.02 V
	1.5 V_{p-p}	1.47 V		1.53 V

Performance Test		Minimum	Test result	Maximum
Analog Amplitude Accuracy				
High Volt Output Path				
AWG5202, AWG5204, AWG5208				
Ch 1 +	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
Ch 2 +	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
AWG5204, AWG5208				
Ch 3 +	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
Ch 4 +	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
AWG5208				
Ch 5 +	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
Ch 6 +	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V

Performance Test		Minimum	Test result	Maximum
Ch 7 +	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
Ch 8 +	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
AWG5202, AWG5204, AWG5208				
Ch 1 –	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
Ch 2 –	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
AWG5204, AWG5208				
Ch 3 –	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
Ch 4 –	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
AWG5208				
Ch 5 –	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V

Performance Test		Minimum	Test result	Maximum
Ch 6 –	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
Ch 7 –	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V
Ch 8 –	Amplitude			
	10 mV_{p-p}	9.5 mV		10.5 mV
	100 mV_{p-p}	98 mV		102 mV
	500 mV_{p-p}	480 mV		520 mV
	5 V_{p-p}	4.92 V		5.08 V

Performance Test			Minimum	Test result	Maximum
Analog Offset Accuracy					
(DC High BW Output Path)					
AWG5202, AWG5204, AWG5208					
Ch 1 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 2 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
AWG5204, AWG5208					
Ch 3 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 4 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
AWG5208					
Ch 5 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 6 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 7 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 8 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V

Performance Test			Minimum	Test result	Maximum
AWG5202, AWG5204, AWG5208					
Ch 1 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 2 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
AWG5204, AWG5208					
Ch 3 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 4 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
AWG5208					
Ch 5 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 6 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 7 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 8 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V

Performance Test			Minimum	Test result	Maximum
Analog Offset Accuracy					
(DC High Volt Output Path)					
AWG5202, AWG5204, AWG5208					
Ch 1 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 2 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
AWG5204, AWG5208					
Ch 3 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 4 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
AWG5208					
Ch 5 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 6 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 7 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 8 +	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V

Performance Test			Minimum	Test result	Maximum
AWG5202, AWG5204, AWG5208					
Ch 1 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 2 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
AWG5204, AWG5208					
Ch 3 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 4 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
AWG5208					
Ch 5 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 6 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 7 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V
Ch 8 –	Offset	Amplitude			
	2 V	500 mV_{pp}	1.935 V		2.065 V
	0 V	500 mV_{pp}	–25 mV		25 mV
	–2 V	500 mV_{pp}	–2.065 V		–1.935 V

Performance test		Minimum	Test result	Maximum
Analog DC Bias Accuracy				
(AC Direct Output Path)				
AWG5202, AWG5204, AWG5208				
Ch 1 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
Ch 2 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
AWG5204, AWG5208				
Ch 3 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
Ch 4 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
AWG5208				
Ch 5 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
Ch 6 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
Ch 7 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
Ch 8 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V

Performance test			Minimum	Test result	Maximum
AWG5202, AWG5204, AWG5208					
	Ch 1 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
	Ch 2 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
AWG5204, AWG5208					
	Ch 3 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
	Ch 4 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
AWG5208					
	Ch 5 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
	Ch 6 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
	Ch 7 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
	Ch 8 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V

Performance test		Minimum	Test result	Maximum
Analog DC Bias Accuracy				
(AC Amplified Output Path)				
AWG5202, AWG5204, AWG5208				
Ch 1 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
Ch 2 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
AWG5204, AWG5208				
Ch 3 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
Ch 4 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
AWG5208				
Ch 5 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
Ch 6 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
Ch 7 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V
Ch 8 +	DC Bias			
	5 V	4.88 V		5.12 V
	0 V	–20 mV		20 mV
	–5 V	–5.12 V		–4.88 V

Performance test			Minimum	Test result	Maximum
AWG5202, AWG5204, AWG5208					
	Ch 1 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
	Ch 2 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
AWG5204, AWG5208					
	Ch 3 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
	Ch 4 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
AWG5208					
	Ch 5 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
	Ch 6 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
	Ch 7 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V
	Ch 8 –	DC Bias			
		5 V	4.88 V		5.12 V
		0 V	–20 mV		20 mV
		–5 V	–5.12 V		–4.88 V

Performance test		Minimum	Test result	Maximum
Marker				
High Level Accuracy				
AWG5202, AWG5204, AWG5208				
CH1:1	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH1:2	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH1:3	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH1:4	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH2:1	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH2:2	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH2:3	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH2:4	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V

Performance test		Minimum	Test result	Maximum
AWG5204, AWG5208				
CH3:1	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH3:2	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH3:3	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH3:4	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH4:1	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH4:2	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH4:3	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH4:4	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
AWG5208				
CH5:1	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH5:2	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH5:3	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH5:4	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V

Performance test		Minimum	Test result	Maximum
CH6:1	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH6:2	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH6:3	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH6:4	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH7:1	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH7:2	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH7:3	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH7:4	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH8:1	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH8:2	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH8:3	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		+25 mV
	–0.3 V	–0.305 V		–0.295 V
CH8:4	+ 1.75 V	1.55 V		1.95 V
	0.0 V	–25 mV		25 mV
	–0.3 V	–0.305 V		–0.295 V

Performance test		Minimum	Test result	Maximum
Marker				
Low Level Accuracy				
AWG5202, AWG5204, AWG5208				
CH1:1	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH1:2	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH1:3	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH1:4	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH2:1	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH2:2	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH2:3	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH2:4	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V

Performance test		Minimum	Test result	Maximum
AWG5204, AWG5208				
CH3:1	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH3:2	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH3:3	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH3:4	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH4:1	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH4:2	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH4:3	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH4:4	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
AWG5208				
CH5:1	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH5:2	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH5:3	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH5:4	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V

Performance test		Minimum	Test result	Maximum
CH6:1	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH6:2	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH6:3	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH6:4	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH7:1	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH7:2	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH7:3	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH7:4	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		+25 mV
	–500 mV	–0.525 V		–0.475 V
CH8:1	+ 1.55 V	1.37 V		1.55 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH8:2	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH8:3	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V
CH8:4	+ 1.55 V	1.37 V		1.73 V
	0.0 V	–25 mV		25 mV
	–500 mV	–0.525 V		–0.475 V

Performance test	Minimum	Test result	Maximum
10 MHz Reference Frequency Accuracy			
	9.99998 MHz		10.00002 MHz