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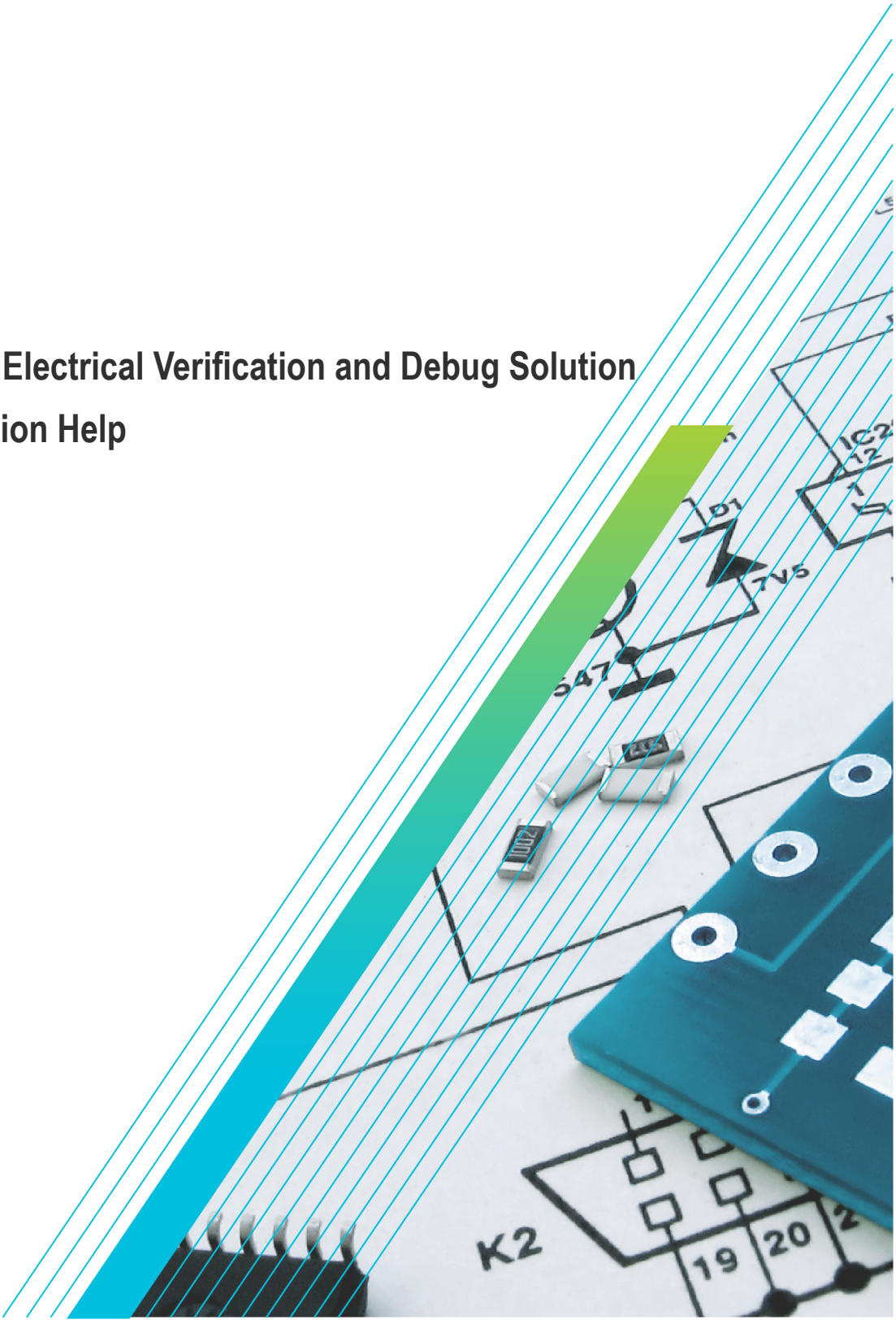
DDR Analysis
Memory Interface Electrical Verification and Debug Solution
Printable Application Help



077-0231-18

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- In North America, call 1-800-833-9200.
- Worldwide, visit *www.tek.com* to find contacts in your area.

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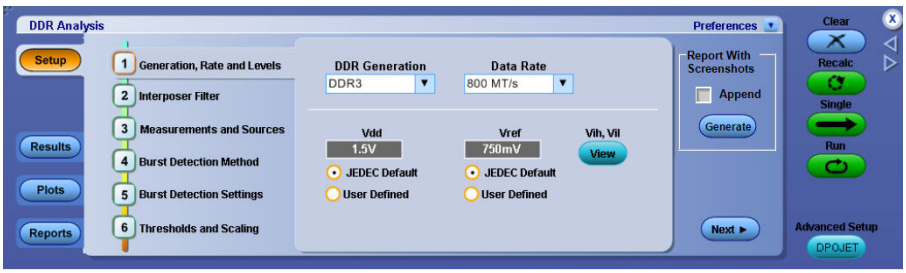
Welcome

DDR (Dual Data Rate) is a dominant and fast-growing memory technology. It offers the high data transfer rates needed for virtually all computing applications, from consumer products to the most powerful servers. The high speeds of these signals require high performance measurement tools.

The DDRA application includes compliance measurements as part of the Tektronix DDR Analysis solution. The DDR Analysis solution enables you to achieve new levels of productivity, efficiency, and measurement reliability. It requires the Jitter and Eye Diagram Analysis tool (Opt. DJA) and the Advanced Search and Mark capability (Opt. ASM).



Some of the DDRA features are:

- Provides debug, analysis, and compliance in one solution for multiple DDR standards such as DDR, DDR2, DDR3, DDR3L, DDR4, LPDDR, LPDDR2, LPDDR3, LPDDR4, LPDDR4X, GDDR3, and GDDR5.
- Enables analysis of compliance measurements either through the DDRA or DPOJET application for all bursts in an acquisition.
- Differentiates data reads from writes or analyzes signal integrity on the clock or on a data (DQ) line during Read or Write cycles, or measures Data to Strobe setup and hold during Write cycles.
- Includes limit files to test measurement pass/fail status per standard, speed grades and speed bins. Supports non-standard speed grades.
- Provides both single-ended and differential measurements on Data, Strobe, Clock, Address and Command signals.
- Includes comprehensive measurement statistics.
- Includes sophisticated graphical analysis tools such as Histograms, Time Trends, Spectrums, Bathtub Plots, and Real-Time Eye® diagrams with superimposition of the strobe eye with the data eye.
- Produces consolidated reports automatically with pass/fail information, statistical measurement results, setup information, limits information, waveform path location, plots, and user comments, if any.
- Automatically applies signal slew rate derating of measurement limits for Address/Command and data signals.
- Dynamically normalizes limits for clock measurements such as tERR based on the measured tCK(avg).
- Logic state configuration using the DDRA user interface.

DDR

DDR is the DRAM (Dynamic Random Access Memory) technology responsible for increasing data transfer rates to meet high-speed requirements and data capacity of computer systems.

DDR2

DDR2 is the Double Data Rate 2 SDRAM (Synchronous Dynamic Random Access Memory) and is widely available in products with data rates up to 1066 MT/s.

DDR3

DDR3 DRAM memory is widely available in products and extends data rates to 1600 MT/s and faster rates to come.

DDR3L

DDR3L (Low voltage) DRAM memory is widely available in products and extends data rates to 1600 MT/s and faster rates to come.

DDR4

DDR4 DRAM memory is widely available in products and extends data rates to 3200 MT/s and faster rates to come.

LPDDR

LPDDR (Low Power DDR) is a technology for mobile phones and portable computing devices, driven by the need for faster operation with long battery life.

LPDDR2

LPDDR2 (Low Power DDR2) is a technology for mobile phones and portable computing devices as it supports advanced power management. It includes a reduced interface voltage of 1.2 V from the 1.8 V specification as compared to LPDDR memory technology. This results in a power consumption reduced by over 50%.

LPDDR3

LPDDR3 (Low Power DDR3) is a technology for mobile phones and portable computing devices as it supports advanced power management. It includes a reduced interface voltage of 1.2 V from the 1.8 V specification as compared to LPDDR memory technology. This results in a power consumption reduced by over 50%.

LPDDR4

LPDDR4 (Low Power DDR4) is an emerging technology for mobile phones and portable computing devices as it supports advanced power management. It includes a reduced interface voltage of 1.1 V from the 1.8 V specification as compared to LPDDR memory technology.

LPDDR4X

LPDDR4X (Low Power DDR4X) is an extension to the LPDDR4 standard. It is identical to LPDDR4, except that additional power is saved by reducing the I/O voltage (Vddq) to 0.6 V rather than 1.1 V.

GDDR3

GDDR3 (Graphic DDR3) offers faster access and is used in graphics-intensive applications such as video cards and gaming systems.

GDDR5

GDDR5 (Graphic DDR5) is a type of high performance dynamic random-access graphics card memory designed for applications requiring high bandwidth.

Introduction

Related documentation

Tektronix manuals and softwares are available at: *www.tektronix.com/manuals* and *www.tektronix.com/software*. Use the following table to determine the document that you need:

Table 1: List of reference documents

For information on	Refer to
• Operating the oscilloscope	Refer to the documentation for your oscilloscope.
• Software warranty • List of available applications • Compatible oscilloscopes • Relevant software and firmware version numbers • Applying a new option key label • Installing an application • Enabling an application • Downloading updates from the Tektronix Web site	For details, refer to *Optional Applications Software on Windows-Based Oscilloscopes Installation Manual*.

Conventions

This online help uses the following conventions:

- When steps require a sequence of selections using the application interface, the > delimiter marks each transition between a menu and an option. For example, **Analyze > DDR Analysis.**
- The terms DDR application and application refer to DDRA.
- The term DPOJET application or DPOJET refers to the Jitter and Eye Diagram Analysis Tool.
- The term oscilloscope refers to any product on which this application runs.
- The term DUT is an abbreviation for Device Under Test.
- User interface screen graphics are taken from a DPO7000 series oscilloscope.

Technical support

Tektronix welcomes your comments about products and services. Contact Tektronix through e-mail, telephone, or the Web site. Click *www.tektronix.com/manuals* for more information. Tektronix also welcomes your feedback. Click *Customer feedback* for suggestions for providing feedback to Tektronix.

Customer feedback

Tektronix values your feedback on our products. To help us serve you better, please send us your suggestions, ideas, or other comments you may have regarding the application or oscilloscope.

Direct your feedback through e-mail to

techsupport@tektronix.com

Or FAX at (503) 627-5695, and include the following information:

General Information

- Oscilloscope series (for example: DPO7000C or DSA/DPO/MSO70000C/D/DX series) and hardware options, if any
- Software version number
- Probes used

Application-specific Information

- Description of the problem such that technical support can duplicate the problem
- If possible, save the oscilloscope and application setup files as `.set` and associated `.xml` files.
- If possible, save the waveform on which you are performing the measurement as a `.wfm` file.

Once you have gathered this information, you can contact technical support by phone or through e-mail. In the subject field, please indicate DDRA Problem and attach the `.set`, `.xml` and `.wfm` files to your e-mail. If there is any query related to the actual measurement results, then you can generate a `.mht` report and send it. If you need to send very large files, technical support can assist you to transfer the files through ftp.

The following items are important, but optional:

- Your name
- Your company
- Your mailing address
- Your phone number
- Your FAX number

Enter your suggestion. Please be as specific as possible.

Please indicate if you would like to be contacted by Tektronix regarding your suggestion or comments.

Getting started

DDRA prerequisites

DDRA application requires DPOJET Advanced (Opt. DJA) and Search and Mark (Opt. ASM) to be enabled.

Requirements and restrictions

DPOJET (DJA) is required to operate DDRA on your oscilloscope. Also refer to subsequent requirements for DPOJET.

Supported probes

The application supports the following probes:

- TAP2500
- TAP1500
- TCP0030
- P6158
- P6101B
- P6246
- P6247 (DPO7254 only)
- P6248 (DPO7254 only)
- P6249
- P6150
- P6158
- P7240
- P7260
- P7330
- P7340A
- P7350
- P7360A
- P7380A
- P7313A
- P7513
- P7520A
- P7520
- P7500 Series TriMode Probes
- P7700 Series TriMode Probes

Installing the application

Refer to the *Optional Application Software on Windows-Based Oscilloscopes Installation Manual* for the following information:

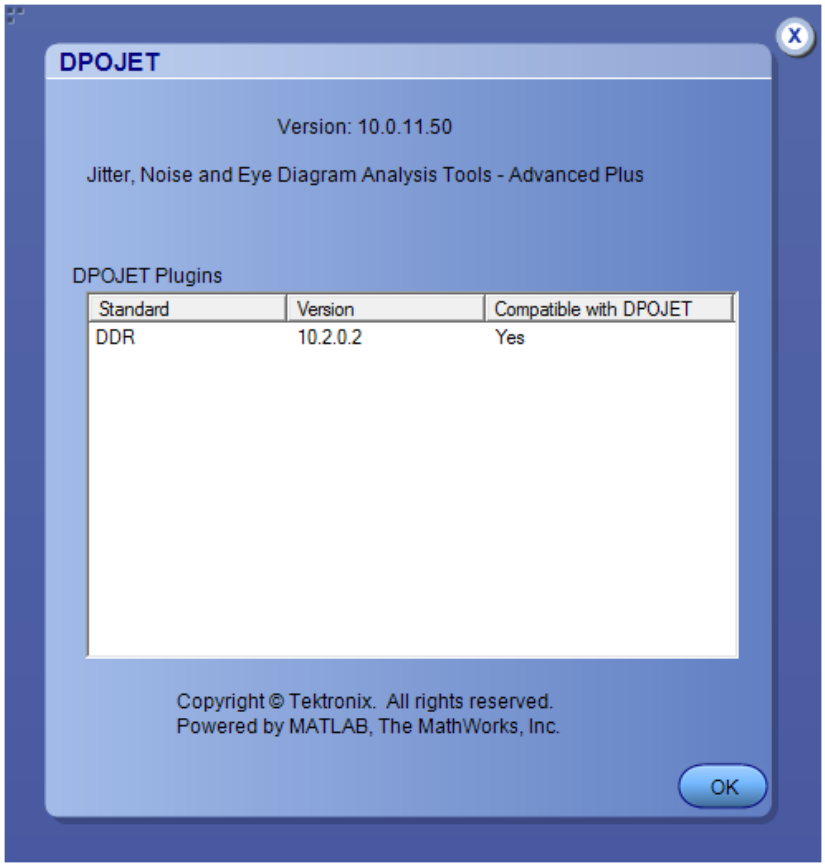
- Software warranty.
- List of available applications, compatible oscilloscopes, and relevant software and firmware version numbers.
- Applying a new option installation key label.
- Installing an application.
- Enabling an application.
- Downloading updates from the Tektronix Web site.

For DDRA application, install both DPOJET and DDRA after re-installing TekScope. The sequence that should be followed:

- TekScope
- DPOJET
- DDRA

Version information

To identify the installed version of the DDRA application, click **Help > About DPOJET**.



Tutorial

Introduction to the tutorial

This tutorial shows how to set up the application, take measurements, and view results as plots or statistics.

Before you begin the tutorial, perform the following tasks:

- Set up the oscilloscope.
- Start the application.
- Recall the tutorial waveform.

Setting up the oscilloscope

The steps to set up the oscilloscope are:

- Click **File > Recall Default Setup** in the oscilloscope menu bar to recall the default settings.
- Press the individual CH1, CH2, CH3, and CH4 buttons as needed to add or remove active waveforms from the display.

Starting the application

On the oscilloscope menu bar, click **Analyze > DDR Analysis** to open the application.

Waveform files

The DDRA application provides the following waveforms at `C:\Users\Public\Tektronix\TekApplications\DDRA\Waveforms\DDR2` for oscilloscopes running the Windows10 operating system:

- DDR2_800_DQS_Write.wfm
- DDR2_800_DQ_Write.wfm
- DDR2_800_CLK.wfm

Note: These waveforms have to be used only for Write bursts and CLK.

Recalling a waveform file

To recall a waveform file, follow these steps:

1. Click **File > Recall** in the oscilloscope menu bar to display the Recall dialog box.
2. Click Waveform icon in the left of the Recall dialog box.
3. Select Ref1, Ref2, Ref3, or Ref4 as the Destination option.
4. Browse to select the waveform. Use the keypad to edit the waveform file name.
5. Click **Recall**.

   The oscilloscope recalls and activates the Reference Waveform control window.
6. Click **On** to display the waveform.
7. Click  to return to the application. Alternatively, DDRA can also be accessed from **Analyze > DDR Analysis**.

Taking a measurement

This tutorial uses the following example:

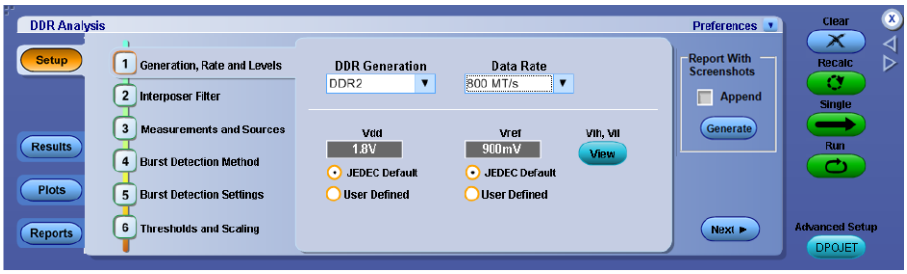
DDR2 800MT/s, Write bursts - Differential measurements

Waveforms Used: DDR2_800_DQS_Write.wfm and DDR2_800_DQ_Write.wfm

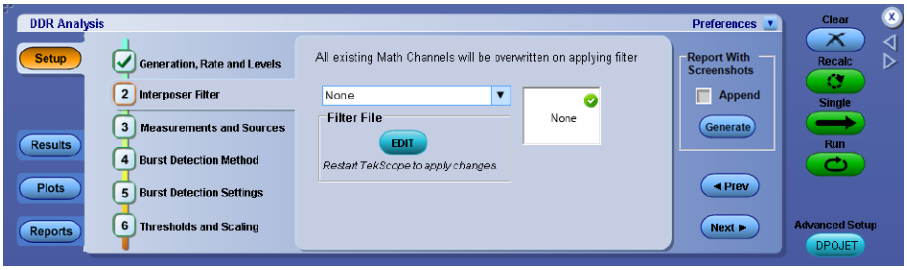
1. To set the application to default values, click **File > Recall Default Setup**.

   Note: This is not necessary if you have just started the application.
2. To view the DDRA application, select **Analyze > DDR Analysis**.
3. At Step 1, select the DDR2 standard and the data rate as 800 MT/s.

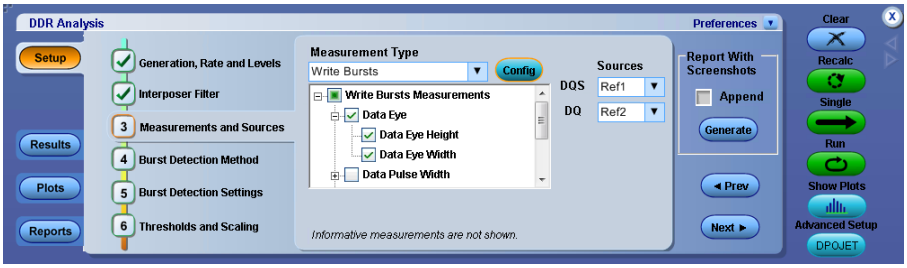
   The default voltage settings are retained as shown.



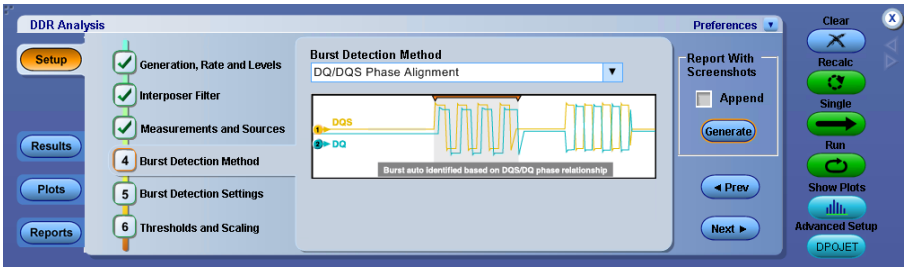
4. At Step 2, select the filter.



5. At Step 3, select the measurements and the associated sources.



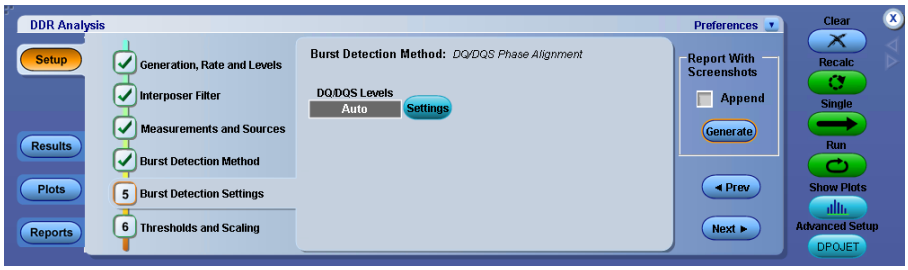
6. At Step 4, select the burst detection method.



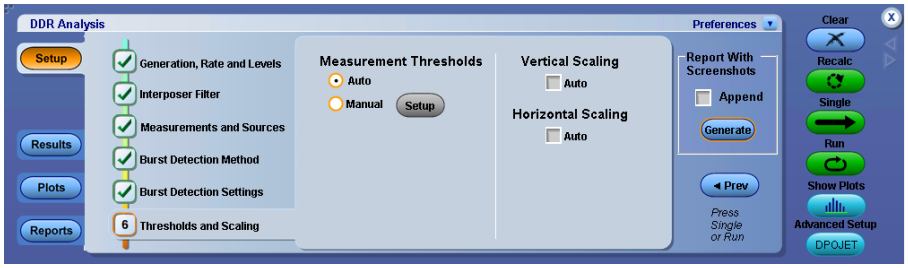
The selected data rate, generation, and measurement type are reflected in ASM (Advanced Search and Mark) on selection in DDRA. Marks are available only for Read and Write bursts measurement type. Configure Search using **Analyze > Search > Configure**. The identified bursts are shown as small inverted marks ( ) in the oscilloscope display area. Each pair of marks specifies the start and stop of a burst. You can traverse from one mark to the other using the Mark Control window. For more details, refer to *Oscilloscope* help.

Note: Logic state+ DQ/DQS Phase Alignment is available only for the MSO series of oscilloscopes.

7. At Step 5, configure the burst detection settings based on the selected burst detection method as shown.

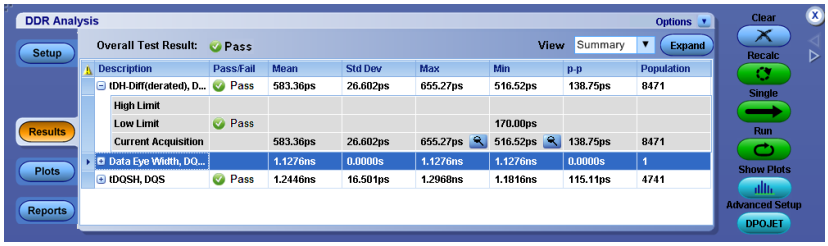


8. At Step 6, retain the settings as shown.

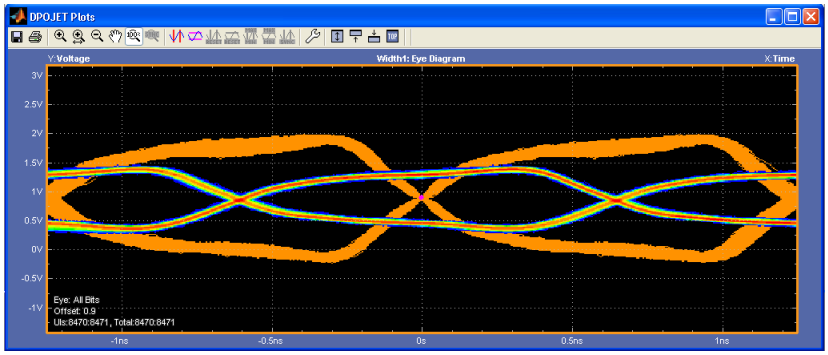


9. Click **Single** to run the application.

   When complete, the result statistics with limits are shown under the Results tab.



The eye diagram plot is displayed as shown.



Operating basics

About basic operations

DDRA user interface

Following are the description of DDRA user interface:

- Use the Single button  to obtain a set of measurements from a single new waveform acquisition. Pushing the button again before process is completed will interrupt the processing cycle.
- Use the Run button  to continuously acquire and accumulate measurements.

  If prior measurements have been acquired and have not been cleared, the new measurements are added to the existing set. Push the button again to interrupt the current acquisition.
- Use the Recalc button  to perform measurements on the waveform currently displayed on the oscilloscope without performing a new acquisition.

  This is useful to modify a configuration parameter and re-run the measurements on the current waveform.
- Use the Clear button  to clear all existing measurement results.

Note: Adding or deleting a measurement, or changing a configuration parameter of an existing measurement, will also cause measurements to be cleared. This is to prevent the accumulation of measurement statistics or sets of statistics that are not coherent.

Basic oscilloscope functions

Application directories

During DDRA application installation, various folders are created as described in the following table.

Type	Directory path	Description
Application executables	`C:\Program Files\TekApplications\DDRA`	Contains DDRA application assembly files.
Limits	`C:\Users\Public\Tektronix\TekApplications\DDRA\Limits`	Contains limit files of DDRA standards and speed grades.
Mask File	`C:\Users\Public\Tektronix\TekApplications\DDRA\Masks`	Contains mask files used for eye measurements.
Symbol Files	`C:\Users\Public\Tektronix\TekScope\BusDecodeTables\DDR`	Contains symbol files.

File name extensions

Table 2: File name extensions

File Extension	Description
`.csv`	An ASCII file containing Comma Separated Values. This file format may be read by any ascii text editor (such as Notepad) or may be imported into spreadsheets such as Excel.

Table continued…

File Extension	Description
.xml	An ASCII file containing measurement setup information, limits or other data in Extensible Markup Language.
.set	A binary file containing oscilloscope setup information in a proprietary format.
.mht	An HTML archive file, compatible with common Windows applications; contains the full report, including text and graphics.
.wfm	A binary file containing an oscilloscope waveform record in a recallable, proprietary format.
.tsf	A symbol file containing various symbols for various logic trigger patterns.

Returning to the application

When you access oscilloscope functions, the DDRA control windows may be replaced by the oscilloscope control windows or by the oscilloscope graticule. You can access oscilloscope functions in the following ways:

- From the menu bar on the oscilloscope, choose **Analyze > DDR Analysis**.
- Alternatively, you can switch between recently used control panels using the forward  or back arrows  on the right corner of the control panel.

Control panel

The Control panel appears on the right side of the application window. Using this panel, you can start or stop the sequence of processes for the application and the oscilloscope to acquire information from the waveform. The controls are Clear, Recall, Single, and Run. The following table describes each of these controls:

Item	Description
Clear	Clears the current result display and resets any statistical results and autoset reference levels. For any input sources that have reference level autoset enabled, this control clears the current reference levels so that they will be recalculated during the next acquisition.
Recall	Runs the selected measurements on the currently displayed waveform(s), without first performing a new acquisition.
Single	Initiates a single new acquisition and runs the selected measurements.
Run	Initiates new acquisitions and runs the selected measurements repeatedly until Stop is selected. For any non-live sources (Reference waveforms or Math waveforms not dependent on a live channel), only a single processing cycle will occur.
Show Plots	Displays the Plot summary window when selected. This button appears in the control panel only when one or more plots have been defined.
Advanced Setup DPOJET 	Transitions to the Jitter and Eye Diagram Analysis application when selected, importing all currently defined DDRA measurements. This button appears in the control panel when you open the DDR analysis application. This is useful to add additional measurements not defined in DDRA, or to change measurement configurations to intentionally deviate from those recommended by DDRA.

Saving and recalling setups

Saving a setup

The DDRA application state is automatically saved along with the oscilloscope state. To save the oscilloscope settings and the application state, do the follow steps:

1. Click **File > Save As > Setup**.
2. In the file browser, select the directory to save the setup file.
3. Select or enter a file name.

   The application appends `*_DDRA.xml` and `*_DPOJET.xml` to store the DDR setup, and *.set to store the oscilloscope settings.
4. Click **Save**.

Note: After the oscilloscope application is started, DDRA needs to be launched at least once before any saved DDRA configuration can be recalled.

Recalling a saved setup

To recall a previously saved set of application and oscilloscope settings, do the following steps:

Note: While recalling setup files with both DDRA and DPOJET saved settings, DDRA setup values get a higher precedence over DPOJET setup values. For example, select a DPOJET measurement and a DDRA measurement, change the ref levels of DPOJET measurement, and save the setup file. On recalling the setup file, you will see that the DPOJET reference level settings are overwritten by the DDRA measurement ref levels.

1. Click **File > Recall**.
2. Click **Setup** in the left column if it is not already selected.
3. Select the directory in the file browser to recall the setup file.
4. Select a .set file and click **Recall**.

Note: If DDRA has been launched at least once since the oscilloscope application was started, only .set files can be selected. Also, any corresponding *_DDRA.xml and *_DPOJET.xml files in the same directory will be recalled as well but the DDRA configuration will be ignored.

Recalling the default setup

To recall the default application and oscilloscope settings, click **File > Recall Default Setup**.

Note: Recalling the default setup sets the DDRA application to DDR3 generation and the data rate to None.

Search and mark

The data rate, generation, and measurement type selected in DDRA are also set in Advanced Search and Mark (ASM). Marks are available only for the Read and Write bursts measurement types. You can configure Search using **Analyze > Search > Configure**. The identified bursts are shown as small inverted marks ( ) in the oscilloscope display area. Each pair of marks specifies the start and stop of a burst. You can move from one mark to the other using the Mark Control window.

Note: LPDDR4/LPDDR4X burst cannot be configured from ASM window.

Limits

A limits file allows you to configure the limits used to determine the Pass or Fail status for tests. Each limits file includes a list of one or more measurements, and the ranges of acceptable values for any or all statistics for each measurement. The measurement include combinations of all measurements and statistical characteristics, and an appropriate range of values for each combination.

The application provides preconfigured limits files for many combinations of standards and speed grades. You can create a limit file by specifying limits for any of the result parameters such as Mean, Std Dev, Max, Min, peak-to-peak, population, MaxPosDelta, and MinPosDelta. For each of these result parameters, you can specify the Upper Limit Equality (UL), and the Lower Limit Equality (LL). The measurement names in the limits file must be entered as mentioned in *About DDR Analysis*.

To include pass/fail status in the result statistics, you can create a custom limits file in the following format using an XML editor or any other editor. If the file is created in any other editor such as Notepad, it should be saved in Unicode format.

The following is a sample of the limit file for DDR2 generation, the data rate being 667 MHz - `DDR2_667MHz_Limits.xml`

```
<?xml version="1.0" encoding="utf-8"?>
<Main>
  <!-- DDR2 667MHz Limits -->
 <Measurement>
  <NAME>tDH-Diff(base)</NAME>
  <STATS>
   <STATS_NAME>Min</STATS_NAME>
   <LIMIT>LL</LIMIT>
   <UL>0</UL>
   <LL>175e-12</LL>
  </STATS>
 </Measurement>
 <Measurement>
  <NAME>tDS-Diff(base)</NAME>
```

```
<STATS>
  <STATS_NAME>Min</STATS_NAME>
  <LIMIT>LL</LIMIT>
  <UL>0</UL>
  <LL>100e-12</LL>
 </STATS>
</Measurement>
</Main>
```

You can find limit files for various data rates of different DDR standards and speed bins at `C:\Users\Public\Tektronix\TekApplications\DDRA\Limits`.

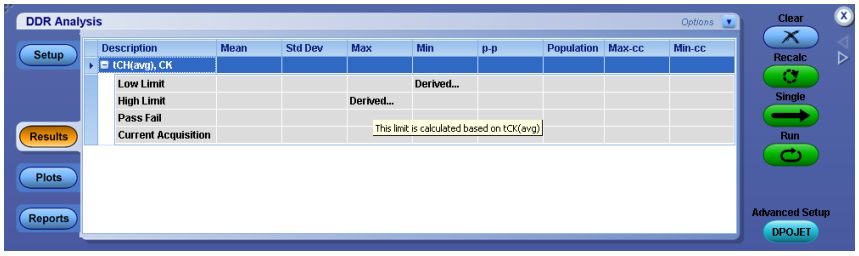
Dynamic limits

The application supports both static (predefined, using limits file) and dynamic limits.

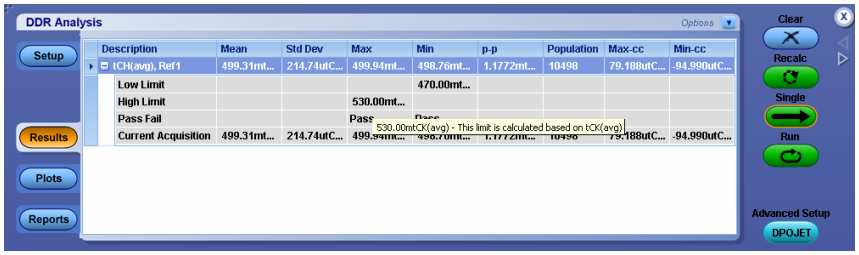
The concept of dynamic limits is explained taking an example of a measurement, tCH(avg):

- If the dynamic limits of a measurement depend on the result of other measurement(s) that have not yet been calculated, the limit field in the Results panel shows Derived... A tool tip displays the message:

  `This limit is calculated based on measurement tCK(avg).`

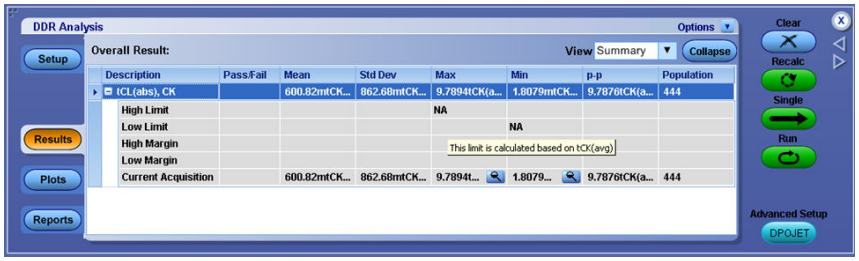


- On clicking Run/Single, the results are shown in the following figure.



- If there is an error in calculating dynamic limits or if the limits are not defined by the specification, the limit text field displayed NA. A tool tip displays the message:

  `This limit is calculated based on measurement tCK(avg).`



Log messages

Dynamic limit failure:

1. The limits for measurement is not defined in the JEDEC specification.
2. The limits for measurement cannot be computed due to unavailability of dependent measurement results.

References

Dynamic Limits for DDR Measurements

Dynamic Limits for DDR2 Measurements

Dynamic Limits for DDR3 Measurements

Dynamic Limits for DDR3L Measurements

Dynamic Limits for DDR4 Measurements

Dynamic Limits for LPDDR Measurements

Dynamic Limits for LPDDR2 Measurements

Dynamic Limits for LPDDR4 Measurements

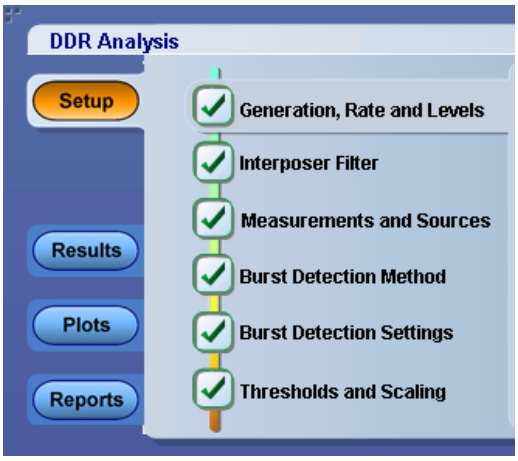
Dynamic Limits for LPDDR4X Measurements

Setting up DDR for analysis

About DDR analysis

The DDR Analysis window allows you to select various standards and to set up and run a pre-configured measurement either through the DDRA or the DPOJET application.

Select **Analyze > DDR Analysis** to open the DDRA application.



The Setup panel in DDR Analysis application includes the following steps:

Generation, Rate and Levels

Interposer Filter

Measurements and Sources

Burst Detection Method

Burst Detection Settings

Thresholds and Scaling

Note: Use the Next/Prev buttons or click directly on the step numbers to move through the steps in the DDR Analysis. The steps for which configuration is complete are denoted.

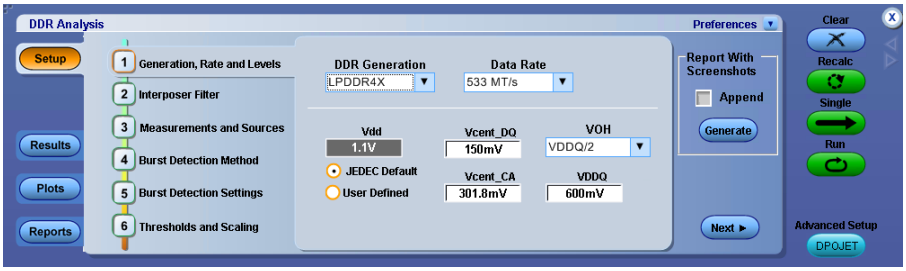
The Setup panel displays hints to help you understand the configuration options wherever applicable.

You can run a set of measurement in either of the two ways:

- Click **Run** to start the acquisition sequence using the selected settings and to view the results in the DDRA window. This is the normal way to generate results.
- Click Advanced Setup DPOJET to move to the DPOJET application where you can add or modify measurements before sequencing. For more details, refer to the *DPOJET* help.
- Click DDR Analysis DDRA in the DPOJET application to return to the DDRA window. Alternatively, you can reselect **Analyze >DDR Analysis** from the menu bar.

Step 1: Generation rate and levels

Select the DDR generation, data rate, and the voltage levels (if required).



1. Select the generation from the DDR Generation drop-down list.
2. Select the data rate from the Data Rate drop-down list.

   On selecting **Custom**, an edit box allows you to enter the value using the virtual keypad. Limit files are not defined for custom data rates for pass/fail status and as a result, the application displays a hint at the bottom of the screen:

   ```
   Please provide a limits file under Jitter and Eye Analysis > Limits.
   ```

   Note: Selecting **Auto** data rates in ASM (under Search > DDR Read or DDR Write) changes the data rate to None in DDRA.
3. Set the voltage levels:
   - If you select JEDEC defaults, the application uses the nominal voltage levels according to the JEDEC specification. The Vdd field is not editable.
   - If you select User Defined, enter the Vdd or Vref voltage values using the virtual keypad.

     Note: The Vcent_DQ and Vcent_CA voltage values are only available for DDR4, LPDDR4, and LPDDR4X. For these generations, the external Vref is not available. Vcent is similar to the traditional Vref parameter but takes into account the actual reference voltage used inside the DRAM is adjusted during write training and is not physically visible at the balls of the DRAM.
4. (Optional) Click **View** to view the Vih and Vil values calculated automatically based on the Vref value. To manually adjust the reference levels, go to *Step6* of DDRA or use the DPOJET source configuration panel.

Vdd	Vdd is the supply voltage for each DDR standard. Vdd is based on DDR generation.

Table continued…

Vref	Vref is the reference voltage for each DDR standard. Vref is calculated using Vdd, which is based on DDR generation. In most cases, Vref=0.5 Vdd.
Vcent_DQ	Vcent_DQ is the voltage at which the cumulative eye of the pin DQx is widest.
Vcent_CA	Vcent_CA is the voltage at which the cumulative eye of the pin CAx is widest.
VOH	VOH is the output voltage swing for LPDDR4 and LPDDR4X. In LPDDR4, VOH = V_{DDQ}/2.5 or V_{DDQ}/3 (*Default*) In LPDDR4X, VOH = V_{DDQ}/1.66 or V_{DDQ}/2 (*Default*)
VDDQ	VDDQ is the voltage internally applied to the I/O buffer. In LPDDR4X, VDDQ is set to the nominal voltage of 0.6 V. In other generations, VDDQ is set to VDD The following table lists the minimum and maximum values of Vdd, Vref, Vcent_DQ, and Vcent_CA in the User Defined mode for all DDR generations:

		DDR [1]	DDR2	DDR3	DDR3L	DDR4	LPDDR	LPDDR2	LPDDR3	LPDDR4	LPDDR4X	GDDR3	GDDR5
Vdd	Default	2.5V	1.8V	1.5V	1.35V	1.2V	1.8V	1.2V	1.2V	1.1V	1.1V	1.8 V	1.5V
	Range	-6 to 6V											
Vref	Default	1.25V	900mV	750mV	675mV		900mV	600mV	600mV			900mV	750mV
	Range	-6 to 6V					-6 to 6V					-6 to 6V	
Vcent_DQ	Default					850mV				201.5 mV	150mV		
	Range					-2V to 2V				0V to 2.5V			
Vcent_CA	Default					600mV				191.5 mV	301.8 mV		
	Range					-2V to 2V				0V to 2.5V			
VDDQ	Default										600mV		
	Range										0V to 5V		
VOH	Default									VDDQ/3	VDDQ/2		
	Options	For LPDDR4 VOH = { VDDQ/3, VDDQ/2.5 } For LPDDR4X VOH = { VDDQ/2, VDDQ/1.66 }											

Vdd and Vref

The configured values of Vdd and Vref are used to calculate $V_{IH(ac)}$min, $V_{IH(dc)}$min, $V_{IL(dc)}$max, and $V_{IL(ac)}$max which are applied on the input signal. These levels are further used for calculating Setup and Hold measurements.

For DDR2, the relationship between Vdd and Vref is as shown in the following tables:

[1] DDR 400 MT/s has Vdd value set to 2.6 V and Vref Value set to 1.3 V

Table 3: Input DC logic level

Symbol	Parameter	Min	Max	Units
$V_{IH(dc)}$	DC input logic high	Vref+0.125	NA	V
$V_{IL(dc)}$	DC input logic low	–0.3	Vref–0.125	V

Table 4: Input AC logic level

Symbol	Parameter	DDR2–400, DDR2–533		DDR2–667, DDR2–800		Units
		Min	**Max**	**Min**	**Max**	
$V_{IH(ac)}$	AC input logic high	Vref+0.250	NA	Vref+0.200	NA	V
$V_{IL(ac)}$	AC input logic low	NA	Vref–0.250	–	Vref+0.200	V

Note: Similar reference voltage levels are defined for the DDR3 standard.

Speed Bins

For each DDR standard, the DDRA application automatically applies limits appropriate for the standard data rates without speed bins. Limit values are different for different speed bins. If you want to test according to a speed bin, you must manually configure the limit values from within DPOJET by manually overriding the limit file before running the measurements. For more details, refer to *Limits* in the *DPOJET* help.

Vih

Vih is the input logic HIGH voltage.

Vil

Vil is the input logic LOW voltage.

Step 2: Interposer filter

Allows you to select and apply the interposer type for each of the sources. Filter.xml file is available at `C:\Users\Public\Filters`. This file can be edited to add different interposer types. The absolute filter path for each source can be specified. You can specify filter files either for all the available sources or only to a subset of sources. Select the appropriate interposer de-embedding filter files before selecting the measurements. It is recommended to do the horizontal autoset before applying any interposer filter files.

When interposer filters are applied, MATH cannot be used as the measurement source in Step 3. It is recommended to manually clear all Math expressions before applying any interposer filters through DDRA. The filter file is applied when the scope acquisition sample rate is supported in the filter file. Math channels get enabled only if the scope sampling rate matches with the sampling rate of the de-embedding filter; otherwise, Math will not be enabled and measurements will not be executed.

Note: The fields and options on the Interposer filter tab appears based on the type of generation selected. The DDRA supports the de-embedding of interposers with live signals only.

Filter types

- **None**: Select if you do not to want to apply filter files. This option is selected by default.
- **Direct Attached**: Select to attach pre-defined filter files.
- **User Defined**: Select to define a pre-defined filter files. If you do not define at least one filter for a source, then after clicking the **Close** button, the Interposer selection defaults to None.

Note: Interposer types such as None, Direct Attached, and User Defined are embedded in the application.

You can add additional filter files by adding the filter file name to the Filter.xml file. Once you update the XML file, restart the TekScope to apply the changes. The names you added are now referenced in the Interposer filter type drop-down list.

Note: If filter files do not exist or there is any typo in entering the path, the application displays a message `Filter File does not exist for <source name> in the path specified`. The list of sources for which the filter files are not found will be listed.

Edit button: Opens the Filter.xml file for editing.

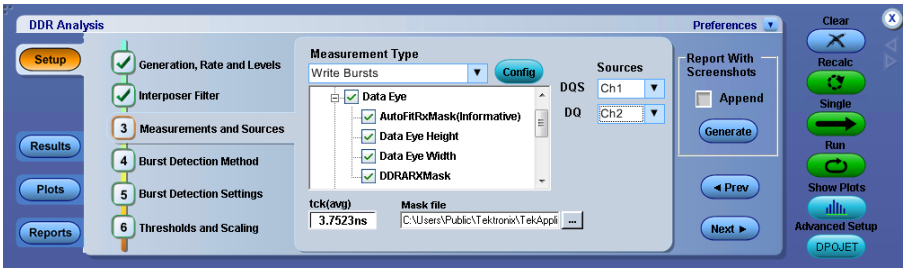
User define filter path

When you select User Defined from the drop-down list, User Defined text is auto populated on the image box .Click the image box to view the User Defined Filter Path dialog box, and then select different filer files for each source by clicking the **Browse** button. You can remove the selected filter file path by clicking the **Clear** button or click the **Clear All** button to clear all the filer paths at once.

Note: The source displayed in User Defined Filter Path dialog box shall be enabled or disabled based on selected generation. Filter files can be selected for subset or all of the available sources. The Filters.xml file is located at `C:\Users\Public\Filters` folder. The filter file can also be modified outside the application.

Step3: Measurements and sources

Select measurements and their corresponding *Sources* in this step. Measurement availability depends on the selected DDR standard. Select the **Measurement Type** (Read Bursts, Write Bursts, Clock(Diff), Clock(Single Ended), DQS(Single Ended, Write), DQS(Single Ended, Read), Address/Command, Overshoot and Undershoot, WCK(Single Ended), WCK(Diff), Refresh, Power Down, Active, Precharge) from the drop-down list. Power Down, Active, Precharge, Refresh types are available only on MSO models. A message prompts you to select one or more measurements before moving to the next step.



Measurement Type Reference Levels

The voltage reference levels for each measurement are automatically set to be consistent with JEDEC guidelines unless they are manually overridden. In cases where none of the chosen measurements have any applicable guidelines or manually set levels, DDRA will automatically choose reference levels based on the signal's maximum and minimum levels. DDRA displays a hint if both Single Ended DQS and Differential DQS measurements are selected at the same time, and measurements made with this configuration may not be accurate due to conflicting ref level requirements. When two or

more measurements are selected in different sub-node categories under a Measurement Type, the following precedence is set for measurement ref levels:

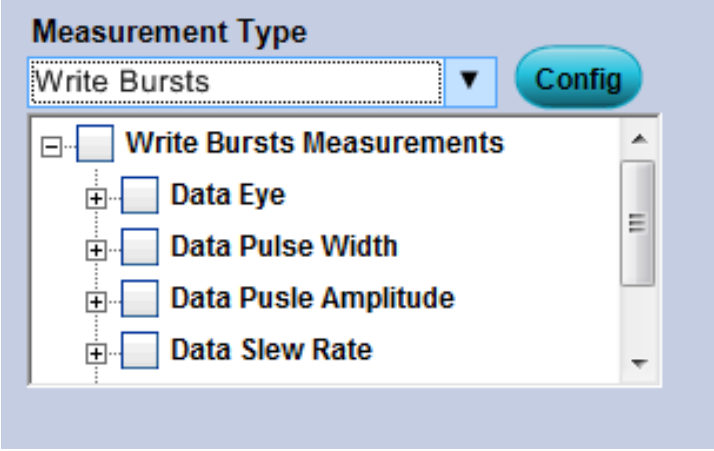
- Slew Rate ref levels
- Single Ended specific ref levels
- Differential specific ref levels

For Example, when Eye Width measurement is selected along with Differential DQS or Single Ended DQS or Slew Rate measurements, Eye measurement may not produce the expected results. This is because the actual mid level needed by Eye Width gets overwritten with SE levels and hence produces no results.

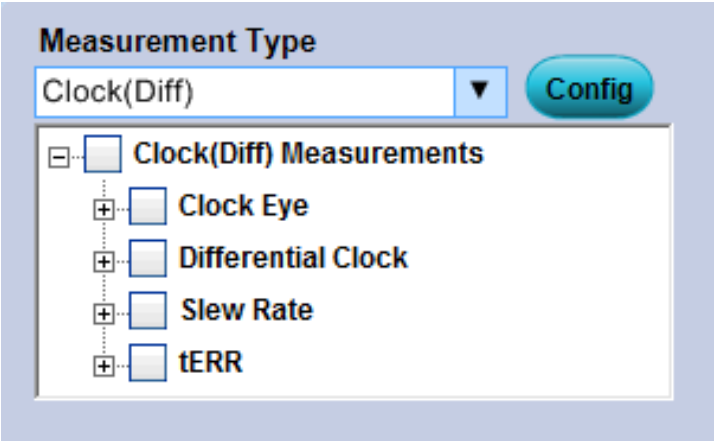
Tree Structure Flow

The measurement tree structure is as follows:

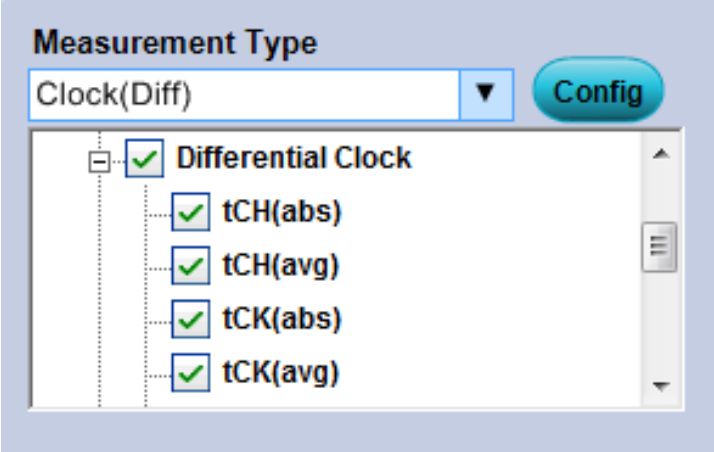
- The tree structure displays only those measurements appropriate for the selected measurement type.



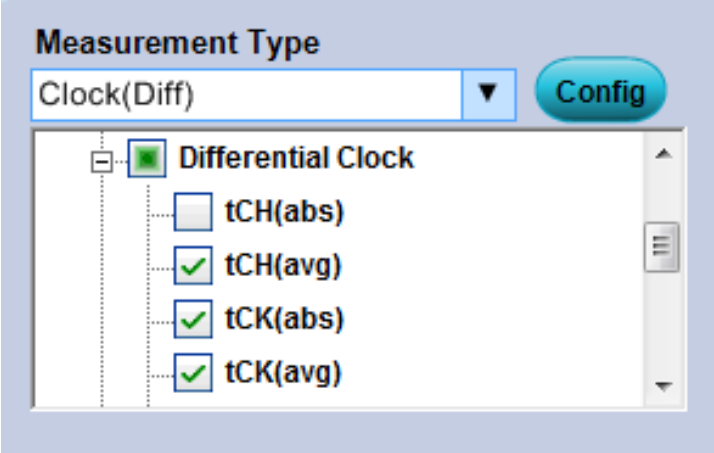
- All generations display both parent and nested elements under measurement type as shown.



- Click ⊞ to expand and show the elements within the parent element.
- Click ⊟ to collapse and hide the elements within the parent element.
- Selecting the parent check box, selects all the children elements. Selecting all the children elements, selects the parent element.



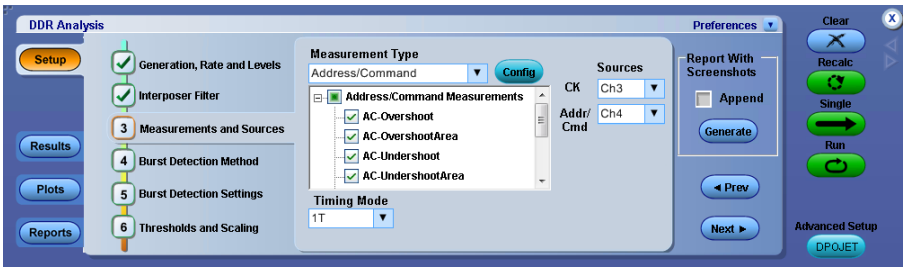
- Clearing the parent check box clears all the children elements.
- When the children include both checked and unchecked elements, the parent element becomes highlighted as shown:



Note: If you move to the next step without selecting any measurements, the application displays the message, `Please select measurements in Step3.`

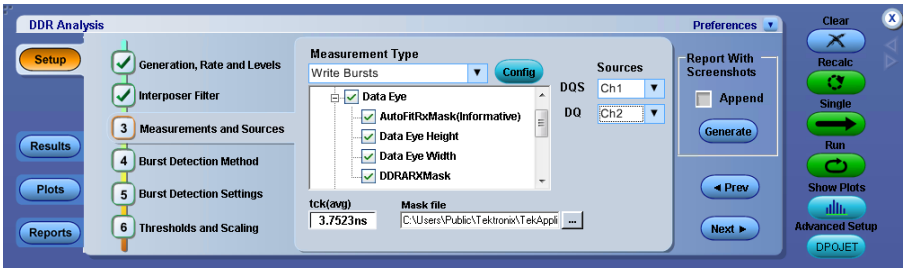
Timing Mode

Select either 1T or 2T depending on memory mode in which DUT are operating. Timing Mode is applicable for DDR3, DDR3L, DDR4 generation Address/Command's Setup and hold measurements.



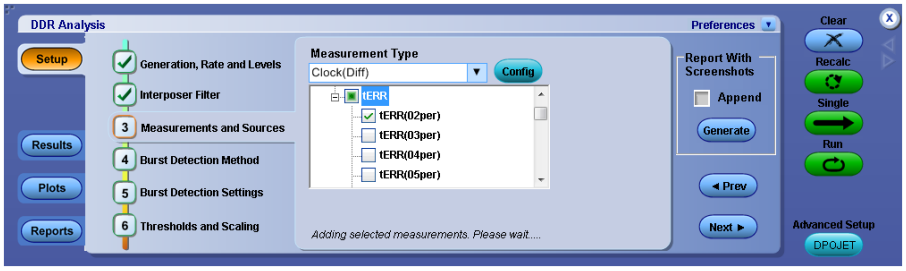
Mask Margin Measurement

You can specify a custom mask file using the Mask file control. The Mask file control allows you to change mask width, mask height, and mask position. When Mask margin measurement is selected, the application will update the default mask file depending on the data rate selected. You should not modify the default mask files.



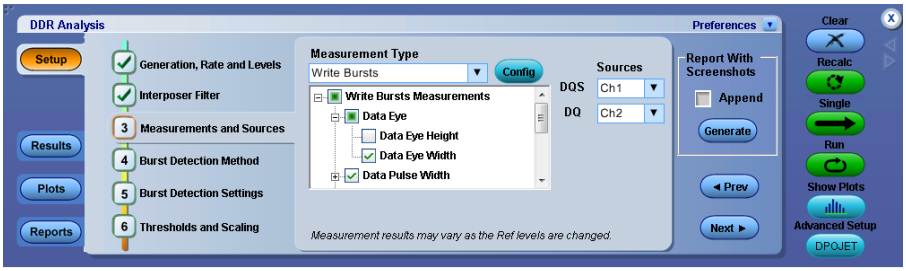
Timing error (tERR) measurements

Timing error measurements such as tERR(02per), tERR(03per), tERR(09per) until tERR(50per) are grouped together and included as a nested element (tERR) under the parent element, Clock(Diff)measurements. Selecting tERR selects all the timing error measurements.



Sources

Select a measurement to view the sources available for the measurement. The sources are mutually exclusive. For each required signal, select the appropriate source. A tool tip displays the required sources for the selected measurement at the nodes of the measurement tree. A maximum of four analog sources are available at a time.



Note: If the same channels are used for DQ/DQS/Clock sources (Example: DQ=Ch1, DQS=Ch1), the application displays a hint `Cannot use the same waveform for different sources`. If Live and Ref channels are used together (Example: Ch1 for DQS and Ref2 for DQ), the application displays a hint `Cannot use Live and Ref waveforms together.`

Reference

Hints

DDR Measurement Sources

DDR2 Measurement Sources

DDR3/DDR3L Measurement Sources

DDR4 Measurement Sources

GDDR5 Measurement Sources

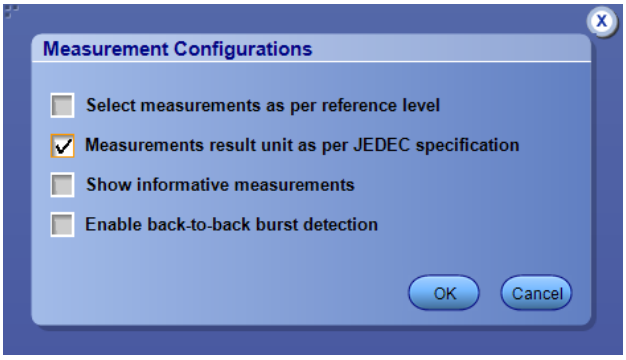
LPDDR Measurement Sources

LPDDR2 Measurement Sources

LPDDR3 Measurement Sources

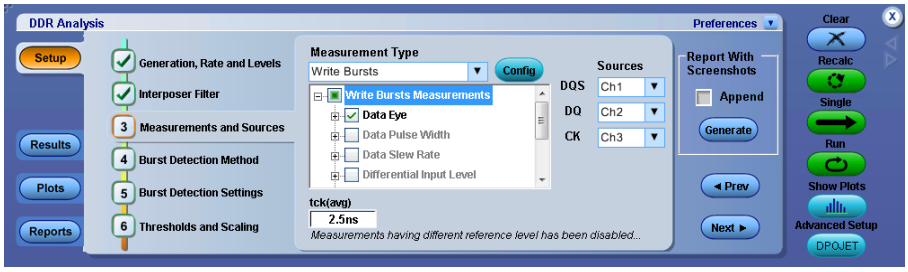
Measurement configurations

Clicking the **Config** button opens the Measurement Configurations dialog box, where you can configure various measurement settings.



Available options:

- **Select measurements as per reference level**: Option to select only those measurements which have the common sources/reference levels. The selected measurements are cleared when this option is toggled. By default, this option is disabled. Selecting this option automates the selection of measurements which have common sources/reference levels under a group and disables other measurements in that group whose sources/reference levels are different.



DDR3 sources/reference levels

The above concept is explained in the following table by taking an example of a measurement, Data Eye Height, of DDR3 generation.

Table 5: Common source and reference levels of Data Eye Height measurement

Generation	Measurement type	Measurement		Sources			Reference levels	
DDR3	Write Burst Measurement		Enabled	Disabled	DQS	DQ	Percentage	Absolute
		Write Burst	Data Eye Height		Ch1	Ch2	Ch1 Ch2	
			Data Eye Width		Ch1	Ch2	Ch1 Ch2	
		Data Plus Width		tDIPW-High	Ch1	Ch2		Ch2
				tDIPW-Low	Ch1	Ch2		Ch2
		Data Slew Rate		Slew Rate-Hold-Fall(DQ)	Ch1	Ch2		Ch2
				Slew Rate-Hold-Rise(DQ)	Ch1	Ch2		Ch2
				Slew Rate-Setup-Fall(DQ)	Ch1	Ch2		Ch2
				Slew Rate-Setup-Rise(DQ)	Ch1	Ch2		Ch2
		Differential strobe	tDQSH		Ch1	Ch2	Ch1	
			tDQSL		Ch1	Ch2	Ch1	
			tDQSS-Diff		Ch1	Ch2	Ch1	
			tDSH-Diff		Ch1	Ch2	Ch1	
			tDSS-Diff		Ch1	Ch2	Ch1	
			tDVAC(DQS)		Ch1	Ch2	Ch1	
			tWPRE		Ch1	Ch2	Ch1	
		Differential Input Level		VIHdiff(AC)	Ch1	Ch2		Ch1
				VILdiff(AC)	Ch1	Ch2		Ch1

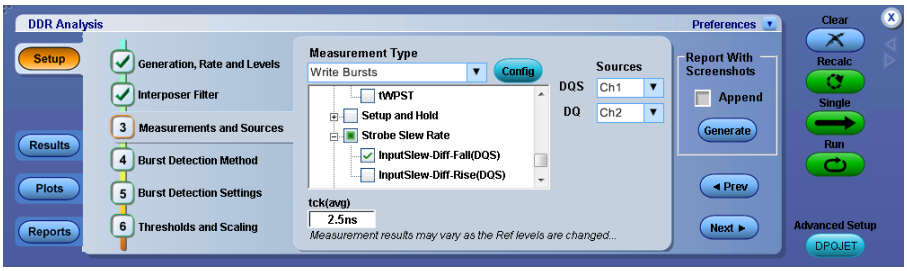
Select DDR3 generation, and then select Write Burst measurement group and based on your selection, the application, by default, considers the sources and reference levels of Data Eye Height measurement, as it falls first in the Write

Bursts measurement group and compare its sources/reference levels with that of other measurements which falls under the Write Burst measurement group.

In the above table, it is shown that the Write Burst measurements and Differential strobe measurements are enabled because the sources and reference levels of Data Eye Height measurement and Differential strobe measurements are common, that is, the source of Data Eye Height and Differential strobe measurement are Ch1 and reference levels are in Percentage. On the other hand, the measurements, Data Plus Width, Data Slew Rate, and Differential Input Level are disabled because their sources and reference levels are not common with that of Data Eye Height measurement.

Effect of not selecting Select Measurements as per reference level option

When you select two or more measurements in a group, the measurement result varies as some measurements have different sources/reference levels as compared to others and selecting all of them will affect the outcome of measurement result. When you select two or more measurements under a group, the application, by default, considers the sources and reference levels of the first measurement selected under that group only. The application compares the sources and reference levels of the first measurement with that of other measurements of that group and if it finds that there is any mismatch between the sources and reference levels of first measurement with that of other selected measurements in that group, it displays a message as `Measurement result may very as the Ref levels are changed`.



For example, first you select the InputSlew-Diff-Fall (DQS) and then select tWPRE from Write Burst measurement group. Here the application considers the sources and reference levels of tWPRE measurement for measurement results. As tWPRE measurement falls first in the Write Bursts measurement group, the application compares sources/reference levels of tWPRE with that of InputSlew-Diff-Fall (DQS). If there is a mismatch, the application displays a message as `Measurement result may very as the Ref levels are changed`.

Now, you have to manually verify and clear the selection of measurements of which sources and reference levels are not common with that of tWPRE measurement.

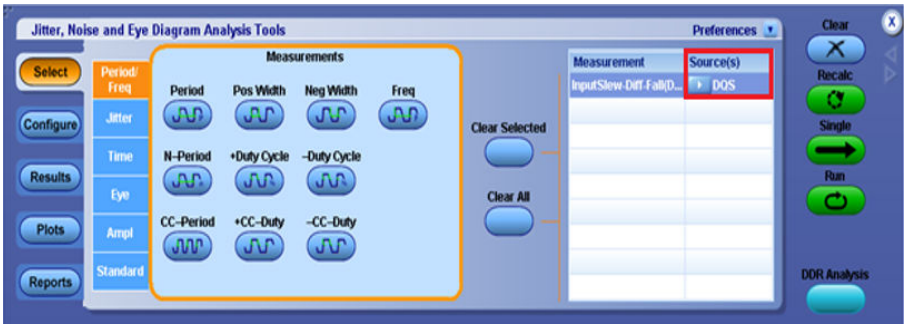
Viewing the sources and reference levels

To view and verify the sources and reference levels of each measurement with that of tWPRE measurement, do the following:

1. First, clear all the selected measurements, if you have selected them earlier from the DDR application, and then select only tWPRE measurement.
2. Click 

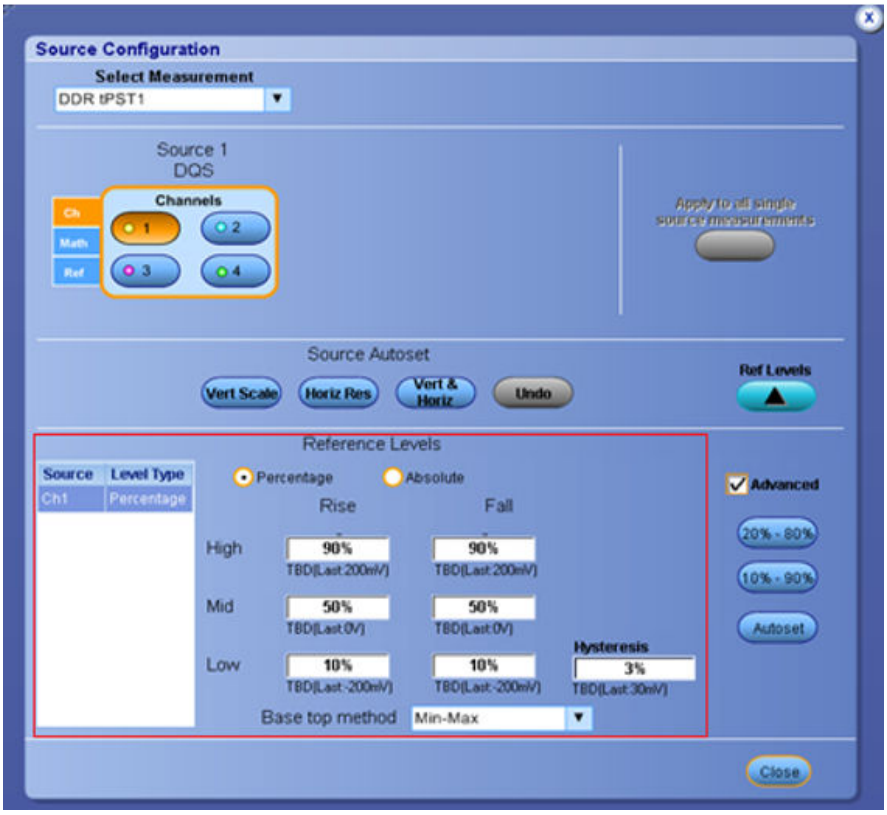
button on the DDR application.

   The DPOJET window appears.



3. On the DPOJET window, click  button.

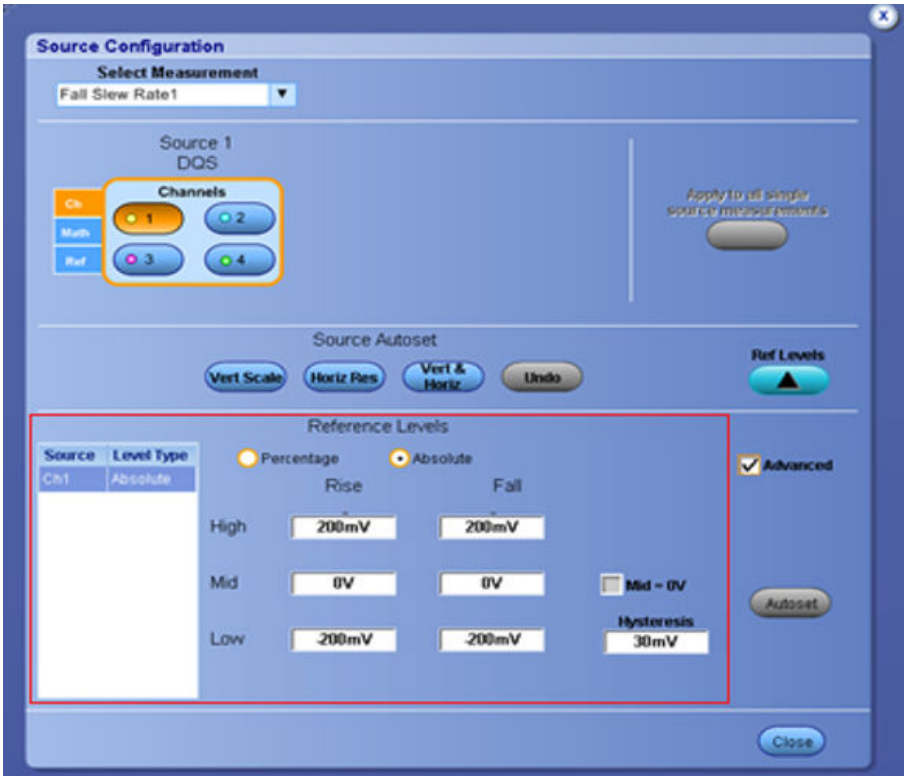
   The Source Configuration dialog box appears, showing the sources /reference levels of tWPRE measurement.



   The Source Configuration dialog box shows the source of tWPRE measurement as Ch1 and reference levels (Level Type) in percentage.

4. Navigate to the DDR application and clear the selection of tWPRE measurement from the group, and then select the InputSlew-Diff-Fall (DQS).

   Sources/reference levels of InputSlew-Diff-Fall (DQS)



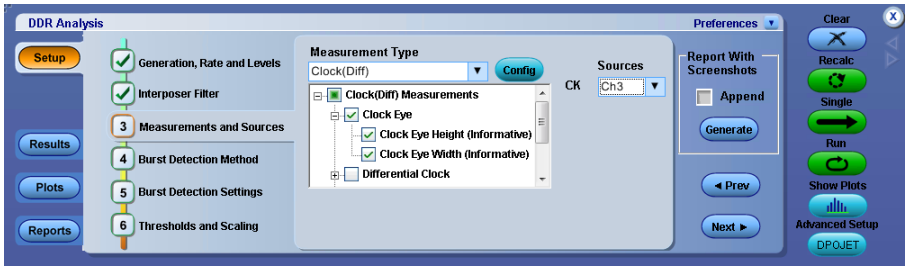
5. Follow the above steps to verify the source and reference level of InputSlew-Diff-Fall (DQS).

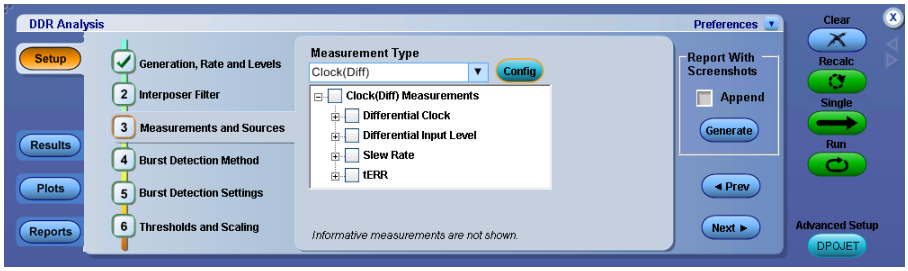
   The Source Configuration dialog box shows the source of InputSlew-Diff-Fall (DQS) as Ch1 and reference level (Level Type) as Absolute. This means that the sources are common but the reference levels (Level Type) of both measurements are different. As reference levels are not common, the measurement result will very. To pass the results, clear the selection of InputSlew-Diff-Fall (DQS) form the group. Sometimes, the values (Rise and fall) will be different (not common) then also the measurement result will vary.

   Note: The same process applies when you select more than two or all measurements in a group or from other groups.

- **Measurements result unit as per JEDEC specification**: Option to configure the measurements result unit as per JEDEC specification. When disabled, time based measurement results will be in seconds. This option is enabled by default.
- **Show informative measurements**: Select this option to show and hide informative measurements in the measurement group as shown.

  For example, select generation as DDR3, and then select Clock (Diff) measurement from the Measurement Type drop-down. The Informative measurements which are in Clock Eye group gets displayed when you select this option as shown below.





When you clear this option, a message is displayed as `Informative measurement are not shown.`

Following table shows the list of informative measurements.

Table 6: Informative measurements

Generation	Measurement Type	Measurement
DDR	Clock(Diff)	Clock Eye Height (Informative)
		Clock Eye Width (Informative)
	DQS(Single Ended, Write)	tDSH(DQS)(Informative)
		tDSS(DQS)(Informative)
		tDH(DQS)(Informative)
		tDS(DQS)(Informative)
		Vix(ac)DQS(Informative)
DDR2	Address/Command	AddrCmd Eye Width(Informative)
	Clock(Diff)	Clock Eye Height (Informative)
		Clock Eye Width (Informative)
	DQS(Single Ended, Read)	tDQSQ(DQS)(Informative)
	DQS(Single Ended, Write)	tDQSS(DQS)(Informative)
		tDSH(DQS)(Informative)
		tDSS(DQS)(Informative)
		tDH(base)DQS(Informative)
		tDH(derated)DQS(Informative)
		tDS(base)DQS(Informative)
		tDS(derated)DQS(Informative)

Table continued…

Generation	Measurement Type	Measurement
DDR3	Address/Command	AddrCmd Eye Width(Informative)
		tIH(max-derated)(Informative)
		tIH(min-derated)(Informative)
		tIS(max-derated)(Informative)
		tIS(min-derated)(Informative)
	Clock(Diff)	Clock Eye Height (Informative)
		Clock Eye Width (Informative)
	DQS(Single Ended, Read)	tDQSS(DQS)(Informative)
		tDSH(DQS)(Informative)
		tDSS(DQS)(Informative)
	DQS(Single Ended, Write)	tDQSS(DQS)(Informative)
		tDSH(DQS)(Informative)
		tDSS(DQS)(Informative)
	Write Bursts	tDH-Diff(max-derated)(Informative)
		tDH-Diff(min-derated)(Informative)
		tDS-Diff(max-derated)(Informative)
		tDS-Diff(min-derated)(Informative)
DDR3L	Address/Command	AddrCmd Eye Width(Informative)
		tIH(max-derated)(Informative)
		tIH(min-derated)(Informative)
		tIS(max-derated)(Informative)
		tIS(min-derated)(Informative)
	Clock(Diff)	Clock Eye Height (Informative)
		Clock Eye Width (Informative)
	DQS(Single Ended, Read)	tDQSS(DQS)(Informative)
		tDSH(DQS)(Informative)
		tDSS(DQS)(Informative)
	DQS(Single Ended, Write)	tDQSS(DQS)(Informative)
		tDSH(DQS)(Informative)
		tDSS(DQS)(Informative)
	Write Bursts	tDH-Diff(max-derated)(Informative)
		tDH-Diff(min-derated)(Informative)
		tDS-Diff(max-derated)(Informative)
		tDS-Diff(min-derated)(Informative)

Table continued…

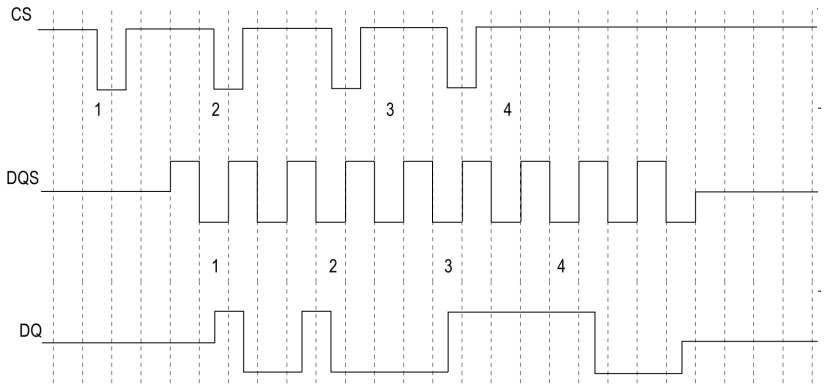
Generation	Measurement Type	Measurement
DDR4	Clock(Diff)	Clock Eye Height (Informative)
		Clock Eye Width (Informative)
		tJIT(duty) Informative
	DQS(Single Ended, Read)	VSEH(DQS#)(Informative)
		VSEH(DQS)(Informative)
		VSEL(DQS#)(Informative)
		VSEL(DQS)(Informative)
	DQS(Single Ended, Write)	VSEH(DQS#)(Informative)
		VSEH(DQS)(Informative)
		VSEL(DQS#)(Informative)
		VSEL(DQS)(Informative)
	Read Bursts	tDVAC(DQS)(Informative)
	Write Bursts	tDVAC(DQS)(Informative)
GDDR3	Clock(Diff)	Clock Eye Height (Informative)
		Clock Eye Width (Informative)
GDDR5	Clock(Diff)	Clock Eye Height (Informative)
		Clock Eye Width (Informative)
LPDDR	Clock(Diff)	Clock Eye Height (Informative)
		Clock Eye Width (Informative)
	DQS(Single Ended, Write)	tDSH(DQS)(Informative)
		tDSS(DQS)(Informative)
		tDH(DQS)(Informative)
		tDS(DQS)(Informative)
LPDDR2	Address/Command	tIH(max-derated)(Informative)
		tIH(min-derated)(Informative)
		tIS(max-derated)(Informative)
		tIS(min-derated)(Informative)
	Clock(Diff)	Clock Eye Height (Informative)
		Clock Eye Width (Informative)
	Write Bursts	tDH-Diff(max-derated)(Informative)
		tDH-Diff(min-derated)(Informative)
		tDS-Diff(max-derated)(Informative)
		tDS-Diff(min-derated)(Informative)
LPDDR3	Clock(Diff)	Clock Eye Height (Informative)
		Clock Eye Width (Informative)

Table continued…

Generation	Measurement Type	Measurement
LPDDR4 / LPDDR4X	Address/Command	AutoFitRxMask(Informative)
	Clock(Diff)	Clock Eye Height (Informative)
		Clock Eye Width (Informative)
		VIHdiff(AC) Informative
		VILdiff(AC) Informative
	Clock(Single Ended)	VSEH(CK#)(Informative)
		VSEH(CK)(Informative)
		VSEL(CK#)(Informative)
		VSEL(CK)(Informative)
	DQS(Single Ended, Write)	VSEH(AC)DQS#(Informative)
		VSEH(AC)DQS(Informative)
		VSEL(AC)DQS#(Informative)
		VSEL(AC)DQS(Informative)
	Write Bursts	AutoFitRxMask(Informative)
		VILdiff(AC) Informative
		VIHdiff(AC) Informative

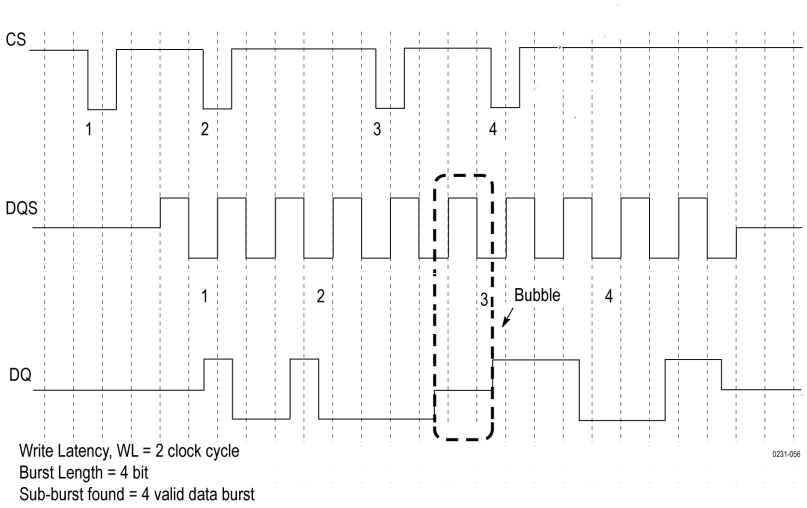
- **Enable back-to-back burst detection**: Identifying the start and end of the burst is particularly difficult to perform during a back-to-back burst, due to the missing preamble pattern in each sub bursts. In case of back-to-back bursts, the strobe seems like one continuous long burst with/without bubble states. Examples of the back-to-back data burst are shown in the following figures.

Note: The Back-to-Back Burst Detection method is applicable only for Chip Select, Latency + DQ/DQS Phase Alignment measurements.



Write Latency, WL = 2 clock cycle
Burst Length = 4 bit
Sub-burst found = 4 valid data burst

Both DQ/DQS Phase Alignment and Chip Select, Latency + DQ/DQS Phase Alignment burst detection methods identifies Read and Write bursts based on the preamble and the phase relation that exist between DQ and DQS. However, in case of back-to-back bursts, the preamble may or may not present for all the sub bursts. This makes it very difficult for the ASM algorithm to separately identify and mark all the sub bursts within a back-to-back burst.



The Chip Select signal is used to identify the bubble states during a back-to-back burst and to mark the valid start bit of each sub-burst within a continuous back-to-back burst. A few assumptions are used in this approach as follow:

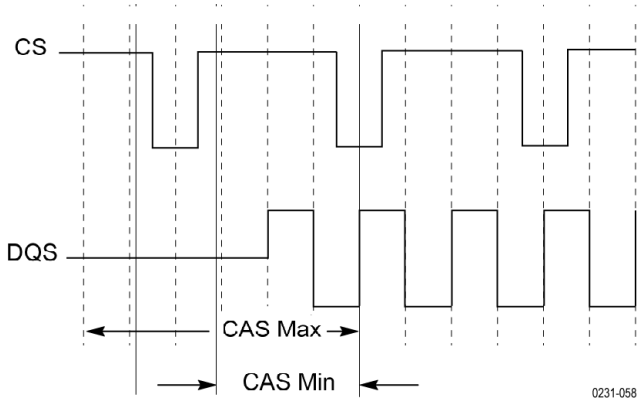
1. Back-to-back burst data are applicable for only one rank at a time, that is, all the sub-bursts in a back-to-back burst are only meant for one single rank/DIMM.
2. In a back-to-back burst, there will be only ONE bubble bit (if any) between any 2 consecutive sub-bursts.
3. All Chip Select transitions during a back-to-back burst, are related to either READ/WRITE data.

The below are the limitations of the algorithms:

1. Two bubble events is not supported.
2. The algorithm does not handle the conditions when another command (for example, PRECHARGE or REFRESH command) happens in the midst of back-to-back bursts. When that happens, the chip select signal is asserted for two clock cycles and therefore we cannot identify which of the two marks corresponds to the READ/WRITE command. In such cases, all the data bits from that point onwards will be ignore.
3. Since in a back-to-back burst, all sub-bursts might not contain the preamble and postamble, it is recommended not to execute measurements those are based on preamble and postamble region of the burst.
4. This feature is available only for DDR3, DDR3L and DDR4 generations.

How to configure CAS_min and CAS_Max

CAS_Max and CAS_min is measured from the CS transition corresponds to the READ/WRITE command to the driving edge of the strobe. Configure CAS_Max and CAS_min in a such a way that both the transitions of the CS signal lie in between. This is shown in the below diagrams.



Features

An option is provided in the Config panel (in Measurement and Sources panel) to enable or disable the back-to-back burst algorithm. By default, this option will be disabled.

On enabling this option, the burst detection method will automatically change to Chip select, Latency + DQ/DQS Phase Alignment. Similarly, either on generation change or on burst detection method change the back-to-back burst detection option will get disabled.

The back-to-back burst detection option is applicable only for Read Bursts, Write Bursts, DQS(Single Ended, Write) and DQS(Single Ended, Read) burst measurements.

Log messages

The following log messages are applicable for LPDDR4/LPDDR4X:

1. The computed tDQS2DQ value is -ve. Please enter the right tDQS2DQ value with UserDefined mode.

   This message is logged when tDQS2DQ mode is auto and the measured tDQS2DQ value is -ve. In this case user has to switch the tDQS2DQ mode to 'User defined' and manually key in the right tDQS2DQ value.
2. There is no Data transitions during the first bit. Please enter the right tDQS2DQ value with UserDefined mode.

   This message is logged when there is no DQ transition in the first bit of the burst. In such cases the algorithm assumes tDQS2DQ as half of the clock unit interval. So it is advised to switch the tDQS2DQ mode to 'User defined' and manually key in the right tDQS2DQ value.
3. There are no isolated bursts in the acquisition. Either increase the record length or change the isolated burst configuration.

   This message is logged when there are no isolated bursts in the acquisition. In this case either:

   a. Increase the record length which increases the possibility of acquiring a isolated burst.
   b. Change the Isolated burst configuration.
   c. Use a different burst identification method.
4. The configured postamble length may not be correct. Please check the configuration.

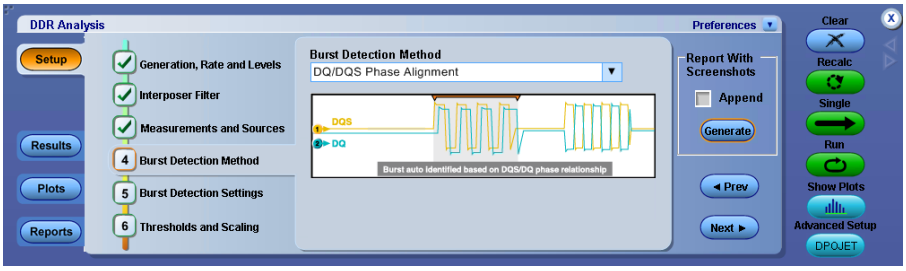
   This message is logged when the acquired isolated Write burst has two extra UIs compared to the configured isolated burst length.
5. The configured preamble type and/or postamble length may not be correct. Please check the configurations.

   This message is logged when the acquired isolated Read burst has two or four extra UIs compared to the configured isolated burst length.
6. Please configure the Burst Match(%) with a smaller value and try again.

   This message is logged when the configured Burst match is higher than any burst' association index in the acquisition. In this case it is advised to decrease the burst match value and try again.

Step 4: Burst detection method

Burst detection is based on the measurement type and generation, and is applicable only for Write Bursts, Read Bursts, DQS(Single Ended, Read), DQS(Single Ended, Write) and Overshoot and Undershoot measurement types.



The application supports the following burst detection methods for DPO/DSA/MSO oscilloscopes:

- *DQ/DQS Phase Alignment*
- *Chip Select, Latency + DQ/DQS Phase Alignment*
- *Logic State + Burst Latency* (Available only on MSO series of oscilloscopes)
- *Visual Search*
- *Preamble pattern matching* on page 34
- *Amplitude based* on page 36
- *Edge count based* on page 38

Note:

- The Preamble Pattern Matching, Amplitude Based, and Edge Count Based detection methods are applicable only to LPDDR4 and LPDDR4X. Click the **Config** button to display the Configuration panel. This option is available for both the DQ-DQS Phase Alignment and Chip Select Latency + DQ-DQS Phase Alignment methods. For Write Bursts and DQS (Single Ended, Write) group measurements, you can specify the tDQS2DQ by selecting User Defined. By default, this is set to Auto so that the ASM (Advanced Search and Mark) algorithm will calculate the tDQS2DQ and use that in burst marking. When User Defined is selected, the value you specify is used for burst marking.
- Current version of the application supports only write bursts having 2 clock cycle preamble.

Reference

Hints

Preamble pattern matching

This algorithm is based on finding the appropriate preamble patterns over the entire acquisition. Each burst's association index (similarity co-efficient) is compared with the user provided threshold to determine whether a burst is READ or WRITE. Available for LPDDR4/LPDDR4X Read Bursts and Write Bursts measurements.

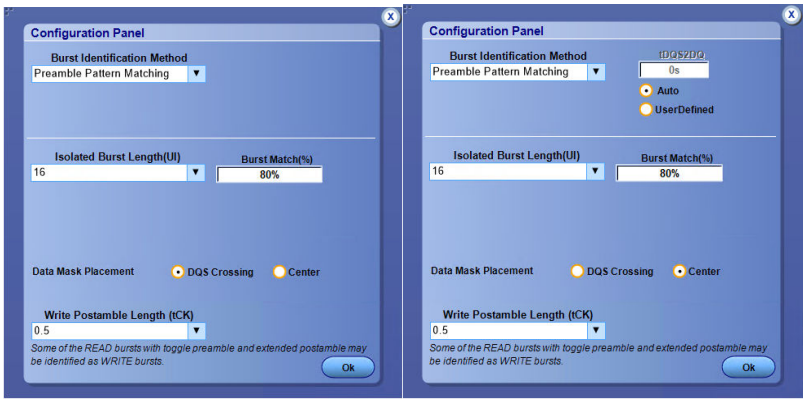


Figure 1: Configuration panel for Write Bursts measurements

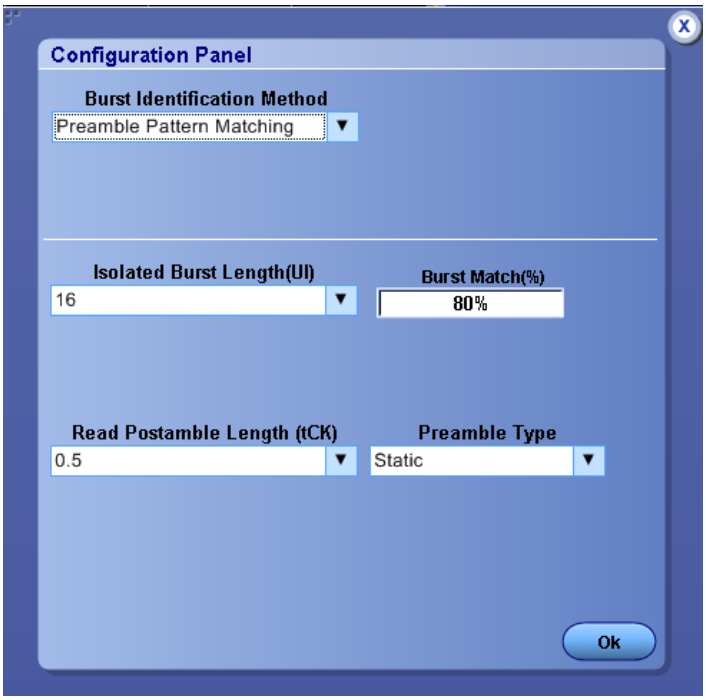


Figure 2: Configuration panel for Read Bursts measurements

Table 7: Configuration Parameters

Parameters	Description
Auto (Available only when **Data Mask Placement= Center**)	tDQS2DQ value is automatically set by the application.
User defined (Available only when **Data Mask Placement= Center**)	tDQS2DQ value can be edited.
Isolated Burst Length (UI)	Specifies the isolated burst length. Values could be 8, 16 or 32.

Table continued…

Parameters	Description
Burst Match(%)	Specifies the burst match with which the burst's association index will be compared. This parameter measures the similarity between READ and WRITE burst preambles.
Write Postamble Length (tCK)	Specifies the WRITE burst postamble length. This could be either 0.5 tCK or 1.5 tCK (extended postamble).
Read Postamble Length (tCK)	Specifies the READ burst postamble length. This could be either 0.5 tCK or 1.5 tCK (extended postamble).
Preamble Type	Specifies the READ burst preamble type as either Static or Toggle. **Note:** This option is applicable only for Read Bursts group measurements.
Data Mask Placement	Sets the 'Mask' position in LPDDR4 or LPDDR4X Write Burst measurement. • **DQS crossing**: Sets the mask position at the DQS Crossing. • **Center**: Sets the mask at the data center.

Limitations

- Needs at least one isolated burst in the acquisition.
- In some scenarios, the algorithm may not distinguish properly between WRITE bursts and READ bursts with toggle preamble and extended postamble.

Amplitude based

Select this method when there is a voltage difference between READ and WRITE burst peak-to-peak level.

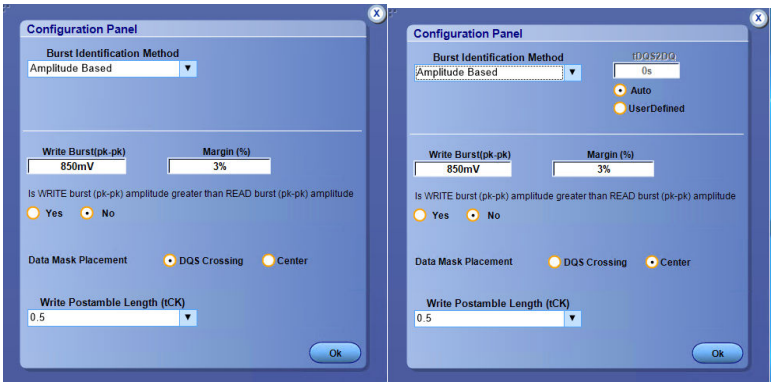


Figure 3: Configuration panel for Write Bursts or DQS (Single Ended, Write) measurements

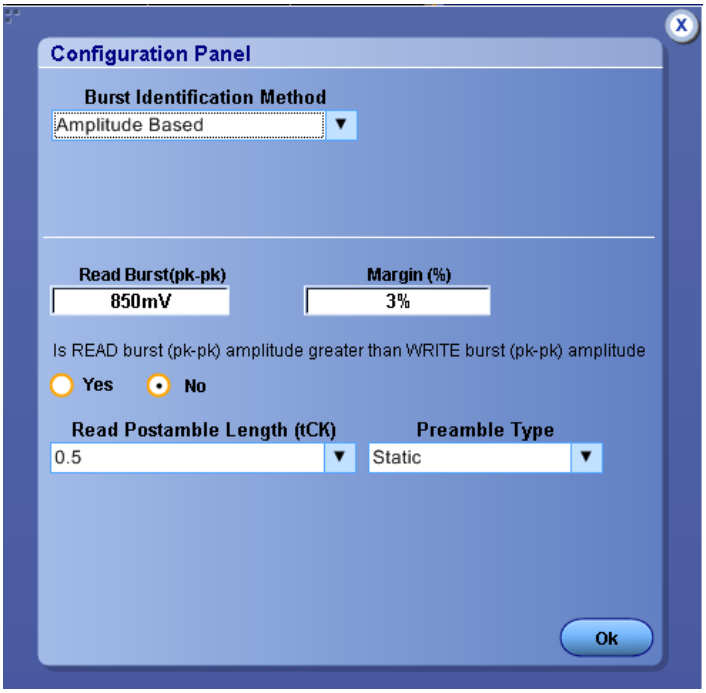


Figure 4: Configuration panel for Read Bursts or DQS (Single Ended, Read) measurements

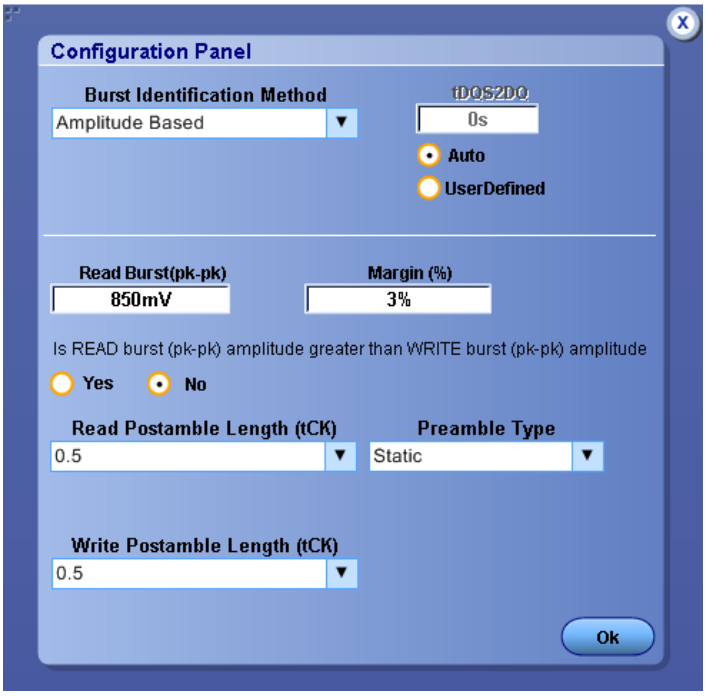


Figure 5: Configuration panel for Overshoot/Undershoot measurements

Table 8: Configuration Parameters

Parameters	Description
Auto (Available only when **Data Mask Placement= Center**)	tDQS2DQ value is automatically set by the application.
User defined (Available only when **Data Mask Placement= Center**)	tDQS2DQ value can be edited.
Read Burst(pk-pk)	Specifies the DQS (pk-pk) voltage level of READ bursts.
Write Burst(pk-pk)	Specifies the DQS (pk-pk) voltage level of WRITE bursts.
Margin (%)	Specifies the voltage variance allowed in terms of percentage of peak-peak voltage.
Is READ burst (pk-pk) amplitude greater than WRITE burst (pk-pk) amplitude	Select Yes or No.
Is WRITE burst (pk-pk) amplitude greater than READ burst (pk-pk) amplitude	Select Yes or No.
Read/ Write Postamble Length (tCK)- Applicable for Overshoot/Undershoot measurements.	Specifies the READ/WRITE burst postamble length. This could be either 0.5 tCK or 1.5 tCK (extended postamble).
Preamble Type	Specifies the READ burst preamble type as either Static or Toggle. **Note:** This option is applicable only for Read Bursts and Overshoot/ Undershoot group measurements.
Data Mask Placement	Sets the 'Mask' position in LPDDR4 or LPDDR4X Write Burst measurement. • **DQS crossing**: Sets the mask position at the DQS Crossing. • **Center**: Sets the mask at the data center.

Edge count based

This algorithm identifies a READ or WRITE burst based on the number of strobe edges present in each burst. This algorithm is available only for the DQS (Single Ended, Write) and Overshoot/Undershot measurements for LPDDR4/ LPDDR4X.

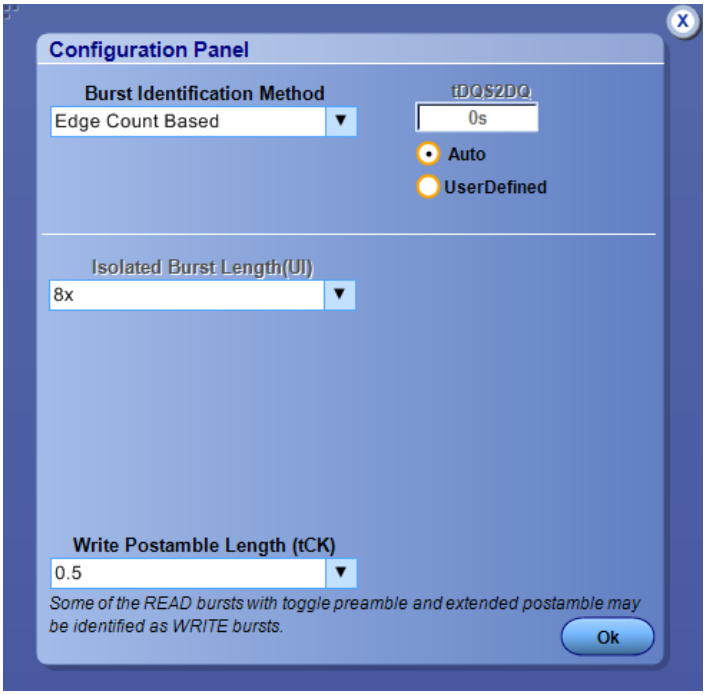


Figure 6: Configuration panel for DQS (Single Ended, Write) measurements

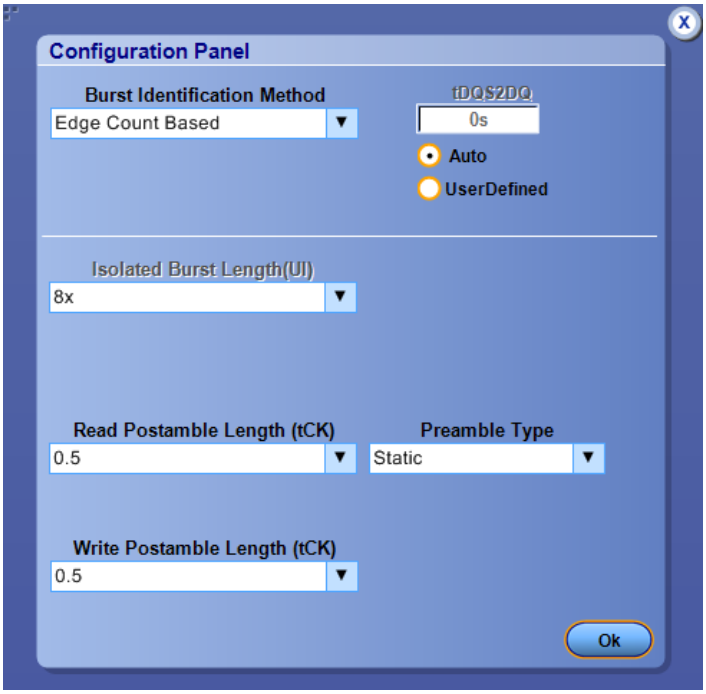


Figure 7: Configuration panel for Overshoot/Undershoot measurements

Table 9: Configuration Parameters

Parameters	Description
Auto	tDQS2DQ value is automatically set by the application.

Table continued…

Parameters	Description
User defined	tDQS2DQ value can be edited.
Read/Write Postamble Length (tCK)-Applicable for LPDDR4/4X measurements.	Specifies the READ/WRITE burst postamble length. This could be either 0.5 tCK or 1.5 tCK (extended postamble).
Preamble Type	Specifies the READ burst preamble type as either Static or Toggle. **Note:** This option is applicable only for Read burst and Overshoot/Undershoot group measurements.

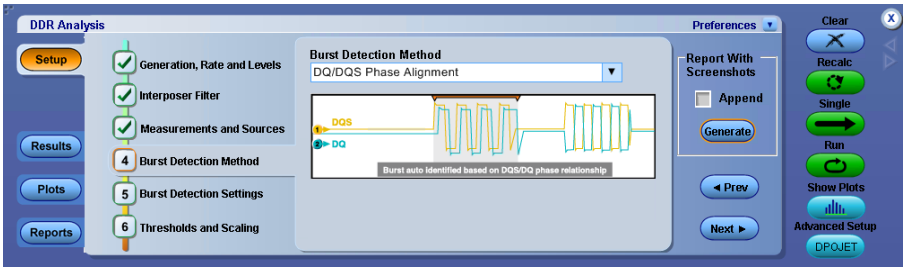
Step 5: Burst detection settings

Displays the settings based on the burst detection method:

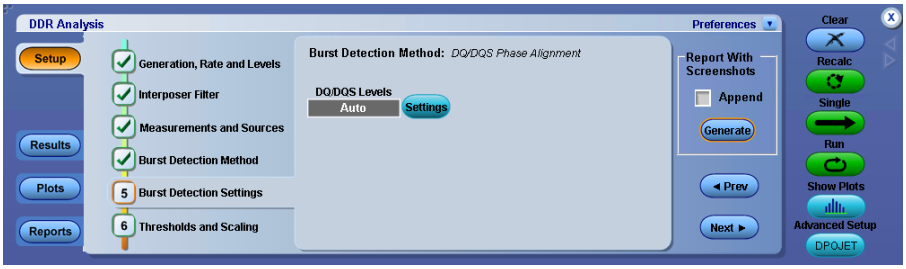
- *DQ/DQS Phase Alignment*
- *Chip Select, Latency+ DQ/DQS Phase Alignment*
- *Logic State + Burst Latency* (Available only for MSO series of oscilloscopes)
- *Visual Search*

DQ/DQS phase alignment

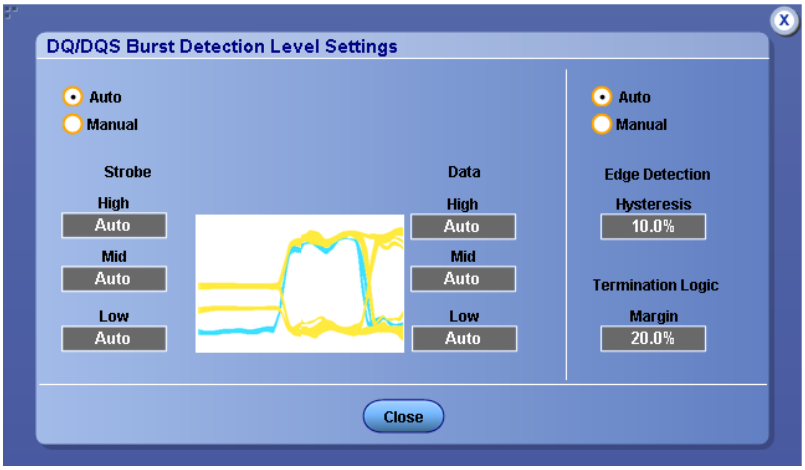
Select the burst detection method as shown.



The DQ/DQS levels indicator shows Auto when both Strobe/Data and Edge detection hysteresis are set to Auto. If one of the options is Manual, then the DQ/DQS levels shows as Manual. Click **Settings** tab to set advanced burst detection parameters.



The Burst Detection Settings panel controls how data bursts are identified within a waveform that includes tri-state levels. For appropriately-probed signals with good signal fidelity, no adjustment to the default values should be required. For signals with poor fidelity or unusual properties, burst detection can be improved by switching to Manual control and adjusting the detection levels.

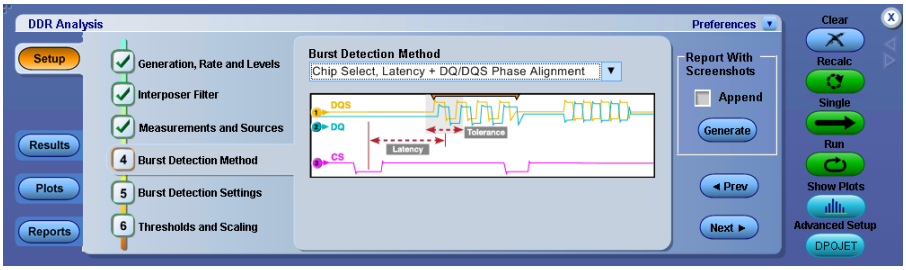


Note: The High/Mid/Low levels used for burst detection have no relationship to the reference levels used for measurement points. The measurement thresholds are defined in *Step6* .

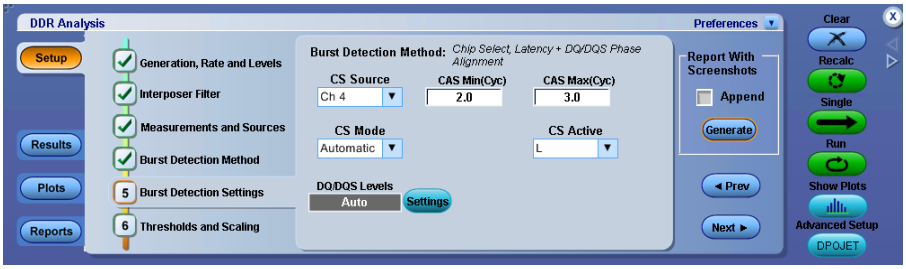
1. Select the type of burst detection level for the search.
   - If you select **Auto**, the application calculates these levels for you. It is recommended unless you find that manual levels are necessary for reliable detection.
   - If you select **Manual**, enter both the Strobe and Data reference levels for the signal (High, Mid, and Low). As you adjust the detection levels, observe the search-and-mark sprites that appear above the waveform. These sprites are dynamically updated as you adjust the levels, helping you to identify levels that properly delimit the selected burst type.
2. These settings need not be changed in most cases:
   - **Edge Detection Hysteresis**: This control configures the internal edge finder's hysteresis band which is used to detect read or write bursts. In the event of noisy inputs, it can be increased to correct marks which may be larger than appropriate.
   - **Termination Logic Margin**: This value can be increased to help in terminating marks on back-to-back writes in cases where otherwise a continuous strobe would cause a write-mark to merge two back-to-back writes.

Chip select latency + DQ/DQS phase alignment

This method identifies Read/Write burst from particular memory rank based on the configured CS signal.



Configure CAS Min(Cyc), CAS Max(Cyc), CS Active and CS Mode as needed.



CS Source

CS Source is used as a logic input to select read or write bursts from particular memory rank. When a chip-select signal source other than none is specified, reads or writes will only be shown when the chip-select source is active.

CS Active

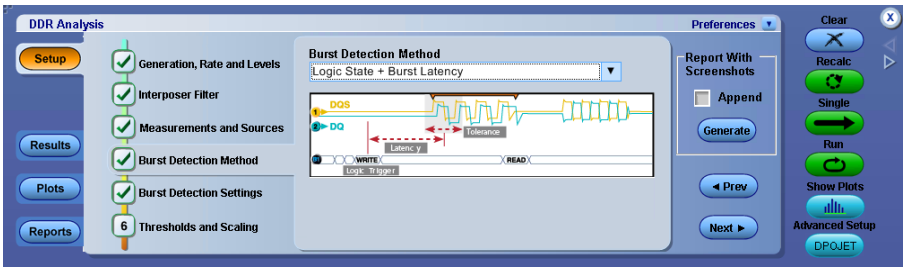
Selects whether the chip-select source logic is considered active high or active low.

CS Mode

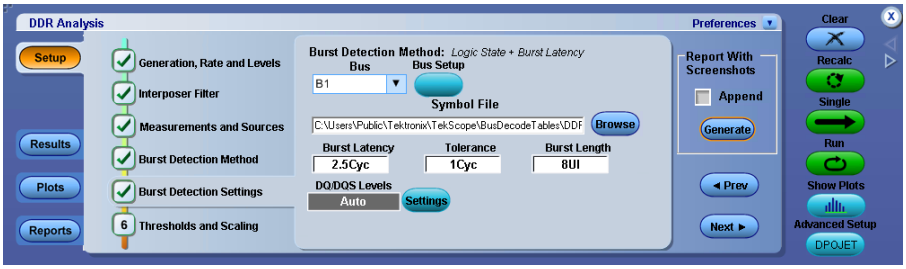
CS Mode consists of two modes – Auto and Manual. CS Auto mode calculates the level automatically for you (as half the peak-to-peak voltage), while manual mode allows you to specify a CS level. In cases where an entire acquisition could occur with no transitions on the chip-select line, you must select the manual mode to set the correct logic level.

Logic state + burst latency

This burst detection method is available only on MSO series of oscilloscopes. You can configure the logic state, burst latency, tolerance, burst length, and DQ/DQS levels.



The DDRA application provides a shortcut, Bus Setup, to configure the bus in the oscilloscope Bus Setup window. Click **Bus Setup** in Step 5 to view the Bus setup screen as shown.

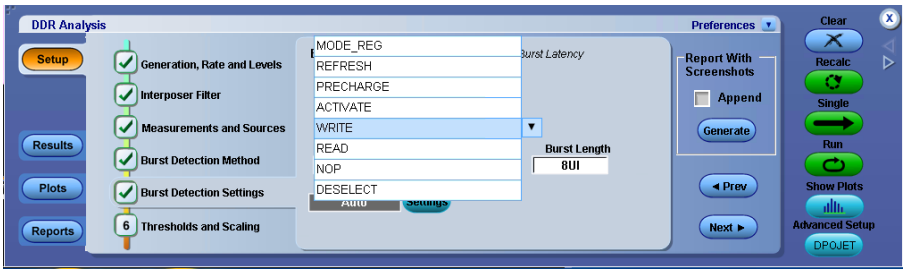


Note: For more details, refer to Bus Setup Control Window (Select Tab) section in your *Oscilloscope* help.

DDRA application lists the buses defined in the bus setup menu. For DDRA to use the logic bus for read/write burst detection, it must have an associated symbol file.

Note: The Burst Length field is not used for LPDDR4/LPDDR4X generation. The LPDDR4/LPDDR4X burst detection algorithm will internally analyze the digital Bus to get the burst length.

By default, the DDRA application displays the symbol file that corresponds to the selected DDR generation in *Step:1*. Click **Browse** to select a symbol file of your choice. On selecting the symbol file, the Logic trigger lists the available patterns as shown. The symbol files per generation are located at `C:\Users\Public\Tektronix\TekScope\busDecodeTables\DDR`.



Edit/customize the symbols based on your requirements and save it in `*.tsf` format. Place the created symbol files for access at `C:\Users\Public\Tektronix\TekScope\busDecodeTables\DDR`. Use Bus setup config menu or browse (Step 5) to access the created symbol file. A sample file for DDR3 (`DDR3 Commands.tsf`) is as shown:

```
#TSF Format    Type        Display Radix    File Radix
#+ Version 2.1.0 PATTERN    BIN        BIN
#Command        Command
#Symbol Name    Pattern
#     CS RAS CAS WE (D3 D2 D1 D0)
#
MODE_REG    0000
REFRESH    0001
PRECHARGE    0010
ACTIVATE    0011
WRITE    0100
READ    0101
NOP    0111
DESELECT    1XXX
```

The DDRA application displays a hint `There may be a possible mismatch in the selected logic trigger and the measurement type. Please verify before continuing when you select a logic state of READ and the measurement type selected is WRITE or vice versa.`

Note: Any change in the symbol file in the DDRA application, is reflected in the oscilloscope Bus configuration menu.

Symbol File

Symbol files are files of alphanumeric symbol names and associated data values and are used to map a group value to a text string. The oscilloscope displays the symbol in place of the numeric value. For more details on symbol file format, refer to your *Oscilloscope* help.

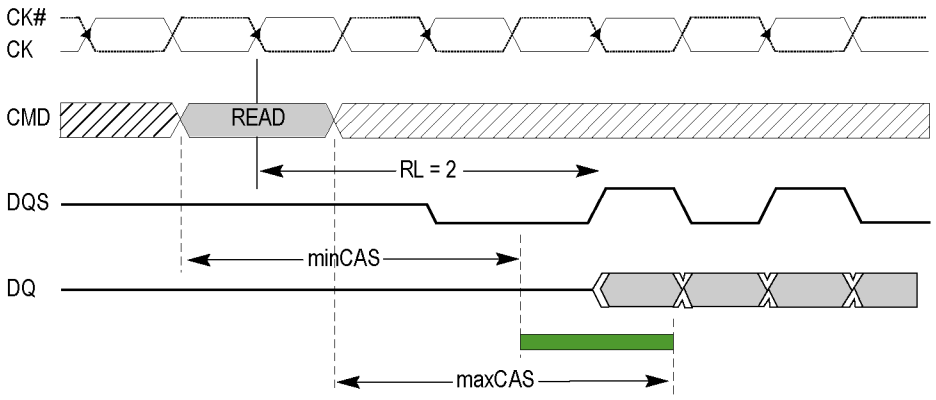
Specify the Burst Latency, Tolerance, and burst length values.

CAS Min and Max

For READ commands, Read Latency (RL) is defined as the delay, in clock cycles, between the rising CLK edge that latches the READ command and the rising DQS edge signifying availability of the first data bit. The Read Latency is equal to the

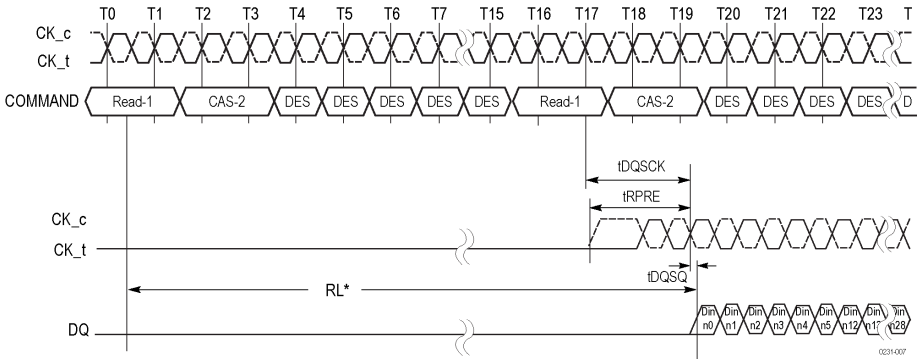
additive Latency and the CAS Latency (RL = AL + CL). CAS Min specifies the minimum time delay between the start of READ bus state and the initial rising DQS edge, for the first bit to be recognized. CAS Max specifies the maximum time delay between the end of the READ bus state and the initial rising DQS edge, for the first bit to be recognized. In the following figure, the actual READ latency is 2 and the CAS Min and CAS Max are set to 2. The green zone indicates where the initial rising DQS edge must be for burst recognition to occur.

For WRITE commands, Write Latency (WL) is defined as the delay, in clock cycles, between the rising CLK edge that latches the WRITE command and the rising DQS edge in the center of the first data bit. The Write Latency is equal to the Additive Latency and the CAS Write Latency (WL = AL + CWL). As with the READ case, the CAS Max and CAS Min parameters define a window following the WRITE bus state where the initial rising DQS edge must be for burst recognition to occur.



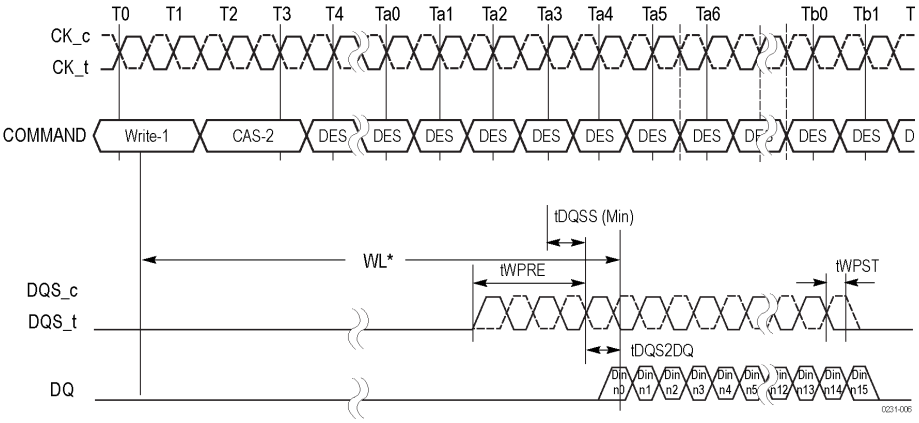
Entering Read Latency(RL) and Write Latency (LW) in case of LPDDR4

Read Latency (RL): Enter the time delay between the mid of the first READ command to start of the data.



In the above diagram, RL* is the latency that you have to enter as Read Latency.

Writer Latency(WL): Enter the time delay between the mid of the first WRITE command and the center of the first data eye.



In the above diagram, WL* is the latency that you have to enter as Writer Latency.

Burst Length

READ and WRITE operations are burst oriented, they start at a selected location, and continue for a burst length. Burst length, specified in cycles, determines where a read/write mark ends after the start of a read/write mark has been identified. Any change in DDR generation resets the burst length to 8.0.

Reference

Salient Features of MSO-DDR Integration Using Digital Channels

Visual search

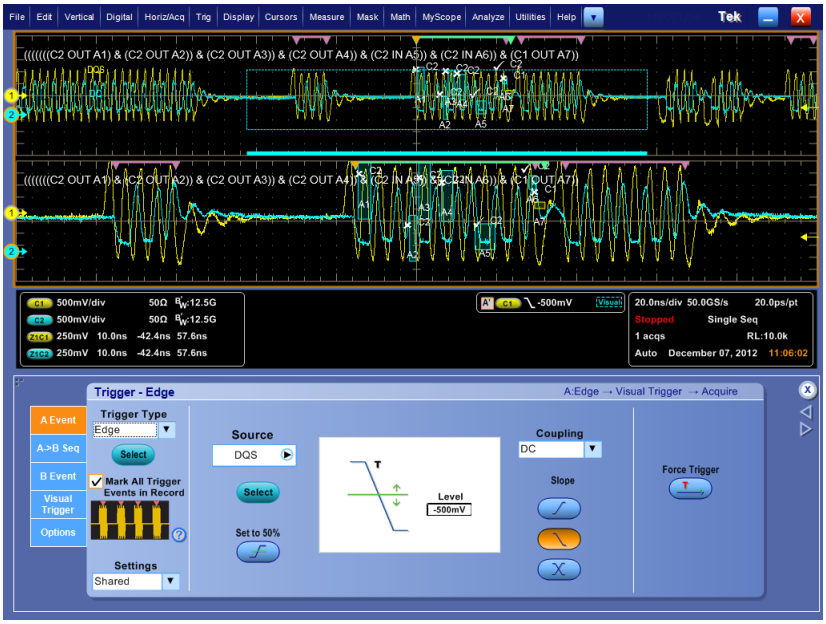
Capturing and analyzing the right part of the waveform can require hours of collecting and sorting through the many acquisitions. The Visual Trigger feature in the oscilloscope makes the identification of the desired waveform events quick and easy by scanning through acquired analog waveforms and graphically comparing them to geometric shapes on the display. By discarding acquired waveforms which do not meet the graphical definition, Visual Triggering extends the trigger capabilities of the oscilloscope beyond the traditional hardware trigger system.

In DDR, Visual Trigger can be used to separate Read Bursts from Write Bursts and mark them. By selecting the Visual Search option in Step 4: Burst Detection Method, these marked bursts can be used for further debugging and analysis.

Marking Read/Write bursts using visual trigger

Visual Trigger can also be used to mark all bursts which have a specific property (for example, marking a Read burst that has a spike just before it comes out of tri-state or marking a Write burst with a known data pattern). The figure below shows Visual Trigger that was used to mark (green marks) Write bursts with a known data pattern.

Along with the Visual search mark, Advanced search and mark (another feature in Tektronix oscilloscopes) has also been used to mark all the Write bursts (pink marks). Visual trigger has been used to isolate a burst with a specific data pattern, which allows the marked burst to be used for further debugging and analysis.



Isolating Read and Write bursts on the DDR3 bus using Visual trigger

DDR3 SDRAM is a high speed, dynamic random access memory internally configured as an eight bank DRAM. It can Read (fetch) and Write data as a burst operation. The burst length can be 4 clock cycles, 8 clock cycles, and can go up to 32 clock cycles so that it can fetch the data byte 1 to 8 bytes in a burst.

DDR3 defines the polarity of the Preamble different for Read and Write. For a Read burst, the Preamble would be negative polarity. For a Write burst, the Preamble would be positive polarity. For DDR3, the Read and Write Preamble widths are defined by parameters tRPRE and tWPRE in the JEDEC specification, and whose minimum value has been defined as 0.9 times that of the clock period.

Additionally, the phase between the Strobe signal (DQS) and Data Signals (DQ) are different for Read and Write. DQS and DQ are aligned for Read bursts and shifted by 90 degrees for Write bursts.

Isolating based on Preamble polarity and phase between DQS and DQ using Visual trigger

Figure 1 shows a screen capture of using Visual Trigger to isolate Read signals based on Preamble polarity and phase difference between the DQS and DQ signals. Channel 1 of the oscilloscope is DQS and Channel 2 is DQ. Areas A1 and A2 are set so that when a signal is captured, there is no DQS signal in these regions. This ensures that the captured signal is coming out of tri-state. Area A3 is set to select the negative polarity of the Preamble. Areas A4 and A5 are set so that the DQ signal does not enter these regions, making sure that the DQS and DQ are aligned.

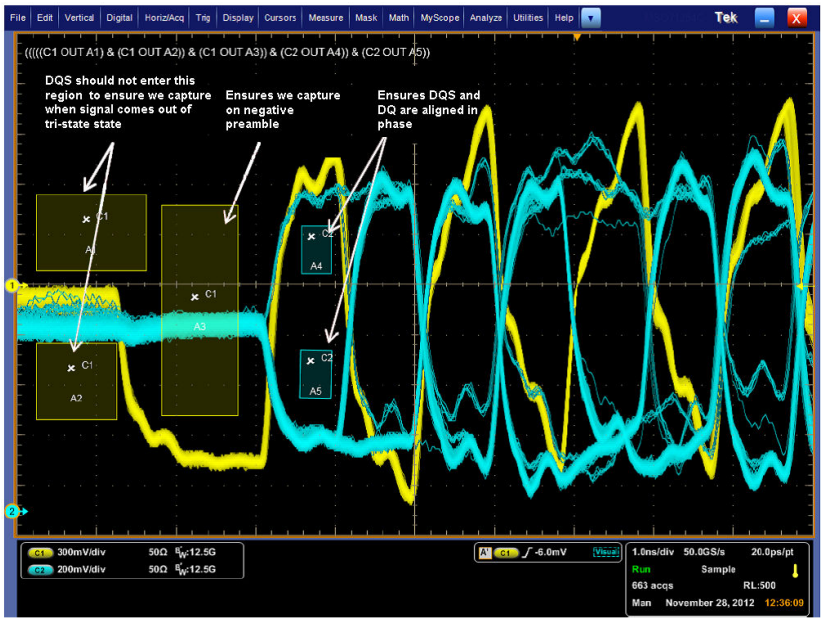


Figure 8: Read burst

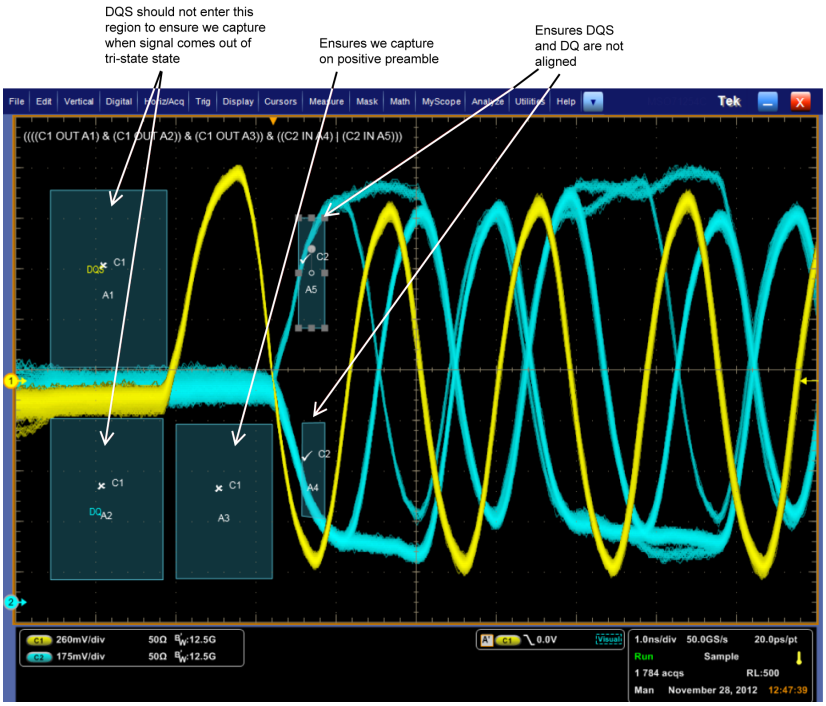
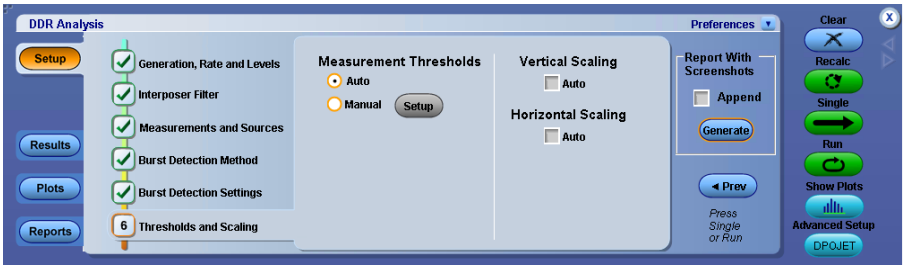


Figure 9: Write burst

Step 6: Thresholds and scaling

The left half of this panel controls selection of critical voltage thresholds used by the measurement algorithms. The right half determines whether scaling is automatically adjusted each time you sequence.



Measurement Thresholds

Select either Auto or Manual as the Measurement Threshold type.

- If you select **Auto**, the application calculates these levels for you based on the DDR generation and speed grade. It is recommended that you use this option.
- If you select **Manual**, set the *measurements levels* by clicking the **Setup** button.

For more details, refer to *Ref Levels* in the *DPOJET* help.

Note: For every measurement selected in DDRA, appropriate reference levels are set in the DPOJET application. You can change these levels, if needed, from the DPOJET application.

Vertical Scaling

Selecting Auto performs autoset on the oscilloscope vertical settings only.

For more details, refer to *Source Autoset* in the *DPOJET* help.

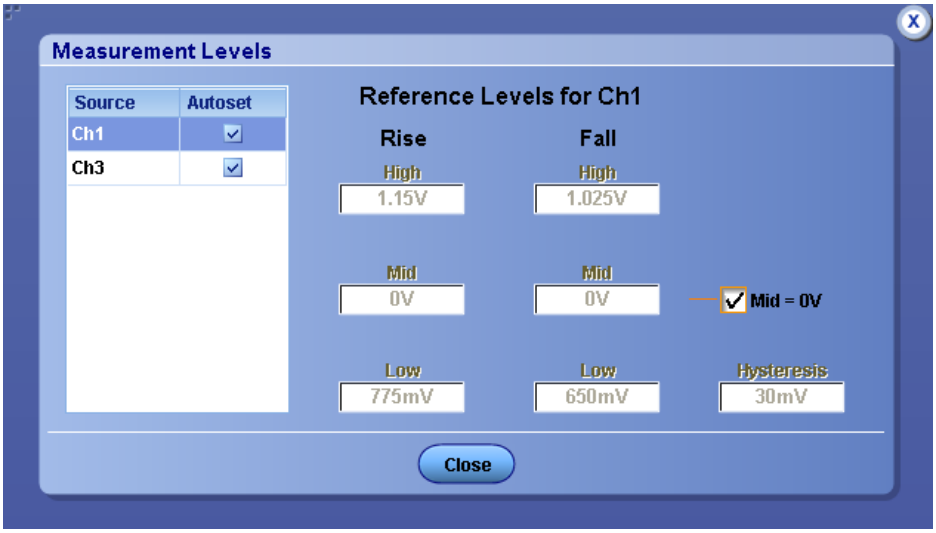
Horizontal Scaling

Selecting Auto will set Record Length to 500K.

Note: If both Vertical and Horizontal are checked, the application performs autoset on both vertical and horizontal oscilloscope settings when Single/Run is selected.

Measurement levels

By definition, edges occur when a waveform crosses specified reference voltage levels. Reference voltage levels must be set so that the application can identify state transitions on a waveform. By default, the application automatically chooses reference voltage levels when necessary.



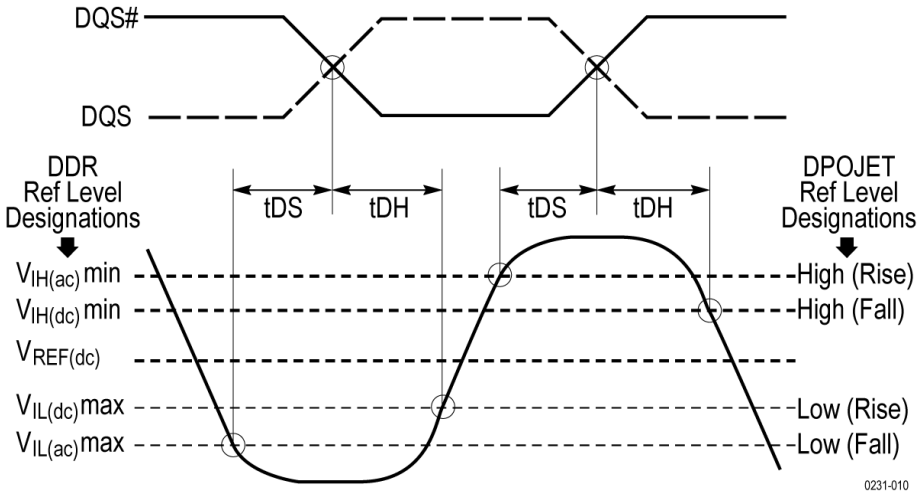
The DDRA application uses three basic reference levels: High, Mid and Low. In addition, a hysteresis value defines a voltage band that prevents a noisy waveform from producing spurious edges. The reference levels and hysteresis are independently set for each source waveform and are specified separately for rising versus falling transitions.

Item	Description
Measurement Reference Levels Setup (one level per source)	
Rise High	Sets the high threshold level for the rising edge of the source.
Rise Mid	Sets the middle threshold level for the rising edge of the source.
Rise Low	Sets the low threshold level for the rising edge of the source.
Fall High	Sets the high threshold level for the falling edge of the source.
Fall Mid	Sets the middle threshold level for the falling edge of the source.
Fall Low	Sets the low threshold level for the falling edge of the source.
Hysteresis	Sets the threshold margin to the reference level which the voltage must cross to be recognized as changing; the margin is the relative reference level plus or minus half the hysteresis- use to filter out spurious events.

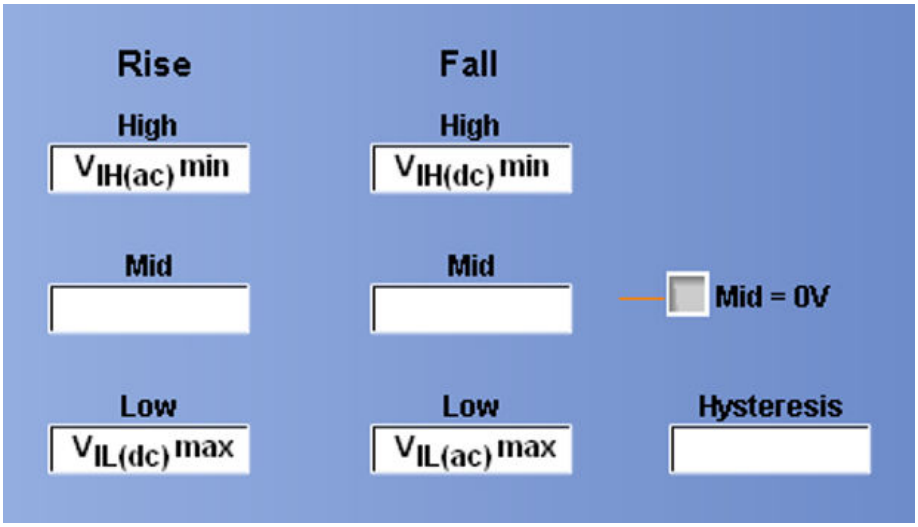
Note: You can also modify reference levels on DPOJET source configuration. Changes done at DPOJET configurations are not saved when a setup file is created.

DDR Setup/Hold Reference Levels: Differential DQS

For systems with a single-ended DQS signal, the waveform reference points for the Setup (tDS) and Hold (tDH) measurements details are as shown.

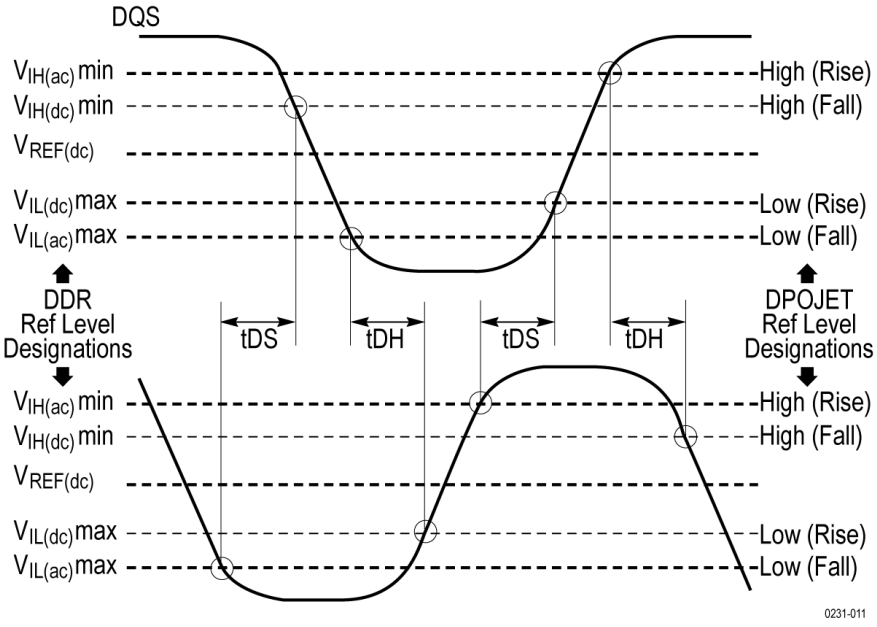


For the Strobe channel, mid reference level should be set to 0 V and the High and Low references are not used. The reference levels for the Data channel are mapped to the source configuration panel as shown.

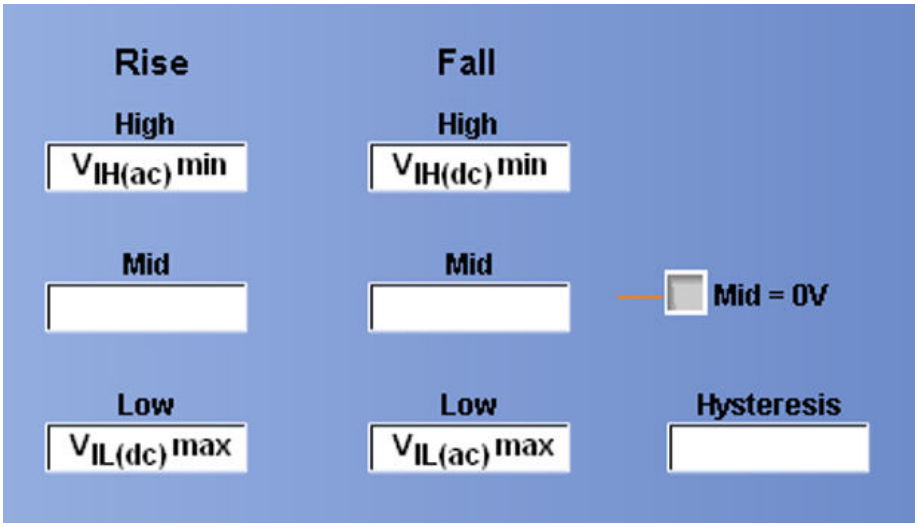


DDR Setup/Hold Reference Levels: Single-Ended DQS

For systems with a single-ended DQS signal, the waveform reference points for the Setup (tDS) and Hold (tDH) measurements details are as shown.

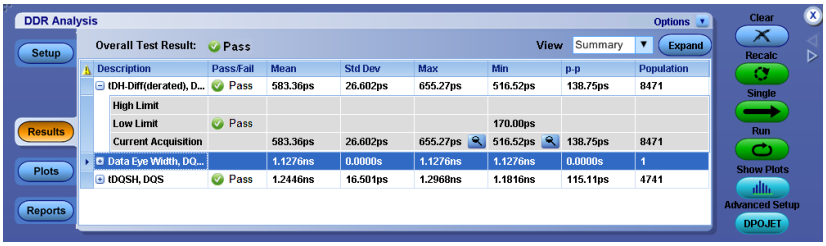


For both Strobe and Data channel, the reference levels are mapped to the source configuration panel as shown.



Results

Result statistics for most of the measurements show Population in terms of UI or transitions. According to the JEDEC specification, the analysis for most of the clock measurements is done for a 200-cycle moving window. However, for clock measurements such as tCL(avg) and tCH(avg), the population is shown as tCK(avg) units. For some measurements such as Data Eye Width, exactly one measurement occurs per acquisition. For such measurements, the population increases by one for each acquisition independent of the number of UI in the acquisition.



For more details, refer to *Viewing Statistical Results* in the *DPOJET* help.

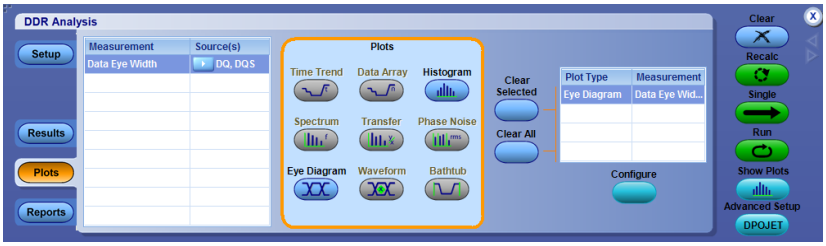
Reference

Dynamic Limits

Plots

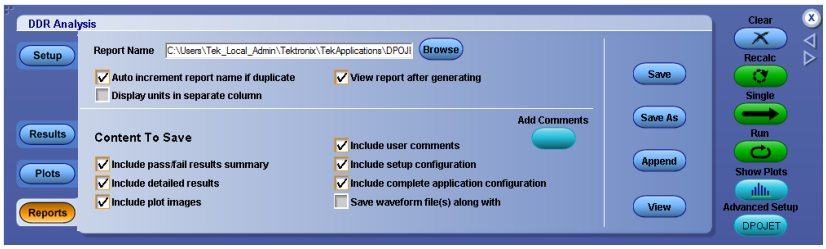
The only measurement for which a plot is automatically configured is *Data Eye Width*, which is available for both Read and Write bursts. However, plots may be added for other measurements through the Plot panel. The plot selection and configuration methods are identical to those used for DPOJET. For more details, refer to the *DPOJET* help.

For acquisitions containing more than one read or write burst, time trend plots connect together all measurements within each burst with a continuous line, but do not draw lines between bursts. If a vertical cursor is placed where it does not intersect a line, the cursor annotation will read NaN (Not a Number).



For more details, refer to *About Configuring Plots* in the *DPOJET* help.

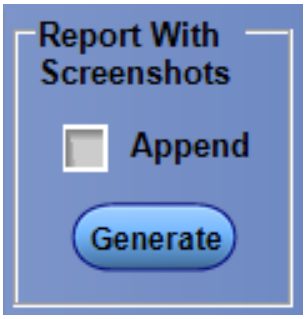
Reports



When measurements re-grouping feature is enabled, you can generate consolidated report for the subsequent runs by using Report option Append. This will add the current settings to an existing report.

For more details, refer to *About Reports* in the *DPOJET* help.

DDRA Report



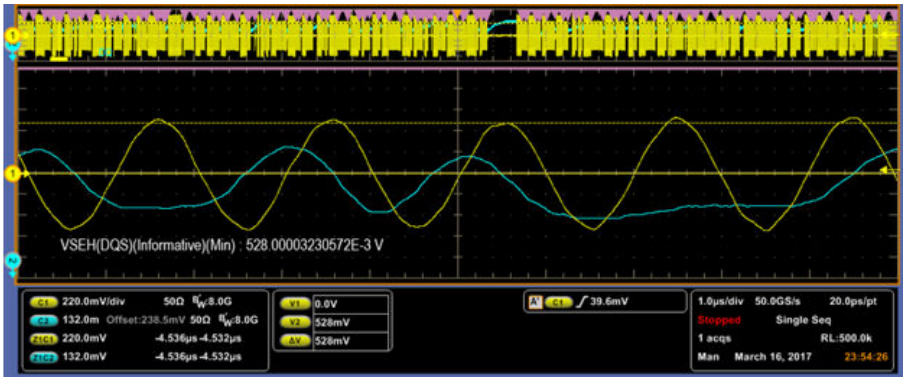
Use this option to generate report with minimum and maximum values of measurement, to display name of selected measurement, and a cursor to show measured region of the waveform. All screen shots are added at the end of the report.

If you click **Generate** button without selecting any measurement, then the application will popup a warning message as `There are currently no results to save. Please run a measurement.` While generating the report, the application starts the screen capture process and a splash screen is displayed showing a message as `Saving images.`

Following are the screen shots based on cursor placed in the report:

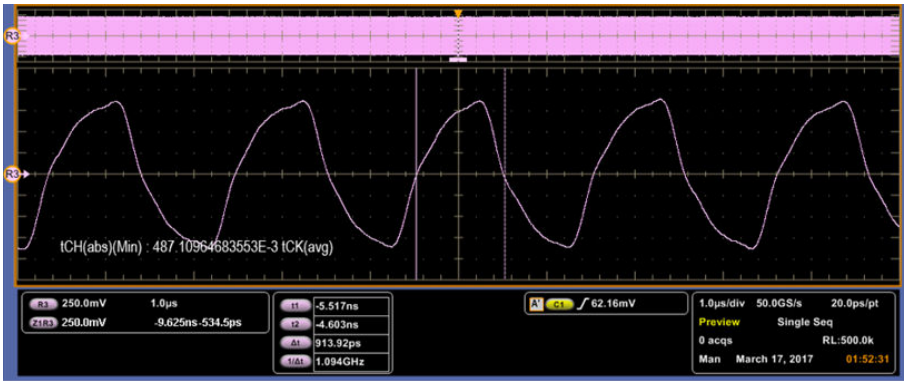
- **Horizontal cursor**: For amplitude measurements, Horizontal cursors are used to mark the measured level.

  Below example shows the minimum voltage level of VSEH(DQS)(Informative) measurement.



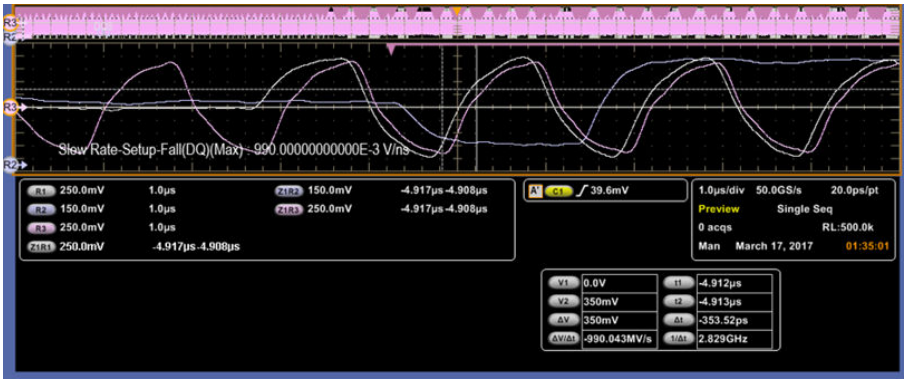
- **Vertical cursor**: For timing measurements, Vertical cursors are used to mark the measured region.

  Below example shows the minimum time measured in tCK(avg) for the tCH(abs) measurement.



- **Screen cursor**: For slew-rate measurements, screen cursors are used to mark the measured region.

  Below screen shot shows an example of screen-cursor.



Switching between the DDRA and DPOJET applications

For advanced analysis, click Advanced Setup DPOJET to switch to the DPOJET application. Likewise, click DDR Analysis DDRA in the DPOJET application to revert to the DDRA application.

The transition behaves as follows:

- The application name in the title bar switches between **DDR Analysis** and **Jitter and Eye Diagram Analysis Tool**.
- Measurement name remains unchanged while traversing from DDRA to DPOJET.
- Measurements added through DDRA application can be termed as DDRA measurements

- DDRA measurements can also be configured in DPOJET. (These configuration changes will make DDRA measurements non-compliant to JEDEC standard)
- Switching between DDRA and DPOJET will retain the measurements added at either applications.
- Measurement execution, results analysis, and report generation can be done from either application.
- Any change in generation or measurement type in DDRA deselects all the currently selected DDRA measurements.
- Switching back from DPOJET to DDRA, always resets focus to the Setup panel.
- DPOJET or DDRA application is always accessible from the oscilloscope menu bar, as an alternative to the quick navigation buttons.
- If DPOJET application is opened from the oscilloscope menu (Analyze > Jitter and Eye Diagram Analysis), the shortcut button to DDR Analysis is not shown. This shortcut only appears if DPOJET is entered from the DDRA interface.
- Any change in the reference voltage levels in DPOJET is reflected in DDRA Step 1, *Vih and Vil*. Vih and Vil specify the static voltage reference levels of the measurements. You can modify these levels either in *Step 6* of DDRA or in the DPOJET source configuration screen.
- Changing reference voltage levels through DPOJET application will not be retained in the setup files created and accessed by DDRA application.

Salient features of MSO-DDRA integration

The following are the salient features of MSO-DDRA integration:

- Use the DDRA user interface for the required settings without exiting from the DDRA Setup panel for digital configuration.
- Logic State burst detection method is more reliable than the conventional DQ/DQS Phase alignment.
- Digital configurations are available at Step 4 and Step 5 of the DDRA application. The Logic pattern or Logic state triggering is used on the digital control signals such as RAS, CAS, CS and WE, which identify the desired burst type.
- Symbol files per DDR generation are available.
- Identify marks using the specified digital control signals and Burst Latency and Tolerance values. The Burst Latency and Tolerance values are important to precisely mark the bursts.

Hints

The DDRA application displays the following hints at different steps:

Hint	Step	Description
Select a standard data rate in DDRA.	*1*	Displayed when data rate is None. When you select a non standard data rate in ASM, the data rate is set to None in DDRA.
GDDR3 not completely supported. Some features may not function.	*1*	Displayed on selecting GDDR3 standard, which does not have standard data rates. Only Data Eye Width measurement is available for both Read and Write bursts.
Please provide a limits file under Jitter and Eye Analysis > Limits.	*1*	Displayed for custom data rates for which limits are not defined. You need to manually configure the limits.
Math sources cannot be selected as a measurement source when filters are applied.	*2*	Displayed when any Interposer Filter is selected.
Cannot use Live and Ref waveforms together.	*3*	Displayed when combination of Ch<x> and Ref<x> sources are selected. Example: For Data Eye Width measurement, Ch1 is assigned to DQ and Ref1 is assigned to DQS.

Table continued…

Hint	Step	Description
Cannot use the same waveform for different sources.	3	Displayed on selecting the same source for DQ and DQS. Example: Data Eye Width using Ch3 for both DQ and DQS.
Measurement results may vary as the Ref levels are changed.	3	Displayed when measurements with different source reference levels are selected.
Adding selected measurements. Please wait…	3	Displayed when tERR measurements are selected under Clock(Diff) measurement type. **Note:** You are advised not to interact with application, until the selection is completed.
Some of the READ bursts with toggle preamble and extended postamble may be identified as WRITE bursts.	4	Displayed only when write postamble length is set to 0.5tCK
Some of the WRITE bursts with 0.5tCK postamble may be identified as READ bursts	4	Displayed only when read postamble length is set to 0.5tck.
Informative measurements are not shown	3	Displayed when you clear the option of Show Informative measurements.
Measurements having different reference level has been disabled.	3	Displayed when you select the option of Select measurements as per reference level.

Derating

Signal slew rate derating is required to verify the setup and hold timing requirements on address/command and data signals. The base setup and hold limits are defined using input signals that have a 1.0 V/ns slew rate. To determine final pass/fail status, the limits must be adjusted based on the actual slew rates of the target signals, according to derating tables appearing in the DDR2 and DDR3 specifications.

Measurement	DDR2	DDR3	DDR3L	LPDDR2	LPDDR3	DDR4
tDH(derated)DQS(Informative)	✓					
tDH-Diff(derated)	✓	✓	✓	✓	✓	
tDH-Diff(max-derated) (Informative)		✓	✓	✓		
tDH-Diff(min-derated) (Informative)		✓	✓	✓		
tDS(derated)DQS(Informative)	✓					
tDS-Diff(derated)	✓	✓	✓	✓	✓	
tDS-Diff(max-derated) (Informative)		✓	✓	✓		
tDS-Diff(min-derated) (Informative)		✓	✓	✓		
tIH(derated)	✓	✓	✓	✓		✓

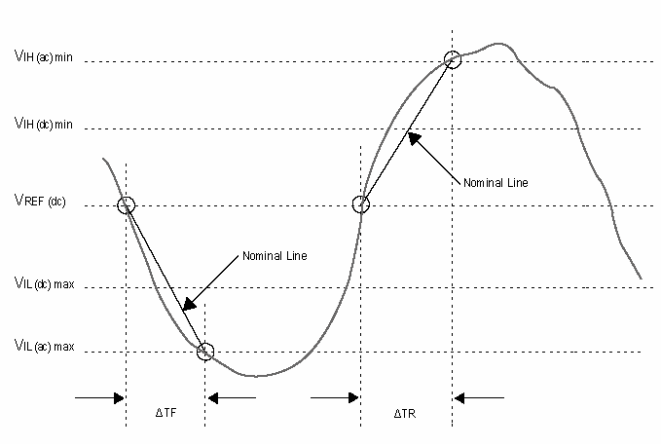
Table continued…

Measurement	DDR2	DDR3	DDR3L	LPDDR2	LPDDR3	DDR4
tIH(derated)CA					✓	
tIH(derated)CS					✓	
tIH(max-derated) (Informative)		✓	✓	✓		
tIH(min-derated) (Informative)		✓	✓	✓		
tIS(derated)	✓	✓	✓	✓		✓
tIS(derated)CA					✓	
tIS(derated)CS					✓	
tIS(max-derated) (Informative)		✓	✓	✓		
tIS(min-derated) (Informative)		✓	✓	✓		

The derated value (Δ) is calculated as per the JEDEC standard using either the DDR Method or Nominal Method, depending on the user configuration.

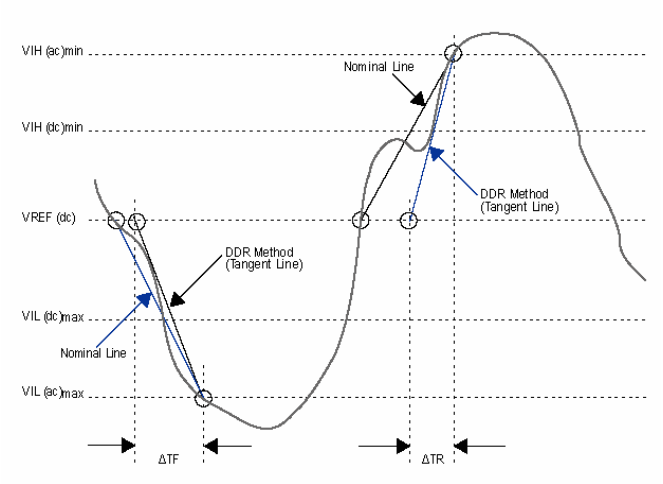
Derating is explained taking an example of Setup(tIS) measurement. The same concept is applicable for other derated measurements.

When the nominal method is set, Setup(tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)min}$. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max.



+

If the DDR Method is set, the application takes the maximum slope. This method is applicable if the actual signal is earlier than the nominal slew rate line.



According to the specified reference levels, rise slew rate is always positive whereas fall slew rate is negative. A single slew rate value is obtained by averaging the absolute values of rise and fall slew rate. Using this value and a similarly-derived slew rate for the clock signal, the total setup time (tIS) is calculated by adding ΔtIS to the tIS(base)limit from the following table:

Table 10: Address/Command Setup and Hold Values

Units(ps)	DDR3–800	DDR3–1066	DDR3–1333	DDR3–1600	Units
tIS(base) AC 175	200	125	65	45	ps
tIS(base) AC150	350	275	190	170	ps
tIH(base)	275	200	140	120	ps

Note: For DDR3 speeds 1333 and 1600 MT/s, the AC 150 reference levels are applied, though the default selection in the *Step 6* is AC175.

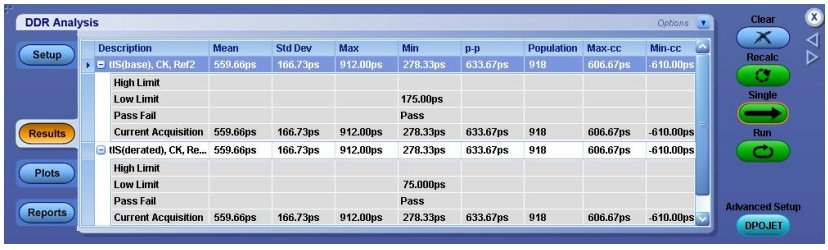
ΔtIS is determined using the derating table, where the Y-axis represents the Address/Command slew rate and the X-axis, the clock differential value. By indexing the Address/Command value and Clock differential value, ΔtIS value is obtained from AC175 table.

The derating values are derived from linear interpolation of measured slew rate. For example: For a Clock differential value= 1.25 V/ns, Address/Command Slew Rate =1.0 V/ns, and AC 175 Threshold selected in Step 6, the resulting derated value is:

$tIS_{deratedlimit} = tIS(base)_{limit} + \Delta tIS$.

$tIS_{deratedlimit} = 200+69.5=269.5$

The result statistics of the both tIS(base) and tIS(derated) are the same as shown in the following figure. In case of derating, the limit values get changed depending on the signal slew rate.



Log messages

Derating failure:

1. Derating limit cannot be computed since the calculated Slew Rate is falling outside of derating table.
2. Derating values cannot be applied as Slew Rate measurement failed.
3. Limit for the base measurement is not specified in the JEDEC specification.
4. Derating limit calculated using either Rise or Fall Slew Rate value.

Reference

DDR Measurement Sources

DDR2 Measurement Sources

DDR3/DDR3LMeasurement Sources

DDR4 Measurement Sources

GDDR3 Measurement Sources

GDDR5 Measurement Sources

LPDDR Measurement Sources

LPDDR2 Measurement Sources

LPDDR3 Measurement Sources

LPDDR4/LPDDR4X Measurement Sources

Measurements

Measurement sources

DDR measurement sources

The sources required for analysis may include DQS(Strobe), DQ(Data), DQS# (Strobe), Clock, Clock#, and Addr/Cmd. Clock and DQS can be either Single-Ended (SE) or Differential (Diff). CS Source is available, as appropriate, as an optional qualifier.

The following table lists the sources required for each DDR measurement:

Table 11: DDR measurement sources

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional [2]**
Write Bursts			
Data Eye			
Data Eye Height	Height	DQ, DQS	
Data Eye Width	Width	DQ, DQS	
Data Pulse Width			
tDIPW-High	Pos Width	DQ	DQS
tDIPW-Low	Neg Width	DQ	DQS
Strobe Measurements			
tDQSH	Pos Width	DQS	DQ
tDQSL	Neg Width	DQS	DQ
tDSS-Diff	Setup	CK, DQS	DQ
tDSH-Diff	Hold	CK, DQS	DQ
tWPRE	DDR tRPRE	DQS	DQ
tWPST	DDR tPST	DQS	DQ
Read Bursts			
Data Eye			
Data Eye Height	Height	DQ, DQS	
Data Eye Width	Width	DQ, DQS	
Strobe Measurements			
tAC-Diff	DDR Setup-Diff	CK, DQ	DQS
tDQSCK-Diff	Skew	CK, DQS	DQ
tQH	Hold	DQS, DQ	
tRPRE	DDR tRPRE	DQS	DQ
tRPST	DDR tPST	DQS	DQ

Table continued…

[2] Additional sources are required for proper identification of bursts by Search and Mark feature.

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional [2]**
DQS(Single Ended, Write)			
Clock-Strobe			
tDSH(DQS)(Informative)	Hold	DQS, CK	DQ
tDSS(DQS)(Informative)	Setup	DQS, CK	DQ
Setup and Hold			
tDH(DQS)(Informative)	Hold	DQS, DQ	
tDS(DQS)(Informative)	Setup	DQS, DQ	
Vix(ac)DQS(Informative)	V-Diff-Xovr	DQS, DQS#	DQ
DQS(Single Ended, Read)			
DQS-DQ Skew			
tDQSQ(DQS)	Setup	DQS, DQ	
Clock(Diff)			
Clock Eye			
Clock Eye Height (Informative)	Height	CK	
Clock Eye Width (Informative)	Width	CK	
Differential Clock			
tCH	Pos Width	CK	
tCK	Period	CK	
tCL	Neg Width	CK	
tHP	Period	CK	
VID(ac)	DDR VID(ac)	CK	
Clock(Single Ended)			
AC-Overshoot(CK#)	Overshoot	CK#	
AC-Overshoot(CK)	Overshoot	CK	
AC-OvershootArea(CK#)	AOS	CK#	
AC-OvershootArea(CK)	AOS	CK	
AC-Undershoot(CK#)	Undershoot	CK#	
AC-Undershoot(CK)	Undershoot	CK	
AC-UndershootArea(CK#)	AUS	CK#	
AC-UndershootArea(CK)	AUS	CK	
Vix(ac)CK	V-Diff-Xovr	CK, CK#	
Address/Command			
AC-Overshoot	Overshoot	ADDR/CMD	
AC-OvershootArea	AOS Per tCK	CK, ADDR/CMD	

Table continued…

[2] Additional sources are required for proper identification of bursts by Search and Mark feature.

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional [2]**
AC-Undershoot	Undershoot	ADDR/CMD	
AC-UndershootArea	AUS Per tCK	CK, ADDR/CMD	
Pulse Width			
tIPW-High	Pos Width	ADDR/CMD	
tIPW-Low	Neg Width	ADDR/CMD	
Setup and Hold			
tIH(base)	DDR Hold-Diff	CK, ADDR/CMD	
tIS(base)	DDR Setup-Diff	CK, ADDR/CMD	
Overshoot/Undershoot			
AC-Overshoot(DQ)	Overshoot	DQ	DQS
AC-Overshoot(DQS)	Overshoot	DQS	DQ
AC-OvershootArea(DQ)	AOS Per UI	DQS, DQ	
AC-OvershootArea(DQS)	AOS	DQS	DQ
AC-Undershoot(DQ)	Undershoot	DQ	DQS
AC-Undershoot(DQS)	Undershoot	DQS	DQ
AC-UndershootArea(DQ)	AUS Per UI	DQS, DQ	
AC-UndershootArea(DQS)	AUS	DQS	DQ

DDR2 measurement sources

The sources required for analysis may include DQS(Strobe), DQ(Data), DQS# (Strobe), Clock, Clock#, CS Source, and Addr/Cmd. Clock and DQS can be either Single-Ended (SE) or Differential (Diff). Read and Write bursts have CS as an optional source.

The following table lists the sources required for each DDR2 measurement:

Table 12: DDR2 measurement sources

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional [2]**
Write Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	
Data Pulse Width			
tDIPW-High	Pos Width	DQ	DQS
tDIPW-Low	Neg Width	DQ	DQS
Data Slew Rate			
Slew Rate-Hold-Fall(DQ)	Fall Slew Rate	DQ	DQS

Table continued…

[2] Additional sources are required for proper identification of bursts by Search and Mark feature.

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
Slew Rate-Hold-Rise(DQ)	Rise Slew Rate	DQ	DQS
Slew Rate-Setup-Fall(DQ)	Fall Slew Rate	DQ	DQS
Slew Rate-Setup-Rise(DQ)	Rise Slew Rate	DQ	DQS
Differential Strobe			
tDQSH	Pos Width	DQS	DQ
tDQSL	Neg Width	DQS	DQ
tDQSS-Diff	Skew	DQS, CK	DQ
tDSH-Diff	Hold	DQS, CK	DQ
tDSS-Diff	Setup	DQS, CK	DQ
tWPRE	DDR tRPRE	DQS	DQ
tWPST	DDR tPST	DQS	DQ
Setup and Hold			
tDH-Diff(base)	DDR Hold-Diff	DQS, DQ	
tDH-Diff(derated)	DDR Hold-Diff	DQS, DQ	
tDS-Diff(base)	DDR Setup-Diff	DQS, DQ	
tDS-Diff(derated)	DDR Setup-Diff	DQS, DQ	
Strobe Slew Rate			
InputSlew-Diff-Fall(DQS)	Fall Slew Rate	DQS	DQ
InputSlew-Diff-Rise(DQS)	Rise Slew Rate	DQS	DQ
Read Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	
Differential Strobe			
tAC-Diff	DDR Setup-Diff	DQ, CK	DQS
tDQSCK	DDR2 tDQSCK	DQS, CK	DQ
tDQSQ-Diff	Setup	DQS, DQ	
tQH	Hold	DQS, DQ	
tRPRE	DDR tRPRE	DQS	DQ
tRPST	DDR tPST	DQS	DQ
DQS(Single Ended, Write)			
Clock-Strobe			
tDQSS(DQS)(Informative)	Skew	DQS, CK	DQ
tDSH(DQS)(Informative)	Hold	DQS, CK	DQ
tDSS(DQS)(Informative)	Setup	DQS, CK	DQ
Setup and Hold			

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
tDH(base)DQS(Informative)	DDR Hold-SE	DQS, DQ	
tDH(derated)DQS(Informative)	DDR Hold-SE	DQS, DQ	
tDS(base)DQS(Informative)	DDR Setup-SE	DQS, DQ	
tDS(derated)DQS(Informative)	DDR Setup-SE	DQS, DQ	
Strobe Slew Rate			
Slew Rate-Hold-SE-Fall(DQS)	Fall Slew Rate	DQS	DQ
Slew Rate-Hold-SE-Rise(DQS)	Rise Slew Rate	DQS	DQ
Slew Rate-Setup-SE-Fall(DQS)	Fall Slew Rate	DQS	DQ
Slew Rate-Setup-SE-Rise(DQS)	Rise Slew Rate	DQS	DQ
Vix(ac)DQS	V-Diff-Xovr	DQS, DQS#	DQ
VSWING(MAX)DQS	Cycle Pk-Pk	DQS	DQ
VSWING(MAX)DQS#	Cycle Pk-Pk	DQS#	DQS,DQ
DQS(Single Ended, Read)			
DQS-DQ Skew			
tDQSQ(DQS)(Informative)	Setup	DQS, DQ	
Vox(ac)DQS	V-Diff-Xovr	DQS, DQS#	DQ
Clock(Diff)			
Clock Eye			
Clock Eye Height (Informative)	Height	CK	
Clock Eye Width (Informative)	Width	CK	
Differential Clock			
tCH(abs)	Pos Width	CK	
tCH(avg)	DDR tCH(avg)	CK	
tCK(abs)	Period	CK	
tCK(avg)	DDR tCK(avg)	CK	
tCL(abs)	Neg Width	CK	
tCL(avg)	DDR tCL(avg)	CK	
tHP	Period	CK	
tJIT(cc)	CC-Period	CK	
tJIT(duty)	DDR tJIT(duty)	CK	
tJIT(per)	DDR tJIT(per)	CK	
VID(ac)	DDR VID(ac)	CK	
Slew Rate			
InputSlew-Diff-Fall(CK)	Fall Slew Rate	CK	
InputSlew-Diff-Rise(CK)	Rise Slew Rate	CK	
tERR			

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional [2]**
tERR(02per to) tERR(11-50per)	DDR tERR(n)	CK	
Clock(Single Ended)			
AC-Overshoot(CK#)	Overshoot	CK#	
AC-Overshoot(CK)	Overshoot	CK	
AC-OvershootArea(CK#)	AOS	CK#	
AC-OvershootArea(CK)	AOS	CK	
AC-Undershoot(CK#)	Undershoot	CK#	
AC-Undershoot(CK)	Undershoot	CK	
AC-UndershootArea(CK#)	AUS	CK#	
AC-UndershootArea(CK)	AUS	CK	
Vix(ac)CK	V-Diff-Xovr	CK, CK#	
Vox(ac)CK	V-Diff-Xovr	CK, CK#	
VSWING(MAX)CK	Cycle Pk-Pk	CK	
VSWING(MAX)CK#	Cycle Pk-Pk	CK#	
Address/Command			
AC-Overshoot	Overshoot	ADDR/CMD	
AC-OvershootArea	AOS Per tCK	CK, ADDR/CMD	
AC-Undershoot	Undershoot	ADDR/CMD	
AC-UndershootArea	AUS Per tCK	CK, ADDR/CMD	
AddrCmd Eye			
AddrCmd Eye Width(Informative)	Width	CK, ADDR/CMD	
Pulse Width			
tIPW-High	Pos Width	ADDR/CMD	
tIPW-Low	Neg Width	ADDR/CMD	
Setup and Hold			
tIH(base)	DDR Hold-Diff	CK, ADDR/CMD	
tIH(derated)	DDR Hold-Diff	CK, ADDR/CMD	
tIS(base)	DDR Setup-Diff	CK, ADDR/CMD	
tIS(derated)	DDR Setup-Diff	CK, ADDR/CMD	
Slew Rate			
Slew Rate-Hold-Fall(Addr/Cmd)	Fall Slew Rate	ADDR/CMD	
Slew Rate-Hold-Rise(Addr/Cmd)	Rise Slew Rate	ADDR/CMD	
Slew Rate-Setup-Fall(Addr/Cmd)	Fall Slew Rate	ADDR/CMD	
Slew Rate-Setup-Rise(Addr/Cmd)	Rise Slew Rate	ADDR/CMD	
Precharge			
tRP(REF)	tCMD-CMD	Bus [3], CK	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
tRP(MRS)	tCMD-CMD	Bus[3], CK	
Overshoot/Undershoot			
AC-Overshoot(DQ)	Overshoot	DQ	DQS
AC-Overshoot(DQS#)	Overshoot	DQS#	DQS,DQ
AC-Overshoot(DQS)	Overshoot	DQS	DQ
AC-OvershootArea(DQ)	AOS Per UI	DQS, DQ	
AC-OvershootArea(DQS#)	AOS	DQS#	DQS,DQ
AC-OvershootArea(DQS)	AOS	DQS	DQ
AC-Undershoot(DQ)	Undershoot	DQ	DQS
AC-Undershoot(DQS#)	Undershoot	DQS#	DQS,DQ
AC-Undershoot(DQS)	Undershoot	DQS	DQ
AC-UndershootArea(DQ)	AUS Per UI	DQS, DQ	
AC-UndershootArea(DQS#)	AUS	DQS#	DQS,DQ
AC-UndershootArea(DQS)	AUS	DQS	DQ

DDR3/DDR3L measurement sources

The sources required for analysis may include DQS(Strobe), DQ(Data), DQS# (Strobe), Clock, Clock#, and Addr/Cmd. Clock and DQS can be either Single-Ended (SE) or Differential (Diff). CS Source is available, as appropriate, as an optional qualifier.

The following table lists the sources required for each DDR3/DDR3L measurement:

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
Write Bursts			
Data Eye			
Data Eye Height	Height	DQ, DQS	
Data Eye Width	Width	DQ, DQS	
Data Pulse Width			
tDIPW-High	Pos Width	DQ	DQS
tDIPW-Low	Neg Width	DQ	DQS
Data Slew Rate			
Slew Rate-Hold-Fall(DQ)	Fall Slew Rate	DQ	DQS
Slew Rate-Hold-Rise(DQ)	Rise Slew Rate	DQ	DQS
Slew Rate-Setup-Fall(DQ)	Fall Slew Rate	DQ	DQS
Slew Rate-Setup-Rise(DQ)	Rise Slew Rate	DQ	DQS
Differential Input Level			
VIHdiff(AC)	Cycle Max	DQS	DQ

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
VILdiff(AC)	Cycle Min	DQS	DQ
Differential Strobe			
tDQSH	Pos Width	DQS	DQ
tDQSL	Neg Width	DQS	DQ
tDQSS-Diff	Skew	CK, DQS	DQ
tDSH-Diff	Hold	CK, DQS	DQ
tDSS-Diff	Setup	CK, DQS	DQ
tDVAC(DQS)	Time Outside Level	DQS	DQ
tWPRE	DDR tWPRE	DQS	DQ
tWPST	DDR tPST	DQS	DQ
Setup and Hold			
tDH-Diff(base)	DDR Hold-Diff	DQS, DQ	
tDH-Diff(derated)	DDR Hold-Diff	DQS, DQ	
tDH-Diff(max-derated)(Informative)	DDR Hold-Diff	DQS, DQ	
tDH-Diff(min-derated)(Informative)	DDR Hold-Diff	DQS, DQ	
tDS-Diff(base)	DDR Setup-Diff	DQS, DQ	
tDS-Diff(derated)	DDR Setup-Diff	DQS, DQ	
tDS-Diff(max-derated)(Informative)	DDR Setup-Diff	DQS, DQ	
tDS-Diff(min-derated)(Informative)	DDR Setup-Diff	DQS, DQ	
Strobe Slew Rate			
InputSlew-Diff-Fall(DQS)	Fall Slew Rate	DQS	DQ
InputSlew-Diff-Rise(DQS)	Rise Slew Rate	DQS	DQ
Time Above AC Level			
tVAC(DQ)	Time Outside Level	DQ	DQS
Read Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	
Data Output Level			
VOH(AC)DQ	Cycle Max	DQ	DQS
VOH(DC)DQ	Cycle Max	DQ	DQS
VOL(AC)DQ	Cycle Min	DQ	DQS
VOL(DC)DQ	Cycle Min	DQ	DQS
Data Pulse Width			
tDIPW-High	Pos Width	DQ	DQS
tDIPW-Low	Neg Width	DQ	DQS

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
Data Slew Rate			
SRQse-Fall(DQ)	Fall Slew Rate	DQ	DQS
SRQse-Rise(DQ)	Rise Slew Rate	DQ	DQS
Differential Output Level			
VOHdiff(AC)	Cycle Max	DQS	DQ
VOLdiff(AC)	Cycle Min	DQS	DQ
Differential Strobe			
tDQSCK-Diff	Skew	DQS, CK	DQ
tDQSQ-Diff	Setup	DQS, DQ	
tDVAC(DQS)	Time Outside Level	DQS	DQ
tQH	Hold	DQS, DQ	
tQSH	Pos Width	DQS	DQ
tQSL	Neg Width	DQS	DQ
tRPRE	DDR tRPRE	DQS	DQ
tRPST	DDR tPST	DQS	DQ
Strobe Slew Rate			
SRQdiff-Fall(DQS)	Fall Slew Rate	DQS	DQ
SRQdiff-Rise(DQS)	Rise Slew Rate	DQS	DQ
DQS(Single Ended, Write)			
Vix(ac)DQS	DDR3 Vix(ac)	DQS, DQS#	DQ
VSEH(DQS#)	Cycle Max	DQS#	DQS,DQ
VSEH(DQS)	Cycle Max	DQS	DQ
VSEL(DQS#)	Cycle Min	DQS#	DQS,DQ
VSEL(DQS)	Cycle Min	DQS	DQ
Clock-Strobe			
tDQSS(DQS)(Informative)	Skew	DQS, CK	DQ
tDSH(DQS)(Informative)	Hold	DQS, CK	DQ
tDSS(DQS)(Informative)	Setup	DQS, CK	DQ
DQS(Single Ended, Read)			
VSEH(DQS#)	Cycle Max	DQS#	DQS,DQ
VSEH(DQS)	Cycle Max	DQS	DQ
VSEL(DQS#)	Cycle Min	DQS#	DQS,DQ
VSEL(DQS)	Cycle Min	DQS	DQ
Clock-Strobe			
tDQSS(DQS)(Informative)	Skew	DQS, CK	DQ
tDSH(DQS)(Informative)	Hold	DQS, CK	DQ

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
tDSS(DQS)(Informative)	Setup	DQS, CK	DQ
Strobe Output Level			
VOH(AC)DQS	Cycle Max	DQS	DQ
VOH(AC)DQS#	Cycle Max	DQS#	DQS,DQ
VOH(DC)DQS	Cycle Max	DQS	DQ
VOH(DC)DQS#	Cycle Max	DQS#	DQS,DQ
VOL(AC)DQS	Cycle Min	DQS	DQ
VOL(AC)DQS#	Cycle Min	DQS#	DQS,DQ
VOL(DC)DQS	Cycle Min	DQS	DQ
VOL(DC)DQS#	Cycle Min	DQS#	DQS,DQ
Clock(Diff)			
Clock Eye			
Clock Eye Height (Informative)	Height	CK	
Clock Eye Width (Informative)	Width	CK	
Differential Clock			
tCH(abs)	Pos Width	CK	
tCH(avg)	DDR tCH(avg)	CK	
tCK(abs)	Period	CK	
tCK(avg)	DDR tCK(avg)	CK	
tCL(abs)	Neg Width	CK	
tCL(avg)	DDR tCL(avg)	CK	
tDVAC(CK)	Time Outside Level	CK	
tJIT(cc)	CC-Period	CK	
tJIT(duty)	DDR tJIT(duty)	CK	
tJIT(per)	DDR tJIT(per)	CK	
Differential Input Level			
VIHdiff(AC)	Cycle Max	CK	
VILdiff(AC)	Cycle Min	CK	
Slew Rate			
InputSlew-Diff-Fall(CK)	Fall Slew Rate	CK	
InputSlew-Diff-Rise(CK)	Rise Slew Rate	CK	
tERR			
tERR(02per to tERR(50per)	DDR tERR(n)	CK	
Clock(Single Ended)			
AC-Overshoot(CK#)	Overshoot	CK#	
AC-Overshoot(CK)	Overshoot	CK	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
AC-OvershootArea(CK#)	AOS	CK#	
AC-OvershootArea(CK)	AOS	CK	
AC-Undershoot(CK#)	Undershoot	CK#	
AC-Undershoot(CK)	Undershoot	CK	
AC-UndershootArea(CK#)	AUS	CK#	
AC-UndershootArea(CK)	AUS	CK	
Vix(ac)CK	DDR3 Vix(ac)	CK, CK#	
VSEH(CK#)	Cycle Max	CK#	
VSEH(CK)	Cycle Max	CK	
VSEL(CK#)	Cycle Min	CK#	
VSEL(CK)	Cycle Min	CK	
Address/Command			
AC-Overshoot	Overshoot	ADDR/CMD	
AC-OvershootArea	AOS Per tCK	CK, ADDR/CMD	
AC-Undershoot	Undershoot	ADDR/CMD	
AC-UndershootArea	AUS Per tCK	CK, ADDR/CMD	
AddrCmd Eye			
AddrCmd Eye Width(Informative)	Width	CK, ADDR/CMD	
Pulse Width			
tIPW-High	Pos Width	ADDR/CMD	
tIPW-Low	Neg Width	ADDR/CMD	
Setup and Hold			
tIH(base)	DDR Hold-Diff	CK, ADDR/CMD	
tIH(derated)	DDR Hold-Diff	CK, ADDR/CMD	
tIH(max-derated)(Informative)	DDR Hold-Diff	CK, ADDR/CMD	
tIH(min-derated)(Informative)	DDR Hold-Diff	CK, ADDR/CMD	
tIS(base)	DDR Setup-Diff	CK, ADDR/CMD	
tIS(derated)	DDR Setup-Diff	CK, ADDR/CMD	
tIS(min-derated)(Informative)	DDR Setup-Diff	CK, ADDR/CMD	
tIS(max-derated)(Informative)	DDR Setup-Diff	CK, ADDR/CMD	
Slew Rate			
Slew Rate-Hold-Fall(Addr/Cmd)	Fall Slew Rate	ADDR/CMD	
Slew Rate-Hold-Rise(Addr/Cmd)	Rise Slew Rate	ADDR/CMD	
Slew Rate-Setup-Fall(Addr/Cmd)	Fall Slew Rate	ADDR/CMD	
Slew Rate-Setup-Rise(Addr/Cmd)	Rise Slew Rate	ADDR/CMD	
Time Above AC Level			

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
tVAC(Addr/Cmd)	Time Outside Level	ADDR/CMD	
Precharge			
tRP(MRS)	tCMD-CMD	Bus, CK	
tRP(ACT)	tCMD-CMD	Bus, CK	
Refresh			
tCKSRE	GDDR5 tCKSRE	Bus [3], CK	
tCKSRX	GDDR5 tCKSRX	Bus, CK	
Overshoot/Undershoot			
AC-Overshoot(DQ)	Overshoot	DQ	DQS
AC-Overshoot(DQS#)	Overshoot	DQS#	DQS,DQ
AC-Overshoot(DQS)	Overshoot	DQS	DQ
AC-OvershootArea(DQ)	AOS Per UI	DQS, DQ	
AC-OvershootArea(DQS#)	AOS	DQS#	DQS,DQ
AC-OvershootArea(DQS)	AOS	DQS	DQ
AC-Undershoot(DQ)	Undershoot	DQ	DQS
AC-Undershoot(DQS#)	Undershoot	DQS#	DQS,DQ
AC-Undershoot(DQS)	Undershoot	DQS	DQ
AC-UndershootArea(DQ)	AUS Per UI	DQS, DQ	
AC-UndershootArea(DQS#)	AUS	DQS#	DQS,DQ
AC-UndershootArea(DQS)	AUS	DQS	DQ

DDR4 measurement sources

The sources required for analysis may include DQS (Strobe), DQS# (Strobe), DQ (Data), Clock, Clock #, and Addr/Cmd. Clock and DQS can be either Single-Ended (SE) or Differential (Diff). Read and Write bursts have CS as an optional source.

The following table lists the sources required for each DDR4 measurement:

Table 13: DDR4 measurement sources

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
Write Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	
DDRARXMask	Mask Hits	DQS, DQ	
Data Pulse Amplitude			

Table continued…

[3] Required digital sources for Bus configuration are: CS#, RAS#, CAS#, WE#.

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
VIHL_AC	DDR VIHLAC	DQS, DQ	
Data Pulse Width			
TdIPW-High	Pos Width	DQ	DQS
TdIPW-Low	Neg Width	DQ	DQS
Data Slew Rate			
srf1	Fall Slew Rate	DQ	DQS
srf2	Fall Slew Rate	DQ	DQS
srr1	Rise Slew Rate	DQ	DQS
srr2	Rise Slew Rate	DQ	DQS
Differential Input Level			
VIHDiffPeak	Cycle Max	DQS	DQ
VILDiffPeak	Cycle Min	DQS	DQ
Differential Strobe			
tDQSH	Pos Width	DQS	DQ
tDQSL	Neg Width	DQS	DQ
tDQSS-Diff	Skew	DQS, CK	DQ
tDSH-Diff	Hold	DQS, CK	DQ
tDSS-Diff	Setup	DQS, CK	DQ
tDVAC(DQS)(Informative)	Time Outside Level	DQS	DQ
tWPRE	DDR tWPRE	DQS	DQ
tWPST	DDR tPST	DQS	DQ
Read Bursts			
Clock-Data			
tHZ(DQ)	DDR tHZDQ	DQ, CK	DQS
tLZ(DQ)	DDR tLZDQ	DQ, CK	DQS
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	
Data Slew Rate			
SRQse-Fall(DQ)	Fall Slew Rate	DQ	DQS
SRQse-Rise(DQ)	Rise Slew Rate	DQ	DQS
Differential Strobe			
tDQSCK-Diff	Skew	DQS, CK	DQ
tDQSQ-Diff	Setup	DQS, DQ	
tDVAC(DQS)(Informative)	Time Outside Level	DQS	DQ
tQH	Hold	DQS, DQ	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
tQSH	Pos Width	DQS	DQ
tQSL	Neg Width	DQS	DQ
tRPRE	DDR tWPRE	DQS	DQ
tRPST	DDR tPST	DQS	DQ
Strobe Slew Rate			
SRQdiff-Fall(DQS)	Fall Slew Rate	DQS	DQ
SRQdiff-Rise(DQS)	Rise Slew Rate	DQS	DQ
DQS(Single Ended, Write)			
AC Level			
VSEH(DQS#)(Informative)	Cycle Max	DQS#	DQS,DQ
VSEH(DQS)(Informative)	Cycle Max	DQS	DQ
VSEL(DQS#)(Informative)	Cycle Min	DQS#	DQS,DQ
VSEL(DQS)(Informative)	Cycle Min	DQS	DQ
Vix(ac)DQS	DDRVix	DQS, DQS#	DQ
DQS(Single Ended, Read)			
AC Level			
VSEH(DQS#)(Informative)	Cycle Max	DQS#	DQS,DQ
VSEH(DQS)(Informative)	Cycle Max	DQS	DQ
VSEL(DQS#)(Informative)	Cycle Min	DQS#	DQS,DQ
VSEL(DQS)(Informative)	Cycle Min	DQS	DQ
Clock-Strobe			
tHZ(DQS)	DDR tHZDQ	DQS, CK	DQ
tLZ(DQS#)	DDR tLZDQ	DQS#, CK	DQS, DQ
Clock(Diff)			
Clock Eye			
Clock Eye Height (Informative)	Height	CK	
Clock Eye Width (Informative)	Width	CK	
Differential Clock			
tCH(abs)	Pos Width	CK	
tCH(avg)	DDR tCH(avg)	CK	
tCK(abs)	Period	CK	
tCK(avg)	DDR tCK(avg)	CK	
tCL(abs)	Neg Width	CK	
tCL(avg)	DDR tCL(avg)	CK	
tDVAC(CK)	Time Outside Level	CK	
tJIT(cc)	CC-Period	CK	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
tJIT(duty) Informative	DDR tJIT(duty)	CK	
tJIT(per)	DDR tJIT(per)	CK	
Slew Rate			
InputSlew-Diff-Fall(CK)	Fall Slew Rate	CK	
InputSlew-Diff-Rise(CK)	Rise Slew Rate	CK	
tERR			
tERR(02per to tERR(50per)	DDR tERR(n)	CK	
Clock(Single Ended)			
AC-Overshoot(AbsMax)(CK#)	Overshoot	CK#	
AC-Overshoot(AbsMax)(CK)	Overshoot	CK	
AC-Overshoot(CK#)	Overshoot	CK#	
AC-Overshoot(CK)	Overshoot	CK	
AC-OvershootArea(AbsMax)(CK#)	AOS	CK#	
AC-OvershootArea(AbsMax)(CK)	AOS	CK	
AC-OvershootArea(CK#)	AOS(AbsMax)	CK#	
AC-OvershootArea(CK)	AOS(AbsMax)	CK	
AC-Undershoot(CK#)	Undershoot	CK#	
AC-Undershoot(CK)	Undershoot	CK	
AC-UndershootArea(CK#)	AUS	CK#	
AC-UndershootArea(CK)	AUS	CK	
Vix(ac)CK	DDR3 Vix(ac)	CK, CK#	
VSEH(CK#)	Cycle Max	CK#	
VSEH(CK)	Cycle Max	CK	
VSEL(CK#)	Cycle Min	CK#	
VSEL(CK)	Cycle Min	CK	
Address/Command			
AC-Overshoot	Overshoot	ADDR/CMD	
AC-Overshoot(AbsMax)	Overshoot	ADDR/CMD	
AC-OvershootArea	AOS(AbsMax) Per tCK	CK, ADDR/CMD	
AC-OvershootArea(AbsMax)	AOS Per tCK	ADDR/CMD,CK	
AC-Undershoot	Undershoot	ADDR/CMD	
AC-UndershootArea	AUS Per tCK	CK, ADDR/CMD	
Pulse Width			
tIPW-High	Pos Width	ADDR/CMD	
tIPW-Low	Neg Width	ADDR/CMD	
Setup and Hold			

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
tIH(base)	DDR Hold-Diff	CK, ADDR/CMD	
tIH(derated)	DDR Hold-Diff	CK, ADDR/CMD	
tIH(Vref)	DDR Hold-Diff(Vref)	CK, ADDR/CMD	
tIS(base)	DDR Setup-Diff	CK, ADDR/CMD	
tIS(derated)	DDR Setup-Diff	CK, ADDR/CMD	
tIS(Vref)	DDR Setup-Diff(Vref)	CK, ADDR/CMD	
Slew Rate			
SRCA_Fall	Fall Slew Rate	ADDR/CMD	
SRCA_Rise	Rise Slew Rate	ADDR/CMD	
Overshoot/Undershoot			
AC-Overshoot(AbsMax)(DQ)	Overshoot	DQ	DQS
AC-Overshoot(AbsMax)(DQS#)	Overshoot	DQS#	DQS,DQ
AC-Overshoot(AbsMax)(DQS)	Overshoot	DQS	DQ
AC-Overshoot(DQ)	Overshoot	DQ	DQS
AC-Overshoot(DQS#)	Overshoot	DQS#	DQS,DQ
AC-Overshoot(DQS)	Overshoot	DQS	DQ
AC-OvershootArea(AbsMax)(DQ)	AOS Per UI	DQS, DQ	
AC-OvershootArea(AbsMax)(DQS#)	AOS	DQS#	DQS,DQ
AC-OvershootArea(AbsMax)(DQS)	AOS	DQS	DQ
AC-OvershootArea(DQ)	AOS(AbsMax) Per UI	DQS, DQ	
AC-OvershootArea(DQS#)	AOS(AbsMax)	DQS#	DQS,DQ
AC-OvershootArea(DQS)	AOS(AbsMax)	DQS	DQ
AC-Undershoot(AbsMax)(DQ)	Undershoot	DQ	DQS
AC-Undershoot(AbsMax)(DQS#)	Undershoot	DQS#	DQS,DQ
AC-Undershoot(AbsMax)(DQS)	Undershoot	DQS	DQ
AC-Undershoot(DQ)	Undershoot	DQ	DQS
AC-Undershoot(DQS#)	Undershoot	DQS#	DQS,DQ
AC-Undershoot(DQS)	Undershoot	DQS	DQ
AC-UndershootArea(AbsMax)(DQ)	AUS Per UI	DQS, DQ	
AC-UndershootArea(AbsMax)(DQS#)	AUS	DQS#	DQS,DQ
AC-UndershootArea(AbsMax)(DQS)	AUS	DQS	DQ
AC-UndershootArea(DQ)	AUS(AbsMax)Per UI	DQS, DQ	
AC-UndershootArea(DQS#)	AUS(AbsMax)	DQS#	DQS,DQ
AC-UndershootArea(DQS)	AUS(AbsMax)	DQS	DQ

GDDR3 measurement sources

The sources required for analysis may include DQ, DQS.

Table 14: GDDR3 measurement sources

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
Write Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQ, DQS	
Read Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	

GDDR5 measurement sources

The sources required for analysis may include DQ, WCK, WCK#, CK, CK#,WE, CS, CAS, RAS, CKE, and Addr/Cmd.

The following table lists the sources required for each GDDR5 measurement:

Table 15: GDDR5 measurement sources

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
Write Bursts			
Data Eye			
Data Eye Height	Height	DQ, WCK	
Data Eye Width	Width	DQ, WCK	
tWRPDE	GDDR5 tBurst-CMD	Bus, [3]WCK	
tWRSRE	GDDR5 tBurst-CMD	Bus [3], WCK	
Read Bursts			
Data Eye			
Data Eye Height	Height	DQ, WCK	
Data Eye Width	Width	DQ, WCK	
tRDPDE	GDDR5 tBurst-CMD	Bus, [3]WCK	
tRDSRE	GDDR5 tBurst-CMD	Bus, [3] WCK	
Clock(Diff)			
Clock Eye			
Clock Eye Height (Informative)	Height	CK	
Clock Eye Width (Informative)	Width	CK	
SSC Downspread(CK)	SSC Freq Dev	CK	
SSC Mod Freq(CK)	SSC Mod Rate	CK	
SSC Profile(CK)	SSC Profile	CK	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
tCH	Pos Width	CK	
tCK	Period	CK	
tCL	Neg Width	CK	
tDVAC(CK)	Time Outside Level	CK	
tHP	Period	CK	
tJIT(cc)	CC-Period	CK	
tJIT(per)	DDR tJIT(per)	CK	
Clock(Single Ended)			
CKSlew-Fall(CK#)	Fall Slew Rate	CK#	
CKSlew-Fall(CK)	Fall Slew Rate	CK	
CKSlew-Rise(CK#)	Rise Slew Rate	CK#	
CKSlew-Rise(CK)	Rise Slew Rate	CK	
VIN(CK#)	High-Low	CK#	
VIN(CK)	High-Low	CK	
Vix(ac)CK	V-Diff-Xovr	CK, CK#	
Address/Command			
tAH	Setup	CK, ADDR/CMD	
tAPW	Period	ADDR/CMD	
tAS	Setup	CK, ADDR/CMD	
tCMDH	Setup	CK, ADDR/CMD	
tCMDPW	Period	ADDR/CMD	
tCMDS	Setup	CK, ADDR/CMD	
Precharge			
tPPD	tCMD-CMD	Bus, ^{3}CK	
tRP(ACT)	tCMD-CMD	Bus, ^{3}CK	
tRP(MRS)	tCMD-CMD	Bus, ^{3}CK	
tRP(REF)	tCMD-CMD	Bus, ^{3}CK	
tRP(SRE)	tCMD-CMD	Bus, ^{3}CK	
tRTPL	tCMD-CMD	Bus, ^{3}CK	
Refresh			
tCKSRE	GDDR5 tCKSRE	Bus, ^{3}CK	
tCKSRX	GDDR5 tCKSRX	Bus, ^{3}CK	
tREFTR(Read)	tCMD-CMD	Bus, ^{3}CK	
tREFTR(Write)	tCMD-CMD	Bus, ^{3}CK	
tRFC	tCMD-CMD	Bus,^{3} CK	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
tXSNRW	tCMD-CMD	Bus,3CK	
Active			
tRAS	tCMD-CMD	Bus,3CK	
tRC	tCMD-CMD	Bus, 3CK	
tRCDRD	tCMD-CMD	Bus,3 CK	
tRCDWR	tCMD-CMD	Bus, 3CK	
Power Down			
tPD	tCMD-CMD	Bus, 3CK	
WCK(Diff)			
SSC Downspread(WCK)	SSC Freq Dev	WCK	
SSC Mod Freq(WCK)	SSC Mod Rate	WCK	
SSC Profile(WCK)	SSC Profile	WCK	
tDVAC(WCK)	Time Outside Level	WCK	
tJIT(cc)	CC-Period	WCK	
tJIT(per)	DDR tJIT(per)	WCK	
tWCK	Period	WCK	
tWCK-DJ	DJ	WCK	
tWCK-Fall-Slew	Fall Slew Rate	WCK	
tWCKH	Pos Width	WCK	
tWCKHP	Period	WCK	
tWCKL	Neg Width	WCK	
tWCK-Rise-Slew	Rise Slew Rate	WCK	
tWCK-RJ	RJ	WCK	
tWCK-TJ	TJ@BER	WCK	
VWCK-SWING	High-Low	WCK	
WCK(Single Ended)			
Slew Rate			
WCKSlew-Fall(WCK#)	Fall Slew Rate	WCK#	
WCKSlew-Fall(WCK)	Fall Slew Rate	WCK	
WCKSlew-Rise(WCK#)	Rise Slew Rate	WCK#	
WCKSlew-Rise(WCK)	Rise Slew Rate	WCK	
VIN-VIX			
VIN(WCK#)	High-Low	WCK#	
VIN(WCK)	High-Low	WCK	
Vix(ac)WCK	V-Diff-Xovr	WCK, WCK#	
VOH-VOL			

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
VOH(WCK#)	High	WCK#	
VOH(WCK)	High	WCK	
VOL(WCK#)	Low	WCK#	
VOL(WCK)	Low	WCK	

LPDDR measurement sources

The sources required for analysis may include DQS (Strobe), DQS# (Strobe), DQ (Data), Clock, Clock #, and Addr/Cmd. Clock and DQS can be either Single-Ended (SE) or Differential (Diff). Read and Write bursts have CS as an optional source.

The following table lists the sources required for each LPDDR measurement:

Table 16: LPDDR measurement sources

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
Write Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQ, DQS	
Data Pulse Width			
tDIPW-High	Pos Width	DQ	DQS
tDIPW-Low	Neg Width	DQ	DQS
Digital Bus Measurement			
tDQSS	DDR tDQSS	Bus [3], DQS	DQ
Setup and Hold			
tDH-Diff(base)	DDR Hold-Diff	DQS, DQ	
tDS-Diff(base)	DDR Setup-Diff	DQS, DQ	
Strobe Measurements			
tDQSH	Pos Width	DQS	DQ
tDQSL	Neg Width	DQS	DQ
tDSH-Diff	Hold	DQS, CK	DQ
tDSS-Diff	Setup	DQS, CK	DQ
tWPRE	DDR tRPRE	DQS	DQ
tWPST	DDR tPST	DQS	DQ
Read Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	
Strobe Measurements			

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
tAC-Diff	DDR Setup-Diff	DQ, CK	DQS
tDQSCK-Diff	Skew	DQS, CK	DQ
tQH	Hold	DQS, DQ	
tRPRE	DDR tRPRE	DQS	DQ
tRPST	DDR tPST	DQS	DQ
DQS(Single Ended, Write)			
Clock-Strobe			
tDSH(DQS)(Informative)	Hold	DQS, CK	DQ
tDSS(DQS)(Informative)	Setup	DQS, CK	DQ
Setup and Hold			
tDH(DQS)(Informative)	Hold	DQS, DQ	
tDS(DQS)(Informative)	Setup	DQS, DQ	
DQS(Single Ended, Read)			
DQS-DQ Skew			
tDQSQ(DQS)	Setup	DQS, DQ	
Clock(Diff)			
Clock Eye			
Clock Eye Height (Informative)	Height	CK	
Clock Eye Width (Informative)	Width	CK	
tCH	Pos Width	CK	
tCK	Period	CK	
tCL	Neg Width	CK	
tHP	Period	CK	
VID(ac)	DDR VID(ac)	CK	
Clock(Single Ended)			
AC-Overshoot(CK#)	Overshoot	CK#	
AC-Overshoot(CK)	Overshoot	CK	
AC-OvershootArea(CK#)	AOS	CK#	
AC-OvershootArea(CK)	AOS	CK	
AC-Undershoot(CK#)	Undershoot	CK#	
AC-Undershoot(CK)	Undershoot	CK	
AC-UndershootArea(CK#)	AUS	CK#	
AC-UndershootArea(CK)	AUS	CK	
Vix(ac)CK	V-Diff-Xovr	CK, CK#	
Address/Command			
AC-Overshoot	Overshoot	ADDR/CMD	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
AC-OvershootArea	AOS Per tCK	CK, ADDR/CMD	
AC-Undershoot	Undershoot	ADDR/CMD	
AC-UndershootArea	AUS Per tCK	CK, ADDR/CMD	
Pulse Width			
tIPW-High	Pos Width	ADDR/CMD	
tIPW-Low	Neg Width	ADDR/CMD	
Setup and Hold			
tIH(base)	DDR Hold-Diff	CK, ADDR/CMD	
tIS(base)	DDR Setup-Diff	CK, ADDR/CMD	
Overshoot/Undershoot			
AC-Overshoot(DQ)	Overshoot	DQ	DQS
AC-Overshoot(DQS)	Overshoot	DQS	DQ
AC-OvershootArea(DQ)	AOS Per UI	DQS, DQ	
AC-OvershootArea(DQS)	AOS	DQS	DQ
AC-Undershoot(DQ)	Undershoot	DQ	DQS
AC-Undershoot(DQS)	Undershoot	DQS	DQ
AC-UndershootArea(DQ)	AUS Per UI	DQS, DQ	
AC-UndershootArea(DQS)	AUS	DQS	DQ

LPDDR2 measurement sources

The sources required for analysis may include DQS (Strobe), DQS# (Strobe), DQ (Data), Clock, Clock #, and Addr/Cmd. DQS and Clock can be either Single-Ended (SE) or Differential (Diff). Read and Write bursts have CS as an optional source.

The following table lists the sources required for each LPDDR2 measurement:

Table 17: LPDDR2 measurement sources

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
Write Bursts			
Data Eye			
Data Eye Width	Width	DQ, DQS	
Data Eye Height	Height	DQS, DQ	
Data Pulse Width			
tDIPW-High	Pos Width	DQ	DQS
tDIPW-Low	Neg Width	DQ	DQS
Data Slew Rate			
Slew Rate-Setup-Fall(DQ)	Fall Slew Rate	DQ	DQS
Slew Rate-Setup-Rise(DQ)	Rise Slew Rate	DQ	DQS

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
Slew Rate-Hold-Fall(DQ)	Fall Slew Rate	DQ	DQS
Slew Rate-Hold-Rise(DQ)	Rise Slew Rate	DQ	DQS
Differential Strobe			
tDSS-Diff	Setup	DQS, CK	DQ
tDSH-Diff	Hold	DQS, CK	DQ
tDQSH	Pos Width	DQS	DQ
tDQSL	Neg Width	DQS	DQ
tWPRE	DDR tWPRE	DQS	DQ
tWPST	DDR tPST	DQS	DQ
tDVAC(DQS)	Time Outside Level	DQS	DQ
Digital Bus Measurement			
tDQSS	DDR tDQSS	Bus, DQS	DQ
Setup and Hold			
tDH-Diff(base)	DDR Hold-Diff	DQS, DQ	
tDH-Diff(derated)	DDR Hold-Diff	DQS, DQ	
tDH-Diff(max-derated)(Informative)	DDR Hold-Diff	DQS, DQ	
tDH-Diff(min-derated)(Informative)	DDR Hold-Diff	DQS, DQ	
tDH-Diff(Vref-based)	Hold	DQS, DQ	
tDS-Diff(base)	DDR Setup-Diff	DQS, DQ	
tDS-Diff(derated)	DDR Setup-Diff	DQS, DQ	
tDS-Diff(max-derated)(Informative)	DDR Setup-Diff	DQS, DQ	
tDS-Diff(min-derated)(Informative)	DDR Setup-Diff	DQS, DQ	
tDS-Diff(Vref-based)	Setup	DQS, DQ	
Strobe Slew Rate			
InputSlew-Diff-Fall(DQS)	Fall Slew Rate	DQS	DQ
InputSlew-Diff-Rise(DQS)	Rise Slew Rate	DQS	DQ
Read Bursts			
Clock-Data			
tHZ(DQ)	DDR tHZDQ	DQ, CK	DQS
tLZ(DQ)	DDR tLZDQ	DQ, CK	DQS
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	
Data Pulse Width			
tDIPW-High	Pos Width	DQ	DQS
tDIPW-Low	Neg Width	DQ	DQS

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
Data Slew Rate			
SRQse-Fall(DQ)	Fall Slew Rate	DQ	DQS
SRQse-Rise(DQ)	Rise Slew Rate	DQ	DQS
Differential Strobe			
tDQSCK	DDR2 tDQSCK	DQS, CK	DQ
tDQSQ-Diff	Setup	DQS, DQ	
tDVAC(DQS)	Time Outside Level	DQS	DQ
tQH	Hold	DQS, DQ	
tQSH	Pos Width	DQS	DQ
tQSL	Neg Width	DQS	DQ
tRPRE	DDR tRPRE	DQS	DQ
tRPST	DDR tPST	DQS	DQ
Strobe Slew Rate			
SRQdiff-Fall(DQS)	Fall Slew Rate	DQS	DQ
SRQdiff-Rise(DQS)	Rise Slew Rate	DQS	DQ
DQS(Single Ended, Write)			
VIXDQ	DDR3 Vix(ac)	DQS, DQS#	DQ
VSEH(AC)DQS	Cycle Max	DQS	DQ
VSEH(AC)DQS#	Cycle Max	DQS#	DQS,DQ
VSEL(AC)DQS	DDR Cycle Min	DQS	DQ
VSEL(AC)DQS#	DDR Cycle Min	DQS#	DQS,DQ
DQS(Single Ended, Read)			
Clock-Strobe			
tHZ(DQS)	DDR tHZDQ	DQS, CK	DQ
Clock(Diff)			
Clock Eye			
Clock Eye Height (Informative)	Height	CK	
Clock Eye Width (Informative)	Width	CK	
Differential Clock			
tCH(abs)	Pos Width	CK	
tCH(avg)	DDR tCH(avg)	CK	
tCK(abs)	Period	CK	
tCK(avg)	DDR tCK(avg)	CK	
tCL(abs)	Neg Width	CK	
tCL(avg)	DDR tCL(avg)	CK	
tDVAC(CK)	Time Outside Level	CK	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
tHP	Period	CK	
tJIT(cc)	CC-Period	CK	
tJIT(duty)	DDR tJIT(duty)	CK	
tJIT(per)	DDR tJIT(per)	CK	
Slew Rate			
InputSlew-Diff-Fall(CK)	Fall Slew Rate	CK	
InputSlew-Diff-Rise(CK)	Rise Slew Rate	CK	
tERR			
tERR(02per) to tERR(50per)	DDR tERR(n)	CK	
Clock(Single Ended)			
AC-Overshoot(CK#)	Overshoot	CK#	
AC-Overshoot(CK)	Overshoot	CK	
AC-OvershootArea(CK#)	AOS	CK#	
AC-OvershootArea(CK)	AOS	CK	
AC-Undershoot(CK#)	Undershoot	CK#	
AC-Undershoot(CK)	Undershoot	CK	
AC-UndershootArea(CK#)	AUS	CK#	
AC-UndershootArea(CK)	AUS	CK	
VIXCA	DDR3 Vix(ac)	CK, CK#	
VSEH(AC)CK	Cycle Max	CK	
VSEH(AC)CK#	Cycle Max	CK#	
VSEL(AC)CK	DDR Cycle Min	CK	
VSEL(AC)CK#	DDR Cycle Min	CK#	
Address/Command			
AC-Overshoot	Overshoot	ADDR/CMD	
AC-OvershootArea	AOS Per UI	CK, ADDR/CMD	
AC-Undershoot	Undershoot	ADDR/CMD	
AC-UndershootArea	AUS Per UI	CK, ADDR/CMD	
Digital Bus Measurement			
tCCDRD	tCMD-CMD	Bus, CK	
tCCDWR	tCMD-CMD	Bus, CK	
Pulse Width			
tIPW-High	Pos Width	ADDR/CMD	
tIPW-Low	Neg Width	ADDR/CMD	
Setup and Hold			
tIH(base)	DDR Hold-Diff	CK, ADDR/CMD	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
tIH(derated)	DDR Hold-Diff	CK, ADDR/CMD	
tIH(max-derated)(Informative)	DDR Hold-Diff	CK, ADDR/CMD	
tIH(min-derated)(Informative)	DDR Hold-Diff	CK, ADDR/CMD	
tIH(Vref-based)	Hold	CK, ADDR/CMD	
tIS(base)	DDR Setup-Diff	CK, ADDR/CMD	
tIS(derated)	DDR Setup-Diff	CK, ADDR/CMD	
tIS(max-derated)(Informative)	DDR Setup-Diff	CK, ADDR/CMD	
tIS(min-derated)(Informative)	DDR Setup-Diff	CK, ADDR/CMD	
tIS(Vref-based)	Setup	CK, ADDR/CMD	
Slew Rate			
Slew Rate-Hold-Fall(Addr/Cmd)	Fall Slew Rate	ADDR/CMD	
Slew Rate-Hold-Rise(Addr/Cmd)	Rise Slew Rate	ADDR/CMD	
Slew Rate-Setup-Fall(Addr/Cmd)	Fall Slew Rate	ADDR/CMD	
Slew Rate-Setup-Rise(Addr/Cmd)	Rise Slew Rate	ADDR/CMD	
Precharge			
tRP	tCMD-CMD	Bus, CK	
tRTP	tCMD-CMD	Bus, CK	
Active			
tRAS	tCMD-CMD	Bus, CK	
tRC	tCMD-CMD	Bus, CK	
tRCDRD	tCMD-CMD	Bus, CK	
tRCDWR	tCMD-CMD	Bus, CK	
Overshoot/Undershoot			
AC-Overshoot(DQ)	Overshoot	DQ	DQS
AC-Overshoot(DQS#)	Overshoot	DQS#	DQS,DQ
AC-Overshoot(DQS)	Overshoot	DQS	DQ
AC-OvershootArea(DQ)	AOS Per UI	DQS, DQ	
AC-OvershootArea(DQS#)	AOS	DQS#	DQS,DQ
AC-OvershootArea(DQS)	AOS	DQS	DQ
AC-Undershoot(DQ)	Undershoot	DQ	DQS
AC-Undershoot(DQS#)	Undershoot	DQS#	DQS,DQ
AC-Undershoot(DQS)	Undershoot	DQS	DQ
AC-UndershootArea(DQ)	AUS Per UI	DQS, DQ	
AC-UndershootArea(DQS#)	AUS	DQS#	DQS,DQ
AC-UndershootArea(DQS)	AUS	DQS	DQ

Note:

1. Additional resources are required so that the Search-and-Mark feature can properly identify bursts.

2. VSSQ/VSSCA values for VSEL(AC)CK, VSEL(AC)CK#, VSEL(AC)DQS and VSEL(AC)DQS# measurements can be configured through DPOJET configuration panel.
3. Overshoot area and Undershoot area are measured over one unit interval (i.e. half clock cycle) of address/command signal.
4. Required digital sources for Bus configuration are: CS_n, CA0, CA1, CA2, CA3. CA3 is required only in case of 'Precharge' measurement type. For all other measurements, only four digital signals (CS, CA0, CA1 and CA2) are sufficient to be probed. However, you have to configure the bus with all five signals with CA3 connected to ground.

LPDDR3 measurement sources

The sources required for analysis may include DQS (Strobe), DQS# (Strobe), DQ (Data), Clock, Clock #, and Addr/Cmd. Clock and DQS can be either Single-Ended (SE) or Differential (Diff). Read and Write bursts have CS as an optional source.

The following table lists the sources required for each LPDDR3 measurement:

Table 18: LPDDR3 measurement sources

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
Write Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	
Data Pulse Width			
tDIPW-High	Pos Width	DQ	DQS
tDIPW-Low	Neg Width	DQ	DQS
Data Slew Rate			
Slew Rate-Hold-Fall(DQ)	Fall Slew Rate	DQ	DQS
Slew Rate-Hold-Rise(DQ)	Rise Slew Rate	DQ	DQS
Slew Rate-Setup-Fall(DQ)	Fall Slew Rate	DQ	DQS
Slew Rate-Setup-Rise(DQ)	Rise Slew Rate	DQ	DQS
Differential Strobe			
tDQSH	Pos Width	DQS	DQ
tDQSL	Neg Width	DQS	DQ
tDSH-Diff	Hold	DQS, CK	DQ
tDSS-Diff	Setup	DQS, CK	DQ
tDVAC(DQS)	Time Outside Level	DQS	DQ
tWPRE	DDR tWPRE	DQS	DQ
tWPST	DDR tPST	DQS	DQ
Digital Bus Measurement			
tDQSS	DDR tDQSS	Bus, DQS	DQ
Setup and Hold			
tDH-Diff(base)	DDR Hold-Diff	DQS, DQ	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
tDH-Diff(derated)	DDR Hold-Diff	DQS, DQ	
tDH-Diff(Vref-based)	Hold	DQS, DQ	
tDS-Diff(base)	DDR Setup-Diff	DQS, DQ	
tDS-Diff(derated)	DDR Setup-Diff	DQS, DQ	
tDS-Diff(Vref-based)	Setup	DQS, DQ	
Strobe Slew Rate			
InputSlew-Diff-Fall(DQS)	Fall Slew Rate	DQS	DQ
InputSlew-Diff-Rise(DQS)	Rise Slew Rate	DQS	DQ
Read Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	
Data Slew Rate			
SRQse-Fall(DQ)	Fall Slew Rate	DQ	DQS
SRQse-Rise(DQ)	Rise Slew Rate	DQ	DQS
Differential Strobe			
tDQSCK	DDR2 tDQSCK	DQS, CK	DQ
tDQSQ-Diff	Setup	DQS, DQ	
tDVAC(DQS)	Time Outside Level	DQS	DQ
tQH	Hold	DQS, DQ	
tQSH	Pos Width	DQS	DQ
tQSL	Neg Width	DQS	DQ
tRPRE	DDR tRPRE	DQS	DQ
tRPST	DDR tPST	DQS	DQ
Strobe Slew Rate			
SRQdiff-Fall(DQS)	Fall Slew Rate	DQS	DQ
SRQdiff-Rise(DQS)	Rise Slew Rate	DQS	DQ
DQS(Single Ended, Write)			
Vix(ac)DQS	DDR3Vix(ac)	DQS, DQS#	DQ
VSEH(AC)DQS	Cycle Max	DQS	DQ
VSEH(AC)DQS#	Cycle Max	DQS#	DQS,DQ
VSEL(AC)DQS	DDR Cycle Min	DQS	DQ
VSEL(AC)DQS#	DDR Cycle Min	DQS#	DQS,DQ
Clock(Diff)			
Clock Eye			
Clock Eye Height (Informative)	Height	CK	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
Clock Eye Width (Informative)	Width	CK	
Differential Clock			
tCH(abs)	Pos Width	CK	
tCH(avg)	DDR tCH(avg)	CK	
tCK(abs)	Period	CK	
tCK(avg)	DDR tCK(avg)	CK	
tCL(abs)	Neg Width	CK	
tCL(avg)	DDR tCL(avg)	CK	
tDVAC(CK)	Time Outside Level	CK	
tJIT(cc)	CC-Period	CK	
tJIT(duty)	DDR tJIT(duty)	CK	
tJIT(per)	DDR tJIT(per)	CK	
Slew Rate			
InputSlew-Diff-Fall(CK)	Fall Slew Rate	CK	
InputSlew-Diff-Rise(CK)	Rise Slew Rate	CK	
tERR			
tERR(02per) to tERR(20per)	DDR tERR(n)	CK	
Clock(Single Ended)			
AC-Overshoot(CK#)	Overshoot	CK#	
AC-Overshoot(CK)	Overshoot	CK	
AC-OvershootArea(CK#)	AOS	CK#	
AC-OvershootArea(CK)	AOS	CK	
AC-Undershoot(CK#)	Undershoot	CK#	
AC-Undershoot(CK)	Undershoot	CK	
AC-UndershootArea(CK#)	AUS	CK#	
AC-UndershootArea(CK)	AUS	CK	
Vix(ac)CK	DDD3 Vix(ac)	CK, CK#	
VSEH(AC)CK	Cycle Max	CK	
VSEH(AC)CK#	Cycle Max	CK#	
VSEL(AC)CK	DDR Cycle Min	CK	
VSEL(AC)CK#	DDR Cycle Min	CK#	
Address/Command [4]			
AC-Overshoot	Overshoot	ADDR/CMD	
AC-OvershootArea	AOS Per UI	CK, ADDR/CMD	
AC-Undershoot	Undershoot	ADDR/CMD	

Table continued…

[4] CA and CS measurements selection is mutually exclusive. See Note 5

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional**
AC-UndershootArea	AOS Per UI	CK, ADDR/CMD	
Pulse Width (CA)			
tIPW-High(CA)	High Time	ADDR/CMD	
tIPW-Low(CA)	Low Time	ADDR/CMD	
Pulse Width (CS)			
tIPW-High(CS)	High Time	ADDR/CMD	
tIPW-Low(CS)	Low Time	ADDR/CMD	
Setup and Hold (CA)			
tIH(base)CA	DDR Hold-Diff	CK, ADDR/CMD	
tIH(derated)CA	DDR Hold-Diff	CK, ADDR/CMD	
tIS(base)CA	DDR Setup-Diff	CK, ADDR/CMD	
tIS(derated)CA	DDR Setup-Diff	CK, ADDR/CMD	
Setup and Hold (CS)			
tIH(base)CS	DDR Hold-Diff	CK, ADDR/CMD	
tIH(derated)CS	DDR Hold-Diff	CK, ADDR/CMD	
tIS(base)CS	DDR Setup-Diff	CK, ADDR/CMD	
tIS(derated)CS	DDR Setup-Diff	CK, ADDR/CMD	
Slew Rate			
Slew Rate-Hold-Fall(Addr/Cmd)	Fall Slew Rate	ADDR/CMD	
Slew Rate-Hold-Rise(Addr/Cmd)	Rise Slew Rate	ADDR/CMD	
Slew Rate-Setup-Fall(Addr/Cmd)	Fall Slew Rate	ADDR/CMD	
Slew Rate-Setup-Rise(Addr/Cmd)	Rise Slew Rate	ADDR/CMD	
Refresh			
tCKSRE	GDDR5 tCKSRE	Bus, CK	
tCKSRX	GDDR5 tCKSRX	Bus, CK	
Overshoot/Undershoot			
AC-Overshoot(DQ)	Overshoot	DQ	DQS
AC-Overshoot(DQS#)	Overshoot	DQS#	DQS,DQ
AC-Overshoot(DQS)	Overshoot	DQS	DQ
AC-OvershootArea(DQ)	AOS Per UI	DQS, DQ	
AC-OvershootArea(DQS#)	AOS	DQS#	DQS,DQ
AC-OvershootArea(DQS)	AOS	DQS	DQ
AC-Undershoot(DQ)	Undershoot	DQ	DQS
AC-Undershoot(DQS#)	Undershoot	DQS#	DQS,DQ
AC-Undershoot(DQS)	Undershoot	DQS	DQ
AC-UndershootArea(DQ)	AUS Per UI	DQS, DQ	
AC-UndershootArea(DQS#)	AUS	DQS#	DQS,DQ

Table continued…

Measurement name		Required signal sources	
DDRA	DPOJET	Performed on	Additional
AC-UndershootArea(DQS)	AUS	DQS	DQ

Note:

1. Additional resources are required so that the Search-and-Mark feature can properly identify bursts.
2. VSSQ/VSSCA values for VSEL(AC)CK, VSEL(AC)CK#, VSEL(AC)DQS and VSEL(AC)DQS# measurements can be configured through DPOJET configuration panel.
3. Undershoot area are measured over one unit interval (i.e. half clock cycle) of address/command signal.
4. Required digital sources for Bus configuration are: CS_n, CA0, CA1, CA2.
5. *Pulse With (CS)* and *Setup and Hold (CS)* group measurements cannot be selected when either *Pulse Width (CA)* or *Setup and Hold (CA)* measurements are selected and vice-versa.

LPDDR4/LPDDR4X measurement sources

The sources required for analysis may include DQS (Strobe), DQS# (Strobe), DQ (Data), Clock, Clock #, and Addr/Cmd. DQ and DQS can be either Single-Ended (SE) or Differential (Diff). Read and Write bursts have CS as an optional source.

The following table lists the sources required for each LPDDR4/LPDDR4X measurement:

Table 19: LPDDR4/LPDDR4X measurement sources

Measurement name		Required signal sources	
DDRA	DPOJET	Performed on	Additional [2]
Write Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	
DDRARXMask	Mask Hits	DQS, DQ	
AutoFitRxMask(Informative)	AutoFit Mask Hits	DQS, DQ	
Data Pulse Amplitude			
VIHL_AC	DDR VIHLAC	DQS, DQ	
Data Pulse Width			
TdIPW-High	Pos Width	DQ	DQS
TdIPW-Low	Neg Width	DQ	DQS
Data Slew Rate			
SRIN_dIVW_Fall	Fall Slew Rate	DQ	DQS
SRIN_dIVW_Rise	Rise Slew Rate	DQ	DQS
Differential Strobe			
tDQS2DQ	DDR tDQS2DQ	DQS, DQ	
tDQSH	Pos Width	DQS	DQ
tDQSL	Neg Width	DQS	DQ
tDSH-Diff	Hold	DQS, CK	DQ
tDSS-Diff	Setup	DQS, CK	DQ

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional [2]**
tWPRE	LPDDR4tWPRE	DQS	DQ
tWPST	DDR tPST	DQS	DQ
Digital Bus Measurement			
tDQSS	DDR tDQSS	Bus [3], DQS	DQ
Strobe Slew Rate			
InputSlew-Diff-Fall(DQS)	Fall Slew Rate	DQS	DQ
InputSlew-Diff-Rise(DQS)	Rise Slew Rate	DQS	DQ
Differential Input Level			
VIHdiff(AC) Informative	Cycle Max	DQS	DQ
VILdiff(AC) Informative	Cycle Min	DQS	DQ
Read Bursts			
Data Eye			
Data Eye Height	Height	DQS, DQ	
Data Eye Width	Width	DQS, DQ	
Data Slew Rate			
SRQse-Fall(DQ)	Fall Slew Rate	DQ	DQS
SRQse-Rise(DQ)	Rise Slew Rate	DQ	DQS
Differential Strobe			
tDQSCK	DDR2 tDQSCK	DQS, CK	DQ
tDQSQ-DBI	Setup	DQS, DQ	
tDQSQ-Diff	Setup	DQS, DQ	
tQH	Hold	DQS, DQ	
tQH_DBI	Hold	DQS, DQ	
tQSH	Pos Width	DQS	DQ
tQSH_DBI	Pos Width	DQS	DQ
tQSL	Neg Width	DQS	DQ
tQSL_DBI	Neg Width	DQS	DQ
tQW_Total	Width	DQS, DQ	
tQW_Total_DBI	Width	DQS, DQ	
tRPRE	DDR tRPRE	DQS	DQ
tRPST	DDR tPST	DQS	DQ
Strobe Slew Rate			
SRQdiff-Fall(DQS)	Fall Slew Rate	DQS	DQ
SRQdiff-Rise(DQS)	Rise Slew Rate	DQS	DQ
DQS(Single Ended, Write)			
AC Level			

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
VSEH(AC)DQS#(Informative)	Cycle Max	DQS#	DQS,DQ
VSEH(AC)DQS(Informative)	Cycle Max	DQS	DQ
VSEL(AC)DQS#(Informative)	Cycle Min	DQS#	DQS,DQ
VSEL(AC)DQS(Informative)	Cycle Min	DQS	DQ
Clock(Diff)			
Clock Eye			
Clock Eye Height (Informative)	Height	CK	
Clock Eye Width (Informative)	Width	CK	
Differential Clock			
tCH(abs)	Pos Width	CK	
tCH(avg)	DDR tCH(avg)	CK	
tCK(abs)	Period	CK	
tCK(avg)	DDR tCK(avg)	CK	
tCL(abs)	Neg Width	CK	
tCL(avg)	DDR tCL(avg)	CK	
tJIT(cc)	CC-Period	CK	
tJIT(duty)	DDR tJIT(duty)	CK	
tJIT(per)	DDR tJIT(per)	CK	
Slew Rate			
InputSlew-Diff-Fall(CK)	Fall Slew Rate	CK	
InputSlew-Diff-Rise(CK)	Rise Slew Rate	CK	
Differential Input Level			
VIHdiff(AC) Informative	Cycle Max	CK	
VILdiff(AC) Informative	Cycle Min	CK	
Clock(Single Ended)			
AC Level			
VSEH(CK#)(Informative)	Cycle Max	CK#	
VSEH(CK)(Informative)	Cycle Max	CK	
VSEL(CK#)(Informative)	Cycle Min	CK#	
VSEL(CK)(Informative)	Cycle Min	CK	
AC-Overshoot(CK#)	Overshoot	CK#	
AC-Overshoot(CK)	Overshoot	CK	
AC-OvershootArea(CK#)	AOS	CK#	
AC-OvershootArea(CK)	AOS	CK	
AC-Undershoot(CK#)	Undershoot	CK#	
AC-Undershoot(CK)	Undershoot	CK	

Table continued…

Measurement name		Required signal sources	
DDRA	**DPOJET**	**Performed on**	**Additional** [2]
AC-UndershootArea(CK#)	AUS	CK#	
AC-UndershootArea(CK)	AUS	CK	
Vix(ac)CK	DDRVix	CK, CK#	
Address/Command			
AC-Overshoot	Overshoot	ADDR/CMD	
AC-OvershootArea	AOS Per tCK	CK, ADDR/CMD	
AC-Undershoot	Undershoot	ADDR/CMD	
AC-UndershootArea	AUS Per tCK	CK, ADDR/CMD	
Pulse Amplitude			
VIHL_AC(CA)	DDR VIHLAC	CK, ADDR/CMD	
Pulse Width			
TCIPW-High	Pos Width	ADDR/CMD	
TCIPW-Low	Neg Width	ADDR/CMD	
Rx Mask			
AutoFitRxMask(Informative)	Autofit Mask Hits	CK, ADDR/CMD	
DDRARXMask	Mask Hits	CK, ADDR/CMD	
Slew Rate			
SRIN_cIVW_Fall	Fall Slew Rate	ADDR/CMD	
SRIN_cIVW_Rise	Rise Slew Rate	ADDR/CMD	
Overshoot/Undershoot			
AC-Overshoot(DQ)	Overshoot	DQ	DQS
AC-Overshoot(DQS#)	Overshoot	DQS#	DQS,DQ
AC-Overshoot(DQS)	Overshoot	DQS	DQ
AC-OvershootArea(DQ)	AOS Per UI	DQS, DQ	
AC-OvershootArea(DQS#)	AOS	DQS#	DQS,DQ
AC-OvershootArea(DQS)	AOS	DQS	DQ
AC-Undershoot(DQ)	Undershoot	DQ	DQS
AC-Undershoot(DQS#)	Undershoot	DQS#	DQS,DQ
AC-Undershoot(DQS)	Undershoot	DQS	DQ
AC-UndershootArea(DQ)	AUS Per UI	DQS, DQ	
AC-UndershootArea(DQS#)	AUS	DQS#	DQS,DQ
AC-UndershootArea(DQS)	AUS	DQS	DQ

Measurement range limits

The following tables lists the measurement range limits of DDR measurements for different data rates:

Note: Measurement range limits are provided for each measurement under the General configure tab of the DPOJET application. These range limits are always ON (OFF is disabled) for two source measurements such as

Skew, Setup, Hold, and others. The range limits are used by the algorithms to associate valid edge of first source to the valid edge of the second source.

Data Rate	1 UI	2 UI
200 MT/s	5 ns	10 ns
266 MT/s	3.7594 ns	7.5188 ns
333 MT/s	3.003 ns	6.006 ns
370 MT/s	2.702 ns	5.404 ns
400 MT/s	2.5 ns	5 ns
533 MT/s	1.875 ns	3.75 ns
667 MT/s	1.4995 ns	2.999 ns
800 MT/s	1.25 ns	2.5 ns
1333 MT/s	0.75 ns	1.5 ns
1600 MT/s	0.625 ns	1.25 ns
1866 MT/s	0.535 ns	1.071 ns
2133 MT/s	0.468 ns	0.937 ns
2400 MT/s	416.66 ps	833.33 ps
2933 MT/s	340.94 ps	681.89 ps
3200 MT/s	312.5 ps	625 ps
4266 MT/s	234.41 ps	468.82 ps

The following measurements (not complete list) have different range limits as shown:

Table 20: Measurement range limits

Measurement	Maximum	Minimum
tDQSCK-Diff	UI	–UI
tDQSQ-Diff	UI / 2	–UI / 2
tAC-Diff	UI / 2	–UI / 2
tDQSCK	UI	–UI
tDQSQ	UI / 2	–UI / 2

Table continued…

Measurement	Maximum	Minimum
tDH-Diff(base)	UI	0
tDH-Diff(derated)	UI	0
tDQSS-Diff	UI	–UI
tDS-Diff(base)	UI	0
tDS-Diff(derated)	UI	0
tDSH-Diff	2 UI	0
tDSS-Diff	2 UI	0
tDQSS	UI	– UI
tDSH	2 UI	0
tDSS	2 UI	0
tDH(base)	UI	0
tDH(derated)	UI	0
tDS(base)	UI	0
tDS(derated)	UI	0
tIH(base)	2 UI	0
tIH(derated)	2 UI	0
tIS(base)	2 UI	0
tIS(derated)	2 UI	0
tQH	1.5 UI	UI / 2

Dynamic limits for each generation

In this section, dynamic limits are shown only for the lowest data rate per generation. Dynamic limits may change for each data rate.

Dynamic limits for DDR measurements

The following table lists the dynamic limits for DDR measurements. For more details, refer to the *DDR JEDEC standard specification*.

Table 21: Dynamic limits for DDR

Measurement	Dynamic limits		
	Min	Max	Units
tCH	0.45	0.55	tCK
tCL	0.45	0.55	tCK
Vix(ac)CK	0.5 * Vdd – 0.2	0.5 * Vdd + 0.2	-
Vix(ac)DQS	0.5 * Vdd – 0.2	0.5 * Vdd + 0.2	-
Vid(ac)	0.7	Vdd + 0.6	-

Dynamic limits for DDR2 measurements

The following table lists the dynamic limits for DDR2 measurements. For more details, refer to the *DDR2 JEDEC standard specification*.

Note: Dynamic limits are the same for all DDR2 data rates except for those data rates specifically mentioned in the table.

Table 22: Dynamic limits for DDR2

Measurement	Data rate (MT/s)	Dynamic limits		
		Min	Max	Units
tCH(avg)	667, 800	0.48	0.52	tCK(avg)
tCL(avg)	667, 800	0.48	0.52	tCK(avg)
tCH(abs)	NA	0.45	0.55	-
tCL(abs)	NA	0.45	0.55	-
tIPW	NA	0.6	NA	-
Vix(ac)CK	NA	0.5 * Vdd – 0.175	0.5 * Vdd + 0.175	-
Vix(ac)DQS	NA	0.5 * Vdd – 0.175	0.5 * Vdd + 0.175	-
Vox(ac)CK	NA	0.5 * Vdd – 0.125	0.5 * Vdd + 0.125	-
Vox(ac)DQS	NA	0.5 * Vdd – 0.125	0.5 * Vdd + 0.125	-
Vid(ac)	NA	0.5	Vdd	-

Dynamic limits for DDR3 measurements

The following table lists the dynamic limits for DDR3 measurements. For more details, refer to the *DDR3 JEDEC standard specification*.

Table 23: Dynamic limits for DDR3

Measurement	Dynamic limits		
	Min	Max	Units
tQH	0.38 * tCK(avg)	-	tCK(avg)
tQSH	0.38 * tCK(avg)	-	tCK(avg)
tQSL	0.38 * tCK(avg)	-	tCK(avg)
tDQSS-SE	-0.25 * tCK(avg)	0.25 * tCK(avg)	tCK(avg)
tDSH-SE	0.2 * tCK(avg)	-	tCK(avg)
tDSS-SE	0.2 * tCK(avg)	-	tCK(avg)
tRPRE	0.9 * tCK(avg)	-	tCK(avg)
tRPST	0.3 * tCK(avg)	-	tCK(avg)
tCH(avg)	0.47 * tCK(avg)	0.53 * tCK(avg)	tCK(avg)
tCL(avg)	0.47 * tCK(avg)	0.53 * tCK(avg)	tCK(avg)
tCH(abs)	0.43 * tCK(avg)	-	tCK(avg)
tCL(abs)	0.43 * tCK(avg)	-	tCK(avg)
VSEH(DQS)	(VDD/2) + 0.175	-	V
VSEH (DQS#)	(VDD/2) + 0.175	-	V
VSEH(CK)	(VDD/2) + 0.175	-	V
VSEH(CK#)	(VDD/2) + 0.175	-	V
VSEL(DQS)	-	(VDD/2) – 0.175	V
VSEL(DQS#)	-	(VDD/2) – 0.175	V
VSEL(CK)	-	(VDD/2) – 0.175	V
VSEL(CK#)	-	(VDD/2) – 0.175	V
VSEH(AC)DQS	(VDD/2) + 0.175	-	V

Table continued…

Measurement	Dynamic limits		
	Min	Max	Units
VSEH(AC)DQS#	(VDD/2) + 0.175	-	V
VSEH(AC)CK	(VDD/2) + 0.175	-	V
VSEH(AC)CK#	(VDD/2) + 0.175	-	V
VSEL(AC)DQS	-	(VDD/2) – 0.175	V
VSEL(AC)DQS#	-	(VDD/2) – 0.175	V
VSEL(AC)CK	-	(VDD/2) – 0.175	V
VSEL(AC)CK#	-	(VDD/2) – 0.175	V
tDQSH	0.45 * tCK(avg)	0.55 * tCK(avg)	tCK(avg)
tDQSL	0.45 * tCK(avg)	0.55 * tCK(avg)	tCK(avg)
tDQSS-Diff	-0.25 * tCK(avg)	0.25 * tCK(avg)	tCK(avg)
tDSS-Diff	-0.2 * tCK(avg)	-	tCK(avg)
tDIPW-SE	600 * tCK(avg)	-	ps
tDQSS-SE	-0.25 * tCK(avg)	0.25 * tCK(avg)	tCK(avg)
tDSH-Diff	0.2 * tCK(avg)	-	tCK(avg)
tDSH-SE	0.2 * tCK(avg)	-	tCK(avg)
tDSS-SE	0.2 * tCK(avg)	-	tCK(avg)
tWPRE	0.9 * tCK(avg)	-	tCK(avg)
tWPST	0.3 * tCK(avg)	-	tCK(avg)

Dynamic limits for DDR4 measurements

The following table lists the dynamic limits for DDR4 measurements. For more details, refer to the *DDR4 JEDEC standard specification*.

Table 24: Dynamic limits for DDR4

Measurement	Dynamic limits		
	Min	Max	Units
tCH(avg)	0.48 * tCK(avg)	0.52 * tCK(avg)	tCK(avg)

Table continued…

Measurement	Dynamic limits		
	Min	Max	Units
tCL(avg)	0.48 * tCK(avg)	0.52 * tCK(avg)	tCK(avg)
tCH(abs)	0.45 * tCK(avg)	NA	tCK(avg)
tCL(abs)	0.45 * tCK(avg)	NA	tCK(avg)
VSEH(CK)	(VDD/2) + 0.100	-	V
VSEH(CK#)	(VDD/2) + 0.100	-	V
VSEL(DQS#)	-	(VDD/2) – 0.175	V
VSEL(CK)	-	(VDD/2) + 0.100	V
VSEL(CK#)	-	(VDD/2) + 0.100	V
tDQSQ-Diff	-	0.16 * tCK(avg)	tCK(avg)/2
tQH	-	0.76 * tCK(avg)	tCK(avg)/2
tQSH	-	0.4 * tCK(avg)	tCK(avg)
tQSL	-	0.4 * tCK(avg)	tCK(avg)
tRPRE	0.9 * tCK(avg) (for 1tCK Preamble Length)	-	tCK(avg)
	1.8 * tCK(avg) (for 2tCK Preamble Length)		
tRPST	0.33 * tCK(avg)	-	tCK(avg)
TdIPW-High	0.58 * UI	-	UI
TdIPW-Low	0.58 * UI	-	UI
tDQSH	0.54 * tCK(avg)	0.46 * tCK(avg)	tCK(avg)
tDQSL	0.54 * tCK(avg)	0.46 * tCK(avg)	tCK(avg)
tDQSS-Diff	-0.27 * tCK(avg) (for 1tCK Preamble Length)	0.27 * tCK(avg) (for 1tCK Preamble Length)	tCK(avg)
	-0.5 * tCK(avg) (for 2tCK Preamble Length)	0.5 * tCK(avg) (for 2tCK Preamble Length)	
tDSS-Diff	-0.18 * tCK(avg)	-	tCK(avg)
tWPRE	0.9 * tCK(avg) (for 1tCK Preamble Length)	-	tCK(avg)
	1.8 * tCK(avg) (for 2tCK Preamble Length)		
tWPST	0.33 * tCK(avg)	-	tCK(avg)
tCK(abs)	tCK(avg)min +tJIT(per)min_tot	tCK(avg)max +tJIT(per)max_tot	tCK(avg)
Vix(ac)CK	-120 mV	120 mV	mV
Vix(ac)DQS	25%	25%	%

Dynamic limits for DDR3L measurements

The following table lists the dynamic limits for DDR3L measurements.

Table 25: Dynamic limits for DDR3L

Measurement	Dynamic limits		
	Min	Max	Units
tCH(avg)	0.47 * tCK(avg)	0.53 * tCK(avg)	tCK(avg)
tCL(avg)	0.47 * tCK(avg)	0.53 * tCK(avg)	tCK(avg)
tCH(abs)	-	0.43 * tCK(avg)	tCK(avg)
tCL(abs)	-	0.43 * tCK(avg)	tCK(avg)
VSEH(DQS)	(VDD/2) + 0.175	-	V
VSEH (DQS#)	(VDD/2) + 0.175	-	V
VSEH(CK)	(VDD/2) + 0.175	-	V
VSEH(CK#)	(VDD/2) + 0.175	-	V
VSEL(DQS)	-	(VDD/2) – 0.175	V
VSEL(DQS#)	-	(VDD/2) – 0.175	V
VSEL(CK)	-	(VDD/2) – 0.175	V
VSEL(CK#)	-	(VDD/2) – 0.175	V
VSEH(AC)DQS	(VDD/2) + 0.175	-	V
VSEH(AC)DQS#	(VDD/2) + 0.175	-	V
VSEH(AC)CK	(VDD/2) + 0.175	-	V
VSEH(AC)CK#	(VDD/2) + 0.175	-	V
VSEL(AC)DQS	-	(VDD/2) – 0.175	V
VSEL(AC)DQS#	-	(VDD/2) – 0.175	V
tDVAC(DQS)	-	-	-
tQH	0.38 * tCK(avg)	-	tCK(avg)
tQSH	0.38 * tCK(avg)	-	tCK(avg)
tQSL	0.38 * tCK(avg)	-	tCK(avg)
tRPRE	0.9 * tCK(avg)	-	tCK(avg)

Table continued…

Measurement	Dynamic limits		
	Min	Max	Units
tRPST	0.3 * tCK(avg)	-	tCK(avg)
tDH-Diff(derated)	0.45 * tCK(avg)	0.55 * tCK(avg)	tCK(avg)
tDQSL	0.45 * tCK(avg)	0.55 * tCK(avg)	tCK(avg)
tDQSS-Diff	-0.25 * tCK(avg)	0.25 * tCK(avg)	tCK(avg)
tDSH-Diff	0.18 * tCK(avg)	-	tCK(avg)
tDSS-Diff	0.18 * tCK(avg)	-	tCK(avg)
tDQSS-SE	-0.27 * tCH(avg)	0.25 * tCH(avg)	tCK(avg)
tDSH-SE	-0.18 * tCH(avg)	-	tCK(avg)
tDSS-SE	-0.18 * tCH(avg)	-	tCK(avg)

Dynamic limits for LPDDR measurements

The following table lists the dynamic limits for LPDDR measurements. For more details, refer to the *LPDDR JEDEC standard specification*.

Table 26: Dynamic limits for LPDDR

Measurement	Dynamic limits		
	Min	Max	Units
tCH	0.45	0.55	tCK
tCL	0.45	0.55	tCK
Vix(ac)CK	0.4 * Vdd	0.6 * Vdd	-
Vix(ac)DQS	0.4 * Vdd	0.6 * Vdd	-
Vid(ac)	0.6 * Vdd	Vdd + 0.6	-

Dynamic limits for LPDDR2 measurements

The following table lists the dynamic limits for LPDDR2 measurements. For more details, refer to the *LPDDR2 JEDEC standard specification*.

Note: Refer to the standard specific JEDEC document for derated measurements such as tIS(derated), tIH(derated), tDS-Diff(derated), and tDH-Diff(derated) for calculating dynamic limits.

Table 27: Dynamic limits for LPDDR2

Measurement	Data rate (MT/s)	Dynamic limits		
		Min	Max	Units
tCH(avg)	NA	0.45	0.55	tCK(avg)
tCL(avg)	NA	0.45	0.55	tCK(avg)
tCH(abs)	NA	0.43	0.57	tCK(avg)
tCL(abs)	NA	0.43	0.57	tCK(avg)
tERR(13–50) [5]		(1 + 0.68ln(n)) * tJIT(per)min	(1 + 0.68ln(n)) * tJIT(per)max	ps
VSEH(AC)DQS	200 to 400 MT/s	(VDD/2) + 0.300	-	V
	466 to 1066 MT/s	(VDD/2) + 0.220	-	V
VSEH(AC)DQS#	200 to 400 MT/s	(VDD/2) + 0.300	-	V
	466 to 1066 MT/s	(VDD/2) + 0.220	-	V
VSEH(AC)CK	200 to 400 MT/s	(VDD/2) + 0.300	-	V
	466 to 1066 MT/s	(VDD/2) + 0.220	-	V
VSEH(AC)CK#	200 to 400 MT/s	(VDD/2) + 0.300	-	V
	466 to 1066 MT/s	(VDD/2) + 0.220	-	V
VSEL(AC)DQS	200 to 400 MT/s	-	(VDD/2) – 0.300	V
	466 to 1066 MT/s	-	(VDD/2) – 0.220	V
VSEL(AC)DQS#	200 to 400 MT/s	-	(VDD/2) – 0.300	V
	466 to 1066 MT/s	-	(VDD/2) – 0.220	V
VSEL(AC)CK	200 to 400 MT/s	-	(VDD/2) – 0.300	V
	466 to 1066 MT/s	-	(VDD/2) – 0.220	V
VSEL(AC)CK#	200 to 400 MT/s	-	(VDDQ/2) – 0.300	V
	466 to 1066 MT/s	-	(VDD/2) – 0.220	V

[5] Includes measurements from tERR13per to tERR50per

Dynamic limits for LPDDR3 measurements

The following table lists the dynamic limits for LPDDR3 measurements. For more details, refer to the *LPDDR3 JEDEC standard specification*.

Note: Refer to the standard specific JEDEC document for derated measurements such as tIS(derated), tIH(derated), tDS-Diff(derated), and tDH-Diff(derated) for calculating dynamic limits.

Table 28: Dynamic limits for LPDDR3

Measurement	Dynamic limits		
	Min	Max	Units
tQH	min(tQSH, tQSL)	-	ps
tQSH	tCH(abs) - 0.05 * tCK(avg)	-	tCK(avg)
tQSL	tCL(abs) - 0.05 * tCK(avg)	-	tCK(avg)
tRPRE	0.9 * tCK(avg)	-	tCK(avg)
tRPST	0.3 * tCK(avg)	-	tCK(avg)
tDQSH	0.4 * tCK(avg)	-	tCK(avg)
tDQSL	0.4 * tCK(avg)	-	tCK(avg)
tDSH-Diff	0.2 * tCK(avg)	-	tCK(avg)
tDSS-Diff	0.2 * tCK(avg)	-	tCK(avg)
tCH(avg)	0.45 * tCK(avg)	0.55 * tCK(avg)	tCK(avg)
tCL(avg)	0.45 * tCK(avg)	0.55 * tCK(avg)	tCK(avg)
tCH(abs)	0.43 * tCK(avg)	0.57 * tCK(avg)	tCK(avg)
tCL(abs)	0.43 * tCK(avg)	0.57 * tCK(avg)	tCK(avg)
tERR(13–50) [6]	(1 + 0.68ln(n)) * tJIT(per)min	(1 + 0.68ln(n)) * tJIT(per)max	ps
VSEH(DQS)	(VDD/2) + 0.150	-	V
VSEH (DQS#)	(VDD/2) + 0.150	-	V
VSEH(CK)	(VDD/2) + 0.150	-	V
VSEH(CK#)	(VDD/2) + 0.150	-	V

Table continued…

[6] Includes measurements from tERR13per to tERR50per

Measurement	Dynamic limits		
	Min	Max	Units
VSEL(DQS)	-	(VDD/2) + 0.150	V
VSEL(DQS#)	-	(VDD/2) + 0.150	V
VSEL(CK)	-	(VDD/2) + 0.150	V
VSEL(CK#)	-	(VDD/2) + 0.150	V
VSEH(AC)DQS	(VDD/ 2) + 0.150	–	V
VSEH(AC)DQS#	(VDD/2) + 0.150	–	V
VSEH(AC)CK	(VDD/2) + 0.150	–	V
VSEH(AC)CK#	(VDD/2) + 0.150	–	V
VSEL(AC)DQS	-	(VDD/2) – 0.150	V
VSEL(AC)DQS#	-	(VDD/2) – 0.150	V
VSEL(AC)CK	-	(VDD/2) – 0.150	V
VSEL(AC)CK#	-	(VDD/2) – 0.150	V
tIPW Low (CA)	0.35 * tCK(avg)	-	tCK(avg)
tIPW Low (CS)	0.7 * tCK(avg)	-	tCK(avg)
tWPRE	0.8 * tCK(avg)	-	tCK(avg)
tWPST	0.4 * tCK(avg)	-	tCK(avg)

Dynamic limits for LPDDR4 and LPDDR4X measurements

The following table lists the dynamic limits for LPDDR4 and LPDDR4X measurements. For more details, refer to the *LPDDR4 JEDEC standard*.

Table 29: Dynamic limits for LPDDR4 / LPDDR4X

Measurement	Dynamic limits		
	Min	Max	Units
tCH (abs)	0.43 * tCK (avg)	0.57	tCK (avg)
tCL (abs)	0.43 * tCK (avg)	0.57	tCK (avg)

Table continued…

Measurement	Dynamic limits		
	Min	Max	Units
tCH (avg)	0.46 * tCK (avg)	0.54	tCK (avg)
tCL (avg)	0.46 * tCK (avg)	0.54	tCK (avg)
tQH	(tQSH, tQSL)	NA	UI
tQH_DBI	(tQSH_DBI, tQSL_DBI)	NA	UI
Vix(ac)CK	-	25%	UI
Vix(ac)DQS	-	20%	UI
tDQSQ-Diff	-	0.18	UI
tQSH	tCH(abs) - 0.05	-	tCK (avg)
tQSH_DBI	tCH(abs) - 0.045	-	tCK (avg)
tQSL	tCL(abs) - 0.05		tCK (avg)
tQSL_DBI	tCL(abs) - 0.045	-	tCK (avg)
tQW_Total	0.75 * tCK (avg)	-	UI
tRPRE	1.8 * tCK (avg)	-	tCK (avg)
tRPST	0.4 * tCK (avg)	-	tCK (avg)
tDQSH	0.4 * tCK (avg)	-	tCK (avg)
tDQSL	0.4 * tCK (avg)	-	tCK (avg)
tDSH-Diff	0.2 * tCK(avg)	-	tCK (avg)
tDSS-Diff	0.2 * tCK(avg)	-	tCK (avg)
TdIPW-High	0.55 * tCK(avg)	-	tCK (avg)
TdIPW-Low	0.55 * tCK(avg)	-	tCK (avg)
tWPRE	1.8 * tCK(avg)	-	tCK (avg)
tWPST	1.4 * tCK(avg)	-	tCK (avg)

Derating values

LPDDR2 Derating values

tDS/tDH derating at AC220 for LPDDR2																									
tDS													tDH												
Slew Rate	DQS, DQS# Differential												Slew Rate	DQS, DQS# Differential											
(V/ns)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0	(V/ns)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
4.0	165	165	165	165	165	165	165	-	-	-	-	-	4.0	98	98	98	98	98	98	98	-	-	-	-	-
3.5	158	158	158	158	158	158	158	-	-	-	-	-	3.5	93	93	93	93	93	93	93	-	-	-	-	-
3.0	147	147	147	147	147	147	147	-	-	-	-	-	3.0	87	87	87	87	87	87	87	-	-	-	-	-
2.5	132	132	132	132	132	132	132	-	-	-	-	-	2.5	78	78	78	78	78	78	78	-	-	-	-	-
2.0	110	110	110	110	110	110	110	-	-	-	-	-	2.0	65	65	65	65	65	65	65	-	-	-	-	-
1.5	74	74	74	74	74	73	73	89	-	-	-	-	1.5	43	43	43	43	43	43	43	59	-	-	-	-
DQ 1.0	0	0	0	0	0	0	0	16	32	-	-	-	DQ 1.0	0	0	0	0	0	0	0	16	32	-	-	-
0.9	-	-	-	-	-	-3	-3	13	29	45	-	-	0.9	-	-	-	-	-	-5	-5	11	27	43	-	-
0.8	-	-	-	-	-	-	8	8	24	40	56	-	0.8	-	-	-	-	-	-	-13	3	19	35	55	-
0.7	-	-	-	-	-	-	-	2	18	34	50	66	0.7	-	-	-	-	-	-	-	-6	10	26	46	78
0.6	-	-	-	-	-	-	-	-	10	26	42	58	0.6	-	-	-	-	-	-	-	-	-3	13	33	65
0.5	-	-	-	-	-	-	-	-	-	4	20	36	0.5	-	-	-	-	-	-	-	-	-	-4	16	48
0.4	-	-	-	-	-	-	-	-	-	-	-7	17	0.4	-	-	-	-	-	-	-	-	-	-	2	34

Figure 10: tDS/tDH derating at AC220 for LPDDR2

tDS/tDH derating at AC300 for LPDDR2																									
tDS													tDH												
Slew Rate	DQS, DQS# Differential												Slew Rate	DQS, DQS# Differential											
(V/ns)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0	(V/ns)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
4.0	225	225	225	225	225	225	225	-	-	-	-	-	4.0	150	150	150	150	150	150	150	-	-	-	-	-
3.5	215	215	215	215	215	215	215	-	-	-	-	-	3.5	143	143	143	143	143	143	143	-	-	-	-	-
3.0	200	200	200	200	200	200	200	-	-	-	-	-	3.0	134	134	134	134	134	134	134	-	-	-	-	-
2.5	180	180	180	180	180	180	180	-	-	-	-	-	2.5	120	120	120	120	120	120	120	-	-	-	-	-
2.0	150	150	150	150	150	150	150	-	-	-	-	-	2.0	100	100	100	100	100	100	100	-	-	-	-	-
1.5	100	100	100	100	100	100	100	116	-	-	-	-	1.5	67	67	67	67	67	67	67	83	-	-	-	-
DQ 1.0	0	0	0	0	0	0	0	16	32	-	-	-	DQ 1.0	0	0	0	0	0	0	0	16	32	-	-	-
0.9	-	-	-	-	-	0	-4	12	28	44	-	-	0.9	-	-	-	-	-	-8	-8	8	24	40	-	-
0.8	-	-	-	-	-	-	-12	4	20	36	52	-	0.8	-	-	-	-	-	-	-20	-4	12	28	48	-
0.7	-	-	-	-	-	-	-	-3	13	29	45	61	0.7	-	-	-	-	-	-	-	-18	-2	14	34	66
0.6	-	-	-	-	-	-	-	-	2	18	34	50	0.6	-	-	-	-	-	-	-	-	-21	-5	15	47
0.5	-	-	-	-	-	-	-	-	-	-12	4	20	0.5	-	-	-	-	-	-	-	-	-	-32	-12	20
0.4	-	-	-	-	-	-	-	-	-	-	-35	-11	0.4	-	-	-	-	-	-	-	-	-	-	-40	-8

Figure 11: tDS/tDH derating at AC300 for LPDDR2

tIS/tIH derating at AC220 for LPDDR2																									
tIS													tIH												
Slew Rate	CK, CK# Differential												Slew Rate	CK, CK# Differential											
(V/ns)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0	(V/ns)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
4.0	165	165	165	165	165	165	165	-	-	-	-	-	4.0	98	98	98	98	98	98	98	-	-	-	-	-
3.5	158	158	158	158	158	158	158	-	-	-	-	-	3.5	93	93	93	93	93	93	93	-	-	-	-	-
3.0	147	147	147	147	147	147	147	-	-	-	-	-	3.0	87	87	87	87	87	87	87	-	-	-	-	-
2.5	132	132	132	132	132	132	132	-	-	-	-	-	2.5	78	78	78	78	78	78	78	-	-	-	-	-
2.0	110	110	110	110	110	110	110	-	-	-	-	-	2.0	65	65	65	65	65	65	65	-	-	-	-	-
1.5	74	74	74	74	74	73	73	89	-	-	-	-	1.5	43	43	43	43	43	43	43	59	-	-	-	-
ADD/CMD 1.0	0	0	0	0	0	0	0	16	32	-	-	-	ADD/CMD 1.0	0	0	0	0	0	0	0	16	32	-	-	-
0.9	-	-	-	-	-	-3	-3	13	29	45	-	-	0.9	-	-	-	-	-	-5	-5	11	27	43	-	-
0.8	-	-	-	-	-	-	-8	8	24	40	56	-	0.8	-	-	-	-	-	-	-13	3	19	35	55	-
0.7	-	-	-	-	-	-	-	2	18	34	50	66	0.7	-	-	-	-	-	-	-	-6	10	26	46	78
0.6	-	-	-	-	-	-	-	-	10	26	42	58	0.6	-	-	-	-	-	-	-	-	-3	13	33	65
0.5	-	-	-	-	-	-	-	-	-	4	20	36	0.5	-	-	-	-	-	-	-	-	-	-4	16	48
0.4	-	-	-	-	-	-	-	-	-	-	-7	17	0.4	-	-	-	-	-	-	-	-	-	-	2	34

Figure 12: tIS/tIH derating at AC220 for LPDDR2

tIS/tIH derating at AC300 for LPDDR2													
tIS													
Slew Rate		CK, CK# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/CMD	4.0	225	225	225	225	225	225	225	-	-	-	-	-
	3.5	215	215	215	215	215	215	215	-	-	-	-	-
	3.0	200	200	200	200	200	200	200	-	-	-	-	-
	2.5	180	180	180	180	180	180	180	-	-	-	-	-
	2.0	150	150	150	150	150	150	150	-	-	-	-	-
	1.5	100	100	100	100	100	100	100	116	-	-	-	-
	1.0	0	0	0	0	0	0	0	16	32	-	-	-
	0.9	-	-	-	-	-	-4	-4	12	28	44	-	-
	0.8	-	-	-	-	-	-	-12	4	20	36	52	-
	0.7	-	-	-	-	-	-	-	-3	13	29	45	61
	0.6	-	-	-	-	-	-	-	-	2	18	34	50
	0.5	-	-	-	-	-	-	-	-	-	-12	4	20
	0.4	-	-	-	-	-	-	-	-	-	-	-35	-11

tIH													
Slew Rate		CK, CK# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/CMD	4.0	150	150	150	150	150	150	150	-	-	-	-	-
	3.5	143	143	143	143	143	143	143	-	-	-	-	-
	3.0	134	134	134	134	134	134	134	-	-	-	-	-
	2.5	120	120	120	120	120	120	120	-	-	-	-	-
	2.0	100	100	100	100	100	100	100	-	-	-	-	-
	1.5	67	67	67	67	67	67	67	83	-	-	-	-
	1.0	0	0	0	0	0	0	0	16	32	-	-	-
	0.9	-	-	-	-	-	-8	-8	8	24	40	-	-
	0.8	-	-	-	-	-	-	-20	-4	12	28	48	-
	0.7	-	-	-	-	-	-	-	-18	-2	14	34	66
	0.6	-	-	-	-	-	-	-	-	-21	-5	15	47
	0.5	-	-	-	-	-	-	-	-	-	-32	-12	20
	0.4	-	-	-	-	-	-	-	-	-	-	-40	-8

Figure 13: tIS/tIH derating at AC300 for LPDDR2

DDR3 and DDR3L Derating values

tDS/tDH derating at AC175 for DDR3-800/1066													
tDS													
Slew Rate		DQS, DQS# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
DQ	4.0	132	132	132	132	132	132	132	-	-	-	-	-
	3.5	125	125	125	125	125	125	125	-	-	-	-	-
	3.0	117	117	117	117	117	117	117	-	-	-	-	-
	2.5	105	105	105	105	105	105	105	-	-	-	-	-
	2.0	88	88	88	88	88	88	88	-	-	-	-	-
	1.5	59	59	59	59	59	59	59	67	-	-	-	-
	1.0	0	0	0	0	0	0	0	8	16	-	-	-
	0.9	-	-	-	-	-	-2	-2	6	14	22	-	-
	0.8	-	-	-	-	-	-	-6	2	10	18	26	-
	0.7	-	-	-	-	-	-	-	-3	5	13	21	29
	0.6	-	-	-	-	-	-	-	-	-1	7	15	23
	0.5	-	-	-	-	-	-	-	-	-	-11	-2	5
	0.4	-	-	-	-	-	-	-	-	-	-	-30	-22

tDH													
Slew Rate		DQS, DQS# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
DQ	4.0	75	75	75	75	75	75	75	-	-	-	-	-
	3.5	72	72	72	72	72	72	72	-	-	-	-	-
	3.0	67	67	67	67	67	67	67	-	-	-	-	-
	2.5	60	60	60	60	60	60	60	-	-	-	-	-
	2.0	50	50	50	50	50	50	50	-	-	-	-	-
	1.5	34	34	34	34	34	34	34	42	-	-	-	-
	1.0	0	0	0	0	0	0	0	8	16	-	-	-
	0.9	-	-	-	-	-	-4	-4	4	12	20	-	-
	0.8	-	-	-	-	-	-	-10	-2	6	14	24	-
	0.7	-	-	-	-	-	-	-	-8	0	8	18	34
	0.6	-	-	-	-	-	-	-	-	-10	-2	8	24
	0.5	-	-	-	-	-	-	-	-	-	-16	-6	10
	0.4	-	-	-	-	-	-	-	-	-	-	-26	-10

Figure 14: tDS/tDH derating at AC175 for DDR3-800/1066

tDS/tDH derating at AC150 for DDR3-800/1066/1333/1600													
tDS													
Slew Rate		DQS, DQS# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
DQ	4.0	113	113	113	113	113	113	113	-	-	-	-	-
	3.5	108	108	108	108	108	108	108	-	-	-	-	-
	3.0	100	100	100	100	100	100	100	-	-	-	-	-
	2.5	90	90	90	90	90	90	90	-	-	-	-	-
	2.0	75	75	75	75	75	75	75	-	-	-	-	-
	1.5	50	50	50	50	50	50	50	58	-	-	-	-
	1.0	0	0	0	0	0	0	0	8	16	-	-	-
	0.9	-	-	-	-	-	0	0	8	16	24	-	-
	0.8	-	-	-	-	-	-	0	8	16	24	32	-
	0.7	-	-	-	-	-	-	-	8	16	24	32	40
	0.6	-	-	-	-	-	-	-	-	15	23	31	39
	0.5	-	-	-	-	-	-	-	-	-	14	22	30
	0.4	-	-	-	-	-	-	-	-	-	-	7	15

tDH													
Slew Rate		DQS, DQS# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
DQ	4.0	75	75	75	75	75	75	75	-	-	-	-	-
	3.5	72	72	72	72	72	72	72	-	-	-	-	-
	3.0	67	67	67	67	67	67	67	-	-	-	-	-
	2.5	60	60	60	60	60	60	60	-	-	-	-	-
	2.0	50	50	50	50	50	50	50	-	-	-	-	-
	1.5	34	34	34	34	34	34	34	42	-	-	-	-
	1.0	0	0	0	0	0	0	0	8	16	-	-	-
	0.9	-	-	-	-	-	-4	-4	4	12	20	-	-
	0.8	-	-	-	-	-	-	-10	-2	6	14	24	-
	0.7	-	-	-	-	-	-	-	-8	0	8	18	34
	0.6	-	-	-	-	-	-	-	-	-10	-2	8	24
	0.5	-	-	-	-	-	-	-	-	-	-16	-6	10
	0.4	-	-	-	-	-	-	-	-	-	-	-26	-10

Figure 15: tDS/tDH derating at AC150 for DDR3-800/1066/1333/1600

tDS/tDH derating at AC135 for DDR3-800/1066/1333/1600													
tDS													
Slew Rate	DQS, DQS# Differential												
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
DQ	4.0	102	102	102	102	102	102	102	-	-	-	-	-
	3.5	97	97	97	97	97	97	97	-	-	-	-	-
	3.0	90	90	90	90	90	90	90	-	-	-	-	-
	2.5	81	81	81	81	81	81	81	-	-	-	-	-
	2.0	68	68	68	68	68	68	68	-	-	-	-	-
	1.5	45	45	45	45	45	45	45	53	-	-	-	-
	1.0	0	0	0	0	0	0	0	8	16	-	-	-
	0.9	-	-	-	-	-	2	2	10	18	26	-	-
	0.8	-	-	-	-	-	-	3	11	19	27	35	-
	0.7	-	-	-	-	-	-	-	14	22	30	38	46
	0.6	-	-	-	-	-	-	-	-	25	33	41	49
	0.5	-	-	-	-	-	-	-	-	-	29	37	45
	0.4	-	-	-	-	-	-	-	-	-	-	30	38

tDH													
Slew Rate	DQS, DQS# Differential												
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
DQ	4.0	75	75	75	75	75	75	75	-	-	-	-	-
	3.5	72	72	72	72	72	72	72	-	-	-	-	-
	3.0	67	67	67	67	67	67	67	-	-	-	-	-
	2.5	60	60	60	60	60	60	60	-	-	-	-	-
	2.0	50	50	50	50	50	50	50	-	-	-	-	-
	1.5	34	34	34	34	34	34	34	42	-	-	-	-
	1.0	0	0	0	0	0	0	0	8	16	-	-	-
	0.9	-	-	-	-	-	-4	-4	4	12	20	-	-
	0.8	-	-	-	-	-	-	-10	-2	6	14	24	-
	0.7	-	-	-	-	-	-	-	-8	0	8	18	34
	0.6	-	-	-	-	-	-	-	-	-10	-2	8	24
	0.5	-	-	-	-	-	-	-	-	-	-16	-6	10
	0.4	-	-	-	-	-	-	-	-	-	-	-26	-10

Figure 16: tDS/tDH derating at AC135 for DDR3-800/1066/1333/1600

ΔtDS, ΔtDH derating in [ps] AC/DC based Alternate AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV Alternate DC 100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV																							
	DQS,DQS# Differential Slew Rate																						
	8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
4.0	34	25	34	25	34	25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3.5	29	21	29	21	29	21	29	21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3.0	23	17	23	17	23	17	23	17	23	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
2.5	-	-	14	10	14	10	14	10	14	10	14	10	-	-	-	-	-	-	-	-	-	-	-	-
2.0	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
1.5	-	-	-	-	-	-	-23	-17	-23	-17	-23	-17	-23	-17	-15	-9	-	-	-	-	-	-	-	-
1.0	-	-	-	-	-	-	-	-	-68	-50	-68	-50	-68	-50	-60	-42	-52	-34	-	-	-	-	-	-
0.9	-	-	-	-	-	-	-	-	-	-	-66	-54	-66	-54	-58	-46	-50	-38	-42	-30	-	-	-	-
0.8	-	-	-	-	-	-	-	-	-	-	-	-	-64	-60	-56	-52	-48	-44	-40	-36	-32	-26	-	-
0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-53	-59	-45	-51	-37	-43	-29	-33	-21	-17
0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-43	-61	-35	-53	-27	-43	-19	-27
0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-39	-66	-31	-56	-23	-40
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-38	-76	-30	-60

DQS Slew rate V/ns

NOTE 1. Cell contents shaded in red are defined as 'not supported'.

Figure 17: tDS/tDH derating at AC135 for DDR3-2133

tIS/tIH derating at AC175 for DDR3-800/1066/1333/1600													
tIS													
Slew Rate	CK, CK# Differential												
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/CMD	4.0	132	132	132	132	132	132	132	140	148	156	164	172
	3.5	125	125	125	125	125	125	125	133	141	149	157	165
	3.0	117	117	117	117	117	117	117	125	133	141	149	157
	2.5	105	105	105	105	105	105	105	113	121	129	137	145
	2.0	88	88	88	88	88	88	88	96	104	112	120	128
	1.5	59	59	59	59	59	59	59	67	75	83	91	99
	1.0	0	0	0	0	0	0	0	8	16	24	32	40
	0.9	-2	-2	-2	-2	-2	-2	-2	6	14	22	30	38
	0.8	-6	-6	-6	-6	-6	-6	-6	2	10	18	26	34
	0.7	-11	-11	-11	-11	-11	-11	-11	-3	5	13	21	29
	0.6	-17	-17	-17	-17	-17	-17	-17	-9	-1	7	15	23
	0.5	-35	-35	-35	-35	-35	-35	-35	-27	-19	-11	-2	5
	0.4	-62	-62	-62	-62	-62	-62	-62	-54	-46	-38	-30	-22

tIH													
Slew Rate	CK, CK# Differential												
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/CMD	4.0	75	75	75	75	75	75	75	83	91	99	109	125
	3.5	72	72	72	72	72	72	72	80	88	96	106	122
	3.0	67	67	67	67	67	67	67	75	83	91	101	117
	2.5	60	60	60	60	60	60	60	68	76	84	94	110
	2.0	50	50	50	50	50	50	50	58	66	74	84	100
	1.5	34	34	34	34	34	34	34	42	50	58	68	84
	1.0	0	0	0	0	0	0	0	8	16	24	34	50
	0.9	-4	-4	-4	-4	-4	-4	-4	4	12	20	30	46
	0.8	-10	-10	-10	-10	-10	-10	-10	-2	6	14	24	40
	0.7	-16	-16	-16	-16	-16	-16	-16	-8	0	8	18	34
	0.6	-26	-26	-26	-26	-26	-26	-26	-18	-10	-2	8	24
	0.5	-40	-40	-40	-40	-40	-40	-40	-32	-24	-16	-6	10
	0.4	-60	-60	-60	-60	-60	-60	-60	-52	-44	-36	-26	-10

Figure 18: tIS/tIH derating at AC175 for DDR3-800/1066/1333/1600

tIS/tIH derating at AC150 for DDR3-800/1066/1333/1600													
tIS													
Slew Rate		CK, CK# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/ CMD	4.0	113	113	113	113	113	113	113	121	129	137	145	153
	3.5	108	108	108	108	108	108	108	116	124	132	140	148
	3.0	100	100	100	100	100	100	100	108	116	124	132	140
	2.5	90	90	90	90	90	90	90	98	106	114	122	130
	2.0	75	75	75	75	75	75	75	83	91	99	107	115
	1.5	50	50	50	50	50	50	50	58	66	74	82	90
	1.0	0	0	0	0	0	0	0	8	16	24	32	40
	0.9	0	0	0	0	0	0	0	8	16	24	32	40
	0.8	0	0	0	0	0	0	0	8	16	24	32	40
	0.7	0	0	0	0	0	0	0	8	16	24	32	40
	0.6	-1	-1	-1	-1	-1	-1	-1	7	15	23	31	39
	0.5	-10	-10	-10	-10	-10	-10	-10	-2	6	14	22	30
	0.4	-25	-25	-25	-25	-25	-25	-25	-17	-9	-1	7	15

tIH													
Slew Rate		CK, CK# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/ CMD	4.0	75	75	75	75	75	75	75	83	91	99	109	125
	3.5	72	72	72	72	72	72	72	80	88	96	106	122
	3.0	67	67	67	67	67	67	67	75	83	91	101	117
	2.5	60	60	60	60	60	60	60	68	76	84	94	110
	2.0	50	50	50	50	50	50	50	58	66	74	84	100
	1.5	34	34	34	34	34	34	34	42	50	58	68	84
	1.0	0	0	0	0	0	0	0	8	16	24	34	50
	0.9	-4	-4	-4	-4	-4	-4	-4	4	12	20	30	46
	0.8	-10	-10	-10	-10	-10	-10	-10	-2	6	14	24	40
	0.7	-16	-16	-16	-16	-16	-16	-16	-8	0	8	18	34
	0.6	-26	-26	-26	-26	-26	-26	-26	-18	-10	-2	8	24
	0.5	-40	-40	-40	-40	-40	-40	-40	-32	-24	-16	-6	10
	0.4	-60	-60	-60	-60	-60	-60	-60	-52	-44	-36	-26	-10

Figure 19: tIS/tIH derating at AC150 for DDR3-800/1066/1333/1600

tIS/tIH derating at AC135 for DDR3-1866/2133													
tIS													
Slew Rate		CK, CK# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/ CMD	4.0	102	102	102	102	102	102	102	110	118	126	134	142
	3.5	97	97	97	97	97	97	97	105	113	121	129	137
	3.0	90	90	90	90	90	90	90	98	106	114	122	130
	2.5	81	81	81	81	81	81	81	89	97	105	113	121
	2.0	68	68	68	68	68	68	68	76	84	92	100	108
	1.5	45	45	45	45	45	45	45	53	61	69	77	85
	1.0	0	0	0	0	0	0	0	8	16	24	32	40
	0.9	2	2	2	2	2	2	2	10	18	26	34	42
	0.8	3	3	3	3	3	3	3	11	19	27	35	43
	0.7	6	6	6	6	6	6	6	14	22	30	38	46
	0.6	9	9	9	9	9	9	9	17	25	33	41	49
	0.5	5	5	5	5	5	5	5	13	21	29	37	45
	0.4	-3	-3	-3	-3	-3	-3	-3	6	14	22	30	38

tIH													
Slew Rate		CK, CK# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/ CMD	4.0	75	75	75	75	75	75	75	83	91	99	109	125
	3.5	72	72	72	72	72	72	72	80	88	96	106	122
	3.0	67	67	67	67	67	67	67	75	83	91	101	117
	2.5	60	60	60	60	60	60	60	68	76	84	94	110
	2.0	50	50	50	50	50	50	50	58	66	74	84	100
	1.5	34	34	34	34	34	34	34	42	50	58	68	84
	1.0	0	0	0	0	0	0	0	8	16	24	34	50
	0.9	-4	-4	-4	-4	-4	-4	-4	4	12	20	30	46
	0.8	-10	-10	-10	-10	-10	-10	-10	-2	6	14	24	40
	0.7	-16	-16	-16	-16	-16	-16	-16	-8	0	8	18	34
	0.6	-26	-26	-26	-26	-26	-26	-26	-18	-10	-2	8	24
	0.5	-40	-40	-40	-40	-40	-40	-40	-32	-24	-16	-6	10
	0.4	-60	-60	-60	-60	-60	-60	-60	-52	-44	-36	-26	-10

Figure 20: tIS/tIH derating at AC135 for DDR3-1866/2133

tIS/tIH derating at AC 125 for DDR3-1866/2133													
tIS													
Slew Rate		CK, CK# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/ CMD	4.0	94	94	94	94	94	94	94	102	110	118	126	134
	3.5	90	90	90	90	90	90	90	98	106	114	122	130
	3.0	84	84	84	84	84	84	84	92	100	108	116	124
	2.5	75	75	75	75	75	75	75	83	91	99	107	115
	2.0	63	63	63	63	63	63	63	71	79	87	95	103
	1.5	42	42	42	42	42	42	42	50	58	66	74	82
	1.0	0	0	0	0	0	0	0	8	16	24	32	40
	0.9	4	4	4	4	4	4	4	12	20	28	36	44
	0.8	6	6	6	6	6	6	6	14	22	30	38	46
	0.7	11	11	11	11	11	11	11	19	27	35	43	51
	0.6	16	16	16	16	16	16	16	24	32	40	48	56
	0.5	15	15	15	15	15	15	15	23	31	39	47	55
	0.4	13	13	13	13	13	13	13	21	29	37	45	53

tIH													
Slew Rate		CK, CK# Differential											
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/ CMD	4.0	75	75	75	75	75	75	75	83	91	99	109	125
	3.5	72	72	72	72	72	72	72	80	88	96	106	122
	3.0	67	67	67	67	67	67	67	75	83	91	101	117
	2.5	60	60	60	60	60	60	60	68	76	84	94	110
	2.0	50	50	50	50	50	50	50	58	66	74	84	100
	1.5	34	34	34	34	34	34	34	42	50	58	68	84
	1.0	0	0	0	0	0	0	0	8	16	24	34	50
	0.9	-4	-4	-4	-4	-4	-4	-4	4	12	20	30	46
	0.8	-10	-10	-10	-10	-10	-10	-10	-2	6	14	24	40
	0.7	-16	-16	-16	-16	-16	-16	-16	-8	0	8	18	34
	0.6	-26	-26	-26	-26	-26	-26	-26	-18	-10	-2	8	24
	0.5	-40	-40	-40	-40	-40	-40	-40	-32	-24	-16	-6	10
	0.4	-60	-60	-60	-60	-60	-60	-60	-52	-44	-36	-26	-10

Figure 21: tIS/tIH derating at AC 125 for DDR3-1866/2133

tDS/tDH derating at AC 160 for DDR3L-800/1066																									
tDS														tDH											
Slew Rate	DQS, DQS# Differential													Slew Rate	DQS, DQS# Differential										
(V/ns)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0		(V/ns)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
4.0	120	120	120	120	120	120	120	-	-	-	-	-		4.0	68	68	68	68	68	68	68	-	-	-	-	-
3.5	115	115	115	115	115	115	115	-	-	-	-	-		3.5	65	65	65	65	65	65	65	-	-	-	-	-
3.0	107	107	107	107	107	107	107	-	-	-	-	-		3.0	60	60	60	60	60	60	60	-	-	-	-	-
2.5	96	96	96	96	96	96	96	-	-	-	-	-		2.5	54	54	54	54	54	54	54	-	-	-	-	-
2.0	80	80	80	80	80	80	80	-	-	-	-	-		2.0	45	45	45	45	45	45	45	-	-	-	-	-
1.5	53	53	53	53	53	53	53	61	-	-	-	-		1.5	30	30	30	30	30	30	30	38	-	-	-	-
DQ 1.0	0	0	0	0	0	0	0	8	16	-	-	-		DQ 1.0	0	0	0	0	0	0	0	8	16	-	-	-
0.9	-	-	-	-	-	-1	-1	7	15	23	-	-		0.9	-	-	-	-	-	-3	-3	5	13	21	-	-
0.8	-	-	-	-	-	-	-3	5	13	21	29	-		0.8	-	-	-	-	-	-	-8	1	9	17	27	-
0.7	-	-	-	-	-	-	-	3	11	19	27	35		0.7	-	-	-	-	-	-	-	-5	3	11	21	37
0.6	-	-	-	-	-	-	-	-	8	16	24	32		0.6	-	-	-	-	-	-	-	-	-4	4	14	30
0.5	-	-	-	-	-	-	-	-	-	4	12	20		0.5	-	-	-	-	-	-	-	-	-	-6	4	20
0.4	-	-	-	-	-	-	-	-	-	-	-8	0		0.4	-	-	-	-	-	-	-	-	-	-	-11	5

Figure 22: tDS/tDH derating at AC 160 for DDR3L-800/1066

tDS/tDH derating at AC130 for DDR3L-800/1066/1333/1600																									
tDS														tDH											
Slew Rate	DQS, DQS# Differential													Slew Rate	DQS, DQS# Differential										
(V/ns)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0		(V/ns)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
4.0	102	102	102	102	102	102	102	-	-	-	-	-		4.0	68	68	68	68	68	68	68	-	-	-	-	-
3.5	97	97	97	97	97	97	97	-	-	-	-	-		3.5	65	65	65	65	65	65	65	-	-	-	-	-
3.0	90	90	90	90	90	90	90	-	-	-	-	-		3.0	60	60	60	60	60	60	60	-	-	-	-	-
2.5	81	81	81	81	81	81	81	-	-	-	-	-		2.5	54	54	54	54	54	54	54	-	-	-	-	-
2.0	68	68	68	68	68	68	68	-	-	-	-	-		2.0	45	45	45	45	45	45	45	-	-	-	-	-
1.5	45	45	45	45	45	45	45	53	-	-	-	-		1.5	30	30	30	30	30	30	30	38	-	-	-	-
DQ 1.0	0	0	0	0	0	0	0	8	16	-	-	-		DQ 1.0	0	0	0	0	0	0	0	8	16	-	-	-
0.9	-	-	-	-	-	2	2	10	18	26	-	-		0.9	-	-	-	-	-	-3	-3	5	13	21	-	-
0.8	-	-	-	-	-	-	3	11	19	27	35	-		0.8	-	-	-	-	-	-	-8	1	9	17	27	-
0.7	-	-	-	-	-	-	-	14	22	30	38	46		0.7	-	-	-	-	-	-	-	-5	3	11	21	37
0.6	-	-	-	-	-	-	-	-	25	33	41	49		0.6	-	-	-	-	-	-	-	-	-4	4	14	30
0.5	-	-	-	-	-	-	-	-	-	29	37	45		0.5	-	-	-	-	-	-	-	-	-	-6	4	20
0.4	-	-	-	-	-	-	-	-	-	-	30	38		0.4	-	-	-	-	-	-	-	-	-	-	-11	5

Figure 23: tDS/tDH derating at AC130 for DDR3L-800/1066/1333/1600

ΔtDS, ΔDH derating in [ps] AC/DC based [a] Alternate AC130 Threshold -> VIH(AC)=VREF(DC)+130mV, VIL(AC)=VREF(DC)-130mV																									
	DQS, DQS# Differential Slew Rate																								
	8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
4.0	33	23	33	23	33	23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3.5	28	19	28	19	28	19	28	19	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3.0	22	15	22	15	22	15	22	15	22	15	-	-	-	-	-	-	-	-	-	-	-	-	-	-
2.5	-	-	13	9	13	9	13	9	13	9	13	9	-	-	-	-	-	-	-	-	-	-	-	-
2.0	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
1.5	-	-	-	-	-	-	-22	-15	-22	-15	-22	-15	-22	-15	-14	-7	-	-	-	-	-	-	-	-
1.0	-	-	-	-	-	-	-	-	-65	-45	-65	-45	-65	-45	-57	-37	-49	-29	-	-	-	-	-	-
0.9	-	-	-	-	-	-	-	-	-	-	-62	-48	-62	-48	-54	-40	-46	-32	-38	-24	-	-	-	-
0.8	-	-	-	-	-	-	-	-	-	-	-	-	-61	-53	-53	-45	-45	-37	-37	-29	-29	-19	-	-
0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-49	-50	-41	-42	-33	-34	-25	-24	-17	-8
0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-37	-49	-29	-41	-21	-31	-13	-15
0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-31	-51	-23	-41	-15	-25
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-28	-56	-20	-40

DQ Slew rate V/ns

a. Cell contents shaded in red are defined as 'not supported'.

Figure 24: tDS/tDH derating at AC130 for DDRL-2133

tIS/tIH derating at AC160 for DDR3L-800/1066/1333/1600													
tIS													
Slew Rate	CK, CK# Differential												
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/CMD	4.0	120	120	120	120	120	120	120	128	136	144	152	160
	3.5	115	115	115	115	115	115	115	123	131	139	147	155
	3.0	107	107	107	107	107	107	107	115	123	131	139	147
	2.5	96	96	96	96	96	96	96	104	112	120	128	136
	2.0	80	80	80	80	80	80	80	88	96	104	112	120
	1.5	53	53	53	53	53	53	53	61	69	77	85	93
	1.0	0	0	0	0	0	0	0	8	16	24	32	40
	0.9	-1	-1	-1	-1	-1	-1	-1	7	15	23	31	39
	0.8	-3	-3	-3	-3	-3	-3	-3	5	13	21	29	37
	0.7	-5	-5	-5	-5	-5	-5	-5	3	11	19	27	35
	0.6	-8	-8	-8	-8	-8	-8	-8	0	8	16	24	32
	0.5	-20	-20	-20	-20	-20	-20	-20	-12	-4	4	12	20
	0.4	-40	-40	-40	-40	-40	-40	-40	-32	-24	-16	-8	0

tIH													
Slew Rate	CK, CK# Differential												
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/CMD	4.0	68	68	68	68	68	68	68	76	84	92	102	118
	3.5	65	65	65	65	65	65	65	73	81	89	99	115
	3.0	60	60	60	60	60	60	60	68	76	84	94	110
	2.5	54	54	54	54	54	54	54	62	70	78	88	104
	2.0	45	45	45	45	45	45	45	53	61	69	79	95
	1.5	30	30	30	30	30	30	30	38	46	54	64	80
	1.0	0	0	0	0	0	0	0	8	16	24	34	50
	0.9	-3	-3	-3	-3	-3	-3	-3	5	13	21	31	47
	0.8	-8	-8	-8	-8	-8	-8	-8	1	9	17	27	43
	0.7	-13	-13	-13	-13	-13	-13	-13	-5	3	11	21	37
	0.6	-20	-20	-20	-20	-20	-20	-20	-12	-4	4	14	30
	0.5	-30	-30	-30	-30	-30	-30	-30	-22	-14	-6	4	20
	0.4	-45	-45	-45	-45	-45	-45	-45	-37	-29	-21	-11	5

Figure 25: tIS/tIH derating at AC160 for DDR3L-800/1066/1333/1600

tIS/tIH derating at AC135 for DDR3L-800/1066/1333/1600													
tIS													
Slew Rate	CK, CK# Differential												
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/CMD	4.0	102	102	102	102	102	102	102	110	118	126	134	142
	3.5	97	97	97	97	97	97	97	105	113	121	129	137
	3.0	90	90	90	90	90	90	90	98	106	114	122	130
	2.5	81	81	81	81	81	81	81	89	97	105	113	121
	2.0	68	68	68	68	68	68	68	76	84	92	100	108
	1.5	45	45	45	45	45	45	45	53	61	69	77	85
	1.0	0	0	0	0	0	0	0	8	16	24	32	40
	0.9	2	2	2	2	2	2	2	10	18	26	34	42
	0.8	3	3	3	3	3	3	3	11	19	27	35	43
	0.7	6	6	6	6	6	6	6	14	22	30	38	46
	0.6	9	9	9	9	9	9	9	17	25	33	41	49
	0.5	5	5	5	5	5	5	5	13	21	29	37	45
	0.4	-3	-3	-3	-3	-3	-3	-3	6	14	22	30	38

tIH													
Slew Rate	CK, CK# Differential												
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/CMD	4.0	68	68	68	68	68	68	68	76	84	92	102	118
	3.5	65	65	65	65	65	65	65	73	81	89	99	115
	3.0	60	60	60	60	60	60	60	68	76	84	94	110
	2.5	54	54	54	54	54	54	54	62	70	78	88	104
	2.0	45	45	45	45	45	45	45	53	61	69	79	95
	1.5	30	30	30	30	30	30	30	38	46	54	64	80
	1.0	0	0	0	0	0	0	0	8	16	24	34	50
	0.9	-3	-3	-3	-3	-3	-3	-3	5	13	21	31	47
	0.8	-8	-8	-8	-8	-8	-8	-8	1	9	17	27	43
	0.7	-13	-13	-13	-13	-13	-13	-13	-5	3	11	21	37
	0.6	-20	-20	-20	-20	-20	-20	-20	-12	-4	4	14	30
	0.5	-30	-30	-30	-30	-30	-30	-30	-22	-14	-6	4	20
	0.4	-45	-45	-45	-45	-45	-45	-45	-37	-29	-21	-11	5

Figure 26: tIS/tIH derating at AC135 for DDR3L-800/1066/1333/1600

tIS/tIH derating at AC125 for DDR3L-1866													
tIS													
Slew Rate	CK, CK# Differential												
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/CMD	4.0	94	94	94	94	94	94	94	102	110	118	126	134
	3.5	90	90	90	90	90	90	90	98	106	114	122	130
	3.0	84	84	84	84	84	84	84	92	100	108	116	124
	2.5	75	75	75	75	75	75	75	83	91	99	107	115
	2.0	63	63	63	63	63	63	63	71	79	87	95	103
	1.5	42	42	42	42	42	42	42	50	58	66	74	82
	1.0	0	0	0	0	0	0	0	8	16	24	32	40
	0.9	3	3	3	3	3	3	3	11	19	27	35	43
	0.8	6	6	6	6	6	6	6	14	22	30	38	46
	0.7	10	10	10	10	10	10	10	18	26	34	42	50
	0.6	16	16	16	16	16	16	16	24	32	40	48	56
	0.5	15	15	15	15	15	15	15	23	31	39	47	55
	0.4	13	13	13	13	13	13	13	21	29	37	45	53

tIH													
Slew Rate	CK, CK# Differential												
(V/ns)		8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.8	1.6	1.4	1.2	1.0
ADD/CMD	4.0	68	68	68	68	68	68	68	76	84	92	102	118
	3.5	65	65	65	65	65	65	65	73	81	89	99	115
	3.0	60	60	60	60	60	60	60	68	76	84	94	110
	2.5	54	54	54	54	54	54	54	62	70	78	88	104
	2.0	45	45	45	45	45	45	45	53	61	69	79	95
	1.5	30	30	30	30	30	30	30	38	46	54	64	80
	1.0	0	0	0	0	0	0	0	8	16	24	34	50
	0.9	-3	-3	-3	-3	-3	-3	-3	5	13	21	31	47
	0.8	-8	-8	-8	-8	-8	-8	-8	1	9	17	27	43
	0.7	-13	-13	-13	-13	-13	-13	-13	-5	3	11	21	37
	0.6	-20	-20	-20	-20	-20	-20	-20	-12	-4	4	14	30
	0.5	-30	-30	-30	-30	-30	-30	-30	-22	-14	-6	4	20
	0.4	-45	-45	-45	-45	-45	-45	-45	-37	-29	-21	-11	5

Figure 27: tIS/tIH derating at AC125 for DDR3L-1866

tDS/tIH derating at AC150 for LPDDR3									
tDS									
Slew Rate (V/ns)		DQS, DQS# Differential							
		10.0	9.0	8.0	7.0	6.0	5.0	4.0	3.0
DQ	6.0	50	50	50	50	50	50	50	-
	5.5	48	48	48	48	48	48	48	-
	5.0	45	45	45	45	45	45	45	-
	4.5	42	42	42	42	42	42	42	-
	4.0	38	38	38	38	38	38	38	-
	3.0	-	-	-	25	25	25	25	38
	2.0	-	-	-	-	0	0	0	13
	1.5	-	-	-	-	-	-25	-25	-12

tDH									
Slew Rate (V/ns)		DQS, DQS# Differential							
		10.0	9.0	8.0	7.0	6.0	5.0	4.0	3.0
DQ	6.0	34	34	34	34	34	34	34	-
	5.5	32	32	32	32	32	32	32	-
	5.0	30	30	30	30	30	30	30	-
	4.5	28	28	28	28	28	28	28	-
	4.0	25	25	25	25	25	25	25	-
	3.0	-	-	-	17	17	17	17	29
	2.0	-	-	-	-	0	0	0	13
	1.5	-	-	-	-	-	-17	-17	-4

Figure 28: tDS/tIH derating at AC150 for LPDDR3

tDS/tDH derating at AC135 for LPDDR3									
tDS									
Slew Rate (V/ns)		DQS, DQS# Differential							
		10.0	9.0	8.0	7.0	6.0	5.0	4.0	3.0
DQ	6.0	45	45	45	45	45	45	45	-
	5.5	43	43	43	43	43	43	43	-
	5.0	41	41	41	41	41	41	41	-
	4.5	38	38	38	38	38	38	38	-
	4.0	34	34	34	34	34	34	34	-
	3.0	-	-	-	23	23	23	23	34
	2.0	-	-	-	-	0	0	0	11
	1.5	-	-	-	-	-	-23	-23	-12

tDH									
Slew Rate (V/ns)		DQS, DQS# Differential							
		10.0	9.0	8.0	7.0	6.0	5.0	4.0	3.0
DQ	6.0	34	34	34	34	34	34	34	-
	5.5	32	32	32	32	32	32	32	-
	5.0	30	30	30	30	30	30	30	-
	4.5	28	28	28	28	28	28	28	-
	4.0	25	25	25	25	25	25	25	-
	3.0	-	-	-	17	17	17	17	29
	2.0	-	-	-	-	0	0	0	13
	1.5	-	-	-	-	-	-17	-17	-4

Figure 29: tDS/tDH derating at AC135 for LPDDR3

tIS/tIH derating at AC150 for LPDDR3									
tIS									
Slew Rate (V/ns)		CK, CK# Differential							
		10.0	9.0	8.0	7.0	6.0	5.0	4.0	3.0
ADD/CMD	6.0	50	50	50	50	50	50	50	-
	5.5	48	48	48	48	48	48	48	-
	5.0	45	45	45	45	45	45	45	-
	4.5	42	42	42	42	42	42	42	-
	4.0	38	38	38	38	38	38	38	-
	3.0	-	-	-	25	25	25	25	38
	2.0	-	-	-	-	0	0	0	13
	1.5	-	-	-	-	-	-25	-25	-12

tIH									
Slew Rate (V/ns)		CK, CK# Differential							
		10.0	9.0	8.0	7.0	6.0	5.0	4.0	3.0
ADD/CMD	6.0	34	34	34	34	34	34	34	-
	5.5	32	32	32	32	32	32	32	-
	5.0	30	30	30	30	30	30	30	-
	4.5	28	28	28	28	28	28	28	-
	4.0	25	25	25	25	25	25	25	-
	3.0	-	-	-	17	17	17	17	29
	2.0	-	-	-	-	0	0	0	13
	1.5	-	-	-	-	-	-17	-17	-4

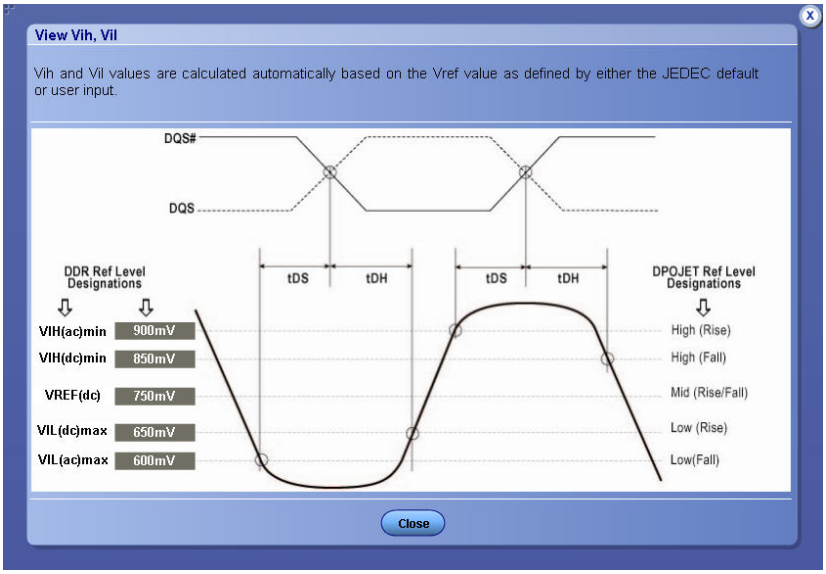
Figure 30: tIS/tIH derating at AC150 for LPDDR3

tIS/tIH derating at AC135 for LPDDR3																	
tIS									tIH								
Slew Rate (V/ns)		CK, CK# Differential								Slew Rate (V/ns)		CK, CK# Differential							
		10.0	9.0	8.0	7.0	6.0	5.0	4.0	3.0			10.0	9.0	8.0	7.0	6.0	5.0	4.0	3.0
ADD/CMD	6.0	45	45	45	45	45	45	45	-	ADD/CMD	6.0	34	34	34	34	34	34	34	-
	5.5	43	43	43	43	43	43	43	-		5.5	32	32	32	32	32	32	32	-
	5.0	41	41	41	41	41	41	41	-		5.0	30	30	30	30	30	30	30	-
	4.5	38	38	38	38	38	38	38	-		4.5	28	28	28	28	28	28	28	-
	4.0	34	34	34	34	34	34	34	-		4.0	25	25	25	25	25	25	25	-
	3.0	-	-	-	23	23	23	23	34		3.0	-	-	-	17	17	17	17	29
	2.0	-	-	-	-	0	0	0	11		2.0	-	-	-	-	0	0	0	13
	1.5	-	-	-	-	-	-23	-23	-12		1.5	-	-	-	-	-	-17	-17	-4

Figure 31: tIS/tIH derating at AC135 for LPDDR3

Vih-Vil reference levels

On clicking the **View** button, the VIH(ac)min, VIH(dc)min, VIL(ac)max, VIL(dc)max and VREF(dc) values are as shown based on the Vref voltage.



The following table lists the Vih and Vil values for all the DDR generations except GDDR3, LPDDR4 and LPDDR4X:

Table 30: VIH and VIL values for DDR generations

Generation	Data rate	VIH(ac)min	VIH(dc)min	VREF(dc)	VIL(dc) max	VIL(ac)max
DDR	200 MT/s	1.56 V	1.4 V	1.25 V	1.1 V	940 mV
	266 MT/s	1.56 V	1.4 V	1.25 V	1.1 V	940 mV
	333 MT/s	1.56 V	1.4 V	1.25 V	1.1 V	940 mV
	400 MT/s	1.61 V	1.45 V	1.3 V	1.15 V	990 mV

Table continued…

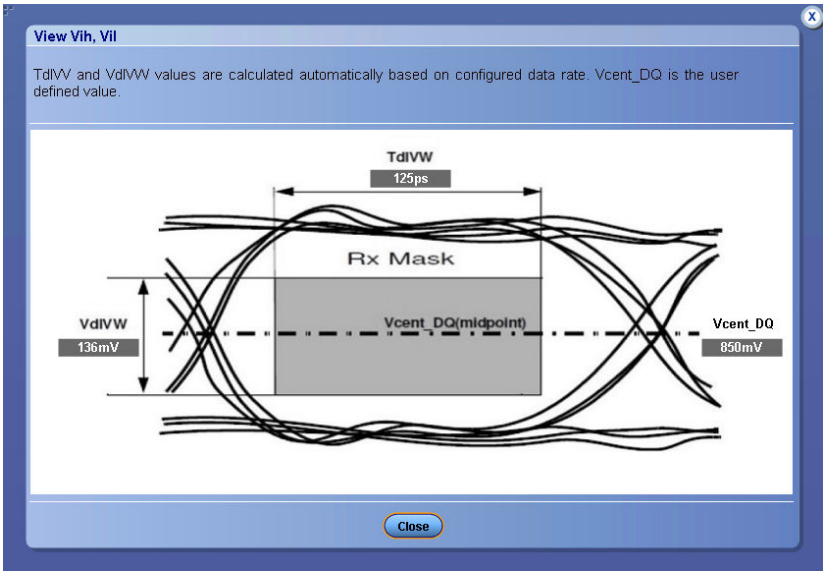
Generation	Data rate	VIH(ac)min	VIH(dc)min	VREF(dc)	VIL(dc) max	VIL(ac)max
DDR2	400 MT/s	1.15 V	1.025 V	900 mV	775 mV	650 mV
	533 MT/s	1.15 V	1.025 V	900 mV	775 mV	650 mV
	667 MT/s	1.1 V	1.025 V	900 mV	775 mV	700 mV
	800 MT/s	1.1 V	1.025 V	900 mV	775 mV	700 mV
DDR3	800 MT/s	925 mV	850 mV	750 mV	650 mV	575 mV
	1066 MT/s	925 mV	850 mV	750 mV	650 mV	575 mV
	1333 MT/s	925 mV	850 mV	750 mV	650 mV	575 mV
	1600 MT/s	925 mV	850 mV	750 mV	650 mV	575 mV
	1866 MT/s	885 mV	850 mV	750 mV	650 mV	615 mV
	2133 MT/s	885 mV	850 mV	750 mV	650 mV	615 mV
DDR3L	800 MT/s	835 mV	765 mV	675 mV	585 mV	515 mV
	1066 MT/s	835 mV	765 mV	675 mV	585 mV	515 mV
	1333 MT/s	835 mV	765 mV	675 mV	585 mV	515 mV
	1600 MT/s	835 mV	765 mV	675 mV	585 mV	515 mV
	1866 MT/s	805 mV	765 mV	675 mV	585 mV	545 mV
DDR4[7]	1600 MT/s	700 mV	675 mV	600 mV	525 mV	500 mV
	1866 MT/s	700 mV	675 mV	600 mV	525 mV	500 mV
	2133 MT/s	700 mV	675 mV	600 mV	525 mV	500 mV
	2400 MT/s	700 mV	675 mV	600 mV	525 mV	500 mV
	2666 MT/s	690 mV	665 mV	600 mV	535 mV	510 mV
	2933 MT/s	690 mV	665 mV	600 mV	535 mV	510 mV
	3200 MT/s	690 mV	665 mV	600 mV	535 mV	510 mV

Table continued…

[7] Applicable for Address/Command measurements

Generation	Data rate	VIH(ac)min	VIH(dc)min	VREF(dc)	VIL(dc) max	VIL(ac)max
GDDR5	4000 MT/s	900 mV	850 mV	750 mV	650 mV	600 mV
	4800 MT/s	900 mV	850 mV	750 mV	650 mV	600 mV
	5000 MT/s	900 mV	850 mV	750 mV	650 mV	600 mV
	5500 MT/s	900 mV	850 mV	750 mV	650 mV	600 mV
LPDDR	200 MT/s	1.44 V	1.26 V	900 mV	540 mv	360 mV
	266 MT/s	1.44 V	1.26 V	900 mV	540 mv	360 mV
	333 MT/s	1.44 V	1.26 V	900 mV	540 mv	360 mV
	370 MT/s	1.44 V	1.26 V	900 mV	540 mv	360 mV
	400 MT/s	1.44 V	1.26 V	900 mV	540 mv	360 mV
LPDDR2	333 MT/s	900 mV	800 mV	600 mV	400 mV	300 mV
	400 MT/s	900 mV	800 mV	600 mV	400 mV	300 mV
	533 MT/s	820 mV	730 mV	600 mV	470 mV	380 mV
	667 MT/s	820 mV	730 mV	600 mV	470 mV	380 mV
	800 MT/s	820 mV	730 mV	600 mV	470 mV	380 mV
	933 MT/s	900 mV	800 mV	600 mV	400 mV	300 mV
	1066 MT/s	820 mV	730 mV	600 mV	470 mV	380 mV
LPDDR3	333 MT/s	750 mV	700 mV	600 mV	500 mV	450 mV
	800 MT/s	750 mV	700 mV	600 mV	500 mV	450 mV
	1066 MT/s	750 mV	700 mV	600 mV	500 mV	450 mV
	1200 MT/s	750 mV	700 mV	600 mV	500 mV	450 mV
	1333 MT/s	750 mV	700 mV	600 mV	500 mV	450 mV
	1466 MT/s	750 mV	700 mV	600 mV	500 mV	450 mV
	1600 MT/s	750 mV	700 mV	600 mV	500 mV	450 mV

The TdIVW and VdIVW values changes for DDR4 generation as shown based on the data rate.



The following table lists the TdIVW and VdIVW values for DDR4:

Table 31: TdIVW, VdIVW values for DDR4 generations

Generation	Data rate	TdIVW	VdIVW
DDR4	1600 MT/s	125ps	136mV
	1860 MT/s	107.18ps	136mV
	2133 MT/s	93.76ps	136mV
	2400 MT/s	83.33ps	130mV
	2666 MT/s	82.52ps	120mV
	2933 MT/s	78.42ps	115mV
	3200 MT/s	71.88ps	110mV

Using digital channels

You must do the following steps when you select Logic State+DQ/DQS Phase Alignment burst detection method in an MSO oscilloscope. The DDR3 signal is an example here, but a few settings must be changed for other DDR standards. Using appropriate label names for digital signals (such as RS, CAS, CS and WE) helps in defining the sources in a bus.

For more details on how to set up digital channels, refer *Setting Up Digital Channels* in your oscilloscope user manual.

Calculating Digital Channel Threshold

Follow the steps to calculate the digital channel threshold:

1. View the analog equivalent of the input digital signal (refer Viewing Analog Characteristics of Digital Waveforms in the MSO oscilloscope user manual).

2. Measure the thresholds for the CS signal as shown in an example:
   - Measure the Min, and Pk-Pk on the analog waveform and calculate the threshold value approximately as follows:

     Threshold Value = Min + 50% of Pk-Pk.
   - For example: If the measured Min value is 450 mV and Pk-Pk is 666 mV, using the above formula, the threshold value is set to 750 mV.

3. Enter the calculated threshold value in the Digital setup dialog box under Threshold.

Note: Thresholds are DUT specific. Carry out the same procedure for every DUT under test.

Configuring Sources for a Bus

The steps to configure source for a bus are:

1. Set up the bus (refer to *Set Up a Parallel Bus* in your MSO oscilloscope user manual).
2. Add sources to the bus. Ensure that the order of sources (MSB to LSB) is in sync with the sources mentioned in the corresponding symbol file.

   For example: DDR3 symbol file specifies the following:

SYMBOL	MSB -> LSB
READ	0101
WRITE	0100

Set up the sources for these symbols as shown in the following figure:

Configuring Burst Latency and Tolerance

The following example shows how Burst Latency and Tolerance values are calculated using DDR3 1066 READ burst signal:

Note: Burst Latency and Tolerance values are specific to a DUT and should be computed for each DUT under test.

1. *Set up digital channels* and *configure the bus*. Connect DQ/DQS to Ch1/Ch2 sources. Press **Single** on the oscilloscope front panel for signal acquisition.
2. Locate the READ burst and place the cursor in the center of the burst. Place the second cursor on the first rising edge oscilloscope of the DQS signal as shown in the following figure:

3. Note the time difference between the two cursors. In this example, it is 10.24 ns (called t1) as shown in the following figure.
4. Place the cursors on two consecutive rising/falling edges of the DQS signal as shown:

5. Note the time difference between the two cursors. It is 1.92 ns (called t2) as shown in the above figure.
6. Calculate CAS Min using the equation:

   CAS Min = t1/t2 – 0.5

   In the above example, CAS Min= (10.24/1.92) – 0.5 ~ 5 (approximately)
7. Calculate CAS Max using the equation:

   CAS Min = t1/t2 + 0.5

   In the above example, CAS Min= (10.24/1.92) + 0.5 ~ 6 (approximately)
8. Configure CAS Min and Max values in DDRA as shown:

Providing inaccurate CAS Min and Max values can result in an offset in Mark start/end calculations which in turn provides inaccurate measurement results. An example of incorrect CAS Min\Max values. is as follows:

Note: You can perform the above steps once and then save the setup. Setup files help to recall the settings corresponding to a particular DUT.

Error codes and warnings

Code	Description
E102	File does not exist.
E103	DPOJET is not able to open the help file. In order to use the help file, please reinstall DPOJET.
E104	Mask Hits measurement requires an Eye diagram plot, but no more plots can be assigned. Please remove a plot before adding a Mask Hits measurement.
E105	The maximum number of plots you can select is 4.
E106	No Spectrum plot data is available.
E202	The upper range must be greater than the lower range.
E400	A measurement failed to complete successfully.
W410	Number of edges are not sufficient for a measurement.
E411	In at least one zone, there are too few edges to complete a measurement.

Table continued…

Code	Description
E424	No edges or UI of the required type were found in the waveform. If this is not a clock signal, check the Vref threshold and record length.
E425	No transitions of the selected Bit Type were found in the waveform.
E500	The record lengths of the source waveforms differ. Please configure for sources with equivalent record lengths.
E1001	Vertical Autoset Failed: Signal on Source x has extreme offset.
E1002	Vertical Autoset Failed: Amplitude of Source x is too small.
E1003	Vertical Autoset Failed: Amplitude or DC offset of Source x is too high.
E1004	Vertical Autoset Failed: No signal on Source x.
E1005	Vertical Autoset Failed: Signal on Source x exceeds top of scale.
E1006	Vertical Autoset Failed: Signal on Source x exceeds bottom of scale.
E1007	Vertical Autoset Failed: Signal on Source x is clipped on top.
E1008	Vertical Autoset Failed: Signal on Source x is clipped on bottom.
E1009	Vertical Autoset Failed: Measurement error (ISDB error code = 6) on Source x.
E1010	Vertical Autoset Failed: Measurement error (ISDB error code = 7) on Source x.
W1011	A change to Source x vertical settings caused overload to disconnect. Original settings are restored and Source x is reconnected. Ignore Oscilloscope message.
E1012	Vertical Autoset Failed: None of the selected measurements use live sources (Ch1-Ch4). Horizontal autoset works for live sources only.
E1013	Vertical Autoset Failed: Invalid signal on Source x.
E1020	Horizontal Autoset Failed: None of the selected measurements use live sources (Ch1-Ch4). Horizontal autoset works for live sources only.
E1021	Horizontal Autoset Failed: On Source x, cannot determine resolution of rising/falling edges.
E1022	Horizontal Autoset Failed: Horizontal resolution is at the maximum.
E1026	Horizontal Autoset Failed: Source amplitude to too low.
E1027	Horizontal Autoset Failed: Signal is clipped at the top - positive clipping.
E1028	Horizontal Autoset Failed: Signal is clipped at the bottom - negative clipping.

Table continued…

Code	Description
E1029	Horizontal Autoset Failed: Signal frequency is extremely low.
E1035	Oscilloscope has gone into invalid state. Please restart the system.
E1040	Autoset Failed: None of the live sources (Ch1-Ch4) selected.
W1051	Ref Level Autoset: Waveform for the source x is clipped.
W1053	Ref Level Autoset: Source amplitude is extremely low.
E1054	Ref Level Autoset: Error in setting reference levels.
E1055	Ref Level Autoset Failed: No waveform to measure.
E1056	Ref Level Autoset: Unstable Histogram for waveform on source x.
E1057	Ref Level Autoset: No selected source.
E1058	Ref Level Autoset Failed: Invalid signal on source x.
E1059	Ref Level Autoset Error: Source x is not defined.
E1061	Since Digital Filters (DSP) are enabled, maximum sampling rate has been retained. To enable adaptive use of lower sampling rate, please choose Analog Only under Vertical. Bandwidth Enhanced.
E1062	The maximum Record Length (RL) in autoset is restricted to 25M, set the RL manually for >25M.
E1063	The minimum Record Length (RL) in autoset is restricted to 500K, set the RL manually for <500K.
E2001	The maximum number of measurements has been reached.
E2002	All the refs are used as sources by the measurements. Export to Ref is not possible.
E2003	Ref ‘x’ is already used as a measurement source.
E2004	Ref ‘x’ is already used as a destination for other measurement.
E2005	No measurement(s) are selected. Export to Ref is not possible.
E2006	No results available to export to ref.
E2007	There are no time trend results for the selected measurement(s).
E2008	No ref destination is selected. Results will not be exported to ref.
E3001	Could not open or create a log file. Please ensure that you have read/write permission to access log folders and files.

Table continued…

Code	Description
E3002	The specified path is invalid (for example: The specified path is not mapped to a drive).
E3003	The specified path, file name or both exceed the system defined length. For Example: On Windows-based platforms, the path name must be less than 248 characters and file names less than 260 characters.
E3004	The specified path directory is read-only or is not empty.
E3005	Please ensure that the file is currently not in use by other process and/or has not exceeded the file size limit.
E3006	Invalid filename: Check whether the file name contains a colon (:) in the middle of the string.
E3007	Select at least one measurement from the table before you save.
E3008	There are currently no results to save. Please run a measurement.
E3009	Current statistics is successfully saved at C:\TekApplications\DPOJET\Log\Statistics.
E3010	Access to file/directory denied. Please ensure that the file/directory has read/write permissions.
E3011	Mask Hits Measurements will not be selected as this feature is not available for Mask Hits measurement.
E3012	Folder does not exist.
E4000	Not enough data points. Unable to render plot(s).
E4001	Internal measurement error. Please remove a measurement and try again.
E4002	Not enough data points for spectrum computation.
E4003	Due to high memory usage, only a portion of the waveform could be processed. Please reduce your record length or the number of measurements.
E4004	An error occurred in the edge extraction process.
E4005	Qualifier: The record length and sample interval must match across the waveforms.
E4006	A maximum of 4096 qualifier zones is supported. The entire waveform will not be processed and hence partial measurement results are available.
E4007	Logic Qualifier enabled and no qualifier zones found.
W4008	The configured Ref voltage for Overshoot must be greater than or equal to the mid autoset ref levels.
W4009	The configured Ref voltage for Undershoot must be lesser than or equal to the mid autoset ref levels.

Table continued…

Code	Description
E4013	The configured Ref voltage must be greater than or equal to the mid autoset ref levels.
E4014	The configured Ref voltage must be lesser than or equal to the mid autoset ref levels.
E4015 [8]OMING	One or more qualifier zones had too few edges for measurement calculation.
E4016	Not enough edges in the waveform for measurement calculation.
E4017	Qualifier not enabled and hence no qualifier zones found. Please enable the qualifier.
E4018	The preamble is incomplete in all the qualifier zones.
E4019 [8]	The preamble is incomplete in one or more qualifier zones.
E4020	The postamble is incomplete in all the qualifier zones.
E4021	The postamble is incomplete in one or more qualifier zones. Displays the zone number (x) for which the preamble/postamble fails.
E4022 [8]	Not enough samples present in the qualifier zones. Please increase the sampling rate and reacquire the waveform.
E4023	The configured ref levels are not correct. The high ref level should be >= Mid and Mid should be >= Low for both Rise and Fall slopes. Reconfigure the ref levels and run the measurement.
E4024	Could not compute proper High and Low values.
W4025	The signal does not cross the configured Ref Voltage and hence the result shows zero population. Please adjust the Ref voltage value.
E4027	From Symbol not found in the acquisition.
E4028	To Symbol not found in the acquisition.
E4029	The configured High Ref voltage must be ≥ to the mid autoset ref levels.
E4030	The configured Low Ref voltage must be ≤ to the mid autoset ref levels.
E4031	The configured High Ref voltage must be ≥ to the mid autoset ref levels and the configured Low Ref voltage must be ≤ to the mid autoset ref levels.
E5005 [9]	Occurs while running setup. Please make sure you have finished any previous setup and closed other applications
W5005	The path or file name exceeds the system limit of 260 characters.

Table continued…

[8] Displays the zone number (x) for which the preamble/postamble fails.

[9] This error occurs during DPOJET installation on a DPO/MSO series of oscilloscopes. Delete the Installshield folder under C:\Program files\Common Files and delete all files and folders under C:\Windows\Temp folder. Restart the installation again.

Code	Description
E9004	Derating will not be applied to the limits as Slew Rate measurements failed.
W9005	Derating value calculated using single Slew Rate measurement value.
W9006	Derating value cannot be computed since the calculated Slew Rate is not present in the derating table [10].
E9007	Derating Error [11].

[10] Signal Slew Rate value is outside the derating table (Ex: If DDR2-800 MT/s tDS derating with a differential probe has a DQS differential slew rate of 0.65 V/ns, this warning message is displayed as the derating table definition starts from 0.8 V/ns).

Derating value is not supported (TBD) in the specification (Ex: If the DQS differential slew rate is 2.0 V/ns and the DQ slew rate is 0.7 V/ns, then the value is "-"(TBD).

Derating will not be applied for the above cases and the base limit will be displayed in the results table.

[11] Slew Rate measurements used to calculate the derated value failed to Run as there are no sufficient edges on the Rise and Fall slopes of the waveform.

Base measurement limits are not defined as per the specification.

Configuration parameters

About parameters

This section describes the DDRA application parameters and includes the menu default settings. Refer to the user manual of your oscilloscope for operating details of other controls, such as front-panel buttons.

The parameter tables list the selections or range of values available for each option, the incremental unit of numeric values, and the default selection or value.

Step 1: Generation rate and levels parameters

Step1 includes the following parameters:

Table 32: Generation, rate and levels parameters

Parameter	Values	Default Value
DDR Generation	DDR, DDR2, DDR3, DDR3L, DDR4, LPDDR, LPDDR2, LPDDR3, LPDDR4, LPDDR4X, GDDR3, GDDR5	DDR3
Data Rate [12]	**DDR**: 200 MT/s, 266 MT/s, 333 MT/s, 400 MT/s, Custom	200 MT/s
	DDR2: 400 MT/s, 533 MT/s, 667 MT/s, 800 MT/s, 1066 MT/s, Custom	400 MT/s
	DDR3: 800 MT/s, 1066 MT/s, 1333 MT/s, 1866 MT/s, 2133 MT/s, Custom	800 MT/s
	DDR3L: 800 MT/s, 1066 MT/s, 1333 MT/s, 1600 MT/s, 1866 MT/s, Custom	800 MT/s
	DDR4: 1600 MT/s, 1866 MT/s, 2133 MT/s, 2400 MT/s, 2666 MT/s, 2933 MT/s, 3200 MT/s, Custom	1600 MT/s
	LPDDR: 200 MT/s, 266 MT/s, Custom	200 MT/s
	LPDDR2: 333 MT/s, 400 MT/s, 533 MT/s, 667 MT/s, 933 MT/s, 1066 MT/s, Custom	333 MT/s
	LPDDR3: 333 MT/s, 800 MT/s, 1066 MT/s, 1200 MT/s, 1333 MT/s, 1466 MT/s, 1600 MT/s, Custom	333 MT/s
	LPDDR4: 533 MT/s, 1066 MT/s, 1600 MT/s, 2133 MT/s, 2400 MT/s, 2667 MT/s, 3200 MT/s, 3733 MT/s, 4266 MT/s, Custom	533 MT/s
	LPDDR4X: 533 MT/s, 1066 MT/s, 1600 MT/s, 2133 MT/s, 2400 MT/s, 2667 MT/s, 3200 MT/s, 3733 MT/s, 4266 MT/s, Custom	533 MT/s
	GDDR3: 500 MT/s, 600 MT/s, 700 MT/s, 800 MT/s, 900 MT/s, 1000 MT/s, Custom	500 MT/s
	GDDR5: 4000 MT/s, 4800 MT/s, 5000 MT/s, 5500 MT/s, Custom	4000 MT/s
	Custom	800 MT/s
Vdd	JEDEC Default, User Defined	JEDEC Default
Vref	JEDEC Default, User Defined	JEDEC Default

Table continued…

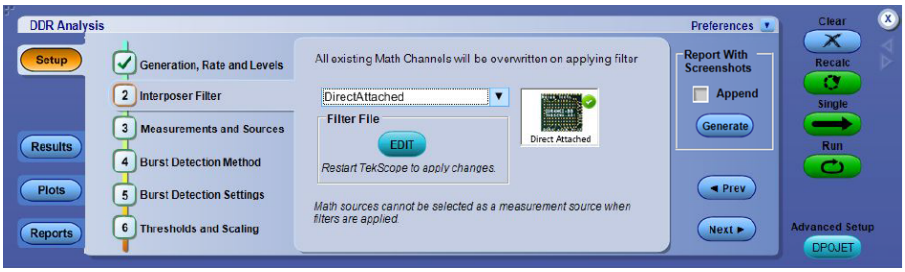
[12] Data rate varies for different DDR standards.

Parameter	Values	Default Value
Vcent_DQ	**DDR4**: User Defined	850 mV
	LPDDR4: User Defined	201.5 mV
	LPDDR4X: User Defined	150 mV
Vcent_CA	**LPDDR4**: User Defined	191.5 mV
VOH	**LPDDR4**: VDDQ/3, VDDQ/2.5	VDDQ/3
	LPDDR4X: VDDQ/2, VDDQ/1.667	VDDQ/2
VDDQ	**LPDDR4X**: User Defined	600 mV
Vref_CA	**DDR4**: User Defined	600 mV

Step 2: Interposer filter parameters

Step 2 includes the following parameters under Filter Type:

- None
- User Defined
- Direct Attached



Step 3: Measurement and sources parameters

Step 3 includes the following parameters under Measurement Type:

- Read Bursts
- Write Bursts
- Clock(Diff)
- Clock(Single Ended)
- DQS(Single Ended, Write)
- DQS(Single Ended, Read)
- Address/Command
- Refresh
- Power Down
- Active
- Precharge
- WCK(Diff)
- WCK(Single Ended)

The sources parameters are as shown in the following table:

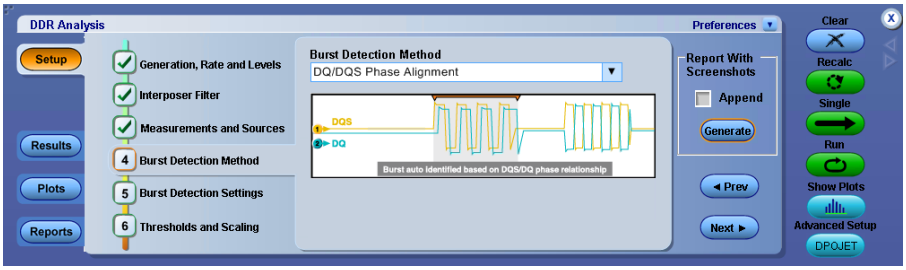
Table 33: Sources parameters

Option	Parameters	Default setting
DQS	Ch1-Ch4, Ref1-Ref4, Math1-Math4	Ch1
DQS#	Ch1-Ch4, Ref1-Ref4, Math1-Math4	Ch4
DQ	Ch1-Ch4, Ref1-Ref4, Math1-Math4	Ch2
Addr/Cmd	Ch1-Ch4, Ref1-Ref4, Math1-Math4	Ch4
CK	Ch1-Ch4, Ref1-Ref4, Math1-Math4	Ch3
CK#	Ch1-Ch4, Ref1-Ref4, Math1-Math4	Ch4
WCK	Ch1-Ch4, Ref1-Ref4, Math1-Math4	Ch1
WCK#	Ch1-Ch4, Ref1-Ref4, Math1-Math4	Ch4
Digital channels	D0-D15 (User should configure digital sources to bus)	None

Step 4: Burst detection method parameters

Step 4 has the following parameters:

- *DQ/DQS Phase Alignment*
- *Chip Select, Latency + DQ/DQS Phase Alignment*
- *Logic State + Burst Latency*
- *Visual Search*



Step 5: Burst detection settings parameters

Step 5 has the following parameters:

Note: The DQ/DQS Phase Alignment settings are same for Chip Select and Logic State Burst Detection methods.

Table 34: Burst detection parameters

Option	Parameters	Default setting
Chip Select, Latency + DQ/DQS Phase Alignment		
CS Source	None, Ch1-Ch4, Ref1-Ref4, Math1-Math4	None
CS Mode [13]	Auto, Manual	Auto

Table continued…

Option	Parameters	Default setting
CAS Min(Cyc) [13]	0–1k	2.0
CS Active [13]	High, Low	Low
CS Level [13]	-50V to +50V	0.0 V
CAS Max(Cyc) [13]	0–1k	3.0
DQ/DQS Levels	Auto, Manual	Auto
DQ/DQS Phase Alignment		
Strobe		
High	Auto, Manual	Auto
Mid	Auto, Manual	Auto
Low	Auto, Manual	Auto
Data		
High	Auto, Manual	Auto
Mid	Auto, Manual	Auto
Low	Auto, Manual	Auto
Edge Detection Hysteresis	Auto, Manual Value: • Min: 0.0 • Max: 50.0	Auto Value: 10.0%
Termination Logic Margin	Auto, Manual Value: • Min: 0.0 • Max: 100	Auto Value: 20.0%
LogicState + Burst Latency DQ/DQS Phase Alignment [14]		
Bus	B1–B16	None
Tolerance	0–50 G	1Cyc

Table continued…

[13] Available only when you select CS source.

[14] Available only for the MSO series of oscilloscopes.

Option	Parameters	Default setting
Burst Latency	0–50 G	2.5Cyc
Burst Length	0–50 G(ui)	8 UI
DQ/DQS Levels	Auto, Manual	Auto
Logic Trigger	MODE_REG, REFRESH, PRECHARGE, ACTIVATE, WRITE, READ, SRX, DESELECT, SRE, PDE	MODE_REG

Step 6: Thresholds and scaling parameters

Step 6 has the following parameters:

Table 35: Thresholds and scaling parameters

Option	Parameters	Default setting
Measurement Thresholds	Auto, Manual	Auto
Vertical Scaling - Auto	Set, Clear	Clear
Horizontal Scaling - Auto	Set, Clear	Clear
Alternate Thresholds [15]	AC160, AC130, AC135, AC175 , AC150, AC125, AC220 , AC300	Varies for data rate and measurement type.
Measurement Levels		
Rise High	–20 V to 20 V	Default varies depends upon DDR generation
Rise Mid	–20 V to 20 V	
Rise Low	–20 V to 20 V	
Fall High	–20 V to 20 V	
Fall Mid	–20 V to 20 V	
Fall Low	–20 V to 20 V	
Hysteresis	0 to 10 V	30 mV

[15] Available for DDR3,DDR3L generation.

Algorithms

About algorithms

The DDRA application can take measurements by selecting either Clock, Strobe, Data or CS Source as sources. The number of waveforms used by the application depends on the type of measurement being taken.

Oscilloscope Setup Guidelines

For all measurements, use the following guidelines to set up the oscilloscope:

- The signal is any channel, reference, or math waveform.
- The vertical scale for the waveform must be set so that the waveform does not exceed the vertical range of the oscilloscope.
- The sample rate must be set to capture sufficient waveform detail and avoid aliasing.
- Longer record lengths increase measurement accuracy but the oscilloscope takes longer to measure each waveform.

Search and Mark Algorithms

DDR search algorithm uses a moving average filter (FIR) to determine start and end of bursts. Filter length is decided based on the configured data rate and minimum burst length for each of the generations.

Once the bursts are marked, the min, max and mid voltage levels are calculated for each of the bursts. The mid-level detected on DQS is then used with a 10% hysteresis band to extract the edges from the DQS signal. These edges are stored and are then used for bit rate estimation.

The algorithm computes phase difference between DQ and DQS edges. This phase difference along with the preamble and postamble information is used to differentiate between READ and WRITE bursts. In the LPDDR4 generation, the strobe preamble compared with the ideal patterns to differentiate READ and WRITE bursts. LPDDR4 burst detection algorithm does not use phase difference between DQ and DQS.

The application scans for first the start of any burst, followed by that burst's termination condition. Once a start condition has been found, only the termination condition is searched until the end-of-record.

tDS(base)DQS(Informative)

tDS(base)DQS(Informative) is the input setup time between DQ and single-ended DQS signal. This measures the elapsed time between the designated edge of a data waveform and when the single-ended strobe (DQS) waveform crosses its own voltage reference level. The closest data edge to the strobe edge that falls within the range limits is used for the measurement.

This measurement is mapped to DPOJET->DDR standard measurement *DDR Setup-SE*.

This measurement is identical to the basic Setup measurement except that instead of using the Mid reference voltage for determining edge times, it uses the High and Low reference voltages for both the Data and Strobe (DQS). For more details on the reference voltage setup, refer to *DDR Setup/Hold reference levels: Single Ended DQS* .

The application calculates this measurement using the following equation:

$T_n^{Setup} = T_i^{Main} - T_n^{2nd}$

Where,

T_n^{Setup} is the setup time.

T_i^{Main} is the strobe (DQS) crossing time of $V_{IH(dc)}$min (for falling strobe edges) or $V_{IL(dc)}$max (for rising strobe edges) voltage level.

T_n ^{2nd} is the data (DQ) crossing time of $V_{IL(ac)}$max (for falling data edges) or $V_{IH(ac)}$min (for rising data edges) voltage level.

tDH(base)DQS(Informative)

tDH(base)DQS(Informative) is the input hold time between DQ and single-ended DQS signal. This measures the elapsed time between the designated edge of the single-ended strobe (DQS) waveform and the designated edge of a data waveform. The closest data edge to the strobe edge that falls within the range limits is used for the measurement.

This measurement is mapped to DPOJET>DDR standard measurement *DDR Hold-SE*.

This measurement is identical to the basic Hold measurement except that instead of using the Mid reference voltage for determining edge times, it uses the High and Low reference voltages for both the data and strobe (DQS). For more details on the reference voltage setup, refer to *DDR Setup/Hold reference levels: Single Ended DQS* .

The application calculates this measurement using the following equation:

T_n ^{Hold} = T_n ^{2nd} - 7_i ^{Main}

Where,

T_n ^{Hold} is the hold time.

T_i ^{Main} is the strobe (DQS) crossing time of $V_{IL(ac)}$max (for falling strobe edges) or $V_{IH(ac)}$min (for rising strobe edges) voltage level.

T_n ^{2nd} is the data (DQ) crossing time of $V_{IH(dc)}$min (for falling data edges) or $V_{IL(dc)}$max (for rising data edges) voltage level.

tDH(derated)DQS(Informative)

tDH(derated)DQS(Informative) measurement is same as *tDH(base)DQS(Informative),* except that the limits are dynamically calculated based on the slew rate of the single ended strobe signal.

tDS-Diff(base)

tDS-Diff(base) is defined as the input setup time between DQ and differential DQS signal. This measures the elapsed time between the designated edge of a data waveform and when the differential strobe (DQS) waveform crosses its own voltage reference level. The closest data edge to the strobe edge that falls within the range limits is used for the measurement.

This measurement is mapped to DPOJET->DDR standard measurement *DDR Setup-Diff*.

This measurement is identical to the basic Setup measurement except that instead of using the Mid reference voltage for determining edge times, it uses the High and Low reference voltages for the Data. The Mid reference level is still used for the Strobe (DQS) signal. For more details on the reference voltage setup, refer to *DDR Setup/Hold reference levels: Differential DQS* .

The application calculates this measurement using the following equation:

T_n ^{Setup} = T_i ^{Main} - T_n ^{2nd}

Where:

T_n ^{Setup} is the setup time.

T_i ^{Main} is the strobe (DQS) crossing time of 50% voltage level in the specified direction.

T_n ^{2nd} is the data (DQ) crossing time of $V_{IL(ac)}$max (for falling data edges) or $V_{IH(ac)}$min (for rising data edges) voltage level.

tDH-Diff(base)

tDH-Diff(base) is defined as the input hold time between Data (DQ) and Differential Strobe (DQS) signal. This measures the elapsed time between the designated edge of the data waveform and the designated edge of a differential strobe waveform. The closest data edge to the strobe edge that falls within the range limits is used for the measurement.

This measurement is mapped to DPOJET->DDR standard measurement *DDR Hold-Diff*.

This measurement is identical to the basic Hold measurement except that instead of using the Mid reference voltage for determining edge times, it uses the High and Low reference voltages for the data. The mid reference level is still used for the strobe (DQS) signal. For more details on the reference voltage setup, refer to *DDR Setup/Hold reference levels: Differential DQS* .

The application calculates this measurement using the following equation:

$T_n^{Hold} = T_n^{2nd} - T_i^{Main}$

Where,

T_n^{Hold} is the hold time.

T_I^{Main} is the strobe (DQS) crossing time of 50% voltage level in the specified direction.

T_n^{2nd} is the data (DQ) crossing time of $V_{IH(dc)}$min (for falling data edges) or $V_{IL(dc)}$max (for rising data edges) voltage level.

tIH(base)

tIH(base) is defined as the input hold time between address/command and differential clock signal. This measures the elapsed time between the designated edge of the address/command waveform and the rising edge of the differential clock waveform. The closest address/command edge to the clock edge that falls within the range limits is used for the measurement.

This measurement is mapped to DPOJET->DDR standard measurement *DDR Hold-Diff*.

This measurement is identical to the basic *Hold* measurement except that instead of using the Mid reference voltage for determining edge times, it uses the High and Low reference voltages for the address/command signal. The mid reference level is still used for the clock signal.

The application calculates this measurement using the following equation:

$T_n^{Hold} = T_n^{2nd} - T_i^{Main}$

Where,

T_n^{Hold} is the hold time.

T_i^{Main} is the clock crossing time of 50% voltage level in the specified direction.

T_n^{2nd} is the address/command crossing time of $V_{IH(dc)}$min (for falling data edges) or $V_{IL(dc)}$max (for rising data edges) voltage level.

tIS(base)

tIS(base) is defined as the input setup time between address/command and differential clock signal. This measures the elapsed time between the designated edge of the address/command waveform and the rising edge of the differential clock waveform. The closest address/command edge to the clock edge that falls within the range limits is used for the measurement.

This measurement is mapped to DPOJET->DDR standard measurement *DDR Setup-Diff*.

This measurement is identical to the basic *Setup* measurement except that instead of using the Mid reference voltage for determining edge times, it uses the High and Low reference voltages for the address/command signal. The mid reference level is still used for the clock signal.

The application calculates this measurement using the following equation:

$T_n^{Setup} = T_i^{Main} - T_n^{2nd}$

Where,

T_n^{Setup} is the setup time.

T_i^{Main} is the clock crossing time of 50% voltage level in the specified direction.

T_n^{2nd} is the address/command crossing time of $V_{IL(ac)}$max (for falling data edges) or $V_{IH(ac)}$min (for rising data edges) voltage level.

tIH(base)CA

tIH(base)CA measurement is same as *tIH(base)*, except that it is measured on the command signal.

tIH(base)CS

tIH(base)CS measurement is same as *tIH(base)*, except that it is measured on the chip select signal.

tIS(base)CA

tIS(base)CA measurement is same as *tIS(base)*, except that it is measured on the command signal.

tIS(base)CS

tIS(base)CS measurement is same as *tIS(base)*, except that it is measured on the chip select signal.

tIS(Vref) / tIS(Vref-based)

tIS(Vref) / tIS(Vref-based) is similar to the *tIS(base)* measurement, except it uses the mid reference level of the clock and VRef_CA level of the address/command signal to measure the setup time.

This measurement is mapped to DPOJET->DDR measurement *DDR Setup-Diff(Vref)*.

The application calculates this measurement using the following equation:

$T_n^{Setup} = T_i^{Main} - T_n^{2nd}$

Where,

T_n^{Setup} is the setup time.

T_i^{Main} is the clock crossing time of 50% voltage level in the specified direction.

T_n^{2nd} is the address/command crossing time of VRef_CA voltage level.

tIH(Vref) / tIH(Vref-based)

tIH(Vref) / tIH(Vref-based) is similar to the *tIH(base)* measurement, except it uses the mid reference level of the clock and VRef_CA level of the address/command signal to measure the hold time.

This measurement is mapped to DPOJET->DDR measurement *DDR Hold-Diff(Vref)*.

The application calculates this measurement using the following equation:

$T_n^{Hold} = T_n^{2nd} - T_i^{Main}$

Where,

T_n^{Hold} is the hold time.

T_i^{Main} is the clock crossing time of 50% voltage level in the specified direction.

T_n^{2nd} is the address/command crossing time of VRef_CA voltage level.

tDH-Diff(Vref-based)

tDH-Diff(Vref-based) is similar to the *tDH-Diff(base)* measurement, except it uses the mid reference level of the strobe and $V_{Ref(dc)}$ level of the data to measure the hold time.

This measurement is mapped to DPOJET base measurement *Hold*.

The application calculates this measurement using the following equation:

$T_n^{Hold} = T_n^{2nd} - T_i^{Main}$

Where,

T_n^{Hold} is the hold time.

T_i^{Main} is the strobe (DQS) crossing time of 50% voltage level in the specified direction.

T_n^{2nd} is the data (DQ) crossing time of $V_{Ref(dc)}$ voltage level.

tDS-Diff(derated)

tDS-Diff(derated) measurement is same as *tDS-Diff(base)*, except that the limits are dynamically calculated based on the slew rate of the signal.

Derating limit is calculated by adding the base limit to the Δt(derating) value, where Δt(derating) is defined based on the measured slew rate of the data and strobe signal. The mean value of the measured slew rate is used for calculating the Δt(derating) value.

$\text{Limit}_{tDS\text{-}Diff(derated)} = \text{Limit}_{tDS\text{-}Diff(base)} + \Delta t(\text{derating})$

tDS-Diff(Vref-based)

tDS-Diff(Vref-based) is similar to the *tDS-Diff(base)* measurement, except it uses the mid reference level of the strobe and $V_{Ref(dc)}$ level of the data to measure the setup time.

This measurement is mapped to DPOJET base measurement *Setup*.

The application calculates this measurement using the following equation:

$T_n^{Setup} = T_i^{Main} - T_n^{2nd}$

Where,

T_n^{Setup} is the setup time.

T_i^{Main} is the strobe (DQS) crossing time of 50% voltage level in the specified direction.

T_n^{2nd} is the data (DQ) crossing time of VRef(dc) voltage level.

tDS(DQS)(Informative)

tDS(DQS)(Informative) measurement is same as *tDS(base)DQS(Informative),* except that it measured at the mid reference level of both data and strobe signal.

This measurement is mapped to DPOJET base measurement *Setup*.

tDH(DQS)(Informative)

tDH(DQS)(Informative) measurement is same as *tDH(base)DQS(Informative),* except that it measured at the mid reference level of both data and strobe signal.

This measurement is mapped to DPOJET base measurement *Hold*.

tDH-Diff(max-derated)(Informative)

tDH-Diff(max-derated)(Informative) measurement is same as *tDH-Diff(derated)*, except that the maximum value of the measured slew rate is used for calculating the Δt(derating) value.

tDS-Diff(max-derated)(Informative)

tDS-Diff(max-derated)(Informative) measurement is same as *tDS-Diff(derated)*, except that the maximum value of the measured slew rate is used for calculating the Δt(derating) value.

tDH-Diff(min-derated)(Informative)

tDH-Diff(min-derated)(Informative) measurement is same as *tDH-Diff(derated)*, except that the minimum value of the measured slew rate is used for calculating the Δt(derating) value.

tDS-Diff(min-derated)(Informative)

tDS-Diff(min-derated)(Informative) measurement is same as *tDS-Diff(derated)*, except that the minimum value of the measured slew rate is used for calculating the Δt(derating) value.

tIS(derated)CA

tIS(derated)CA measurement is same as *tIS(derated)*, except that it is measured on the command signal.

tIH(derated)

tIH(derated) measurement is same as *tIH(base)*, except that the limits are dynamically calculated based on the slew rate of the signal.

Derating limit is calculated by adding the base limit to the Δt(derating) value, where Δt(derating) is defined based on the measured slew rate of the address/command and clock signal. The mean value of the measured slew rate is used for calculating the Δt(derating) value.

Limit $_{tIH(derated)}$ = Limit $_{tIH(base)}$ + Δt(derating)

tIS(derated)

tIS(derated) measurement is same as *tIS(base)*, except that the limits are dynamically calculated based on the slew rate of the signal.

Derating limit is calculated by adding the base limit to the Δt(derating) value, where Δt(derating) is defined based on the measured slew rate of the address/command and clock signal. The mean value of the measured slew rate is used for calculating the Δt(derating) value.

Limit $_{tIS(derated)}$ = Limit $_{tIS(base)}$ + Δt(derating)

tIH(derated)CA

tIH(derated)CA measurement is same as *tIH(derated)*, except that it is measured on the command signal.

tIS(derated)CS

tIS(derated)CS measurement is same as *tIS(derated)*, except that it is measured on the chip select signal.

tIH(derated)CS

tIH(derated)CS measurement is same as *tIH(derated)*, except that it is measured on the chip select signal.

tIH(max-derated)(Informative)

tIH(max-derated)(Informative) measurement is same as *tIH(derated)*, except that the maximum value of the measured slew rate is used for calculating the Δt(derating) value.

tIS(max-derated)(Informative)

tIS(max-derated)(Informative) measurement is same as *tIS(derated)*, except that the maximum value of the measured slew rate is used for calculating the Δt(derating) value.

tIS(min-derated)(Informative)

tIS(min-derated)(Informative) measurement is same as *tIS(derated)*, except that the minimum value of the measured slew rate is used for calculating the Δt(derating) value.

tDS(derated)DQS(Informative)

tDS(derated)DQS(Informative) measurement is same as *tDS(base)DQS(Informative)*, except that the limits are dynamically calculated based on the slew rate of the single ended signal.

tIH(min-derated)(Informative)

tIH(min-derated)(Informative) measurement is same as *tIH(derated)*, except that the minimum value of the measured slew rate is used for calculating the Δt(derating) value.

tCMDS

tCMDS is defined as the input setup time between command and differential clock signal. This measurement uses Vref level for the command signal and mid reference level for differential clock signal.

This measurement is mapped to DPOJET base measurement Setup.

tCMDH

tCMDH measurement is same as *tCMDS*, except that it is measures the input hold time between command and differential clock signal.

tAS

tAS measurement is same as *tCMDS,* except that it is measured on the address signal.

tAH

tAH measurement is same as *tCMDH*, except that it is measured on the address signal.

tCL(avg)

tCL(avg) is defined as the average low pulse width calculated across a sliding 200 cycle window of consecutive low pulses.

This measurement is mapped to DPOJET->DDR standard measurement *DDR tCL(avg*).

The application calculates this measurement using the following equation:

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / \left(N \times tCK(avg) \right)$$

Where,

N=200, which is configurable.

Range: 200≤N≤1M

tCK(avg)

tCK(avg) is calculated as the average clock period across a sliding 200-cycle window.

This measurement is mapped to DPOJET->DDR standard measurement *DDR tCK(avg)*.

The application calculates this measurement using the following equation:

$$tCK(avg) = \left(\sum_{j=1}^{200} tCK_j \right) / N$$

Where,

N=200, which is configurable.

Range: 200≤N≤1M

tCH(avg)

tCH(avg) is defined as the average high pulse width calculated across a sliding 200 cycle window of consecutive high pulses.

This measurement is mapped to DPOJET->DDR standard measurement *DDR tCK(avg).*

The application calculates this measurement using the following equation:

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / \left(N \times tCK(avg) \right)$$

Where,

N=200, which is configurable.

Range: 200 ≤ N ≤ 1M

tJIT(duty)

tJIT(duty) is the largest elapsed time between the tCH from tCH(avg) or tCL from tCL(avg) for a 200-cycle window. This value represents the maximum of the accumulated value across a 200-cycle moving window.

This measurement is mapped to DPOJET->DDR standard measurement *DDR tJIT(duty)*.

The application calculates this measurement using the following equation:

$$tJIT(duty) = Min/max\ of\ \{tJIT(CH), tJIT(CL)\}$$

Where,

tJIT(CH) = $\{tCH_i$ - tCH(avg)$\}$

tJIT(CL) = $\{tCL_i$- tCL(avg)$\}$

i =1 to N which is configurable between 200 ≤ N ≤ 1M

tJIT(per)

tJIT(per) is the largest elapsed time between the tCK from tCK(avg) for a 200-cycle sliding window. In case of GDDR5 generation, *tJIT(per)* is measured on WCK instead of clock signal.

This measurement is mapped to DPOJET->DDR standard measurement *DDR tJIT(per)*.

The application calculates this measurement using the following equation:

$$tJIT(per) = Min/max\ of\ \{tCK_i - tCK(avg)\}$$

Where,

i=1 to N which is configurable between 200 ≤ N ≤ 1M

tCK(abs) / tCK

tCK(abs)/tCK is the absolute clock period. It is the elapsed time between consecutive rising crossings of the mid reference CK voltage level.

This measurement is mapped to DPOJET base measurement *Period*.

tCL(abs) / tCL

tCL(abs)/tCL is the low pulse width of the differential clock signal. It is the amount of time the waveform remains below the mid reference voltage level.

This measurement is mapped to DPOJET base measurement *Neg Width*.

tWCKL

tWCKL measurement is same as *tCL*, except that it is measured on the differential WCK signal.

tWCKH

tWCKH measurement is same as *tCH*, except that it is measured on the differential WCK signal.

tERR (n per)

tERR(n per) is defined as the cumulative error across multiple consecutive cycles from tCK(avg). In other words *tERR(n per)* is the time difference between the sum of clock period for a 200-cycle window to n times *tCK(avg)*. The number of cycles to be used is defined by n, is configurable from 2 to 50.

This measurement is mapped to DPOJET->DDR standard measurement *DDR tERR(n)*.

The application calculates this measurement using the following equation:

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

Where,

n = 2 for tERR(2 per)

n = 3 for tERR(3 per)

n = 4 for tERR(4 per)

n = 5 for tERR(5 per) and so on.

tERR (m-n per)

tERR(m-n per) is defined as the cumulative error across multiple consecutive predefined cycles from *tCK(avg)*. This is measured similar to *tERR(n per).*

This measurement is mapped to DPOJET->DDR standard measurement *DDR tERR(m-n)*.

Where,

$6 \leq n \leq 10$ for tERR(6-10 per)

$11 \leq n \leq 50$ for tERR(11-50 per)

$13 \leq n \leq 50$ for tERR(13-50 per)

tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles. In case of GDDR5 generation, *tJIT(cc)* is measured on WCK instead of clock signal.

This measurement is mapped to DPOJET base measurement *CC-Period*.

The application calculates this measurement using the following equation:

$$tJIT(cc) = Max\ of\ |tCK_{i+1} - tCK_i|$$

tHP

tHP is the minimum of the absolute half period of clock signal.

This measurement is mapped to DPOJET base measurement *Period*.

The application calculates this measurement using the following equation:

$$tHP = Min(tCH(abs), tCL(abs))$$

Where,

tCH(abs) is the minimum of the actual instantaneous clock high time.

tCL(abs) is the minimum of the actual instantaneous clock low time.

tDH-Diff(derated)

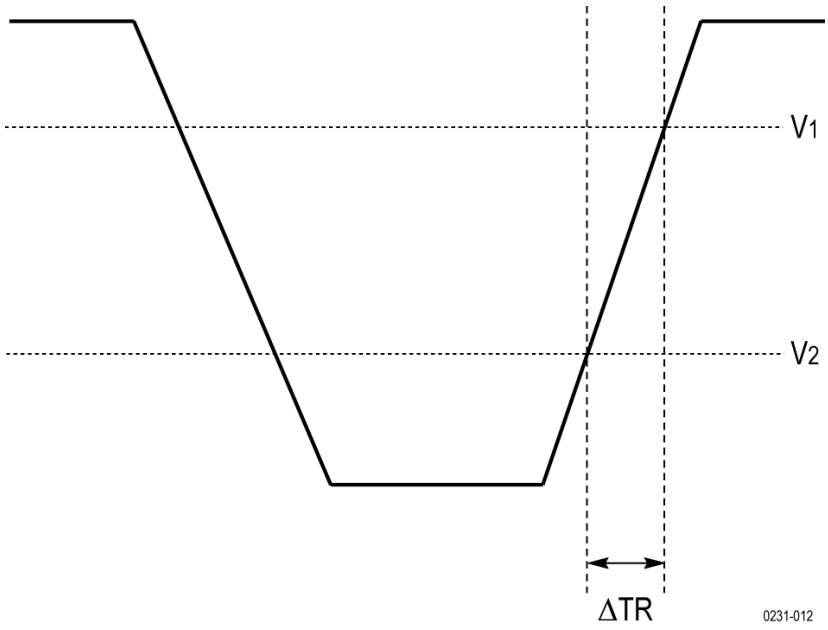
tDH-Diff(derated) measurement is same as *tDH-Diff(base)*, except that the limits are dynamically calculated based on the slew rate of the signal.

Derating limit is calculated by adding the base limit to the Δt(derating) value, where Δt(derating) is defined based on the measured slew rate of the data and strobe signal. The mean value of the measured slew rate is used for calculating the Δt(derating) value.

Limit $_{tDH\text{-}Diff(derated)}$ = Limit $_{tDH\text{-}Diff(base)}$ + Δt(derating)

Rise Slew Rate Measurements

Rise slew rate is defined as the rate of change of voltage on the rising edge of the signal. This is measured between two designated voltage levels on each of the rising edges. It is assumed that the signal has the monotonic slope between these designated voltage levels.



Rise Slew Rate = $(V_1 - V_2) / \Delta TR$

All 'Rise Slew Rate' measurements are mapped to DPOJET base measurement *Rise Slew Rate*.

srr1

srr1 is measured on input data signal from 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint).

srr2

srr2 is measured on input data signal from the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) above Vcent_DQ(midpoint).

SRCA_Rise

SRCA_Rise is measured on the address/command signal from $V_{IHCA(AC)Min}$ to $V_{ILCA(DC)Max}$ voltage level.

SRIN_cIVW_Rise

SRIN_cIVW_Rise is measured on the address/command signal from 0.5*VcIVW_Total below Vcent_CA to the last transition through 0.5*VcIVW_Total above Vcent_CA.

SRIN_dIVW_Rise

SRIN_dIVW_Rise is measured on the input data signal from 0.5*VdIVW_Total below Vcent_DQ to the last transition through 0.5*VdIVW_Total above Vcent_DQ.

SRQse-Rise(DQ)

SRQse-Rise(DQ) is measured on the output data signal from V_{OL}(AC)to V_{OH}(AC) voltage level.

SRQdiff-Rise(DQS)

SRQdiff-Rise(DQS) is measured on the output differential strobe signal from $V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$ voltage level.

InputSlew-Diff-Rise(CK)

InputSlew-Diff-Rise(CK) is measured on the differential clock signal from $V_{ILdiffmax}$ to $V_{IHdiffmin}$ voltage level.

Slew Rate-Setup-Rise(DQ)

Slew Rate-Setup-Rise(DQ) is measured on the input data signal from $V_{REF(dc)}$ to $V_{IH(ac)}$min voltage level.

Slew Rate-Hold-Rise(DQ)

Slew Rate-Hold-Rise(DQ) is measured on the input data signal from $V_{IL(dc)}$max to $V_{REF(dc)}$ voltage level.

Slew Rate-Hold-Rise(Addr/Cmd)

Slew Rate-Hold-Rise(Addr/Cmd) is measured on the address/command signal from $V_{IL(dc)}$max to $V_{REF(dc)}$ voltage level.

Slew Rate-Setup-Rise(Addr/Cmd)

Slew Rate-Setup-Rise(Addr/Cmd) is measured on the address/command signal from $V_{REF(dc)}$ to $V_{IH(ac)}$min voltage level.

InputSlew-Diff-Rise(DQS)

InputSlew-Diff-Rise(DQS) is measured on the differential strobe signal from $V_{ILdiffmax}$ to $V_{IHdiffmin}$ voltage level.

Slew Rate-Setup-SE-Rise(DQS)

Slew Rate-Setup-SE-Rise(DQS) is measured on the single ended input strobe signal from $V_{REF(dc)}$ to $V_{IH(ac)}$min voltage level.

Slew Rate-Hold-SE-Rise(DQS)

Slew Rate-Hold-SE-Rise(DQS) is measured on the single ended input strobe signal from $V_{IL(dc)}$max to $V_{REF(dc)}$ voltage level.

CKSlew-Rise(CK) / CKSlew-Rise(CK#)

CKSlew-Rise(CK) / CKSlew-Rise(CK#) is measured on single ended clock (either on true or complement) signal from VREFC crossing to VIXCK(AC) voltage level.

WCKSlew-Rise(WCK) / WCKSlew-Rise(WCK#)

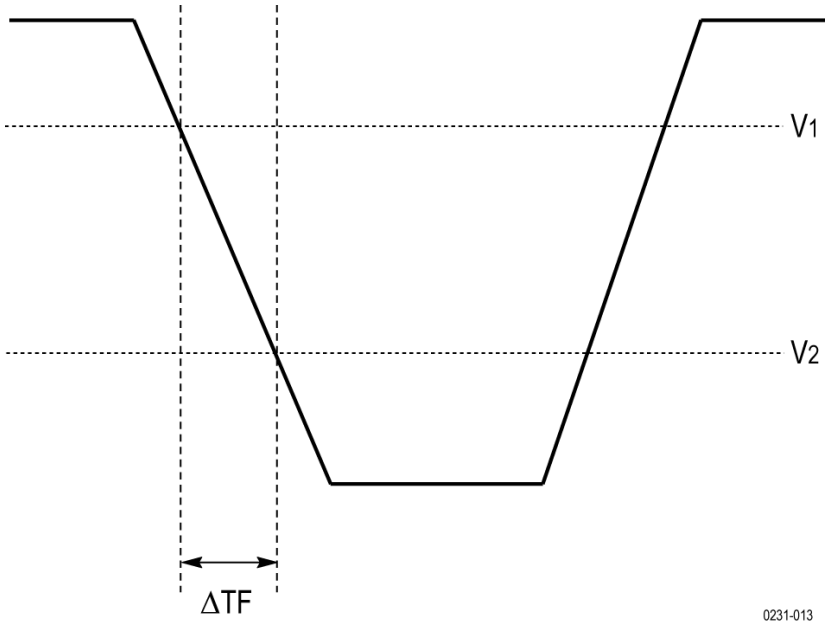
WCKSlew-Rise(WCK) / WCKSlew-Rise(WCK#) is measured on single ended WCK (either on true or complement) signal from VREFD crossing to VIXWCK(AC) voltage level.

tWCK-Rise-Slew

tWCK-Rise-Slew is measured on the differential WCK signal from 10% to 90% of voltage level.

Fall Slew Rate Measurements

Fall slew rate is defined as the rate of change of voltage on the falling edge of the signal. This is measured between two designated voltage levels on each of the falling edges. It is assumed that the signal has the monotonic slope between these designated voltage levels.



Fall Slew Rate = $(V_1 - V_2) / \Delta TF$

All 'Fall Slew Rate' measurements are mapped to DPOJET base measurement *Fall Slew Rate*.

srf1

srf1 is measured on the input data signal from 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint).

srf2

srf2 is measured on the input data signal from the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) below Vcent_DQ(pin mid).

SRCA_Fall

SRCA_Fall is measured on the address/command signal from $V_{ILCA(DC)Max}$ to $V_{IHCA(AC)Min}$ voltage level.

SRIN_cIVW_Fall

SRIN_cIVW_Fall is measured on the address/command signal from 0.5*VcIVW_Total above Vcent_CA to the last transition through 0.5*VcIVW_Total below Vcent_CA.

SRIN_dIVW_Fall

SRIN_dIVW_Fall is measured on the input data signal from 0.5*VdIVW_Total above Vcent_DQ to the last transition through 0.5*VdIVW_Total below Vcent_DQ.

SRQse-Fall(DQ)

SRQse-Fall(DQ) is measured on the output data signal from V_{OH}(AC) $_{to}$ V_{OL}(AC)voltage level.

SRQdiff-Fall(DQS)

SRQdiff-Fall(DQS) is measured on the output differential strobe signal from $V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$ voltage level.

InputSlew-Diff-Fall(CK)

InputSlew-Diff-Fall(CK) is measured on the differential clock signal from $V_{IHdiffmin}$ to $V_{ILdiffmax}$ voltage level.

Slew Rate-Setup-Fall(DQ)

Slew Rate-Setup-Fall(DQ) is measured on the input data signal from $V_{REF(dc)}$ to $V_{IL(ac)}$max voltage level.

Slew Rate-Hold-Fall(DQ)

Slew Rate-Hold-Fall(DQ) is measured on the input data signal from $V_{IH(dc)}$min to $V_{REF(dc)}$ voltage level.

Slew Rate-Setup-Fall(Addr/Cmd)

Slew Rate-Setup-Fall(Addr/Cmd) is measured on the address/command signal from $V_{REF(dc)}$ to $V_{IL(ac)}$max voltage level.

Slew Rate-Hold-Fall(Addr/Cmd)

Slew Rate-Hold-Fall(Addr/Cmd) is measured on the address/command signal from $V_{IH(dc)}$min to $V_{REF(dc)}$ voltage level.

InputSlew-Diff-Fall(DQS)

InputSlew-Diff-Fall(DQS) is measured on the differential strobe signal from $V_{IHdiffmin}$ to $V_{ILdiffmax}$ voltage level.

Slew Rate-Setup-SE-Fall(DQS)

Slew Rate-Setup-SE-Fall(DQS) is measured on the single ended input strobe signal from $V_{REF(dc)}$ to $V_{IL(ac)}$max voltage level.

Slew Rate-Hold-SE-Fall(DQS)

Slew Rate-Hold-SE-Fall(DQS) is measured on the single ended input strobe signal from $V_{IH(dc)}$min to $V_{REF(dc)}$ voltage level.

CKSlew-Fall(CK) / CKSlew-Fall(CK#)

CKSlew-Fall(CK) / CKSlew-Fall(CK#) is measured on single ended clock (either on true or complement) signal from VIXCK(AC) crossing to VREFC voltage level.

WCKSlew-Fall(WCK) / WCKSlew-Fall(WCK#)

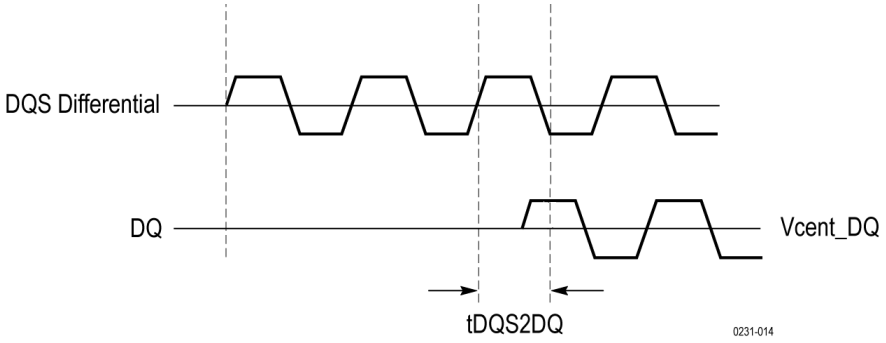
WCKSlew-Fall(WCK) / WCKSlew-Fall(WCK#) is measured on single ended WCK (either on true or complement) signal from VIXWCK(AC) crossing to VREFD voltage level.

tWCK-Fall-Slew

tWCK-Fall-Slew is measured on the differential WCK signal from 90% to 10% of voltage level.

tDQS2DQ

tDQS2DQ is defined as the time skew between the driving edge of the strobe to the center of the first data eye at Vcent_DQ level. You need to configure the right Vcent_DQ value in step-1 (Generation rate and Levels) before executing this measurement.



Note: At least in one burst, DQ should have a transition during the first bit; otherwise, the measured value may not be accurate.

This measurement is mapped to DPOJET->DDR measurement *DDR tDQS2DQ*.

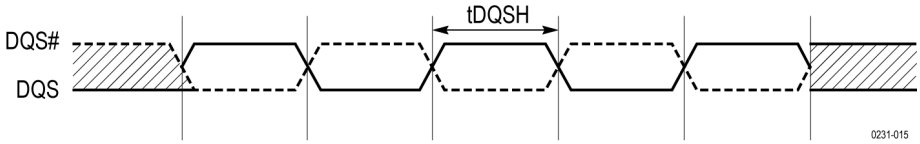
tDQS2DQ is from strobe crossing to the center of the actual receiver switch point range. If the measured DQ eyes have margin w.r.t. the Rx Mask spec, then it is not a 'fail'. Likewise, if the range of the receiver switch point is smaller than the Rx Mask, then it is not a 'fail'.

Hence no limit is applied for *tDQS2DQ* measurement. You need to analyze the measured value and come to the pass/fail conclusion.

tDQSH

tDQSH is defined as the high pulse width on the differential input strobe signal. This is the amount of time the waveform remains above the mid reference voltage level.

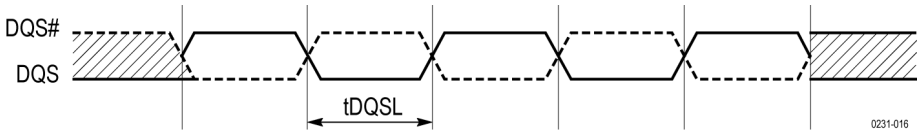
This measurement is mapped to DPOJET base measurement *Pos Width*.



tDQSL

tDQSL is defined as the low pulse width on the differential input strobe signal. This is the amount of time the waveform remains below the mid reference voltage level.

This measurement is mapped to DPOJET base measurement *Neg Width*.



TdIPW-Low / tDIPW-Low

TdIPW-Low / tDIPW-Low is defined as the low pulse width of the data signal. This is the amount of time the waveform remains below the Vcent_DQ or Vref voltage level between any two successive edges.

This measurement is mapped to DPOJET base measurement *Neg Width*.

TdIPW-High / tDIPW-High

TdIPW-High / tDIPW-High is defined as the high pulse width of the data signal. This is the amount of time the waveform remains above the Vcent_DQ or Vref voltage level between any two successive edges.

This measurement is mapped to DPOJET base measurement *Pos Width*.

TCIPW-High / tIPW-High

TCIPW-High / tIPW-High is defined as the high pulse width of the address/command signal. This is the amount of time the waveform remains above the Vcent_CA / Vref_CA / Vref voltage level between any two successive edges.

This measurement is mapped to DPOJET base measurement *Pos Width*.

TCIPW-Low / tIPW-Low

TCIPW-Low / tIPW-Low is defined as the low pulse width of the address/command signal. This is the amount of time the waveform remains below the Vcent_CA / Vref_CA / Vref voltage level between any two successive edges.

This measurement is mapped to DPOJET base measurement *Neg Width*.

tIPW-High(CA)

tIPW-High(CA) measurement is same as *tIPW-High*, except that it is measured on the command signal.

tIPW-High(CS)

tIPW-High(CS) measurement is same as *tIPW-High*, except that it is measured on the chip select signal.

tIPW-Low(CA)

tIPW-Low(CA) measurement is same as *tIPW-Low*, except that it is measured on the command signal.

tIPW-Low(CS)

tIPW-Low(CS) measurement is same as *tIPW-Low*, except that it is measured on the chip select signal.

tAPW

tAPW is defined as the pulse width of the address signal. This is the amount of time the waveform remains above or below the Vref voltage level between any two successive edges.

This measurement is mapped to DPOJET base measurement *Period*.

tWCK

tWCK measurement is same as *tAPW,* except that it is measured on the differential WCK signal and at mid reference level.

tCMDPW

tCMDPW measurement is same as *tAPW,* except that it is measured on the command signal.

tWCKHP

tWCKHP is defined as the minimum half period of the WCK signal. This is the amount of time the waveform remains above the Vref voltage level between any two successive rising edges.

This measurement is mapped to DPOJET base measurement *Period*.

Data Eye Width

Data Eye Width is defined as the minimum horizontal eye opening of the data signal at the mid reference level.

This measurement is mapped to DPOJET base measurement *Width* with 'Eye Diagram' plot enabled.

This is measured using the following equation:

$T_{Eye\_Width} = UI_{Avg} - TIE_{Pk\text{-}Pk}$

Where,

UI_{Avg} is the average UI

$TIE_{Pk\text{-}Pk}$ is the peak to peak time interval error.

Clock Eye Width (Informative)

Clock Eye Width (Informative) measurement is same as *Data Eye Width*, except that it is measured on the differential clock signal.

AddrCmd Eye Width (Informative)

AddrCmd Eye Width (Informative) measurement is same as *Data Eye Width,* except that it is measured on the address/command signal.

Data Eye Height

Data Eye Height is defined as the minimum vertical eye opening of the data signal at the UI center.

This measurement is mapped to DPOJET base measurement *Height.*

Clock Eye Height (Informative)

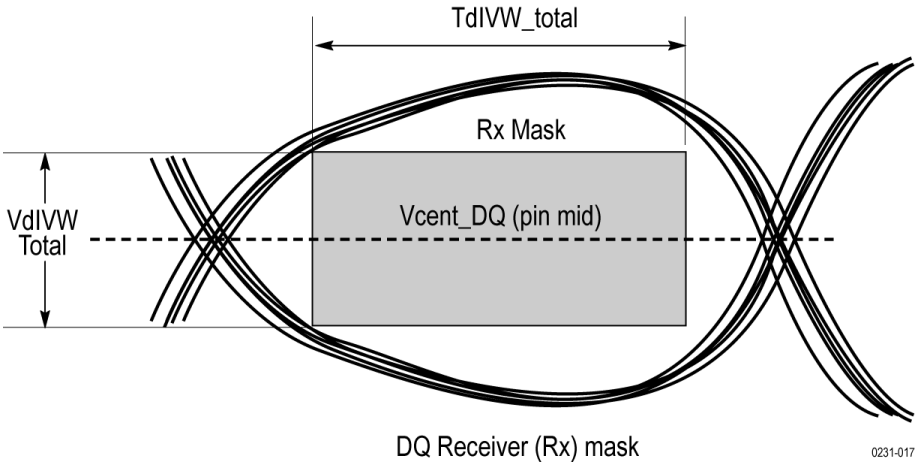
Clock Eye Height (Informative) measurement is same as *Data Eye Height,* except that it is measured on the differential clock signal.

DDRARXMask

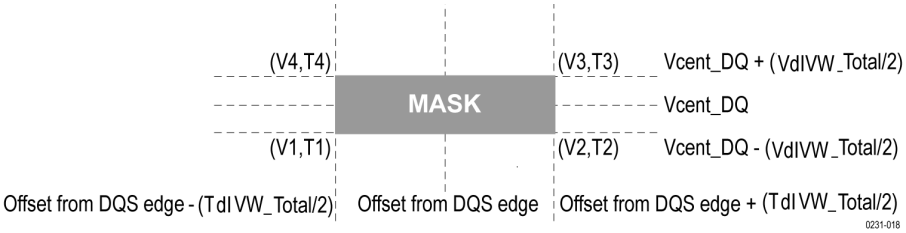
DDRARXMask defines the area that must not encroach by the input signal in order for the DRAM input receiver to successfully capture the valid input signal. This measurement reports the number of unit intervals in the acquisition for which mask hits occurred, for the specified mask.

This measurement is mapped to DPOJET base measurement *Mask Hits*.

The input data receiver compliance mask for voltage and timing is shown as below:

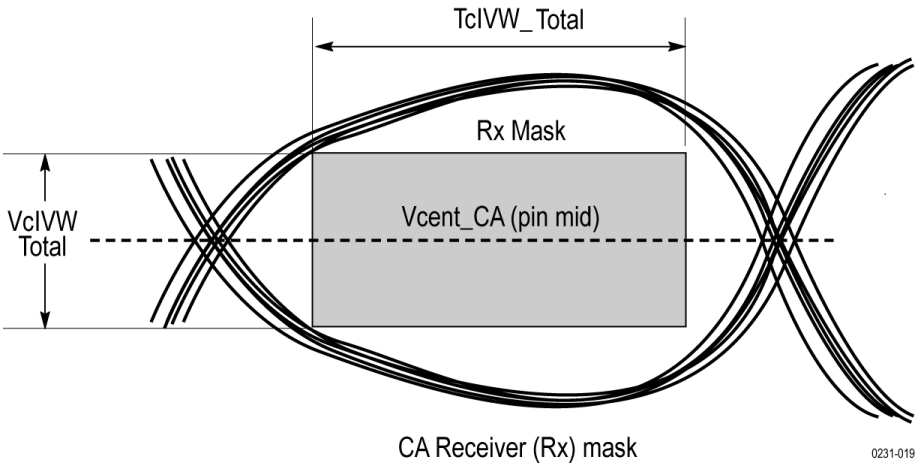


The application will dynamically create the mask depending on the configured data rate and Vcent_DQ:

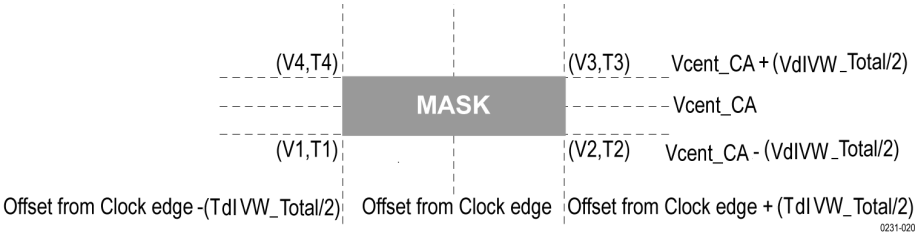


The position of the data Rx mask in the horizontal direction is controlled by tDQS2DQ and in the vertical direction, it is controlled by Vcent_DQ value.

The address/command receiver compliance mask for voltage and timing is shown as below:



The application will dynamically create the mask depending on the configured data rate and Vcent_CA:



The position of the address/command Rx mask in the vertical direction can be controlled by adjusting the Vcent_DQ value.

The mask file format is as below:

```
:MASK:USER:LAB "DDR4, 1600 MT/s";
:MASK:USER:SEG1:POINTS 0.0000E-12,0.0,0.0000E-12,0.0,0.0000E-12,0.0,0.0000E-12,0.0;
:MASK:USER:SEG2:POINTS -6.25E-11, 0.782, 6.25E-11, 0.782, 6.25E-11, 0.918, -6.25E-11, 0.918;
:MASK:USER:SEG3:POINTS 0.0000E-12,0.0,0.0000E-12,0.0,0.0000E-12,0.0,0.0000E-12,0.0;
```

You can edit the highlighted section of the mask file with the new mask coordinates. The coordinates should be entered in the order V4, T4, V3, T3, V2, T2, V1 and T1.

AutoFitRxMask (Informative)

AutoFitRxMask (Informative) is similar to that of *DDRARXMask* measurement, except that it is mapped to DPOJET base measurement *Autofit Mask Hits*. This measurement tries to adjust the mask automatically in the horizontal direction, so that mask hits are minimized.

Overshoot Measurement

Overshoot is defined as the maximum peak amplitude above the Vdd / VDDQ reference level on the specified signal.

All *Overshoot* Measurements are mapped to DPOJET base measurement *Overshoot*.

If the input waveform never exceeds the Vdd level, then the measurement will return a population of 0 events.

AC-Overshoot(DQS)

AC-Overshoot(DQS) is measured on the single ended strobe signal.

AC-Overshoot(DQS#)

AC-Overshoot(DQS#) is measured on the single ended complementary strobe signal.

AC-Overshoot(CK)

AC-Overshoot(CK) is measured on the single ended clock signal.

AC-Overshoot(CK#)

AC-Overshoot(CK#) is measured on the single ended complementary clock signal.

AC-Overshoot(DQ)

AC-Overshoot(DQ) is measured on the data signal.

AC-Overshoot

AC-Overshoot is measured on the address/command signal.

Undershoot Measurements

Undershoot is defined as the maximum peak amplitude below the Vss reference level on the specified signal.

All *Undershoot* Measurements are mapped to DPOJET base measurement *Undershoot.*

If the input waveform never goes below the Vss level, then the measurement will return a population of 0 events.

AC-Undershoot(DQS)

AC-Undershoot(DQS) is measured on the single ended strobe signal.

AC-Undershoot(DQS#)

AC-Undershoot(DQS#) is measured on the single ended complement strobe signal.

AC-Undershoot(CK)

AC-Undershoot(CK) is measured on the single ended clock signal.

AC-Undershoot(CK#)

AC-Undershoot(CK#) is measured on the single ended complement clock signal.

AC-Undershoot(DQ)

AC-Undershoot(DQ) is measured on the data signal.

AC-Undershoot

AC-Undershoot is measured on the address/command signal.

AbsMax Undershoot Measurements

AbsMax Undershoot is defined as the maximum peak amplitude below the (Vss - 0.3V) reference level on the specified signal.

All AbsMax *Undershoot* Measurements are mapped to DPOJET base measurement *Undershoot.*

If the input waveform never goes below the (Vss - 0.3V) level, then the measurement will return a population of 0 events.

AC-Undershoot(AbsMax)(DQS)

AC-Undershoot(AbsMax)(DQS) is measured on the single ended strobe signal.

AC-UndershootArea(AbsMax)(DQS#)

AC-UndershootArea(AbsMax)(DQS#) is measured on the single ended complement strobe signal. This measurement is mapped to DPOJET->DDR measurement *AUS.*

AC-Undershoot(AbsMax) (DQ)

AC-Undershoot(AbsMax) (DQ) is measured on the data signal.

AbsMax Overshoot Measurements

AbsMax Overshoot is defined as the maximum peak amplitude above (Vdd+0.24V) reference level on the specified signal.

All AbsMax *Overshoot* Measurements are mapped to DPOJET base measurement *Overshoot.*

If the input waveform never exceeds the (Vdd+0.24V) level, then the measurement will return a population of 0 events.

AC-Overshoot(AbsMax)(DQS)

AC-Overshoot(AbsMax)(DQS) is measured on the single ended strobe signal.

AC-Overshoot(AbsMax)(DQS#)

AC-Overshoot(AbsMax)(DQS#) is measured on the single ended complement strobe signal.

AC-Overshoot(AbsMax)(CK)

AC-Overshoot(AbsMax)(CK) is measured on the single ended clock signal.

AC-Overshoot(AbsMax)(CK#)

AC-Overshoot(AbsMax)(CK#) is measured on the single ended complement clock signal.

AC-Overshoot(AbsMax)(DQ)

AC-Overshoot(AbsMax)(DQ) is measured on the data signal.

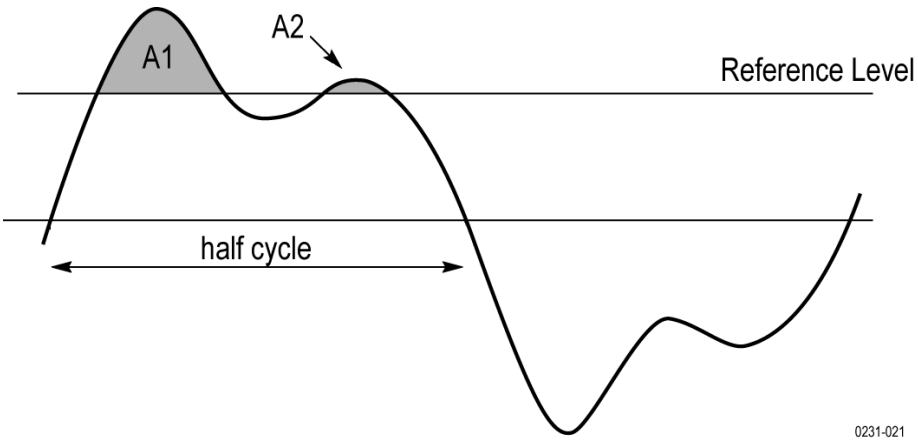
AC-Overshoot(AbsMax)

AC-Overshoot(AbsMax) is measured on the address/command signal.

Overshoot Area Measurements

Overshoot Area is defined as the total area of the signal which crosses specified reference level.

If the input waveform never exceeds the reference level, then the measurement will return a population of 0 events.



The *Overshoot Area* is measured using the continuous integration method, such that only the portion of the area which crosses reference level is considered in the area calculation. In the above diagram (A1 + A2) is the total overshoot area over half cycle.

In general,

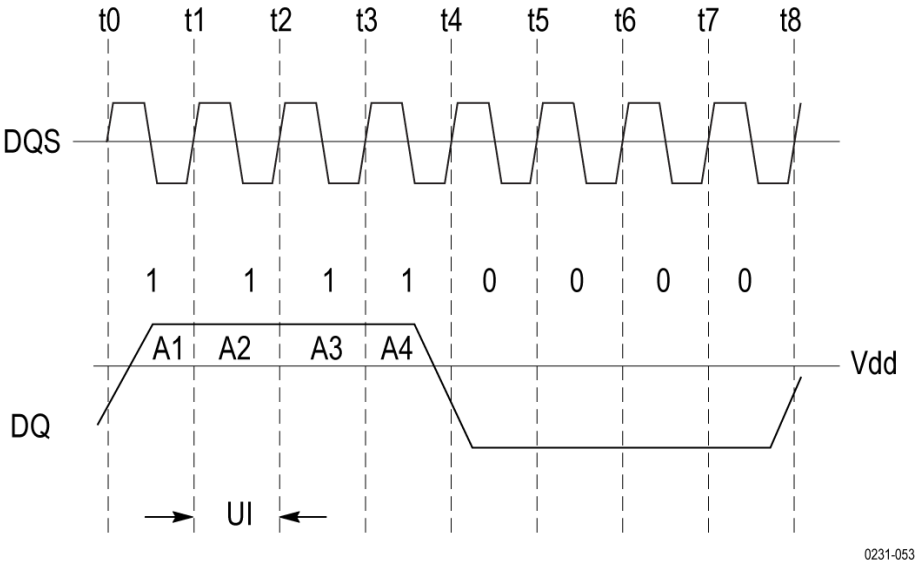
$$\text{Area} = \int_{t=0}^{UI} |f(t) - g(t)|\, dt \qquad \text{if f(t)} \geq \text{g(t)}$$

Where,

f(t) is function of the given signal

g(t) is function of the one or two reference voltages.

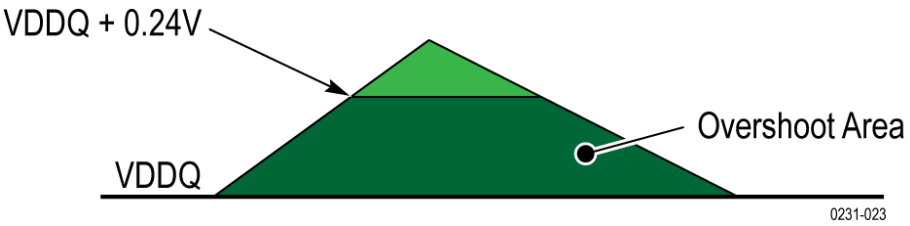
Overshoot Area is measured over one unit interval. This is illustrated in the below diagram, by taking data and strobe signal.



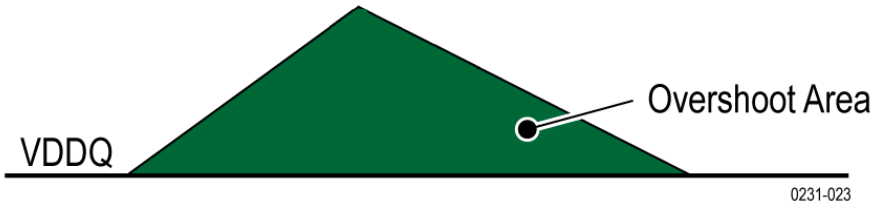
The address/command signal of LPDDR2 and LPDDR3 generations are of double data rate such that one $\text{UI} = \frac{2}{Data\ Rate}$.

Whereas, the address/command signal in all other generations are of single data rate such that one $\text{UI} = \frac{1}{Data\ Rate}$

In DDR4, *Overshoot Area* is measured between two reference voltages, VDDQ and (VDDQ+0.24V).



Whereas, in all other generations, *Overshoot Area* is measured above the Vdd or VDDQ reference level.



AC-Overshoot(DQS)

AC-Overshoot(DQS) is measured on the single ended strobe signal.

AC-OvershootArea(DQS#)

AC-OvershootArea(DQS#) is measured on the single ended complement strobe signal. In DDR4, this measurement is mapped to DPOJET->DDR measurement *AOS(AbsMax)*. Whereas, in all other generations, this is mapped to DPOJET->DDR measurement *AOS*.

AC-Overshoot(CK)

AC-Overshoot(CK) is measured on the single ended clock signal.

AC-OvershootArea(CK#)

AC-OvershootArea(CK#) is measured on the single ended complement clock signal. In DDR4, this measurement is mapped to DPOJET->DDR measurement *AOS(AbsMax)*. Whereas, in all other generations, this is mapped to DPOJET->DDR measurement *AOS*.

AC-OvershootArea(DQ)

AC-OvershootArea(DQ) is measured on the data signal. In DDR4, this measurement is mapped to DPOJET->DDR measurement *AOS(AbsMax) Per UI*. Whereas, in all other generations, this is mapped to DPOJET->DDR measurement *AOS Per UI*.

AC-OvershootArea

AC-OvershootArea is measured on the address/command signal. In DDR4, this measurement is mapped to DPOJET->DDR measurement *AOS(AbsMax) Per tCK*. In LPDDR2 and LPDDR3, this is mapped to DPOJET->DDR measurement *AOS Per UI* and in all other generations, this is mapped to DPOJET->DDR measurement*AOS Per tCK*.

AbsMax Overshoot Area Measurements

This is same as that of *Overshoot Area* measurements, except that it measures the area of the signal which crosses (VDDQ +0.24V) reference level.

AC-OvershootArea(AbsMax)(DQS)

AC-OvershootArea(AbsMax)(DQS) is measured on the single ended strobe signal. This measurement is mapped to DPOJET->DDR measurement *AOS.*

AC-OvershootArea(AbsMax)(DQS#)

AC-OvershootArea(AbsMax)(DQS#) is measured on the single ended complement strobe signal. This measurement is mapped to DPOJET->DDR measurement *AOS.*

AC-OvershootArea(AbsMax)(CK)

AC-OvershootArea(AbsMax)(CK) is measured on the single ended clock signal. This measurement is mapped to DPOJET->DDR measurement *AOS*.

AC-OvershootArea(AbsMax)(CK#)

AC-OvershootArea(AbsMax)(CK#) is measured on the single ended complement clock signal. This measurement is mapped to DPOJET->DDR measurement AOS.

AC-OvershootArea(AbsMax)(DQ)

AC-OvershootArea(AbsMax)(DQ) is measured on the data signal. This measurement is mapped to DPOJET->DDR measurement *AOS Per UI*.

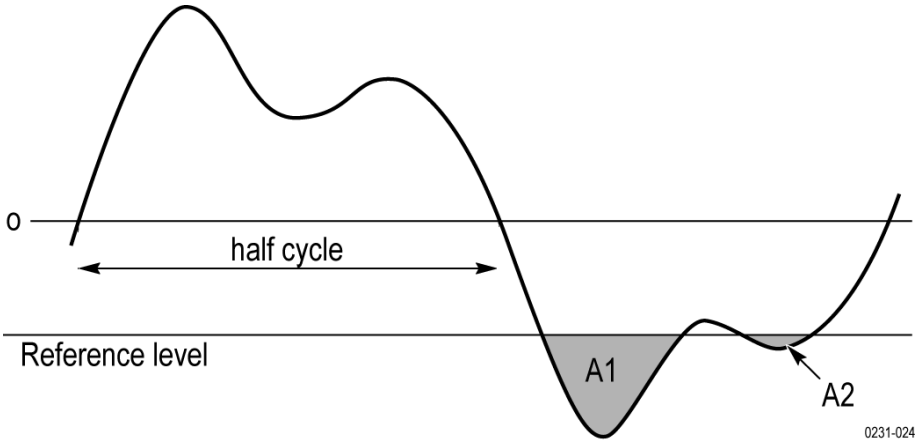
AC-OvershootArea(AbsMax)

AC-OvershootArea (AbsMax) is measured on the address/command signal. This measurement is mapped to DPOJET->DDR measurement *AOS Per tCK*.

Undershoot Area Measurements

Undershoot Area is defined as the total area of the signal which crosses specified reference level.

If the input waveform never exceeds the reference level, then the measurement will return a population of 0 events.



The *Undershoot Area* is measured using the continuous integration method, such that only the portion of the area which crosses reference level is considered in the area calculation. In the above diagram (A1 + A2) is the total undershoot area over half cycle.

In general,

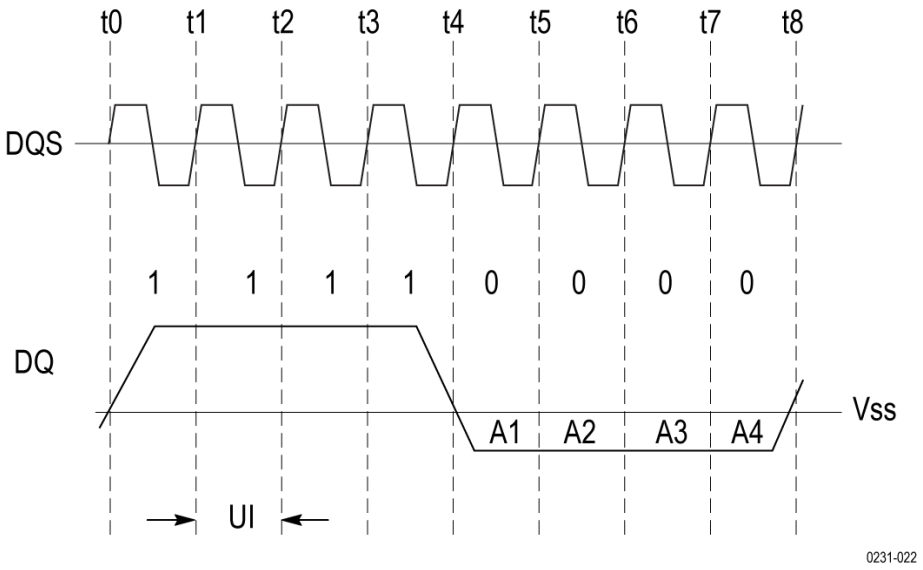
$\text{Area} = \int_{t=0}^{UI} |f(t) - g(t)|\, dt$ if f(t) ≤ g(t)

Where,

f(t) is function of the given signal

g(t) is function of the one or two reference voltage.

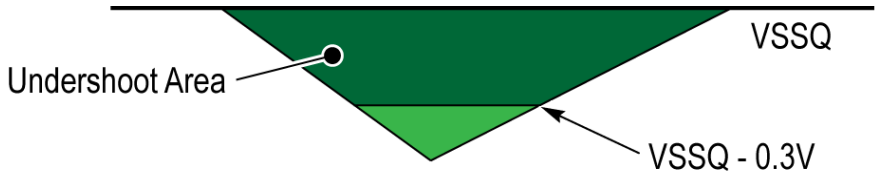
Undershoot Area is measured over one unit interval. This is illustrated in the below diagram, by taking data and strobe signal.



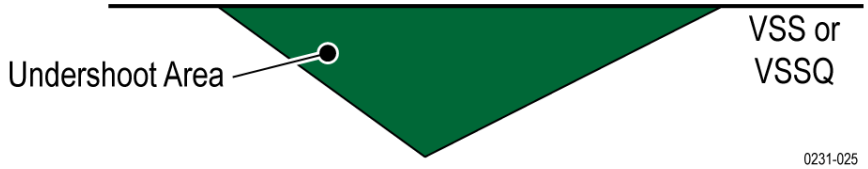
The address/command signal of LPDDR2 and LPDDR3 generations are of double data rate such that one $UI = \frac{2}{Data\ Rate}$.

Whereas, the address/command signal in all other generations are of single data rate such that one $UI = \frac{1}{Data\ Rate}$

In DDR4, *Undershoot Area* for strobe and data signal is measured between two reference voltages, VSSQ and (VSQ - 0.3V).



Whereas, in all other generations, *Undershoot Area* is measured below the VSS or VSSQ reference level.



AC-UndershootArea(DQS)

AC-UndershootArea(DQS) is measured on the single ended strobe signal. In DDR4, this measurement is mapped to DPOJET->DDR measurement *AUS(AbsMax)*. Whereas, in all other generations, this is mapped to DPOJET->DDR measurement *AUS*.

AC-UndershootArea(DQS#)

AC-UndershootArea(DQS#) is measured on the single ended complement strobe signal. In DDR4, this measurement is mapped to DPOJET->DDR measurement *AUS(AbsMax)*. Whereas, in all other generations, this is mapped to DPOJET->DDR measurement *AUS*.

AC-UndershootArea(CK)

AC-UndershootArea(CK) is measured on the single ended clock signal. This measurement is mapped to DPOJET->DDR measurement *AUS*.

AC-UndershootArea(CK#)

AC-UndershootArea(CK#) is measured on the single ended complement clock signal. This measurement is mapped to DPOJET->DDR measurement *AUS*.

AC-UndershootArea(DQ)

AC-UndershootArea(DQ) is measured on the data signal. In DDR4, this measurement is mapped to DPOJET->DDR measurement *AUS(AbsMax) Per UI*. Whereas, in all other generations, this is mapped to DPOJET->DDR measurement *AUS Per UI*.

AC-UndershootArea

AC-UndershootArea is measured on the address/command signal. In LPDDR2 and LPDDR3, this measurement is mapped to DPOJET->DDR measurement *AUS Per UI* and in all other generations, this is mapped to DPOJET->DDR measurement *AUS Per tCK*.

AbsMax Undershoot Area Measurements

This is same as that of *Undershoot Area* measurements, except that it measures the area of the signal which crosses (VSSQ - 0.3V) reference level.

AC-UndershootArea(AbsMax)(DQS#)

AC-UndershootArea(AbsMax)(DQS#) is measured on the single ended complement strobe signal. This measurement is mapped to DPOJET->DDR measurement *AUS.*

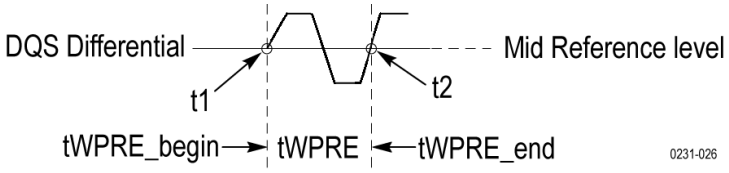
AC-UndershootArea(AbsMax)(DQ)

AC-UndershootArea(AbsMax)(DQ) is measured on the data signal. This measurement is mapped to DPOJET->DDR measurement *AUS Per UI*.

tWPRE

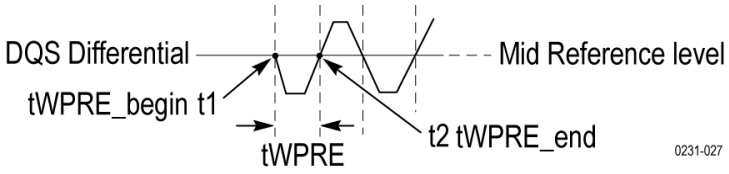
tWPRE is defined as the width of Write burst' preamble. It is measured from the exit of tristate to the first driving edge of the differential strobe.

The Write preamble in case of DDR3, DDR3L, DDR4 and LPDDR3 is as below:



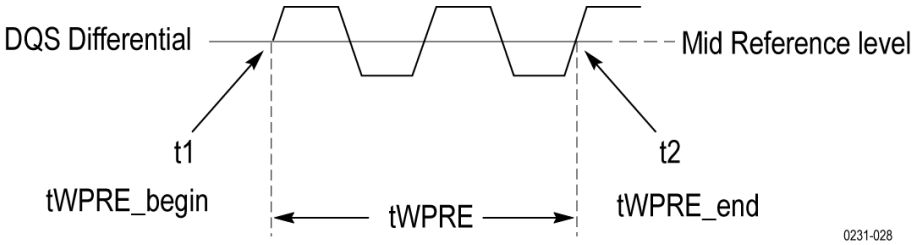
For these generations, this measurement is mapped to DPOJET->DDR measurement *DDR tWPRE*.

The Write preamble in case of DDR, DDR2, LPDDR and LPDDR2 is as below:



For these generations, this measurement is mapped to DPOJET->DDR measurement *DDR tRPRE*.

The Write preamble in case of LPDDR4 and LPDDR4X is as below:



For these generations, this measurement is mapped to DPOJET->DDR measurement *LPDDR4 tWPRE*.

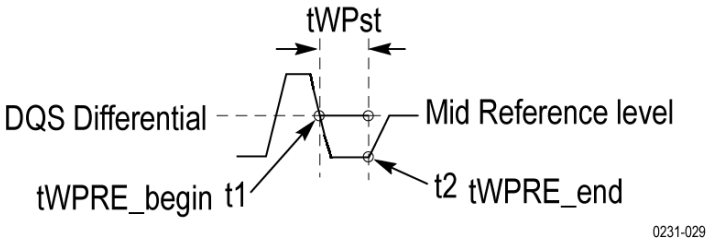
tWPST

tWPST is defined as the width of Write burst' postamble. It is measured from the last falling edge crossing mid reference level to the start of an undriven state (as judged by a rising trend per JEDEC specs).

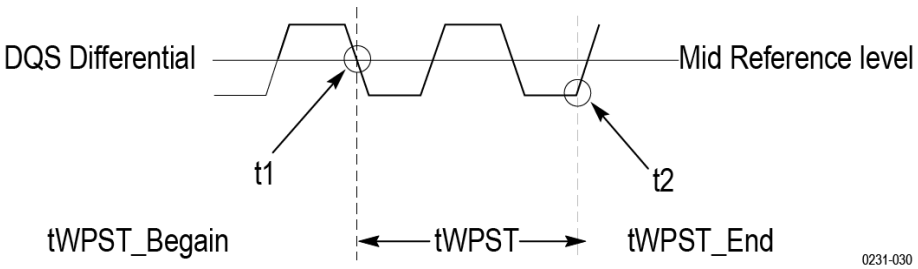
This measurement is mapped to DPOJET->DDR measurement *DDR tPST*.

The length of the Write postamble could be either 0.5 tCK or 1.5 tCK (also known as extended postamble).

The following schematic shows a Write postamble with 0.5tCK.



The following schematic shows a Write postamble with 1.5tCK.



tRPST

tRPST is defined as the width of Read burst' postamble. This measurement is same as *tWPST,* except that it measures on the Read bursts.

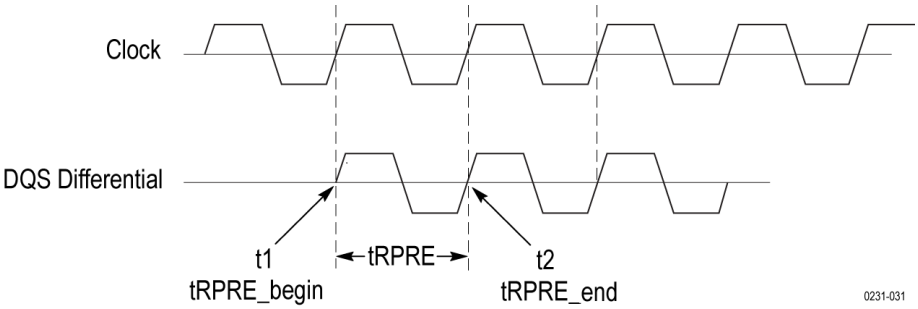
tRPRE

tRPRE is defined as the width of the Read burst' preamble. This is measured from the exit of tristate to the first driving edge of the differential strobe.

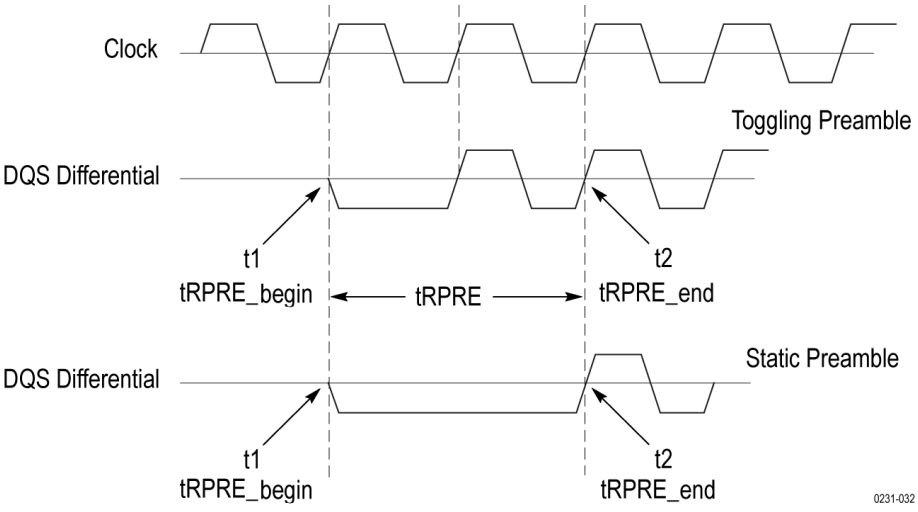
In DDR4, this measurement is mapped to DPOJET->DDR measurement *DDR tWPRE,* whereas for all other generations this is mapped to DPOJET->DDR measurement *DDR tPST*

The length of the Read preamble varies across different generations.

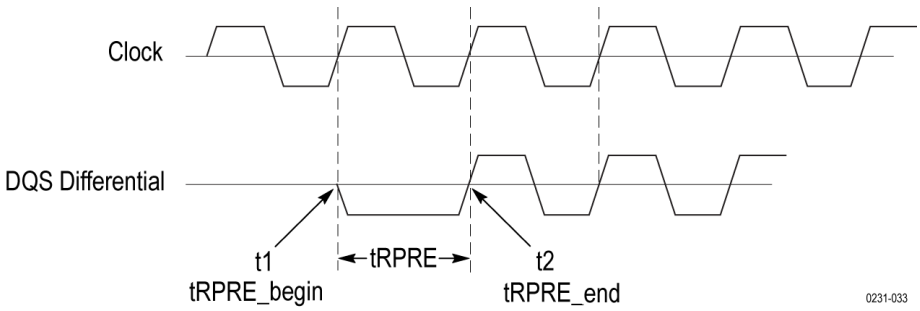
The following schematic shows a Read preamble for DDR4 generation:



The following schematic shows a Read preamble for LPDDR4 and LPDDR4X generations.



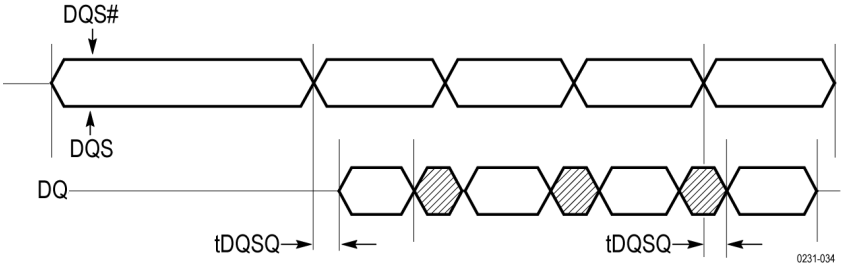
The following schematic shows a Read preamble for all the remaining DDR generations.



tDQSQ-Diff

tDQSQ-Diff describes the latest valid transition of the associated DQ pins. In other words, *tDQSQ-Diff* is the skew between differential strobe and the associated DQ signals. The closest data edge to the strobe edge that falls within the range limits is used for the measurement.

This measurement is mapped to the DPOJET base measurement *Setup*.



tDQSQ-DBI

tDQSQ-DBI measurement is same as *tDQSQ-Diff*, except that it measures the skew between strobe and data when Data Bus Inversion (DBI) is enabled

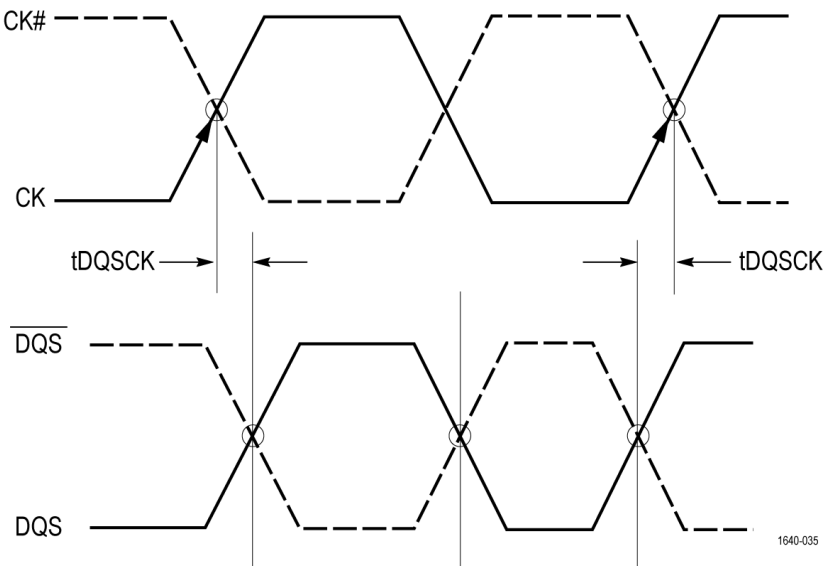
tDQSQ(DQS) / tDQSQ(DQS)(Informative)

tDQSQ(DQS) / tDQSQ(DQS)(Informative) measurement is same as *tDQSQ-Diff*, except that it measures the skew between the single ended strobe and data.

tDQSCK-Diff

tDQSCK-Diff is defined as the skew between the actual position of a rising output strobe edge relative to differential clock. For both the signals, the edge locations are determined by the mid-reference voltage levels. The closest strobe edge to the clock edge that falls within the range limits is used for the measurement. This is measurement is applicable for the Read bursts.

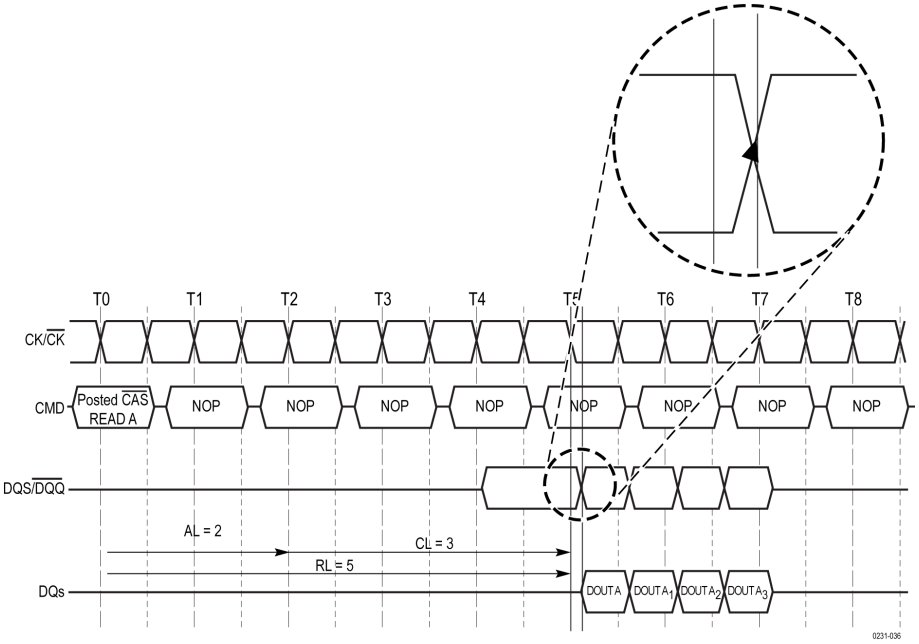
This measurement is mapped to DPOJET base measurement *Skew*.



tDQSCK

tDQSCK is the strobe output access time from differential clock. *tDQSCK* is measured between the rising edge of clock before or after the differential strobe Preamble time. The edge locations are determined by the mid-reference voltage levels.

This measurement is mapped to DPOJET->DDR measurement *DDR2 tDQSCK*.



The application calculates this measurement using the following equation:

$tDQSCK = T_n - T_{DQS(n)}$

Where,

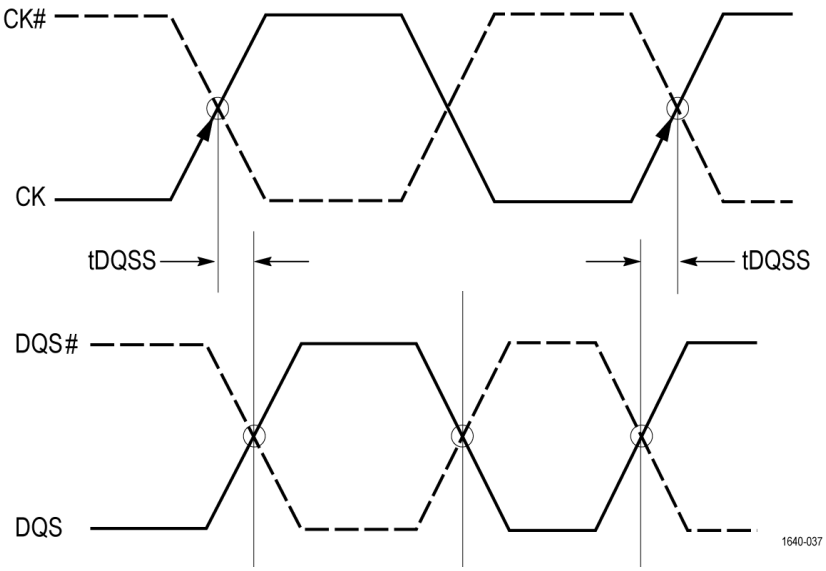
T_n specifies the clock edges.

$T_{DQS(n)}$ specifies the DQS edges.

tDQSS-Diff

tDQSS-Diff is defined as the skew between the actual position of a rising input strobe edge relative to differential clock. For both the signals, the edge locations are determined by the mid-reference voltage levels. The closest strobe edge to the clock edge that falls within the range limits is used for the measurement. This is measurement is applicable for the Write bursts.

This measurement is mapped to DPOJET base measurement *Skew*.



tDQSS(DQS)(Informative)

tDQSS(DQS)(Informative) measurement is same as *tDQSS-Diff*, except that it is measured on the single ended strobe signal.

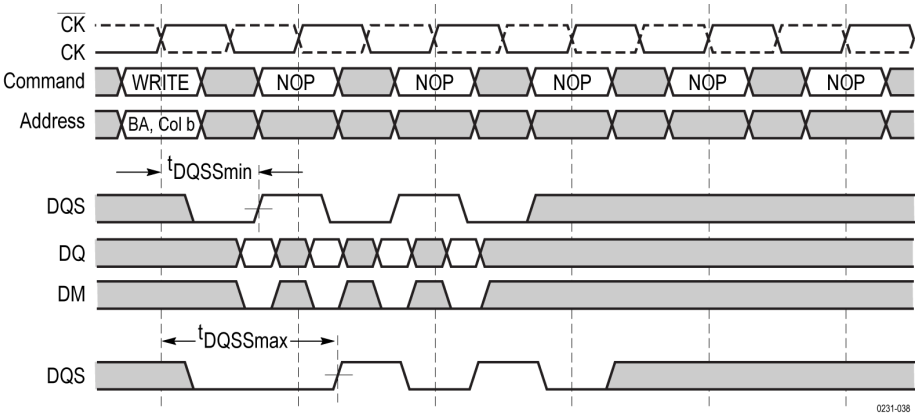
tDQSS

tDQSS measures the time taken from a WRITE event in DDR bus to the first strobe latching transition. This measurement has two sources - a digital Bus and analog strobe signal.

Measurement internally sets up Bus search to look for WRITE events. For every WRITE event in the bus search output, the algorithm finds and associates the first rising edge of strobe within the DDR Write burst.

This measurement is available only on 64-bit MSO instruments. Measurement gets selected only if there is a Bus source configured.

This measurement is mapped to DPOJET->DDR measurement *DDR tDQSS*.



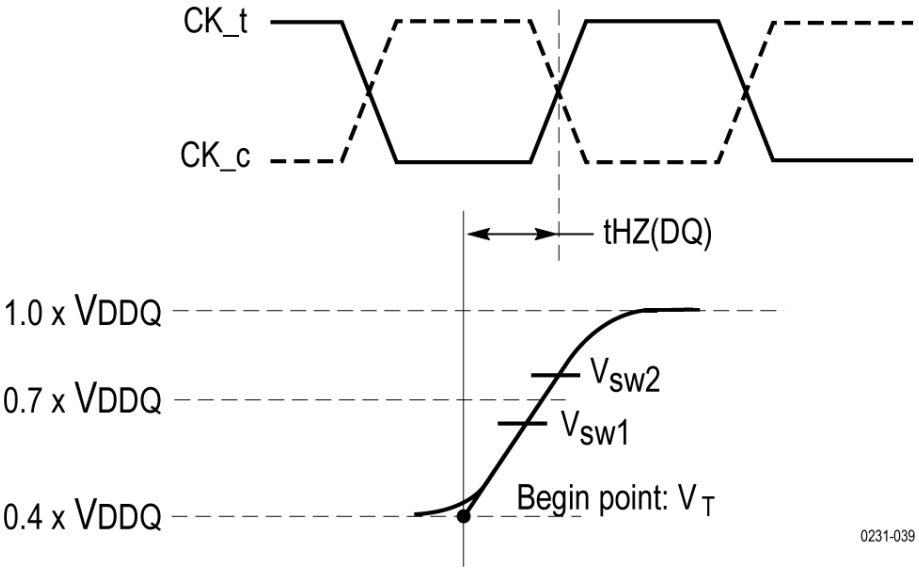
tHZ(DQ)

tHZ(DQ) is defined as DQ high impedance time from differential clock edge. This measures the elapsed time from when the device output is no longer driving to the designated rising clock edge. The designated rising clock edge is calculated using the below formula:

tHZ(DQ) with BL8: CK_t - CK_c rising crossing at RL + 4 nCK

tHZ(DQ) with BC4: CK_t - CK_c rising crossing at RL + 2 nCK

This measurement is computed from the extrapolated point V_T established by extending the slope between V_{sw1} and V_{sw2} to the designated rising edge of clock.



This measurement is mapped to DPOJET->DDR measurement *DDR tHZDQ.*

tHZ(DQS)

tHZ(DQS) measurement is same as *tHZ(DQ)*, except that it is measured on the single-ended strobe and differential clock signal.

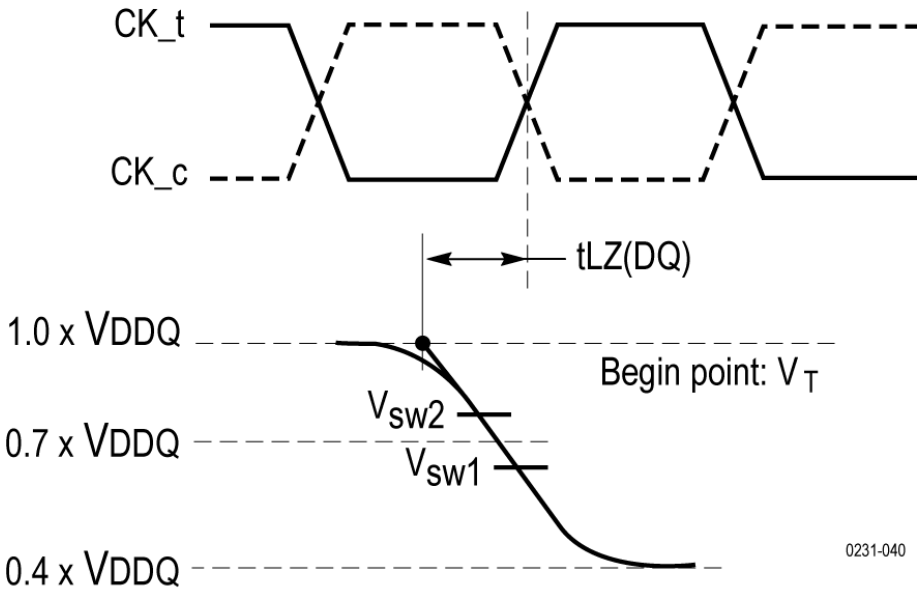
tLZ(DQS)

tLZ(DQS) measurement is same as *tLZ(DQ),* except that it is measured on the single ended strobe and differential clock signal.

tLZ(DQ)

tLZ(DQ) is defined as DQ low impedance time from differential clock edge. This measures the elapsed time from when the device output begins driving to the designated rising clock edge.

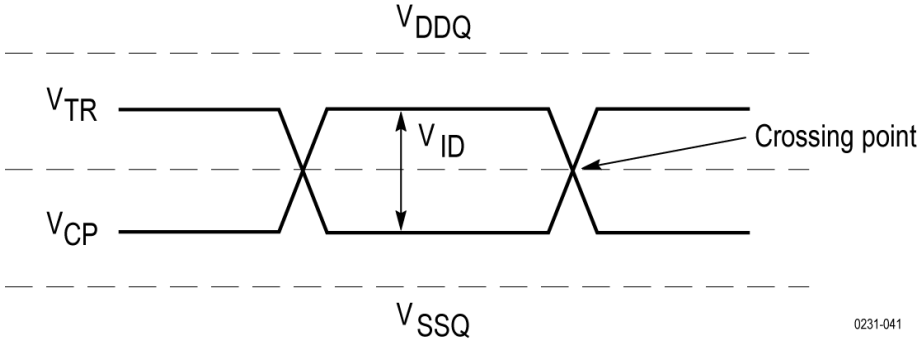
This measurement is computed from the extrapolated point V_T established by extending the slope between V_{sw1} and V_{sw2} to the designated rising edge of clock.



This measurement is mapped to DPOJET->DDR measurement *DDR tLZDQ.*

VID(ac)

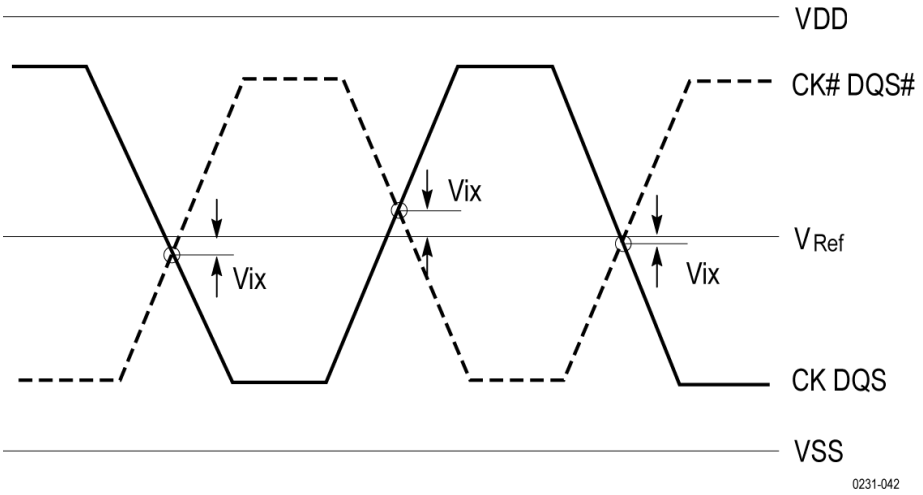
VID(ac) specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input signal and V_{CP} is the complement input signal.



This measurement is mapped to DPOJET base measurement *DDR VID(ac)*

Vix(ac)CK

Vix(ac)CK is defined as the differential input cross-point voltage measured from the actual crossover voltage of true and its complement signal to a designated reference voltage. This is measured on the single ended clock signal.



The application calculates this measurement using the following equation:

$V_n^{CrossOver} = (V_n^{ActualCrossOver} - V_{Ref})$

Where,

$V_n^{ActualCrossOver}$ is the crossing between positive and complement signals.

V_{Ref} is the designated reference voltage.

For DDR3, DDR3L, DDR4 and LPDDR3 generations the reference voltage is defined as Vdd/2. For these generations, this measurement is mapped to DPOJET->DDR measurement *DDR3 Vix(ac)*.

For LPDDR4 and LPDDR4X generations the reference voltage is defined as Vswing/2, where

Vswing/2(avg) = $0.5(V_{DQS\_t} + V_{DQS\_c})$ where the average is over one burst. For these two generations, this measurement is mapped to DPOJET->DDR measurement *DDRVix*.

For DDR, DDR2, LPDDR and GDDR5 generations, the reference voltage is set to VSSQ. For these generations, this measurement is mapped to DPOJET base measurement *V-Diff-Xovr*.

Vix(ac)DQS

Vix(ac)DQS measurement is same as *Vix(ac)CK,* except that it is measured on the single ended strobe signal and with respect to different reference level as specified below.

For DDR3, DDR3L and LPDDR3 generations the reference voltage is defined as Vdd/2. For these generations, this measurement is mapped to DPOJET->DDR measurement *DDR3 Vix(ac)*.

For DDR4, LPDDR4 and LPDDR4X generations the reference voltage is defined as Vswing/2, where Vswing/2(avg) = $0.5(V_{DQS\_t} + V_{DQS\_c})$ where the average is over one burst. For these two generations, this measurement is mapped to DPOJET->DDR measurement *DDRVix*.

For DDR2 generations the reference voltage is defined as VSSQ. Here the measurement is mapped to DPOJET base measurement *V-Diff-Xovr*.

Vix(ac)DQS(Informative)

Vix(ac)DQS(Informative) measurement is same as *Vix(ac)DQS,* where in the reference voltage is defined as VSSQ and DPOJET base measurement *V-Diff-Xovr* is used for the computation.

Vix(ac)WCK

Vix(ac)WCK measurement is same as *Vix(ac)DQS(Informative),* except that it is measured on the single ended WCK signal.

VIXDQ

VIXDQ measurement is same as *Vix(ac)DQS,* where in the reference voltage is defined as VDDQ/2 and DPOJET->DDR measurement *DDR3 Vix(ac)* is used for the computation.

VIXCA

VIXCA measurement is same as *Vix(ac)CK,* where in the reference voltage is defined as VDDCA/2 and DPOJET->DDR measurement *DDR3 Vix(ac)* is used for the computation.

Vox(ac)DQS

Vox(ac)DQS measurement is same as *Vix(ac)DQS*, except that it is measured on the single ended output strobe with respect to a reference voltage VSSQ.

This measurement is mapped to DPOJET base measurement *V-Diff-Xovr.*

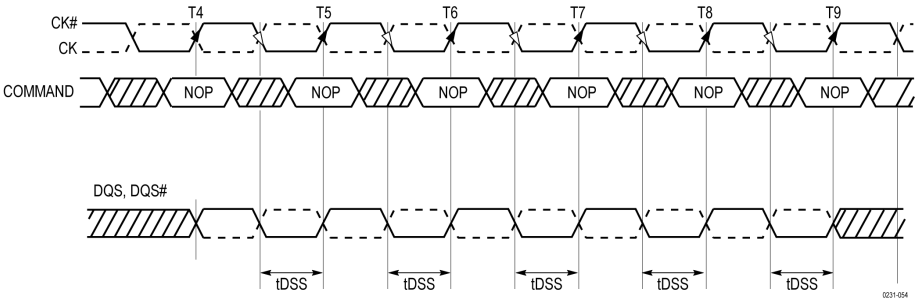
Vox(ac)CK

Vox(ac)CK is same as *Vox(ac)DQS*, except that it is measured on the single-ended output clock signal.

tDSS-Diff

tDSS-Diff is defined as the elapsed setup time from the differential strobe falling edge to the differential clock rising edge.

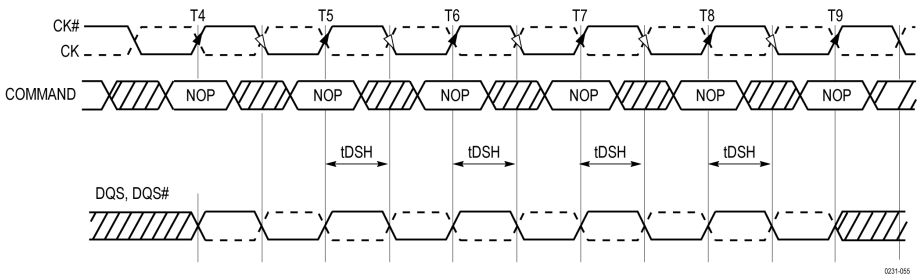
This measurement is mapped to DPOJET base measurement *Setup*.



tDSH-Diff

tDSH-Diff is defined as the elapsed hold time from the differential strobe falling edge to the differential clock rising edge.

This measurement is mapped to DPOJET base measurement *Hold*.



tDSS(DQS)(Informative)

tDSS(DQS)(Informative) measurement is same as *tDSS-Diff*, except that it is measured on the single ended strobe signal.

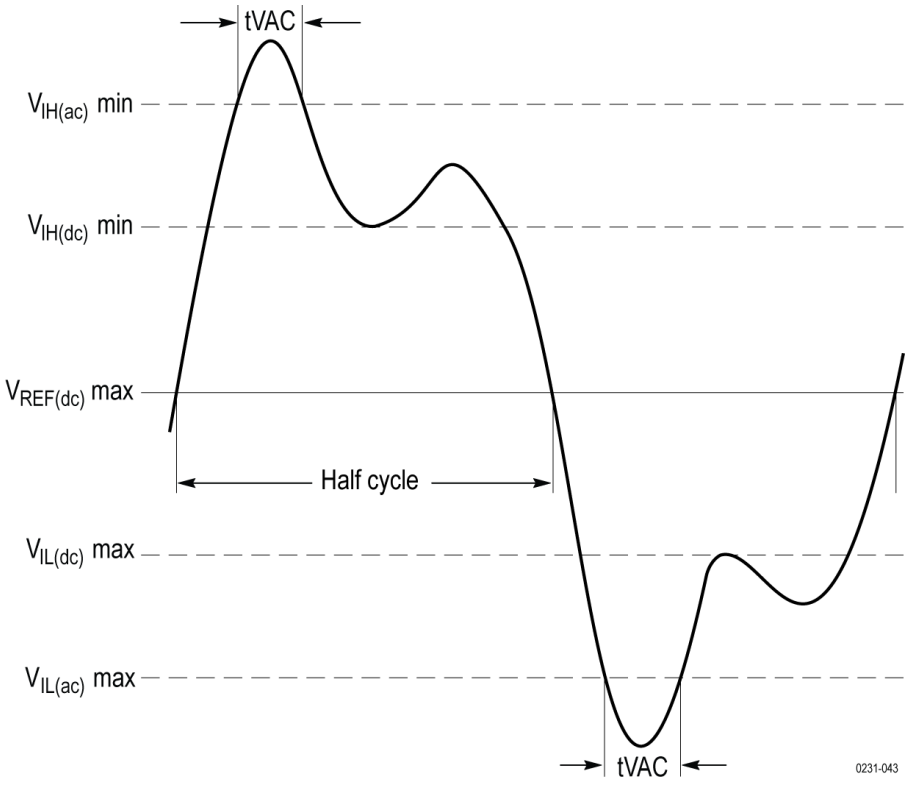
tDSH(DQS)(Informative)

tDSH(DQS)(Informative) measurement is same as *tDSH-Diff*, except that it is measured on the single-ended strobe signal.

tVAC(DQ)

tVAC(DQ) is defined as the minimum time, the input data signal to remain above/below $V_{IH/IL}$(ac) level after each valid transition.

This measurement is mapped to DPOJET base measurement *Time Outside Level*.



tVAC(Addr/Cmd)

tVAC(Addr/Cmd) measurement is same as *tVAC(DQ)*, except that it is measured on the address/command signal.

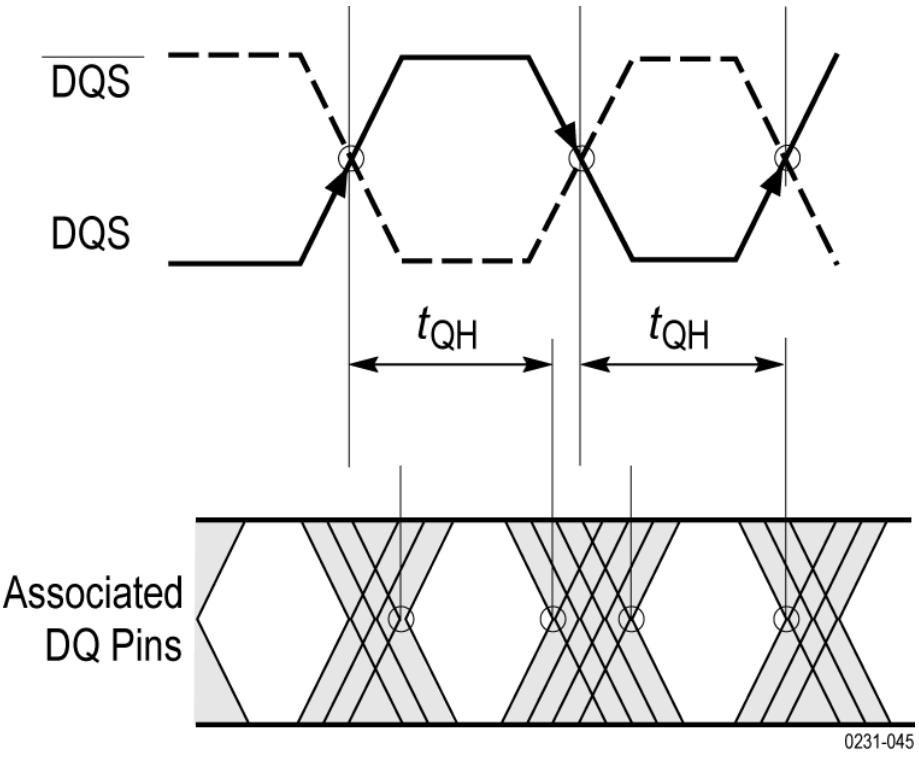
tDVAC(DQS) / tDVAC(DQS)(Informative)

tDVAC(DQS) / tDVAC(DQS)(Informative) measurement is same as *tDVAC(CK)*, except that it is measured on the differential strobe signal.

tQH

tQH is defined as the output data hold time from differential strobe mid reference level. This describes the earliest invalid transition of the associated DQ pins.

This measurement is mapped to DPOJET base measurement *Hold*.



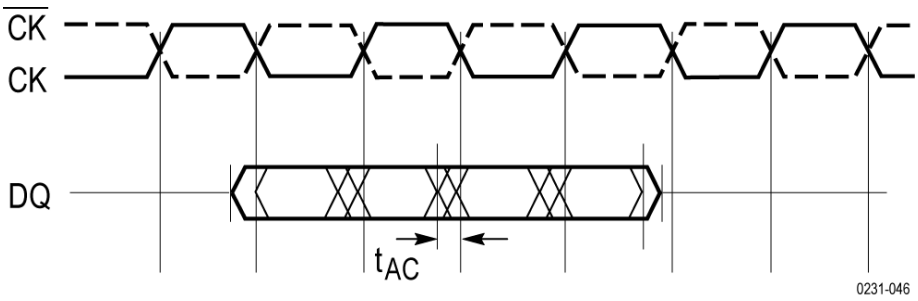
tQH_DBI

tQH_DBI measurement is same as *tQH*, except that it measures the time when Data Bus Inversion (DBI) is enabled.

tAC-Diff

tAC-Diff is the output data access time from differential clock.

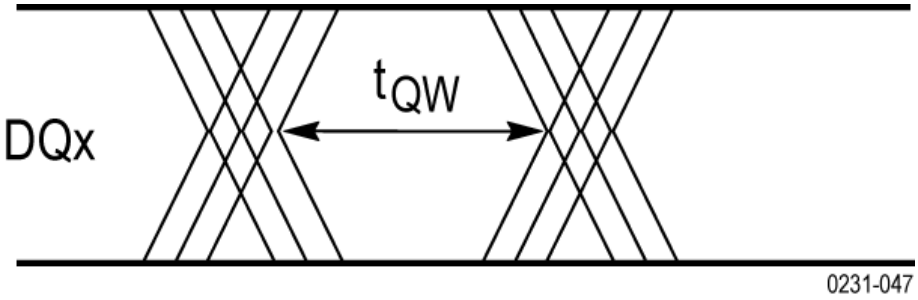
This measurement is mapped to DPOJET->DDR measurement *DDR Setup-Diff*.



tQW-Total

tQW-Total is defined as the valid window time for the output data over any one DQ pin.

This is mapped to DPOJET base measurement *Width*.



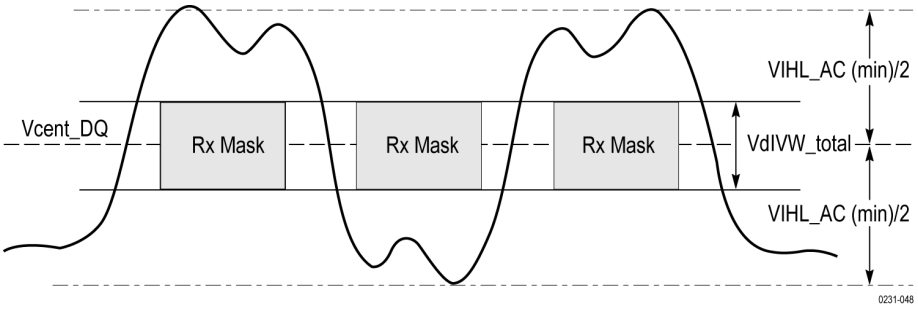
tQW-Total_DBI

tQW-Totat_DBI measurement is same as *tQW_Total*, except that it measures the time when Data Bus Inversion (DBI) is enabled.

VIHL_AC

VIHL_AC defines the input data pulse peak to peak amplitude. This is measured with respect to Vcent_DQ value. DQ only input pulse amplitude into the receiver must meet or exceed VIHL_AC(min) at any point over the total UI. Note that VIHL_AC(min) does not have to be met when no transitions are occurring.

In DDR4, this measurement is mapped to DPOJET base measurement *Cycle Pk-Pk,* whereas across all generations, VIHL_AC is mapped to DPOJET->DDR measurement *DDR VIHLAC*.



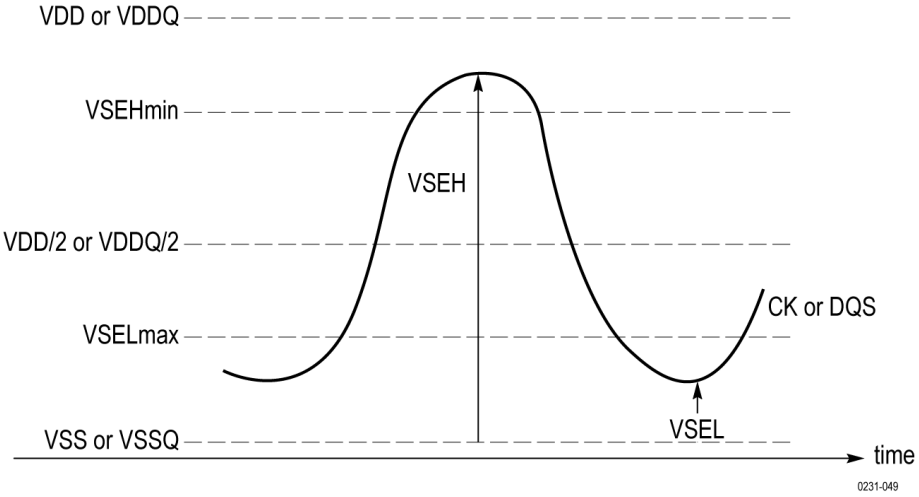
VIHL_AC(CA)

VIHL_AC(CA) measurement is same as *VIHL_AC*, except that it is measured on the address/command signal with respect to Vcent_CA level.

VSEH(DQS) / VSEH(DQS)(Informative)

VSEH(DQS) / VSEH(DQS)(Informative) is defined as the high level voltage for the single-ended strobe signal.

This measurement is mapped to DPOJET base measurement *Cycle Max*.



VSEH(DQS#) / VSEH(DQS#)(Informative)

VSEH(DQS#) / VSEH(DQS#)(Informative) measurement is same as *VSEH(DQS),* except that it is measured on the single-ended complement strobe signal.

VSEH(CK) / VSEH(CK)(Informative) / VSEH(AC)CK

VSEH(CK) / VSEH(CK)(Informative) / VSEH(AC)CK measurement is same as *VSEH(DQS),* except that it is measured on the single-ended clock signal.

VSEH(CK#) / VSEH(CK#)(Informative) / VSEH(AC)CK#

VSEH(CK#) / VSEH(CK#)(Informative) / VSEH(AC)CK# measurement is same as *VSEH(DQS),* except that it is measured on the single-ended complement clock signal.

VSEH(AC)DQS / VSEH(AC)DQS(Informative)

VSEH(AC)DQS / VSEH(AC)DQS(Informative) measurement is same as *VSEH(DQS)*.

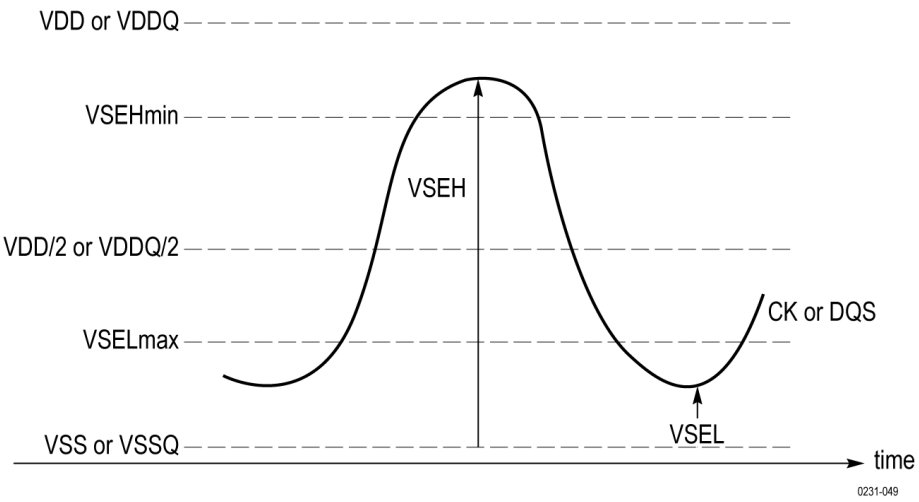
VSEH(AC)DQS# / VSEH(AC)DQS#(Informative)

VSEH(AC)DQS# / VSEH(AC)DQS#(Informative) measurement is same as *VSEH(DQS#)*.

VSEL(DQS) / VSEL(DQS)(Informative)

VSEL(DQS) / VSEL(DQS)(Informative) is defined as the low level voltage for the single-ended strobe signal.

This measurement is mapped to DPOJET base measurement *Cycle Min*.



VSEL(CK) / VSEL(CK)(Informative) / VSEL(AC)CK

VSEL(CK) / VSEL(CK)(Informative) / VSEL(AC)CK measurement is same as *VSEL(DQS)*, except that it is measured on the single-ended clock signal.

VSEL(CK#) / VSEL(CK#)(Informative) / VSEL(AC)CK#

VSEL(CK#) / VSEL(CK#)(Informative) / VSEL(AC)CK# measurement is same as *VSEL(DQS)*, except that it is measured on the single-ended complement clock signal.

VSEL(AC)DQS / VSEL(AC)DQS(Informative)

VSEL(AC)DQS / VSEL(AC)DQS(Informative) measurement is same as *VSEL(DQS)*.

VSEL(DQS#) / VSEL(DQS#)(Informative)

VSEL(DQS#) / VSEL(DQS#)(Informative) measurement is same as *VSEL(DQS)*, except that it is measured on the single-ended complement strobe signal.

tQSH

tQSH is the high pulse width of the differential output strobe signal. It is the amount of time the waveform remains above the mid reference voltage level.

This measurement is mapped to DPOJET base measurement *Pos Width*.

tQSL

tQSL is the low pulse width of the differential output strobe signal. It is the amount of time the waveform remains below the mid reference voltage level.

This measurement is mapped to DPOJET base measurement *Neg Width*.

tQSH_DBI

tQSH_DBI measurement is same as *tQSH*, except that it measures the pulse width when Data Bus Inversion (DBI) is enabled.

tQSL_DBI

tQSL_DBI measurement is same as *tQSL,* except that it measures the pulse width when Data Bus Inversion (DBI) is enabled.

VSWING(MAX)DQS

VSWING(MAX)DQS is defined as maximum peak-to-peak swing voltage of the single-ended input strobe signal.

This measurement is mapped to DPOJET base measurement *Cycle Pk-Pk*.

VSWING(MAX)DQS#

VSWING(MAX)DQS# measurement is same as *VSWING(MAX)DQS*, except that it is measured on the single ended complement input strobe signal.

VSWING(MAX)CK

VSWING(MAX)CK measurement is same as *VSWING(MAX)DQS*, except that it is measured on the single-ended clock signal.

VSWING(MAX)CK#

VSWING(MAX)CK# measurement is same as *VSWING(MAX)DQS*, except that it is measured on the single ended complement clock signal.

VIN(CK)

VIN(CK) is defined as input voltage level of the single-ended clock signal.

This measurement is mapped to DPOJET base measurement *High-Low*.

VIN(CK#)

VIN(CK#) measurement is same as VIN(CK), except that it is measured on the single-ended complement clock signal.

VIN(WCK)

VIN(WCK) measurement is same as VIN(CK), except that it is measured on the single-ended WCK signal.

VOL(WCK#)

VOL(WCK#) measurement is same as *VOL(WCK),* except that it is measured on the single ended complement WCK signal.

VOHdiff(AC)

VOHdiff(AC) is defined as the AC high voltage level of the differential output strobe signal.

This measurement is mapped to DPOJET base measurement *Cycle Max*.

VOLdiff(AC)

VOLdiff(AC) is defined as the AC low voltage level of the differential output strobe signal.

This measurement is mapped to DPOJET base measurement *Cycle Min*.

VILdiff(AC)

VILdiff(AC) measurement is same as *VOLdiff(AC)*, except that it is measured on the differential input strobe or clock signal.

VIHdiff(AC)

VIHdiff(AC) measurement is same as *VOHdiff(AC)*, except that it is measured on the differential input strobe or clock signal.

VOH(AC)DQ

VOH(AC)DQ is defined as the AC high voltage level on the output data signal. This measurement will verify that whether the high level voltage value of the output data signal is greater than the conformance higher limits of the VOH(AC) value specified in the JEDEC specification.

This measurement is mapped to DPOJET base measurement *Cycle Max*.

VOH(AC)DQS

VOH(AC)DQS measurement is same as *VOH(AC)DQ*, except that it is measured on the single-ended input strobe signal.

VOH(AC)DQS#

VOH(AC)DQS# measurement is same as *VOH(AC)DQ,* except that it is measured on the single ended input complement strobe signal.

VOL(AC)DQ

VOL(AC)DQ is defined as the AC low voltage level on the output data signal. This measurement will verify that whether the low level voltage value of the output data signal is lower than the conformance lower limits of the VOL(AC) value specified in the JEDEC specification.

This measurement is mapped to DPOJET base measurement *Cycle Min*.

VOL(AC)DQS

VOL(AC)DQS measurement is same as *VOL(AC)DQ,* except that it is measured on the single ended input strobe signal.

VOL(AC)DQS#

VOL(AC)DQS# measurement is same as VOL(AC)DQ, except that it is measured on the single-ended input complement strobe signal.

VOH(DC)DQ

VOH(DC)DQ is defined as the DC high voltage level on the output data signal. This measurement will verify that whether the high level voltage value of the output data signal is greater than the conformance higher limits of the VOH(DC) value specified in the JEDEC specification.

This measurement is mapped to DPOJET base measurement *Cycle Max*.

VOH(DC)DQS

VOH(DC)DQS measurement is same as *VOH(DC)DQ*, except that it is measured on the single ended input strobe signal.

VOH(DC)DQS#

VOH(DC)DQS# measurement is same as *VOH(DC)DQ*, except that it is measured on the single ended input complement strobe signal.

VOL(DC)DQ

VOL(DC)DQ is defined as the DC low voltage level on the output data signal. This measurement will verify that whether the low level voltage value of the output data signal is lower than the conformance lower limits of the VOL(DC) value specified in the JEDEC specification.

This measurement is mapped to DPOJET base measurement *Cycle Min*.

VOL(DC)DQS

VOL(DC)DQS measurement is same as *VOL(DC)DQ*, except that it is measured on the single-ended input strobe signal.

VOL(DC)DQS#

VOL(DC)DQS# measurement is same as *VOL(DC)DQ*, except that it is measured

on the single ended input complement strobe signal.

VOH(WCK)

VOH(WCK) measurement is same as *VOH(DC)DQ*, except that it is measured on the single ended WCK signal. This measurement is mapped to DPOJET base measurement High.

VOH(WCK#)

VOH(WCK#) measurement is same as *VOH(WCK)*, except that it is measured on the single ended complement WCK signal.

VOL(WCK)

VOL(WCK) measurement is same as *VOL(DC)DQ*, except that it is measured on the single ended WCK signal. This measurement is mapped to DPOJET base measurement *Low*.

VOL(WCK#)

VOL(WCK#) measurement is same as *VOL(WCK)*, except that it is measured on

the single ended complement WCK signal.

SSC Mod Freq(CK)

SSC Mod Freq(CK) measures the SSC modulation frequency for the differential clock signal. A low pass filter with default cut off frequency of 1.98 MHz is used for the measurement.

This measurement is mapped to DPOJET base measurement *SSC Mod Rate*.

SSC Mod Freq(WCK)

SSC Mod Freq(WCK) measurement is same as *SSC Mod Freq(CK)*, except that it is measured on the differential WCK signal.

SSC Downspread(CK)

SSC Downspread(CK) measures the SSC frequency deviation of differential clock signal in ppm (parts per million). A low pass filter with default cut off frequency of 1.98 MHz is used for the measurement.

This measurement is mapped to DPOJET base measurement *SSC Freq Dev*.

SSC Downspread(WCK)

SSC Downspread(WCK) measurement is same as *SSC Downspread(CK)*, measurement except that it is measured on the differential WCK signal.

SSC Profile(CK)

SSC Profile(CK) measures the modulation profile of the spread spectrum clocking (SSC) for the differential clock signal. Using the profile, you can analyze the SSC modulation rate by using the horizontal cursors and the peak-to-peak frequency deviation by using the vertical cursors.

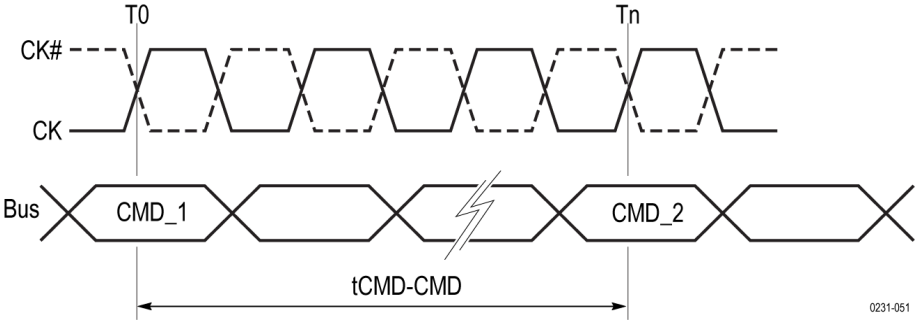
This measurement is mapped to DPOJET base measurement *SSC Profile*.

SSC Profile(WCK)

SSC Profile(WCK) measurement is same as *SSC Profile(CK)*, except that it is measured on the differential WCK signal.

Digital Measurements (Command to Command)

The below measurements measures the elapsed time between two bus states, for example CMD_1 and CMD_2. For each bus state, the relevant timing point is considered with respect to the rising edge of a separately specified clock source. These measurements are mapped to DPOJET base measurement *tCmd-Cmd*.



All these measurements are available only on the MSO instruments.

tRFC

tRFC is defined as the elapsed time between a REFRESH command to the successive ACTIVE command. This is the minimum time required to be present between any two REFRESH commands.

tREFTR(Read)

tREFTR(Read) is defined as the elapsed time between a REFRESH command to the successive RDTR command. This defines the time interval at which a valid RDTR command allowed after any REFRESH command.

tREFTR(Write)

tREFTR(Write) measurement is same as *tREFTR(Read)*, except that it measures the elapsed time between a REFRESH command to the successive WRTR command.

tXSNRW

tXSNRW is defined as the elapsed time between a SRX command to the successive PRECHARGE command. A delay of at least *tXSNRW* must be satisfied before a valid command not requiring a locked PLL/DLL can be issued to the device to allow for completion of any internal refresh in progress.

tPD

tPD is defined as the minimum power down entry to exit time. This is measured from PDE command to successive SRX command, with respect the rising edge of the clock signal.

tRC

tRC is defined as the time interval between two successive ACTIVE commands on the same bank.

tRAS

tRAS is defined as the elapsed time between an ACTIVE command to the successive PRECHARGE command.

tRCDRD

tRCDRD is defined as the elapsed time between an ACTIVE command to the successive READ command.

tRCDWR

tRCDWR is defined as the elapsed time between an ACTIVE command to the successive WRITE command.

tRTPL / tRTP

tRTPL / tRTP is defined as the elapsed time between a READ command to the successive PRECHARGE command on the same bank with bank groups enabled.

tPPD

tPPD is defined as the elapsed time between any two successive PRECHARGE commands.

tRP(REF)

tRP(REF) is defined as the elapsed time between a PRECHARGE command to the successive REFRESH command.

tRP(SRE)

tRP(SRE) is defined as the elapsed time between a PRECHARGE command to the successive SRE command.

tRP(MRS)

tRP(MRS) is defined as the elapsed time between a PRECHARGE command to the successive 'MODE REGISTER SET' command.

tRP(ACT) / tRP

tRP(ACT) / tRP is defined as the elapsed time between an PRECHARGE command to the successive ACTIVE command.

tCKESR

tCKESR is defined as the minimum pulse width of CKE (Clock Enable) signal during Self-Refresh. This is measured as the elapsed time between 'Enter Self Refresh' command the successive 'Exit Self Refresh' command.

tXSRRD

tXSRRD is defined as the elapsed time between an 'Exit Self Refresh' command to the successive READ command.

tXSRWR

tXSRWR is defined as the elapsed time between an 'Exit Self Refresh' command to the successive WRITE command.

tCCDRD

tCCDRD is defined as the elapsed time between any two successive READ commands.

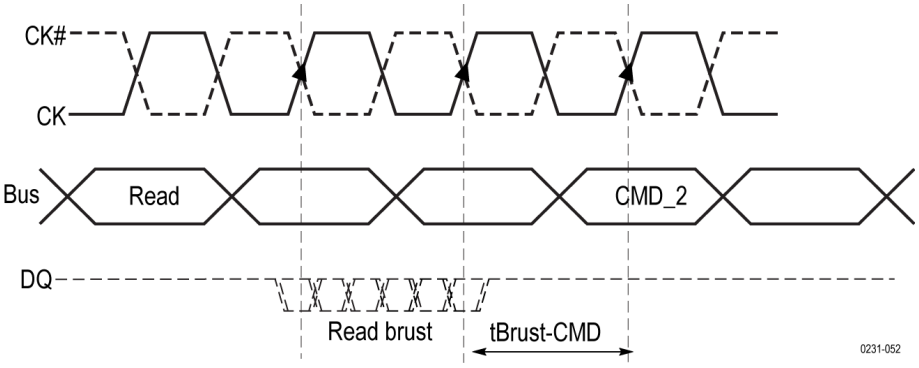
tCCDWR

tCCDWR is defined as the elapsed time between any two successive WRITE commands.

Digital Measurements (Burst to Command)

The below measurements, measures the elapsed time between the last data element of a Read or Write burst to the next bus state. The next bus state depends on the command of interest which is configured in the search. This measurement requires that the Bus source and DPOJET Qualifiers should be turned on for DDR read or DDR Write searches.

These measurements are mapped to DPOJET->DDR measurement *GDDR5 tBurst-CMD*.



All these measurements are available only on the MSO instruments.

tWRSRE

tWRSRE is defined as the elapsed time between the last WCK clock edge within a Write burst and start of the SELF REFRESH command.

tWRPDE

tWRPDE is defined as the elapsed time between the last WCK clock edge within a Write burst and start of the POWER DOWN ENTRY command.

tRDSRE

tRDSRE is defined as the elapsed time between the last WCK clock edge within a Read burst and start of the SELF REFRESH command.

tRDPDE

tRDPDE is defined as the elapsed time between the last WCK clock edge within a Read burst and start of the POWER DOWN ENTRY command.

Digital Measurements (Others)

tCKSRE

tCKSRE is defined as the valid clock cycles required after Self Refresh Entry (SRE) command. Changing the input clock frequency or the supply voltage is permissible only *tCKSRE* after SRE command is registered.

This measurement is mapped to DPOJET->DDR measurement *GDDR5 tCKSRE*.

Note: This measurement is available only on the MSO instruments.

tCKSRX

tCKSRX is defined as the valid clock cycles required before the Self Refresh Exit (SRX) command. Changing the input clock frequency or the supply voltage is permissible provided the new clock frequency or supply voltage is stable for *tCKSRX* prior to SRX command.

This measurement is mapped to DPOJET->DDR measurement *GDDR5 tCKSRX*.

Note: This measurement is available only on the MSO instruments.

tWCK-TJ

tWCK-TJ is defined as the total jitter at a Bit Error Rate of 1e-12. This is an extrapolated value that predicts a peak-to-peak jitter that will only be exceeded with a probability equal to 1e-12.

This measurement is mapped to DPOJET base measurement *TJ@BER*.

tWCK-RJ

tWCK-RJ is measures the random jitter component of the differential WCK signal.

This measurement is mapped to DPOJET base measurement *RJ*.

VWCK-SWING

VWCK-SWING is defined as the voltage swing of the differential WCK signal.

This measurement is mapped to DPOJET base measurement *High-Low*.

tCH(abs)/ tCH

tCH(abs)/ tCH is the high pulse width of the differential clock signal. It is the amount of time the waveform remains above the mid reference voltage level.

This measurement is mapped to DPOJET base measurement *Pos Width*.

tDVAC(WCK)

tDVAC(WCK) measurement is same as *tDVAC(CK)*, except that it is measured on the differential WCK signal.

Programmer Manual

About the GPIB program

You can use remote GPIB commands to communicate with the DDRA application. Query measurement results using DPOJET commands. Sequence commands using DPOJET commands. Setup reports, logging, statistics, and limits using DPOJET commands. An example of a GPIB program is included with the DPOJET application in `C:\Users\Public\Tektronix\TekApplications\DPOJET\Examples`.

The example shows how a GPIB program executes the DPOJET application to do the following tasks:

1. Start the application.
2. Recall a setup.
3. Take a measurement.
4. View measurement results and plots.
5. Exit the application.

Note: Commands are not case and space sensitive. Your program will operate correctly even if you do not follow the capitalization and spacing precisely.

GPIB reference materials

To use GPIB commands with your oscilloscope, you can refer to the following materials:

- The GPIB Program Example in `C:\Users\Public\Tektronix\TekApplications\DPOJET\Examples` for guidelines to use while designing a GPIB program.
- The Parameters topics for range of values, minimum units and default values of parameters.
- The programmer information in the online help of your oscilloscope.

Argument types

The syntax shows the format that the instrument returns in response to a query. This is also the preferred format when sending the command to the instrument though any of the formats are accepted. This documentation represents these arguments as follows:

Table 36: Argument types

Symbol	Meaning
`<NR1>`	Signed integer value.
`<NR2>`	Floating point value without an exponent.
`<NR3>`	Floating point value with an exponent.
`double`	Double precision floating point with exponent.
`<QString>`	Quoted string of ASCII text.

General commands

DDRA:GENERATEReport (No Query Form)

This command generates the report with best case and worst case screen shots embedded.

Syntax

`DDRA:GENERATEReport`

Inputs

NA

Outputs

Generates the report with best and worst case screen shots.

Examples

`DDRA:GENERATEReport`, generates the report with best and worst case screen shots.

DDRA:APPENDReport

This is to enable/disable the append report feature.

Syntax

`DDRA:APPENDReport {0 | 1}`

Inputs

1- Enables the append report feature.

0- Disables the append report feature.

Outputs

{0 | 1}

Examples

`DDRA:APPENDReport 1`, enables the append report feature.

DDRA:ACTIVATE (No Query Form)

This command launches or brings the DDRA Application to focus.

Syntax

`DDRA:ACTIVATE`

Inputs

NA

Outputs

NA

Examples

`DDRA:ACTIVATE`, launch the DDRA Application; when the command is executed for the first time else will bring the application to focus.

DDRA:VERsion? (Query Only)

This command queries the DDRA Application version.

Syntax

`DDRA:VERSion?`

Inputs

NA

Outputs

NA

Examples

`DDRA:VERSION?` returns the currently installed application version.

Measurement and Sources commands

DDRA:INFORMAtivemeas

This command sets or queries the informative measurement option.

Syntax

`DDRA:INFORMAtivemeas {0 | 1}`

Inputs

0 - Hide the informative measurements.

1 - Show the informative measurements.

Outputs

{0 | 1}

Examples

`DDRA:INFORMAtivemeas 1`, shows the informative measurements.

`DDRA:INFORMAtivemeas?` returns 0, hides the informative measurements.

DDRA:ISOLBurstlen

This command sets or queries the Isolated Burst Length (UI) value for Preamble Pattern Matching.

Syntax

`DDRA:ISOLBurstlen { 8 | 16 | 32 }`

`DDRA:ISOLBurstlen?`

Inputs

`8, 16, 32`: Represents the isolated burst length.

Outputs

{ 8 | 16 | 32 }

Examples

`DDRA:ISOLBurstlen 16`, sets the isolated burst length to 16 bit.

`DDRA:ISOBurstlen?` returns 8, which indicates the isolated burst length is set to 8 bit.

Note: Applicable for LPDDR4, LPDDR4X measurements.

DDRA:BACKTOBAckburst

This command sets or queries the feature status - Enable back-to-back burst detection.

Syntax

```
DDRA:BACKTOBAckburst { 1 | 0 }
```

```
DDRA:BACKTOBAckburst?
```

Inputs

`1`: Enables the feature; Enable back-to-back burst detection.

`0`: Disables the feature; Enable back-to-back burst detection.

Outputs

{ 1 | 0 }

Examples

`DDRA:BACKTOBAckburst 1`, enables the Enable back-to-back burst detection check box.

`DDRA:BACKTOBAckburst?` returns 0, which indicates Enable back-to-back burst detection is disabled.

DDRA:MEASType

This command sets or queries the measurement type for the selected generation.

Syntax

```
DDRA:MEASType { WRITEbursts | READbursts | CKDiff | CKSE | DQSSERead |
DQSSEWrite | ADDRCMD | WCKDiff | WCKSE | REFResh | PRECHArge | POWERDown |
ACTIve | OVERSHOOTUNDERShoot }
```

```
DDRA:MEASType?
```

Inputs

`WRITEbursts` - Write Bursts

`READbursts` - Read Bursts

`CKDiff` - Clock(Diff)

`CKSE` - Clock(Single Ended)

`DQSSERead` - DQS(Single Ended, Read)

`DQSSEWrite` - DQS(Single Ended, Write)

`ADDRCMD` - Address/Command

`OVERSHOOTUNDERShoot` - Overshoot/Undershoot

`WCKDiff` - WCK(Diff)

`WCKSE` - WCK(Single Ended)

`REFResh` - Refresh

`PRECHArge` - Precharge

`POWERDown` - Power Down

`ACTIve` - Active

Outputs

{ WRITEbursts | READbursts | CKDiff | CKSE | DQSSERead | DQSSEWrite | ADDRCMD | WCKDiff | WCKSE | REFResh | PRECHArge | POWERDown | ACTIve | OVERSHOOTUNDERShoot }

Examples

`DDRA:MEASType DQSSERead`, sets the measurement type as DQS(Single Ended, Read).

`DDRA:MEASType?` returns CKDiff, which indicates the measurement type is selected to CKDiff.

DDRA:ADDMeas (No Query Form)

This command selects/adds the measurement specified as the argument.

Syntax

`DDRA:ADDMeas {<Measurement PI name>}`

Inputs

`<Measurement PI name>` - Refer table below for measurement PI name.

Outputs

NA

Examples

`DDRA:ADDMeas ACOVRSHOOT` selects or adds the "AC-Overshoot" measurement.

Table 37: Measurement and its PI Name

Measurement	Measurement PI name
AC-Overshoot	ACOVRSHOOT
AC-Overshoot(AbsMax)	ACOVRSHOOTAM
AC-Overshoot(AbsMax)(CK#)	ACOVRSHOOTAMCKB
AC-Overshoot(AbsMax)(CK)	ACOVRSHOOTAMCK
AC-Overshoot(AbsMax)(DQ)	ACOVRSHOOTAMDQ
AC-Overshoot(AbsMax)(DQS#)	ACOVRSHOOTAMDQSB
AC-Overshoot(AbsMax)(DQS)	ACOVRSHOOTAMDQS
AC-Overshoot(CK#)	ACOVRSHOOTCKBAR
AC-Overshoot(CK)	ACOVRSHOOTCK
AC-Overshoot(DQ)	ACOVRSHOOTDQ
AC-Overshoot(DQS#)	ACOVRSHOOTDQSBAR
AC-Overshoot(DQS)	ACOVRSHOOTDQS
AC-OvershootArea	ACOVRSHOOTAREA

Table continued…

Measurement	Measurement PI name
AC-OvershootArea(AbsMax)	ACOVRSHOOTAREAAM
AC-OvershootArea(AbsMax)(CK#)	ACOVRSHOOTAREAAMCKB
AC-OvershootArea(AbsMax)(CK)	ACOVRSHOOTAREAAMCK
AC-OvershootArea(AbsMax)(DQ)	ACOVRSHOOTAREAAMDQ
AC-OvershootArea(AbsMax)(DQS#)	ACOVRSHOOTAREAAMDQSB
AC-OvershootArea(AbsMax)(DQS)	ACOVRSHOOTAREAAMDQS
AC-OvershootArea(CK#)	ACOVRSHOOTAREACKBAR
AC-OvershootArea(CK)	ACOVRSHOOTAREACK
AC-OvershootArea(DQ)	ACOVRSHOOTAREADQ
AC-OvershootArea(DQS#)	ACOVRSHOOTAREADQSBAR
AC-OvershootArea(DQS)	ACOVRSHOOTAREADQS
AC-Undershoot	ACUNDSHOOT
AC-Undershoot(AbsMax)(DQ)	ACUNDSHOOTAMDQ
AC-Undershoot(AbsMax)(DQS#)	ACUNDSHOOTAMDQSB
AC-Undershoot(AbsMax)(DQS)	ACUNDSHOOTAMDQS
AC-Undershoot(CK#)	ACUNDSHOOTCKBAR
AC-Undershoot(CK)	ACUNDSHOOTCK
AC-Undershoot(DQ)	ACUNDSHOOTDQ
AC-Undershoot(DQS#)	ACUNDSHOOTDQSBAR
AC-Undershoot(DQS)	ACUNDSHOOTDQS
AC-UndershootArea	ACUNDSHOOTAREA
AC-UndershootArea(AbsMax)(DQ)	ACUNDSHOOTAREAAMDQ
AC-UndershootArea(AbsMax)(DQS#)	ACUNDSHOOTAREAAMDQSB
AC-UndershootArea(AbsMax)(DQS)	ACUNDSHOOTAREAAMDQS
AC-UndershootArea(CK#)	ACUNDSHOOTAREACKBAR
AC-UndershootArea(CK)	ACUNDSHOOTAREACK
AC-UndershootArea(DQ)	ACUNDSHOOTAREADQ
AC-UndershootArea(DQS#)	ACUNDSHOOTAREADQSBAR
AC-UndershootArea(DQS)	ACUNDSHOOTAREADQS
AddrCmd Eye Width(Informative)	ADDRCMDEYEWIDTH
AutoFitRxMask(Informative)	AUTOFITRxmask
CKSlew-Fall(CK#)	CKSLEWFALLCKBAR
CKSlew-Fall(CK)	CKSLEWFALLCK
CKSlew-Rise(CK#)	CKSLEWRISECKBAR
CKSlew-Rise(CK)	CKSLEWRISECK
Clock Eye Height (Informative)	CLOCKEYEHEIGHT
Clock Eye Width (Informative)	CLOCKEYEWIDTH

Table continued…

Measurement	Measurement PI name
Data Eye Height	DATAEYEHEIGHT
Data Eye Width	DATAEYEWIDTH
DDRARXMask	DDRARXMASK
InputSlew-Diff-Fall(CK)	INPUTSLEWDIFFFALLCK
InputSlew-Diff-Fall(DQS)	INPUTSLEWDIFFFALLDQS
InputSlew-Diff-Rise(CK)	INPUTSLEWDIFFRISECK
InputSlew-Diff-Rise(DQS)	INPUTSLEWDIFFRISEDQS
Slew Rate-Hold-Fall(Addr/Cmd)	SLEWHOLDFALLADDRCMD
Slew Rate-Hold-Fall(DQ)	SLEWHOLDFALLDQ
Slew Rate-Hold-Rise(Addr/Cmd)	SLEWHOLDRISEADDRCMD
Slew Rate-Hold-Rise(DQ)	SLEWHOLDRISEDQ
Slew Rate-Hold-SE-Fall(DQS)	SLEWHOLDSEFALLDQS
Slew Rate-Hold-SE-Rise(DQS)	SLEWHOLDSERISEDQS
Slew Rate-Setup-Fall(Addr/Cmd)	SLEWSETUPFALLADDRCMD
Slew Rate-Setup-Fall(DQ)	SLEWSETUPFALLDQ
Slew Rate-Setup-Rise(Addr/Cmd)	SLEWSETUPRISEADDRCMD
Slew Rate-Setup-Rise(DQ)	SLEWSETUPRISEDQ
Slew Rate-Setup-SE-Fall(DQS)	SLEWSETUPSEFALLDQS
Slew Rate-Setup-SE-Rise(DQS)	SLEWSETUPSERISEDQS
SRCA_Fall	SRCAFALL
SRCA_Rise	SRCARISE
srf1	SRF1
srf2	SRF2
SRIN_cIVW_Fall	SRINCIVWFALL
SRIN_cIVW_Rise	SRINCIVWRISE
SRIN_dIVW_Fall	SRINDIVWFALL
SRIN_dIVW_Rise	SRINDIVWRISE
SRQdiff-Fall(DQS)	SRQDIFFFALLDQS
SRQdiff-Rise(DQS)	SRQDIFFRISEDQS
SRQse-Fall(DQ)	SRQSEFALLDQ
SRQse-Rise(DQ)	SRQSERISEDQ
srr1	SRR1
srr2	SRR2
SSC Downspread(CK)	SSCDOWNSPREADCK
SSC Downspread(WCK)	SSCDOWNSPREADWCK
SSC Mod Freq(CK)	SSCMODFREQCK
SSC Mod Freq(WCK)	SSCMODFREQWCK

Table continued…

Measurement	Measurement PI name
SSC Profile(CK)	SSCPROFILECK
SSC Profile(WCK)	SSCPROFILEWCK
tAC-Diff	TACDIFF
tAH	TAH
tAPW	TAPW
tAS	TAS
tCCDRD	TCCDRD
tCCDWR	TCCDWR
tCH	TCH
tCH(abs)	TCHABS
tCH(avg)	TCHAVG
TCIPW-High	TCIPWHIGH
TCIPW-Low	TCIPWLOW
tCK	TCK
tCK(abs)	TCKABS
tCK(avg)	TCKAVG
tCKESR	TCKESR
tCKSRE	TCKSRE
tCKSRX	TCKSRX
tCL	TCL
tCL(abs)	TCLABS
tCL(avg)	TCLAVG
tCMDH	TCMDH
tCMDPW	TCMDPW
tCMDS	TCMDS
tDH(base)DQS(Informative)	TDHBASEDQS
tDH(derated)DQS(Informative)	TDHDERATEDDQS
tDH(DQS)(Informative)	TDHDQS
tDH-Diff(base)	TDHDIFFBASE
tDH-Diff(derated)	TDHDIFFDERATED
tDH-Diff(max-derated)(Informative)	TDHDIFFMAXDERATED
tDH-Diff(min-derated)(Informative)	TDHDIFFMINDERATED
tDH-Diff(Vref-based)	TDHDIFFVREFBASED
tIS(derated)	TISDERATED
tIH(derated)	TIHDERATED
TdIPW-High	TDIPWHIGH
TdIPW-Low	TDIPWLOW

Table continued…

Measurement	Measurement PI name
tDQS2DQ	TDQS2DQ
tDQSCK	TDQSCK
tDQSCK-Diff	TDQSCKDIFF
tDQSH	TDQSH
tDQSL	TDQSL
tDQSQ(DQS)	TDQSQDQS
tDQSQ(DQS)(Informative)	TDQSQDQS
tDQSQ-DBI	TDQSQDBI
tDQSQ-Diff	TDQSQDIFF
tDQSS	TDQSS
tDQSS(DQS)(Informative)	TDQSSDQS
tDQSS-Diff	TDQSSDIFF
tDS(base)DQS(Informative)	TDSBASEDQS
tDS(derated)DQS(Informative)	TDSDERATEDDQS
tDS(DQS)(Informative)	TDSDQS
tDS-Diff(base)	TDSDIFFBASE
tDS-Diff(derated)	TDSDIFFDERATED
tDS-Diff(max-derated)(Informative)	TDSDIFFMAXDERATED
tDS-Diff(min-derated)(Informative)	TDSDIFFMINDERATED
tDS-Diff(Vref-based)	TDSDIFFVREFBASED
tDSH(DQS)(Informative)	TDSHDQS
tDSH-Diff	TDSHDIFF
tDSS(DQS)(Informative)	TDSSDQS
tDSS-Diff	TDSSDIFF
tDVAC(CK)	TDVACCK
tDVAC(DQS)	TDVACDQS
tDVAC(DQS)(Informative)	TDVACDQS
tDVAC(WCK)	TDVACWCK
tERR(02per)	TERR2PER
tERR(03per)	TERR3PER
tERR(04per)	TERR4PER
tERR(05per)	TERR5PER
tERR(06per)	TERR6PER
tERR(07per)	TERR7PER
tERR(08per)	TERR8PER
tERR(09per)	TERR9PER
tERR(10per)	TERR10PER

Table continued…

Measurement	Measurement PI name
tERR(11-50per)	TERR11TO50PER
tERR(11per)	TERR11PER
tERR(12per)	TERR12PER
tERR(13per)	TERR13PER
tERR(14per)	TERR14PER
tERR(15per)	TERR15PER
tERR(16per)	TERR16PER
tERR(17per)	TERR17PER
tERR(18per)	TERR18PER
tERR(19per)	TERR19PER
tERR(20per)	TERR20PER
tERR(21per)	TERR21PER
tERR(22per)	TERR22PER
tERR(23per)	TERR23PER
tERR(24per)	TERR24PER
tERR(25per)	TERR25PER
tERR(26per)	TERR26PER
tERR(27per)	TERR27PER
tERR(28per)	TERR28PER
tERR(29per)	TERR29PER
tERR(30per)	TERR30PER
tERR(31per)	TERR31PER
tERR(32per)	TERR32PER
tERR(33per)	TERR33PER
tERR(34per)	TERR34PER
tERR(35per)	TERR35PER
tERR(36per)	TERR36PER
tERR(37per)	TERR37PER
tERR(38per)	TERR38PER
tERR(39per)	TERR39PER
tERR(40per)	TERR40PER
tERR(41per)	TERR41PER
tERR(42per)	TERR42PER
tERR(43per)	TERR43PER
tERR(44per)	TERR44PER
tERR(45per)	TERR45PER
tERR(46per)	TERR46PER

Table continued…

Measurement	Measurement PI name
tERR(47per)	TERR47PER
tERR(48per)	TERR48PER
tERR(49per)	TERR49PER
tERR(50per)	TERR50PER
tERR(6-10per)	TERR6TO10PER
tHP	THP
tHZ(DQ)	THZDQ
tHZ(DQS)	THZDQS
tIH(base)	TIHBASE
tIH(base)CA	TIHBASECA
tIH(base)CS	TIHBASECS
tIH(derated)	TIHDERATED
tIH(derated)CA	TIHDERATEDCA
tIH(derated)CS	TIHDERATEDCS
tIH(max-derated)(Informative)	TIHMAXDERATED
tIH(min-derated)(Informative)	TIHMINDERATED
tIH(Vref)	TIHVREF
tIH(Vref-based)	TIHVREFBASED
tIPW-High	TIPWHIGH
tIPW-High(CA)	TIPWHIGHCA
tIPW-High(CS)	TIPWHIGHCS
tIPW-Low	TIPWLOW
tIPW-Low(CA)	TIPWLOWCA
tIPW-Low(CS)	TIPWLOWCS
tIS(base)	TISBASE
tIS(base)CA	TISBASECA
tIS(base)CS	TISBASECS
tIS(derated)	TISDERATED
tIS(derated)CA	TISDERATEDCA
tIS(derated)CS	TISDERATEDCS
tIS(max-derated)(Informative)	TISMAXDERATED
tIS(min-derated)(Informative)	TISMINDERATED
tIS(Vref)	TISVREF
tIS(Vref-based)	TISVREFBASED
tJIT(cc)	TJITCC
tJIT(duty) Informative	TJITDUTY
tJIT(per)	TJITPER

Table continued…

Measurement	Measurement PI name
tLZ(DQ)	TLZDQ
tLZ(DQS#)	TLZDQSBAR
tPD	TPD
tPPD	TPPD
tQH	TQH
tQH_DBI	TQHDBI
tQSH	TQSH
tQSH_DBI	TQSHDBI
tQSL	TQSL
tQSL_DBI	TQSLDBI
tQW_Total	TQW
tQW_Total_DBI	TQWDBI
tRAS	TRAS
tRC	TRC
tRCDRD	TRCDRD
tRCDWR	TRCDWR
tRDPDE	TRDPDE
tRDSRE	TRDSRE
tREFTR(Read)	TREFTRREAD
tREFTR(Write)	TREFTRWRITE
tRFC	TRFC
tRP	TRP
tRP(ACT)	TRPACT
tRP(MRS)	TRPMRS
tRP(REF)	TRPREF
tRP(SRE)	TRPSRE
tRPRE	TRPRE
tRPST	TRPST
tRTP	TRTP
tRTPL	TRTPL
tVAC(Addr/Cmd)	TVACADDRCMD
tVAC(DQ)	TVACDQ
tWCK	TWCK
tWCK-DJ	TWCKDJ
tWCK-Fall-Slew	TWCKFALLSLEW
tWCKH	TWCKH
tWCKHP	TWCKHP

Table continued…

Measurement	Measurement PI name
tWCKL	TWCKL
tWCK-Rise-Slew	TWCKRISESLEW
tWCK-RJ	TWCKRJ
tWCK-TJ	TWCKTJ
tWPRE	TWPRE
tWPST	TWPST
tWRPDE	TWRPDE
tWRSRE	TWRSRE
tXSNRW	TXSNRW
tXSRRD	TXSRRD
tXSRWR	TXSRWR
VID(ac)	VIDAC
VIHdiff(AC)	VIHDIFFAC
VIHL_AC	VIHLAC
VIHL_AC(CA)	VIHLACCA
VIHDiffPeak	VIHDIFFPEAK
VIHdiff(AC) Informative	VIHDIFFACINFORMATIVE
VILdiff(AC)	VILDIFFAC
VILDiffPeak	VILDIFFPEAK
VILdiff(AC) Informative	VILDIFFACINFORMATIVE
VIN(CK#)	VINCKBAR
VIN(CK)	VINCK
VIN(WCK#)	VINWCKBAR
VIN(WCK)	VINWCK
Vix(ac)CK	VIXACCK
Vix(ac)DQS	VIXACDQS
Vix(ac)DQS(Informative)	VIXACDQS
Vix(ac)WCK	VIXACWCK
VIXCA	VIXCA
VIXDQ	VIXDQ
VOH(AC)DQ	VOHACDQ
VOH(AC)DQS	VOHACDQS
VOH(AC)DQS#	VOHACDQSBAR
VOH(DC)DQ	VOHDCDQ
VOH(DC)DQS	VOHDCDQS
VOH(DC)DQS#	VOHDCDQSBAR
VOH(WCK#)	VOHWCKBAR

Table continued…

Measurement	Measurement PI name
VOH(WCK)	VOHWCK
VOHdiff(AC)	VOHDIFFAC
VOL(AC)DQ	VOLACDQ
VOL(AC)DQS	VOLACDQS
VOL(AC)DQS#	VOLACDQSBAR
VOL(DC)DQ	VOLDCDQ
VOL(DC)DQS	VOLDCDQS
VOL(DC)DQS#	VOLDCDQSBAR
VOL(WCK#)	VOLWCKBAR
VOL(WCK)	VOLWCK
VOLdiff(AC)	VOLDIFFAC
Vox(ac)CK	VOXACCK
Vox(ac)DQS	VOXACDQS
VSEH(AC)CK	VSEHACCK
VSEH(AC)CK#	VSEHACCKBAR
VSEH(AC)DQS	VSEHACDQS
VSEH(AC)DQS#	VSEHACDQSBAR
VSEH(AC)DQS#(Informative)	VSEHACDQSBAR
VSEH(AC)DQS(Informative)	VSEHACDQS
VSEH(CK#)	VSEHCKBAR
VSEH(CK#)(Informative)	VSEHCKBAR
VSEH(CK)	VSEHCK
VSEH(CK)(Informative)	VSEHCK
VSEH(DQS#)	VSEHDQSBAR
VSEH(DQS#)(Informative)	VSEHDQSBAR
VSEH(DQS)	VSEHDQS
VSEH(DQS)(Informative)	VSEHDQS
VSEL(AC)CK	VSELACCK
VSEL(AC)CK#	VSELACCKBAR
VSEL(AC)DQS	VSELACDQS
VSEL(AC)DQS#	VSELACDQSBAR
VSEL(AC)DQS#(Informative)	VSELACDQSBAR
VSEL(AC)DQS(Informative)	VSELACDQS
VSEL(CK#)	VSELCKBAR
VSEL(CK#)(Informative)	VSELCKBAR
VSEL(CK)	VSELCK
VSEL(CK)(Informative)	VSELCK

Table continued…

Measurement	Measurement PI name
VSEL(DQS#)	VSELDQSBAR
VSEL(DQS#)(Informative)	VSELDQSBAR
VSEL(DQS)	VSELDQS
VSEL(DQS)(Informative)	VSELDQS
VSWING(MAX)CK	VSWINGMAXCK
VSWING(MAX)CK#	VSWINGMAXCKBAR
VSWING(MAX)DQS	VSWINGMAXDQS
VSWING(MAX)DQS#	VSWINGMAXDQSBAR
VWCK-SWING	VWCKSWING
WCKSlew-Fall(WCK#)	WCKSLEWFALLWCKBAR
WCKSlew-Fall(WCK)	WCKSLEWFALLWCK
WCKSlew-Rise(WCK#)	WCKSLEWRISEWCKBAR
WCKSlew-Rise(WCK)	WCKSLEWRISEWCK

DDRA:ADDMEASGroup (No Query Form)

This command selects/adds the measurement group specified as the argument filter file.

Syntax

`DDRA:ADDMEASGroup <"Measurement Group Name">`

Inputs

`<"Measurement Group Name">` specifies the actual measurement group name.

Outputs

NA

Examples

`DDRA:ADDMEASGroup "Data Pulse Width"` adds/selects all the measurements under measurement group Data Pulse Width.

DDRA:CLEARMeas (No Query Form)

This command clears all/selected measurement.

Syntax

`DDRA:CLEARMeas { ALL | <Measurement PI Name> }`

Inputs

`ALL` Clear all selected measurements

`<Measurement PI Name>` refer to *Measurements PI name mapping* in command `DDRA:ADDMeas`

Outputs

NA

Examples

DDRA:CLEARMeas ALL, clears all the selected measurements.

DDRA:SOURCE? (Query Only)

This command queries all the sources in use.

Syntax

DDRA:SOURCE?

Inputs

NA

Outputs

<SignalSource>: { CH1, CH2, CH3, CH4, MATH1, MATH2, MATH3, MATH4, REF1, REF2, REF3, REF4 }

Examples

DDRA:SOURCE? returns "CH1","CH2", which indicates currently used sources as CH1 and CH2.

DDRA:SOURCE:ADDRcmd

This command sets or gets the signal source assigned to Address/Command signal.

Syntax

DDRA:SOURCE:ADDRcmd <SignalSource>

DDRA:SOURCE:ADDRcmd?

Inputs

<SignalSource>: { CH1, CH2, CH3, CH4, MATH1, MATH2, MATH3, MATH4, REF1, REF2, REF3, REF4 }

Outputs

<SignalSource>

Examples

DDRA:SOURCE:ADDRcmd CH1, assigns the Address/Command signal with the source as CH1.

DDRA:SOURCE:ADDRcmd? returns CH2, which indicates an Address/Command signal is assigned with the signal source to CH2.

DDRA:SOURCE:CLOCK

This command sets or queries the signal source assigned to Clock signal.

Syntax

DDRA:SOURCE:CLOCK <SignalSource>

DDRA:SOURCE:CLOCK?

Inputs

<SignalSource>: { CH1, CH2, CH3, CH4, MATH1, MATH2, MATH3, MATH4, REF1, REF2, REF3, REF4 }

Outputs

<SignalSource>

Examples

DDRA:SOURCE:CLOCK CH1, assigns the Clock signal with the source as CH1.

DDRA:SOURCE:CLOCK? returns MATH1, which indicates the Clock signal is assigned with the signal source to MATH1.

DDRA:SOURCE:CLOCKBar

This command sets or queries the signal source assigned to Clock Bar signal.

Syntax

DDRA:SOURCE:CLOCKBar <SignalSource>

DDRA:SOURCE:CLOCKBar?

Inputs

<SignalSource>: { CH1, CH2, CH3, CH4, MATH1, MATH2, MATH3, MATH4, REF1, REF2, REF3, REF4 }

Outputs

<SignalSource>

Examples

DDRA:SOURCE:CLOCKBar CH1, assigns the Clock Bar signal with the source as CH1.

DDRA:SOURCE:CLOCKBar? returns CH4, which indicates the Clock Bar signal is assigned with the signal source to CH4.

DDRA:SOURCE:DATa

This command sets or queries the signal source assigned to Data signal.

DDRA:SOURCE:DATa <SignalSource>

DDRA:SOURCE:DATa?

<SignalSource>:{ CH1, CH2, CH3, CH4, MATH1, MATH2, MATH3, MATH4, REF1, REF2, REF3, REF4 }

Outputs

<SignalSource>

Examples

DDRA:SOURCE:DATa CH1, assigns the Data signal with the source as CH1.

DDRA:SOURCE:DATa? returns CH2, which indicates the Data signal is assigned with the signal source to CH2.

DDRA:SOURCE:STROBE

This command sets or queries the signal source assigned to Strobe signal.

Syntax

DDRA:SOURCE:STROBE <SignalSource>

DDRA:SOURCE:STROBE?

Inputs

<SignalSource>: { CH1, CH2, CH3, CH4, MATH1, MATH2, MATH3, MATH4, REF1, REF2, REF3, REF4 }

Outputs

<SignalSource>

Examples

DDRA:SOURCE:STROBE CH1, assigns the Strobe signal with the source as CH1.

DDRA:SOURCE:STROBE? return CH3, which indicates the Strobe signal is assigned with the signal source to CH3.

DDRA:SOURCE:STROBEBar

This command sets or queries the signal source assigned to Strobe Bar (DQS#) signal.

Syntax

DDRA:SOURCE:STROBEBar <SignalSource>

DDRA:SOURCE:STROBEBar?

Inputs

<SignalSource>: { CH1, CH2, CH3, CH4, MATH1, MATH2, MATH3, MATH4, REF1, REF2, REF3, REF4 }

Outputs

<SignalSource>

Examples

DDRA:SOURCE:STROBEBar CH1, assigns the Strobe Bar (DQS#) signal with the source as CH1.

DDRA:SOURCE:STROBEBar? returns REF4, which indicates the Strobe Bar (DQS#) signal is assigned with the signal source to REF4.

DDRA:SOURCE:WCK

This command sets or queries the signal source assigned to WCK signal.

Syntax

DDRA:SOURCE:WCK <SignalSource>

DDRA:SOURCE:WCK?

Inputs

<SignalSource>: { CH1, CH2, CH3, CH4, MATH1, MATH2, MATH3, MATH4, REF1, REF2, REF3, REF4 }

Outputs

<SignalSource>

Examples

DDRA:SOURCE:WCK CH1, assigns the WCK signal with the source as CH1.

DDRA:SOURCE:WCK? returns CH2, which indicate the WCK signal is assigned with the signal source to CH2.

DDRA:SOURCE:WCKBar

This command sets or queries the signal source assigned to WCK Bar (WCK#) signal.

Syntax

`DDRA:SOURCE:WCKBar <SignalSource>`

`DDRA:SOURCE:WCKBar?`

Inputs

`<SignalSource>`: { CH1, CH2, CH3, CH4, MATH1, MATH2, MATH3, MATH4, REF1, REF2, REF3, REF4 }

Outputs

<SignalSource>

Examples

`DDRA:SOURCE:WCKBar CH1`, assigns the WCK Bar (WCK#) signal with the source as CH1.

`DDRA:SOURCE:WCKBar?` returns REF2, which indicates the WCK Bar (WCK#) signal is assigned with the signal source to REF2.

DDRA:TCKAVG

This command sets or queries the tck(avg) value in seconds.

Syntax

`DDRA:TCKAVG {<NR2> | <NR3>}`

`DDRA:TCKAVG?`

Inputs

`<NR2> or <NR3>` is the tck(avg) value in seconds and can be a floating point with or without exponent.

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:TCKAVG 3.7523E-9`, sets the tck(avg) value to 3.7523 ns

`DDRA:TCKAVG?` returns 3.7523E-9, which indicates the tck(avg) value is set to 3.7523E-9 seconds.

DDRA:TIMINGMode

This command sets or queries the Timing Mode value.

Syntax

`DDRA:TIMINGmode { 1 | 2 }`

`DDRA:TIMINGmode?`

Inputs

`1` is 1T

`2` is 2T

Outputs

{ 1 | 2 }

Examples

`DDRA:TIMINGmode 2`, sets the Timing Mode value to 2T.

`DDRA:TIMINGmode?` returns 1T, which indicates the Timing Mode value is set to 1T.

Note: Applicable for DDR3, DDR3L, DDR4 Address/Command measurements.

DDRA:RXMASKFile

This command sets or queries the RX Mask file path.

Syntax

`DDRA:RXMASKFile <file path>`

`DDRA:RXMASKFile?`

Inputs

`<file path>` is an absolute file path of mask file.

Outputs

<file path>

Examples

`DDRA:RXMASKFile "C:\Users\Public\Tektronix\TekApplications\DDRA\Masks \LPDDR4.msk"`, sets the file path for RX Mask as "C:\Users\Public\Tektronix\TekApplications\DDRA\Masks \LPDDR4.msk".

`DDRA:RXMASKFile?` returns and indicates the mask file path is set to "C:\Users\Public\Tektronix\TekApplications \DDRA\Masks\LPDDR4.msk" .

DDRA:MASKMARGIN

This command queries the value for TdiVW and VdiVW.

Syntax

`DDRA:MASKMARGIN?`

Inputs

`NA`

Outputs

<NR3>

Examples

`DDRA:MASKMARGIN?` returns TdiVW in ps and VdiVW in volts.

DDRA:MASKMARGINTIME

This command queries the values of time mask margin.

Syntax

DDRA:MASKMARGINTIME?

Inputs

NA

Outputs

<NR3>

Examples

DDRA:MASKMARGINTIME? returns the time mask margin T1, T2, T3, and T4 in seconds.

DDRA:MASKMARGINVOLTAGE

This command queries the values of voltage mask margin.

Syntax

DDRA:MASKMARGINVOLTAGE?

Inputs

NA

Outputs

<NR3>

Examples

DDRA:MASKMARGINVOLTAGE? returns the voltage mask margin V1, V2, V3, and V4 in volts.

DDRA:DATAMASKPLACEMENT

This command sets the ‘Mask’ position in LPDDR4 or LPDDR4X Write Burst ‘Data Eye’ measurement ‘DDRARXMask’. The 'Data Mask Placement' can be set between DQS-Crossing / Data Center.

Syntax

DDRA:DATAMASKPLACEMENT { CENTER |DQSCROSSING}

DDRA:DATAMASKPLACEMENT?

Inputs

DQSCROSSING: To get the mask at the DQS Crossing.

CENTER: To get the mask at the data center.

Outputs

{ CENTER | DQSCROSSING}

Examples

DDRA:DATAMASKPLACEMENT CENTER, sets mask at the Data Center.

DDRA:DATAMASKPLACEMENT? returns DQSCROSSING, which indicates the mask position is set to DQSCROSSING. By default, the mask placement sets at DQS crossing.

DDRA:MEASGrouping

This command sets or queries the feature status - Enable back-to-back burst detection.

Syntax

`DDRA:BACKTOBAckburst { 1 | 0 }`

`DDRA:BACKTOBAckburst?`

Inputs

`1`: enables the Enable back-to-back burst detection feature.

`0`: disables the Enable back-to-back burst detection feature.

Outputs

{ 1 | 0 }

Examples

`DDRA:BACKTOBAckburst 1`, sets the Enable back-to-back burst detection check box.

`DDRA:BACKTOBAckburst?` returns 0, which indicates the Enable back-to-back burst detection is disabled.

DDRA:RESULTJEDECunit

This command sets or queries the feature status - Measurements result unit as per JEDEC specification.

Syntax

`DDRA:RESULTJEDECunit { 1 | 0 }`

`DDRA:RESULTJEDECunit?`

Inputs

`1`: enables the feature; Measurements result unit as per JEDEC specification.

`0`: disables the feature; Measurements result unit as per JEDEC specification.

Outputs

{ 1 | 0 }

Examples

`DDRA:RESULTJEDECunit 1`, enables the Measurements result unit as per JEDEC specification.

`DDRA:RESULTJEDECunit?` returns 0, which indicates the Measurements result unit as per JEDEC specification is disabled.

DDRA:SPECREVISION

This command sets or queries the JEDEC specification revision for DDR4/LPDDR4.

Syntax

`DDRA:SPECREVISION <bool value>`

`DDRA:SPECREVISION?`

Inputs

0: Uncheck

1: Check

Outputs

0 | 1

Examples

`DDRA:SPECREVISION 0`, uncheck the JEDEC specification revision for DDR4/LPDDR4.

`DDRA:SPECREVISION?` returns 1, checks the JEDEC specification revision for DDR4/LPDDR4.

Note: Applicable for DDR4, LPDDR4 measurements.

DDRA:VDQSMID

This command sets or queries the VDQS_Mid value in volts.

Syntax

`DDRA:VDQSMID {<NR2> | <NR3>}`

`DDRA:VDQSMID?`

Inputs

`<NR2>, <NR3>` is VDQS_MID value in volts and can be floating point value with or without exponent.

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:VDQSMID 500.00E-3`, sets the VDQSMID value to 500 mV.

`DDRA:VDQSMID?` returns 500.0000E-3, which indicates the current VDQSMid value is set to 500 mV.

Note: Applicable for DDR4 measurements.

Burst Detection Method commands

DDRA:BURSTDETectmethod

This command sets or queries the Burst Detection Method.

Syntax

`DDRA:BURSTDETectmethod { DQDQS | CHIPselect | LOGICstate | VISUALSEARCH | NONE }`

`DDRA:BURSTDETectmethod?`

Inputs

`DQDQS` - DQ/DQS Phase Alignment

`CHIPselect` - Chip Select, Latency + DQ/DQS Phase Alignment

`LOGICstate` - Logic State + Burst Latency

`VISUALSEARCH` - Visual Search

`NONE` - None

Outputs

{ DQDQS | CHIPselect | LOGICstate | VISUALSEARCH | NONE }

Examples

`DDRA:BURSTDETectmethod DQDQS`, sets the Burst detection method to DQ/DQS Phase Alignment.

`DDRA:BURSTDETectmethod?` returns DQ/DQS, which indicates the Burst detection method is set to DQ/DQS Phase Alignment.

DDRA:TDQS2DQMode

This command sets or queries the status of tDQS2DQ mode.

Syntax

`DDRA:TDQS2DQMode { Auto | UserDefined }`

`DDRA:TDQS2DQMode?`

Inputs

`Auto` - application will automatically set the tDQS2DQ value in seconds.

`UserDefined` - will allow the user to set the value for tDQS2DQ in seconds.

Outputs

{ Auto | UserDefined }

Examples

`DDRA:TDQS2DQMode Auto`, sets the tDQS2DQ to Automatic mode and the value will be calculated by application.

`DDRA:TDQS2DQMode?` returns UserDefined, which indicates the tDQS2DQ value is set to UserDefined mode.

Note: Applicable for LPDDR4 measurements.

DDRA:TDQS2DQ

This command sets or queries the tDQS2DQ value in seconds.

Syntax

`DDRA:TDQS2DQ {<NR2> | <NR3>}`

`DDRA:TDQS2DQ?`

Inputs

`<NR2> or <NR3>` is the tDQS2DQ value in seconds and can be a floating point with or without exponent.

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:TDQS2DQ 5e-9`, sets the tDQS2DQ to 5 ns.

`DDRA:TDQS2DQ?` returns 5.0000E-9, which indicates the tDQS2DQ value is set to 5.0000E-9 seconds (5 ns).

Note: Applicable for LPDDR4, LPDDR4X measurements.

DDRA:BURSTIDMethod

This command sets or queries the Burst Identification method.

Syntax

`DDRA:BURSTIDMethod { PREAMPattern | AMPBased | EDGECountbased}`

`DDRA:BURSTIDMethod?`

Inputs

`PREAMPattern` - Preamble Pattern Matching

`AMPBased` - Amplitude Based

`EDGECountbased` - Edge Count Based

Outputs

{ PREAMPattern | AMPBased | EDGECountbased}

Examples

`DDRA:BURSTIDMethod AMPBased`, sets the Burst Identificaiton method to Preamble Pattern Matching.

`DDRA:BURSTIDMethod?` returns EDGECountbased, which indicates the Burst Identification method is set to Edge Count Based.

Note: Applicable for LPDDR4 measurements.

DDRA:ISOLBurstlen

This command sets or queries the Isolated Burst Length (UI) value for Preamble Pattern Matching.

Syntax

`DDRA:ISOLBurstlen { 8 | 16 | 32 }`

`DDRA:ISOLBurstlen?`

Inputs

`8, 16, 32`: Represents the isolated burst length.

Outputs

{ 8 | 16 | 32 }

Examples

`DDRA:ISOLBurstlen 16`, sets the isolated burst length to 16 bit.

`DDRA:ISOBurstlen?` returns 8, which indicates the isolated burst length is set to 8 bit.

Note: Applicable for LPDDR4, LPDDR4X measurements.

DDRA:BURSTMatch

This command sets or queries the Burst Match percentage for Preamble Pattern matching burst identification method.

Syntax

`DDRA:BURSTMatch <NR2>`

`DDRA:BURSTMatch?`

Inputs

`<NR2>` - burst match percentage value between 0 and 100.

Outputs

<NR2>

Examples

`DDRA:BURSTMatch 75`, sets match to 75%

`DDRA:BURSTMatch?` returns 82.0000, which indicates the Burst match is set to 82%

Note: Applicable for LPDDR4, LPDDR4X measurements.

DDRA:BURSTPK2Pk

This command sets or queries the Write Burst(pk-pk) in volts for Amplitude Based burst identification method.

Syntax

`DDRA:BURSTPK2Pk {<NR2> | <NR3>}`

`DDRA:BURSTPK2Pk?`

Inputs

`<NR2> or <NR3>` - Write Burst(pk-pk) value in volts and can be a floating point with or without exponent.

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:BURSTPK2Pk 0.7`, sets Write Burst(pk-pk) to 700 mV

`DDRA:BURSTPK2Pk?` returns 700.0000E-3, which indicates the Write Burst pk-pk value is set to 700 mV.

Note: Applicable for LPDDR4, LPDDR4X measurements.

DDRA:AMPBasedmargin

This command sets or queries the margin percentage value for the Amplitude Based Burst identification method.

Syntax

`DDRA:AMPBasedmargin {<NR2> | <NR3>}`

```
DDRA:AMPBasedmargin?
```

Inputs

<NR2> or <NR3> is the margin percentage value.

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:AMPBasedmargin 4.5`, sets the margin value to 4.5%.

`DDRA:AMPBasedmargin?` returns 2.5000, which indicates the margin percentage value is set to 2.5%.

Note: Applicable for LPDDR4, LPDDR4X measurements.

DDRA:WRITEAmpgtread

This command sets or queries the Boolean value, when the WRITE burst (pk-pk) amplitude greater than READ burst (pk-pk) amplitude for Amplitude Based burst identification method.

Syntax

```
DDRA:WRITEAmpgtread { 0 | 1 }
DDRA:WRITEAmpgtread?
```

Inputs

`0` - No

`1` - Yes

Outputs

{ 0 | 1 }

Examples

`DDRA:WRITEAmpgtread 1`, sets Yes; the WRITE burst (pk-pk) amplitude greater than READ burst (pk-pk) amplitude.

`DDRA:WRITEAmpgtread?` returns 0, which indicates the value for WRITE burst (pk-pk) amplitude greater than READ burst (pk-pk) amplitude is set to No.

Note: Applicable for LPDDR4, LPDDR4X measurements.

DDRA:PREAmbletype

This command sets or queries the Preamble Type for Read measurements.

Syntax

```
DDRA:PREAmbletype { Static | Toggle }
DDRA:PREAmbletype?
```

Inputs

`Static` - Static

`Toggle` - Toggle

Outputs

{ Static | Toggle }

Examples

`DDRA:PREAmbletype Toggle`, sets the Preamble Type as TOGGLE.

`DDRA:PREAmbletype?` returns Static, which indicates the Preamble Type is set to Static.

Note: Applicable for LPDDR4, LPDDR4X measurements.

DDRA:READPOSTamble

This command sets or queries the Read Postamble Length (tCK).

Syntax

`DDRA:READPOSTamble { 0.5 | 1.5 }`

`DDRA:READPOSTamble?`

Inputs

`{ 0.5 | 1.5 }` in tCK

Outputs

{ 0.5 | 1.5 }

Examples

`DDRA:READPOSTamble 0.5`, sets the Read Postamble Length to 0.5 tCK

`DDRA:READPOSTamble?` returns 500.0000E-3, which indicates the Read Postamble Length is set to 0.5 tCK

Note: Applicable for LPDDR4, LPDDR4X measurements.

DDRA:WRITEPOSTamble

This command sets or queries the Write Postamble Length (tCK).

Syntax

`DDRA:WRITEPOSTamble { 0.5 | 1.5 }`

`DDRA:WRITEPOSTamble?`

Inputs

`{ 0.5 | 1.5 }` in tCK

Outputs

{ 0.5 | 1.5 }

Examples

`DDRA:WRITEPOSTamble 0.5`, sets the Write Postamble Length to 0.5 tCK.

`DDRA:WRITEPOSTamble?` returns 500.0000E-3, which indicates the Write Postamble Length is set to 0.5 tCK.

Note: Applicable for LPDDR4, LPDDR4X measurements.

DDRA:APPLYBurstconfig (No Query Form)

This command applies the Burst detection configurations.

Syntax

`DDRA:APPLYBurstconfig`

Inputs

NA

Outputs

NA

Examples

`DDRA:APPLYBurstconfig` applies the Burst identification settings done by the user.

Note: Applicable for LPDDR4, LPDDR4X measurements.

DDRA:DDR4:READPREAMBLELENGTH

This command sets or queries the read preamble length for DDR4.

Syntax

`DDRA:DDR4:READPREAMBLELENGTH <value>`

`DDRA:DDR4:READPREAMBLELENGTH?`

Inputs

1, 2

Outputs

1 | 2

Examples

`DDRA:DDR4:READPREAMBLELENGTH 1`, sets the read preamble length to 1.

`DDRA:DDR4:READPREAMBLELENGTH?` returns 2, which indicates the read preamble length is set to 2.

DDRA:DDR4:WRITEPREAMBLELENGTH

This command sets or queries the write preamble length for DDR4.

Syntax

`DDRA:DDR4:WRITEPREAMBLELENGTH <value>`

`DDRA:DDR4:WRITEPREAMBLELENGTH?`

Inputs

1, 2

Outputs

1 | 2

Examples

`DDRA:DDR4:WRITEPREAMBLELENGTH 2`, sets the write preamble length to 2.

`DDRA:DDR4:WRITEPREAMBLELENGTH?` returns 1, which indicates the write preamble length is set to 1.

DDRA:DDR4:APPLYBURSTCONFIG

This command sets the burst detection settings configured for DDR4 generation.

Syntax

`DDRA:DDR4:APPLYBURSTCONFIG`

Inputs

NA

Outputs

NA

Examples

`DDRA:DDR4:APPLYBURSTCONFIG` applies the burst identification settings done by the user.

Note: Applicable for DDR4 measurements.

Burst Detection Settings commands

DDRA:BURSTLevelmode

This command sets or queries the DQ/DQS Levels mode.

Syntax

`DDRA:BURSTLEVELmode { AUTO | MANUAL }`

`DDRA:BURSTLEVELmode?`

Inputs

`AUTO` - sets the Burst level to Automatic mode.

`MANUAL` - sets the Burst level to Manual mode.

Outputs

{ AUTO | MANUAL }

Examples

`DDRA:BURSTLEVELmode AUTO`, sets the DQ/DQS Levels mode to Automatic.

`DDRA:BURSTLEVELmode?` returns MANUAL, which indicates the DQ/DQS Levels mode is set to MANUAL.

DDRA:DQDQSLEVELSTAtus? (Query Only)

This command queries the DQ/DQS Levels status.

Syntax

`DDRA:DQDQSLEVELSTAtus?`

Inputs

NA

Outputs

Provides the DQ/DQS level status.

Examples

`DDRA:DQDQSLEVELSTAtus?`, returns AUTO and indicates the DQ/DQS Levles status is set to Automatic.

DDRA:STROBEHIGH

This command sets or queries the Strobe High value in volts for DQ/DQS Levels.

Syntax

`DDRA:STROBEHIGH <NR3>`

`DDRA:STROBEHIGH?`

Inputs

`<NR3>` - floating value

Outputs

<NR3>

Examples

`DDRA:STROBEHIGH 0.9`, sets the Strobe High value to 900 mV.

`DDRA:STROBEHIGH?` returns 900.0000E-3, which indicates the Strobe High value is set to 900 mV.

DDRA:STROBEMID

This command sets or queries the Strobe Mid value in volts for DQ/DQS Levels.

Syntax

`DDRA:STROBEMID <NR3>`

`DDRA:STROBEMID?`

Inputs

`<NR3>` - floating value

Outputs

<NR3>

Examples

`DDRA:STROBEMID -0.081`, sets the Strobe Mid value to -81 mV

DDRA:STROBEMID? returns -81.0000E-3, which indicates the Strobe Mid value is set to -81 mV

DDRA:STROBELOW

This command sets or queries the Strobe Low value in volts for DQ/DQS Levels.

Syntax

DDRA:STROBELOW <NR3>

DDRA:STROBELOW?

Inputs

<NR3> - floating value

Outputs

<NR3>

Examples

DDRA:STROBELOW -1.1, sets the Strobe Low value to -1.10 V

DDRA:STROBELOW? returns -1.1000, which indicates the Strobe Low value is set to -1.1 V

DDRA:DATAHIGH

This command sets or queries the Data High value in volts for DQ/DQS Levels.

Syntax

DDRA:DATAHIGH <NR3>

DDRA:DATAHIGH?

Inputs

<NR3> - floating value

Outputs

<NR3>

Examples

DDRA:DATAHIGH 1.2, sets the Data High value to 1.2 V.

DDRA:DATAHIGH? returns 1.2000, which indicates the Data High value is set to 1.2 V.

DDRA:DATAMID

This command sets or queries the Data Mid value in volts for DQ/DQS Levels.

Syntax

DDRA:DATAMID <NR3>

DDRA:DATAMID?

Inputs

<NR3> - floating value

Outputs

<NR3>

Examples

DDRA:DATAMID 600E-3, sets the Data Mid value to 600 mV.

DDRA:DATAMID? returns 600.0000E-3, which indicates the Data Mid value is set to 600 mV.

DDRA:DATALOW

This command sets or queries the Data Low value in volts for DQ/DQS Levels.

Syntax

DDRA:DATALOW <NR3>

DDRA:DATALOW?

Inputs

<NR3> - floating value

Outputs

<NR3>

Examples

DDRA:DATALOW 0.04, sets the Data Low value to 4 mV.

DDRA:DATALOW? returns 4.0000E-3, which indicates the Data Low value is set to 4 mV.

DDRA:ADVBURSTLevelmode

This command sets or queries the DQ/DQS Advanced Burst Levels mode.

Syntax

DDRA:ADVBURSTLevelmode { AUTO | MANUAL }

DDRA:ADVBURSTLevelmode?

Inputs

AUTO - sets the advanced burst level to Automatic mode.

MANUAL - sets the advanced burst level to Manual mode.

Outputs

{ AUTO | MANUAL }

Examples

DDRA:ADVBURSTLevelmode AUTO, sets the DQ/DQS Advanced Burst Levels mode to Automatic.

DDRA:ADVBURSTLevelmode? returns MANUAL, which indicates the DQ/DQS Advanced Burst Levles mode is set to MANUAL .

DDRA:HYSTEREsis

This command sets or queries the Edge Detection Hysteresis.

Syntax

DDRA:HYSTEREsis <NR3>

DDRA:HYSTEREsis?

Inputs

<NR3> - floating point value between 0 and 50.

Outputs

<NR3>

Examples

DDRA:HYSTEREsis 8, set the Edge Detection Hysteresis to 8%.

DDRA:HYSTEREsis? returns 30.0000, which indicates the Edge Detection Hysteresis is set to 30%.

DDRA:MARGIN

This command sets or queries the Termination Logic Margin.

Syntax

DDRA:MARGin <NR3>

DDRA:MARGin?

Inputs

<NR3> - floating point value between 0 and 100.

Outputs

<NR3>

Examples

DDRA:MARGin 5, sets the Termination Logic Margin to 5%.

DDRA:MARGin? returns 1.5000, which indicates the Termination Margin Logic is set to 15%.

DDRA:CSSOUrce

This command sets or queries the signal source for Chip Select Source.

Syntax

DDRA:SOURCE:CSSOUrce <SignalSource>

DDRA:SOURCE:CSSOUrce?

Inputs

<SignalSource>: { CH1, CH2, CH3, CH4, MATH1, MATH2, MATH3, MATH4, REF1, REF2, REF3, REF4 }

Outputs

<SignalSource>

Examples

DDRA:SOURCE:CSSOUrce CH1, assigns the Chip Select Source signal with the source as CH1.

DDRA:SOURCE:CSSOUrce? returns CH2, which indicates the Chip Select Source signal is assigned with the signal source to CH2.

Note: Applicable for Chip Select burst detection method.

DDRA:CASMIN

This command sets or queries the CAS Min(Cyc) value.

Syntax

DDRA:CASMIN <NR3>

DDRA:CASMIN?

Inputs

<NR3> - float value

Outputs

<NR3>

Examples

DDRA:CASMIN 2, assigns the CAS Min(Cyc) value to 2.

DDRA:CASMIN? returns 2, which indicates the CAS Min(Cyc) value is set to 2.

Note: Applicable for Chip Select burst detection method.

DDRA:CASMAX

This command sets or queries the CAS Max(Cyc) value.

Syntax

DDRA:CASMAX <NR3>

DDRA:CASMAX?

Inputs

<NR3> - floating point value

Outputs

<NR3>

Examples

DDRA:CASMAX 800, assigns the CAS Min(Cyc) value to 800.

DDRA:CASMAX? returns 300, which indicates the CAS Min(Cyc) value is set to 300.

Note: Applicable for Chip Select burst detection method.

DDRA:CSMOde

This command sets or queries the signal source for Chip Select Mode.

Syntax

DDRA:CSMOde { AUTO | MANUAL}

DDRA:CSSMOde?

Inputs

AUTO - Automatic

MANUAL - Manual

Outputs

{ AUTO | MANUAL}

Examples

DDRA:CSMOde AUTO, assigns the Chip Select Mode to Automatic.

DDRA:CSMOde? returns MANUAL, which indicates the Chip Select Mode is set to MANUAL.

Note: Applicable for Chip Select burst detection method .

DDRA:CSLEvel

This command sets or queries the Chip Select Voltage Level in volts.

Syntax

DDRA:CSLEvel <NR3>

DDRA:CSLEvel?

Inputs

<NR3> floating point value between -50 V to 50 V

Outputs

<NR3>

Examples

DDRA:CSLEvel 1, assigns the CS Level to 1 V.

DDRA:CSLEvel? returns 6.0000, which indicates the Chip Select Voltage Level is set to 6 V.

Note: Applicable for Chip Select burst detection method.

DDRA:CSACTive

This command sets or queries the signal source for Chip Select Mode.

Syntax

DDRA:CSACTive { H | L }

DDRA:CSACTive?

Inputs

L - Low

H - High

Outputs

{H|L}

Examples

DDRA:CSACTive H, sets the Chip Select Active Mode to High.

DDRA:CSACTive? returns H, which indicates the Chip Select Active Mode is set to low.

Note: Applicable for Chip Select burst detection method.

DDRA:BUS

This command sets or queries the Bus.

Syntax

DDRA:BUS {<BusName>}

DDRA:BUS?

Inputs

<BusName> - { B1 to B16 }

Outputs

{<BusName>}

Examples

DDRA:BUS B1, sets the Bus to B1 for measurement execution.

DDRA:BUS? returns B5, which indicates the Bus B5 is configured for measurement execution.

Note: Applicable for Logic State burst detection method. Bus Configurations has to be done before assignment.

DDRA:SYMBOLFile

This command sets or queries the symbol file path for selected Bus.

Syntax

DDRA:SYMBOLFile {<FilePath>}

DDRA:SYMBOLFile?

Inputs

<FilePath> - Symbol file path which is used for the configured and selected Bus.

Outputs

{<FilePath>}

Examples

DDRA:SYMBOLFile "C:\Users\Public\Tektronix\TekScope\BusDecodeTables\DDR\DDR3 Commands.tsf", sets Symbol file for selected Bus as DDR3 Commands.tsf.

DDRA:SYMBOLFile? returns the selected symbol file path as "C:\Users\Public\Tektronix\TekScope\BusDecodeTables\DDR\DDR Commands.tsf".

Note: Applicable for Logic State burst detection method. Bus Configurations and selection has to be done before.

DDRA:LOGICTrigger

This command sets or queries the symbol value to be triggered for the selected bus.

Syntax

DDRA:LOGICTrigger <TriggerAt>

DDRA:LOGICTrigger?

Inputs

<TriggerAt>: { WRITE, READ, DESELECT, PRECHARGE, REFRESH, MODE_REG, ACTIVATE, NOP … }

Outputs

<TriggerAt>

Examples

DDRA:LOGICTrigger WRITE, sets the symbol to be triggered at WRITE for the selected bus.

DDRA:LOGICTrigger? returns READ, which indicates the user selected trigger value for the selected bus is set to READ.

DDRA:BURSTLAtency

This command sets or queries the Burst Latency Cycle.

Syntax

DDRA:BURSTLAtency <NR3>

DDRA:BURSTLAtency?

Inputs

<NR3> floating point value between -1 to 100 Cycle

Outputs

<NR3>

Examples

DDRA:BURSTLAtency 2.5, sets the burst latency with 2.5 Cycle

DDRA:BURSTLAtency? returns 3.5000, which indicates the burst latency is set to 3.5 Cycle.

Note: Applicable for Logic State burst detection method.

DDRA:BURSTTOlerance

This command sets or queries the Burst Tolerance Cycle.

Syntax

`DDRA:BURSTTOlerance <NR3>`

`DDRA:BURSTTOlerance?`

Inputs

`<NR3>` floating point value between -1 to 100 Cycles

Outputs

<NR3>

Examples

`DDRA:BURSTTOlerance 1`, sets the burst tolerance with 1 Cycle.

`DDRA:BURSTTOlerance?` returns 3.0000, which indicates the burst tolerance is set to 3 Cycles.

Note: Applicable for Logic State burst detection method.

DDRA:BURSTLEngth

This command sets or queries the Burst Length UI.

Syntax

`DDRA:BURSTLEngth <NR3>`

`DDRA:BURSTLEngth?`

Inputs

`<NR3>` floating point value between -1 to 100 UI

Outputs

<NR3>

Examples

`DDRA:BURSTLEngth 8`, sets the burst length to 8 UI.

`DDRA:BURSTLEngth?` returns 6.0000, which indicates the burst length is set to 6 UI.

Note: Applicable for Logic State burst detection method.

Threshold and Scaling commands

DDRA:MEASTHRESholdmode

This command sets or queries the Measurements Thresholds mode.

Syntax

`DDRA:MEASTHRESholdmode { AUTO | MANUAL }`

`DDRA:MEASTHRESholdmode?`

Inputs

AUTO - sets the Measurements Thresholds to Automatic mode.

MANUAL - sets the Measuremetns Thresholds to Manual mode.

Outputs

{ AUTO | MANUAL }

Examples

DDRA:MEASTHRESholdmode AUTO, sets the Measurements Thresholds mode to Automatic.

DDRA:MEASTHRESholdmode? returns MANUAL, which indicates the Measurements Thresholds mode is set to MANUAL.

DDRA:ALTernatethresholds

This command sets or queries the Alternate Threshold value.

Syntax

DDRA:ALTernatethresholds {<AlternateThreshold>}

DDRA:ALTernatethresholds?

Inputs

<AlternateThreshold>: { AC160, AC135, AC130, AC175, AC150, AC125, AC220, AC300 }

Outputs

{<AlternateThreshold>}

Examples

DDRA:ALTernatethresholds AC160, sets the alternate threshold to AC160.

DDRA:ALTernatethresholds? returns AC125, which indicates the selected alternate threshold value is set to AC125.

DDRA:HORIzontalscaling

This command sets or queries the status for Auto Horizontal Scaling.

Syntax

DDRA:HORIzontalscaling { 0 | 1 }

DDRA:HORIzontalscaling?

Inputs

0 - disabled

1 - enabled

Outputs

{ 0 | 1 }

Examples

DDRA:HORIzontalscaling 1, enables the Auto Horizontal Scaling.

`DDRA:HORIzontalscaling?` returns 0, which indicates the Auto Horizontal Scaling is disabled.

DDRA:VERTicalscaling

This command sets or queries the status for Auto Vertical Scaling.

Syntax

```
DDRA:VERTicalscaling { 0 | 1 }
DDRA:VERTicalscaling?
```

Inputs

`0` - disabled

`1` - enabled

Outputs

{ 0 | 1 }

Examples

`DDRA:VERTicalscaling 1`, enables the Auto Vertical Scaling.

`DDRA:VERTicalscaling?` returns 0, which indicates the Auto Vertical Scaling is disabled.

Interposer Filter commands

DDRA:FLTtype

This command sets or queries the Interposer Filter type.

Syntax

```
DDRA:FILTERType { "None" | "UserDefined" | "DirectAttached" | <QString> }
DDRA:FILTERType?
```

Inputs

`"None", "UserDefined", "DirectAttached", <QString>`

Outputs

{ "None" | "UserDefined" | "DirectAttached" | <QString> }

Examples

`DDRA:FILTERType "UserDefined"`, sets the Interposer filter type as UserDefined.

`DDRA:FILTERType?` returns "DirectAttached", which indicates the interposer filter type is set to DirectAttached.

DDRA:FILTERFile

This command sets or queries the Interposer Filter file for the specified signal type.

Syntax

```
DDRA:FILTERFile <SignalType>,<FilterPath>
DDRA:FILTERFile? <SignalType>
```

Inputs

<SignalType> is the signal type values; { DIFFDQS | DIFFCK | DIFFWCK | SEDQS | SEDQSBAR | DQ | ADDRCMD | SECK | SECKBAR | SEWCK | SEWCKBAR }

<FilterPath> is the absolute path of the filter file.

Outputs

<FilterPath>

Examples

DDRA:FILTERFile DIFFDQS,"C:\Users\Public\Filters\GDDR5\UserDefined\SingleEnded\GDDR5MCI_DS-SE-SIM_renorm_read_8GHz.flt" , assigns the Differential DQS signal with the filter "C:\Users\Public\Filters\GDDR5\UserDefined\SingleEnded\GDDR5MCI_DS-SE-SIM_renorm_read_8GHz.flt" filter.

DDRA:FILTERFile? DIFFDQS returns and indicates the Differential DQS signal is assigned with the filter "C:\Users\Public\Filters\GDDR5\UserDefined\SingleEnded\GDDR5MCI_DS-SE-SIM_renorm_read_8GHz.flt".

DDRA:CLEARFILTERfile (No Query Form)

This command clears all or associated filter file with the specified signal type.

Syntax

DDRA:CLEARFILTERfile <SignalType>

Inputs

<SignalType>: { DIFFDQS, DIFFCK DIFFWCK, SEDQS, SEDQSBAR, DQ, ADDRCMD, SECK, SECKBAR, SEWCK, SEWCKBAR, ALL }

Outputs

NA

Examples

DDRA:CLEARFILTERfile DIFFDQS, clears the filter file associated with Differential DQS signal.

DDRA:CLEARFILTERfile ALL, clears all the filter files associated with all signal types.

Generation Rate and Levels commands

DDRA:GENeration

This command sets or queries the Generation.

Syntax

DDRA:GENEeration { DDR | DDR2 | DDR3 | DDR3L | DDR4 | LPDDR | LPDDR2 | LPDDR3 |LPDDR4 | LPDDR4X | GDDR3 | GDDR5 }

DDRA:GENEration?

Inputs

{ DDR, DDR2, DDR3, DDR3L, DDR4, LPDDR, LPDDR2, LPDDR3, LPDDR4, LPDDR4X, GDDR3, GDDR5 } are the generation available.

Outputs

{ DDR | DDR2 | DDR3 | DDR3L | DDR4 | LPDDR | LPDDR2 | LPDDR3 | LPDDR4 | LPDDR4X | GDDR3 | GDDR5 }

Examples

`DDRA:GENeration DDR3L`, sets the DDRA Generation to DDR3L.

`DDRA:GENeration?` returns DDR3L, which indicates the generation is set to DDR3L.

DDRA:DATARate

This command sets or queries the Data Rate for the selected generation.

Syntax

`DDRA:DATARate {<NR1> | CUSTOM}`

`DDRA:DATARate?`

Inputs

`<NR1>` is the data rate for the selected generation; { 200, 266, 333, 370, 400, 500, 533, 600, 667, 700, 800, 900, 933, 1000, 1066, 1200, 1333, 1466, 1600, 1866, 2133, 2400, 2666, 2667, 2933, 3200, 3733, 4000, 4266, 4800, 5000, 5500}

`CUSTOM` specifies that user can enter any data rate value that may not be available in the list.

Outputs

{<NR1> | CUSTOM}

Examples

`DDRA:DATARate "2133"`, sets the data rate value to 2133.

`DDRA:DATARate?` returns 2133, which indicates the current data rate value is set to 2133.

DDRA:CUSTOMRate

This command sets or queries the Custom Data Rate value for the selected generation.

Syntax

`DDRA:CUSTOMRate <NR1>`

`DDRA:CUSTOMRate?`

Inputs

`<NR1>` is custom data rate value to be set

Outputs

<NR1>

Examples

`DDRA:CUSTOMRate 1333E+3`, sets the data rate value to 1333E+3.

`DDRA:CUSTOMRate?` returns 1333E+3 , which indicates the current Custom data rate value is set to 1333E+3.

Note: Data Rate value has to be set to CUSTOM before setting value for custom data rate.

DDRA:VDDMode

This command sets or queries the VDD mode for the selected generation.

Syntax

`DDRA:VDDMode { JEDec | Manual }`

`DDRA:VDDMode?`

Inputs

`JEDec, Manual`

Outputs

{ JEDec | Manual }

Examples

`DDRA:VDDMode Manual`, sets the VDD mode to Manual.

`DDRA:VDDMode?` returns JEDec, which indicates the current VDD mode value is set to JEDec.

DDRA:VDD

This command sets or queries the VDD value in volts.

Syntax

`DDRA:VDD {<NR2> | <NR3>}`

`DDRA:VDD?`

Inputs

`<NR2> or <NR3>` is user defined VDD value and can be floating point value with or without exponent.

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:VDD 1.23`, sets the VDD value to 1.2300 V.

`DDRA:VDD?` returns 1.2300, which indicates the current VDD value is set to 1.2300 V.

Note: VDD mode has to be set to Manual before setting value for VDD.

DDRA:VREFMode

This command sets or queries the Vref mode.

Syntax

`DDRA:VREFMode { JEDec | Manual }`

`DDRA:VREFMode?`

Inputs

`JEDec, Manual`

Outputs

{ JEDec | Manual }

Examples

`DDRA:VREFMode Manual`, sets the Vref mode value to Manual.

`DDRA:VREFMode?` returns JEDec, which indicates the current Vref mode value is set to JEDec.

DDRA:VREF

This command sets or queries the Vref value in volts.

Syntax

`DDRA:VREF {<NR2> | <NR3>}`

`DDRA:VREF?`

Inputs

`<NR2> or <NR3>` is VRef value in volts and can be floating point value with or without exponent.

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:VREF 200.00E-3`, sets the VDD value to 200 mV.

`DDRA:VREF?` returns 200.00E-3, which indicates the current Vref value is set to 200.00E-3 V or 200 mV.

Note: Vref mode has to be set to Manual before setting value for VREF.

DDRA:VREFDC? (Query Only)

This command queries the Vref value in volts.

Syntax

`DDRA:VREFDC?`

Inputs

NA

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:VREFDC?` returns 200.00E-3, which indicates the current Vref value is set to 200.00E-3 V or 200 mV

Note: Vref mode has to be set to Manual before setting value for VREF.

DDRA:VIHACMin? (Query Only)

This command queries the VIH(ac)min value in volts.

Syntax

`DDRA:VIHACMin?`

Inputs

NA

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:VIHACMin?` returns 925.0000E-3, which indicates the current VIH(ac)min value is set to 925.0000E-3 V or 925 mV

DDRA:VIHDCMin? (Query Only)

This command queries the VIH(dc)min value in volts.

Syntax

`DDRA:VIHDCMin?`

Inputs

NA

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:VIHDCMin?` returns 850.0000E-3, which indicates the current VIH(dc)min value is set to 850.0000E-3 V or 850 mV.

DDRA:VILACMax? (Query Only)

This command queries the VIL(ac)max value in volts.

Syntax

`DDRA:VILACMax?`

Inputs

NA

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:VILACMax?` returns 575.0000E-3, which indicates the current VIL(ac)max value is set to 575.0000E-3 V or 575 mV.

DDRA:VILDCMax? (Query Only)

This command queries the VIL(dc)max value in volts.

Syntax

`DDRA:VILDCMax?`

Inputs

NA

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:VILDCMax?` returns 650.0000E-3, which indicates the current VIL(dc)max value is set to 650.0000E-3 V or 650 mV.

DDRA:VCENTDQ

This command sets or queries the Vcent_DQ value in volts.

Syntax

`DDRA:VCENTDQ {<NR2> | <NR3>}`

`DDRA:VCENTDQ?`

Inputs

`<NR2> or <NR3>` is Vcent_DQ value in volts and can be floating point value with or without exponent.

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:VCENTDQ 500.00E-3`, sets the Vcent_DQ value to 500 mV.

`DDRA:VCENTDQ?` returns 500.0000E-3, which indicates the current Vcent_DQ value is set to 500.0000E-3 V or 500 mV.

Note: Applicable for DDR4, LPDDR4 and LPDDR4X Generations.

DDRA:VCENTCA

This command sets or queries the Vcent_CA /Vref_CA value in volts.

Syntax

`DDRA:VCENTCA {<NR2> | <NR3>}`

`DDRA:VCENTCA?`

Inputs

`<NR2> or <NR3>` is Vcent_CA or Vref_CA value in volts and can be a floating point value with or without exponent.

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:VCENTCA 500.00E-3`, sets the VCentCA value to 500 mV.

DDRA:VCENTCA? returns 500.0000E-3, which indicates the current VCentCA value is set to 500.0000E-3 V or 500 mV.

Note: Applicable for DDR4, LPDDR4 and LPDDR4X Generations.

DDRA:VOH

This command sets or queries the VOH value.

Syntax

```
DDRA:VOH {"VDDQ/3" | "VDDQ/2.5" | "VDDQ/2" | "VDDQ/1.667"}
DDRA:VOH?
```

Inputs

"VDDQ/3" and "VDDQ/2.5" are applicable for LPDDR4

"VDDQ/2" and "VDDQ/1.667" are applicable for LPDDR4X

Outputs

{"VDDQ/3" | "VDDQ/2.5" | "VDDQ/2" | "VDDQ/1.667"}

Examples

DDRA:VOH "VDDQ/2.5", sets the VOH value to VDDQ/2.5.

DDRA:VOH? returns VDDQ/2.5, which indicates the current VOH value is set ot VDDQ/2.5.

Note: Applicable for LPDDR4 and LPDDR4X Generations.

DDRA:VDDQ

This command sets or queries the VDDQ value in Volts.

Syntax

```
DDRA:VDDQ {<NR2> | <NR3>}
DDRA:VDDQ?
```

Inputs

<NR2> or <NR3> is VDDQ value in volts and can be floating point value with or without exponent.

Outputs

{<NR2> | <NR3>}

Examples

DDRA:VDDQ 500.00E-3, sets the VDDQ value to 500 mV.

DDRA:VDDQ? returns 500.0000E-3, which indicates the current VDDQ value is set to 500.0000E-3 V or 500mV.

Note: Applicable for LPDDR4X Generation.

DDRA:TDIvw? (Query Only)

This command queries TDIvw value.

Syntax

`DDRA:TDIvw?`

Inputs

NA

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:TDIvw?` returns 125.0000-12, which indicates the TDIvw value is set to 125.0000-12.

DDRA:VDIvw? (Query Only)

This command gets VDIvw value.

Syntax

`DDRA:VDIvw?`

Inputs

NA

Outputs

{<NR2> | <NR3>}

Examples

`DDRA:VDIvw?` returns 136.0000-3, which indicates the VDIvw value is set to 136.0000-3.

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