DSA8300 Digital Serial Analyzer Practices for Measurements on 25 Gb/s Signaling

Application Note

071-3207-01

Tektronix

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1. Overview of 25+ Gb/s signaling for 100GBE, 32GFC, OIF CEI and similar standards

1.1. The environment for 25 Gb/s electrical signaling

Electrical interconnect (chip-to-chip, chip-to-module, board to board in the box), electrical backplane, and short (<15m) Infiniband-grade passive cables have to support systems fronted with optical 100 Gb/s signaling in standards such as 100GbE Optical (802.3ba) and OTN. Original system designs accomplished this by using 10x10G electrical signaling which has been developed previously to support 10 Gb/s optical links (802.3ae, for example).

Since the routing of 10x10G signals is difficult and complex - the optical modules require gear-boxes on both ends (transfer of 10x10 to 4x25 in the transmitter, then back in the receiver) - the industry is transitioning to a more efficient 4x25 electrical interconnect.

The first standard body in the move to 25 Gb/s signaling is the OIF CEI, with the VSR, SR, and LR (very short reach, short reach, long reach) standards. Under development is the Ethernet's 802.3bm 100GBASE-KR4 backplane standard, as well as the Ethernet interconnect standard, 802.bj CAUI4. These standards are the primary interest to this paper.

This paper is focused on the oscilloscope as a tool of choice for the physical layer measurements. From a practical point of view sampling oscilloscopes or the fastest real-time oscilloscopes are a solution; other alternatives, such as BERT error detector, currently support neither all of the measurements nor the accuracy (jitter floor, noise floor) needed.

A companion paper "Measurement of 25 Gb/s signals: requirements on Test and Measurement equipment" discusses the broader measurement system trade-offs, including the comparison of Real-time and Sampling Oscilloscopes' performances for 25 Gb/s signaling. To summarize its result, the Real-Time Oscilloscope can be used for characterization of 25 Gb/s, but it is more expensive for inferior performance; its main advantage is it's convenience.

1.2. Measurement considerations

With this background, this application note comments on the measurement setup questions for oscilloscope - and particularly sampling oscilloscope - measurements for characterization and compliance of the transmitter and the stressed eye generator. Although most of this market uses the same NRZ[1] signaling as that of the 10 Gb/s standards, there are significant challenges in the speed-up to 25 Gb/s. For example, this is the first time that a large field of implementers has been forced to move from the traditional SMA/3.5 mm /2.92mm ("K") connector system to higher performance interconnects, such as 2.4 mm connector.

[1] A part of the market will use PAM4 at 13.8 GBaud; this signaling is not discussed in this paper.

2. Bandwidth requirements and Interconnect selection

It is our purpose here to present a repeatable, practical measurement system setup. There are the following considerations to keep in mind:

The interconnect should have sufficient bandwidth without frequency-domain irregularities ("suck-outs"), large time-domain aberrations, or large frequency dependency of loss across the bandwidth of interest.

Besides connector and cable choice, the obvious optimization is the length of interconnect; an attempt should be made at every step to limit the length of cables, minimize the number of connectors and components.

2.1. Bandwidth requirements

2.1.1 Standards' position

At 25 Gb/s the standards often require measurement equipment with a frequency bandwidth of 40 GHz. Furthermore, in a first for an electrical standard, a Bessel-Thompson filter response is required by the CEI VSR[2].

As of this writing, using a connector/cable system interconnect with just 40 GHz of BW might be interpreted as allowable by standards; however it is marginal; for characterization of important components in particular (e.g. silicon), Tektronix recommends a higher bandwidth interconnect, e.g. 50 GHz.

2.1.2 Connector and Cable Moding and Insertion Loss

As is well known, a connector's or cable's inner (hollow) diameter limits the highest frequency that can be carried without moding. For example, 2.92 mm connectors and cables are limited to carrying ca. 40 GHz signals based on their inner diameter limitation, and a smaller connector geometry is needed for higher frequency limit.

Other sources describe the mechanism behind the wave propagation and moding; for our purposes it is important to note that the effects of moding when only slightly exceeding the maximum bandwidth of the interconnect are not always pernicious. In particular, for a very short interconnect (dividers, adapters) the moding can be insignificant if different modes are not given enough distance to appreciably disperse in time.

On the other hand, longer and flexible interconnect, e.g. cables, are very harmful to signal integrity if moding – significant 'suck-outs typically result from destructive mode re-combination, and these effects will be dependent on cable position, tightening, etc.

[2] As of this writing the standards are not explicit on how closely does the frequency response of the measurement equipment need to track the ideal Bessel-Thompson response, nor does it explain up to how high a frequency should it track. The optical world has stabilized on specifying that the response has to match the B-T filter with a certain tolerance up to 1.5 * the bit-rate frequency; that is, a 28 Gb/s measurement system would have to track the B-T to 42 GHz.

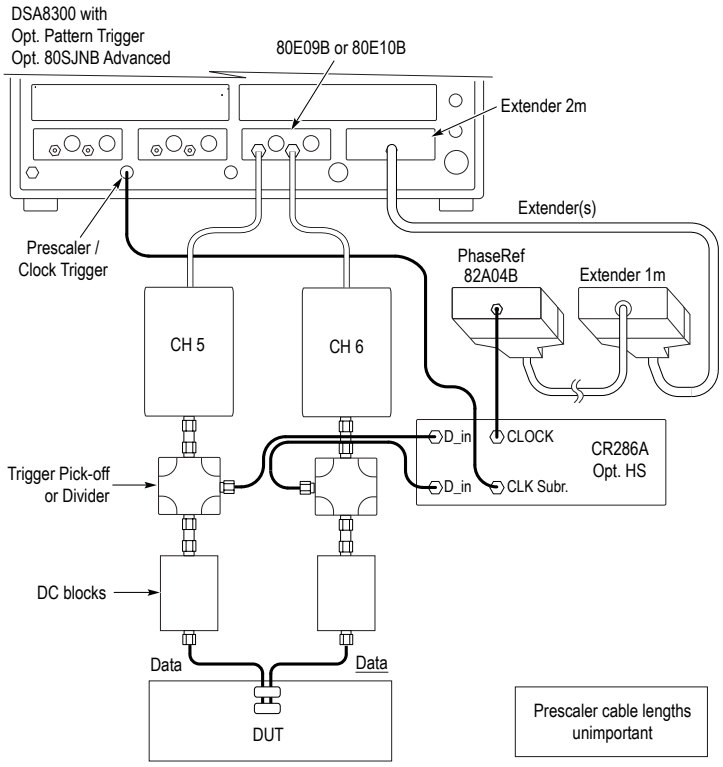

Figure 1. Measurement setup with direct HW Clock Recovery.

2.2. Connector recommendations

Tektronix recommends designing the measurements for bandwidth higher than 40 GHz. This implies a departure from the SMA-compatible 2.92 mm connector ("K") connector. The next higher bandwidth choice is the 50 GHz bandwidth of 2.4 mm connectors; the 50 GHz interconnect is a good choice - it is higher than the minimum bandwidth required; it is forward compatible with an even faster "V" connector system; yet it is neither too scarce nor very expensive.

It is possible to also use a 1.85 mm (aka "V") connectorized interconnect; "V" connectors are compatible with 2.4 mm connectors, and V connectors support BW beyond 70 GHz.

Most signals from CMOS components manufactured before 2015 will not have enough bandwidth to benefit from a "V" interconnect (over the 2.4 mm interconnect), however the informed user has to make the final decision as to what connectors (2.4 mm or 1.85 mm "V") to use.

In rare cases the system interconnect can be made with 2.92 mm ("K" components); if this is attempted care should be taken that the 3.5 mm or SMA cables are avoided.

An easy exception to the 2.4 mm recommendation is the stressed eye generator used for the receiver test, which generates a purposefully slow-edged signal. In the stressed eye generation setup it is not necessary to preserve 50 GHz interconnect since the signal has to pass through approximately 20 GHz filters anyway.

3. Interconnect De-embedding

Acquired signals' processing and analysis can be used to de-embed parts of the interconnect for the purposes of observing the signal at a measurement plane different from the real acquisition plane. This has become a commercially available functionality of signal processing packages for the oscilloscopes, e.g. in the SDLA (Serial Data Link Analysis) functionality of the 80SJNB Advanced jitter package, or the SDLA package for real-time oscilloscopes.

In the space of 25+ Gb/s standards, there are two main applications where de-embedding can be considered:

- De-embedding of the fixture – e.g. the test board
- De-embedding of the interconnect between the oscilloscope and the fixture

In practical deployment the de-embedding functionality is often not as applicable as would be convenient. For example in real-time oscilloscopes the acquisition system's resolution is barely above 5 ENOB (Effective Number Of Bits) of full scale signal, and for fractional signal features or low energy parts of the spectrum the resolution is correspondingly fractional. Only a small amount of de-embedding can be used before the signal captures yield unacceptable result.

Sampling oscilloscopes do offer higher resolution, and de-embedding is more practical. Even then remember that de-embedding turns loss into noise, thus minimizing the amount of de-embedding is important.

In any case of de-embedding, it is critical to acquire high quality network description (S-parameters) of the signal under test. It is self-evident that e.g. an impact of a 20 dB suck-out in the network measurement will create a 20 dB spike in the result – and render the experiment useless.

Recommendation:

Focus your effort on minimizing the length and loss of the interconnect, its quality and repeatability. Only after this has been accomplished, apply de-embedding as needed.

4. External Clock Recovery and its Interconnect

Typically the DUT's – the Serial Data transmission devices themselves - operate with the clock recovery circuit (CR) in the receiver (RX). Thus, the standards mandate that the measurement device incorporates a 'worst possible allowed RX CR'. The concept of 'worst possible RX CR' means that the CR of the measurement device should be no better than the CR of the worst compliant receiver. In a sampling oscilloscope setup the CR is either in a separate CRU (Clock Recovery Unit) or in a circuit built into the acquisition module; similar options exist in the case of a BERT Error detector.

Typically the advantage of an external clock recovery include higher flexibility (e.g. the same CRU can be used with an oscilloscope or with a BERT), and higher functionality – such as access to the analog PLL control voltage for troubleshooting of clock problems.

In the case of a real time oscilloscope the clock recovery can be implemented in software. The advantage of a software clock recovery is its extensive flexibility and a lack of interconnect impact. The disadvantage is the fact that low probability clock problems are nearly impossible to find with a software clock recovery.

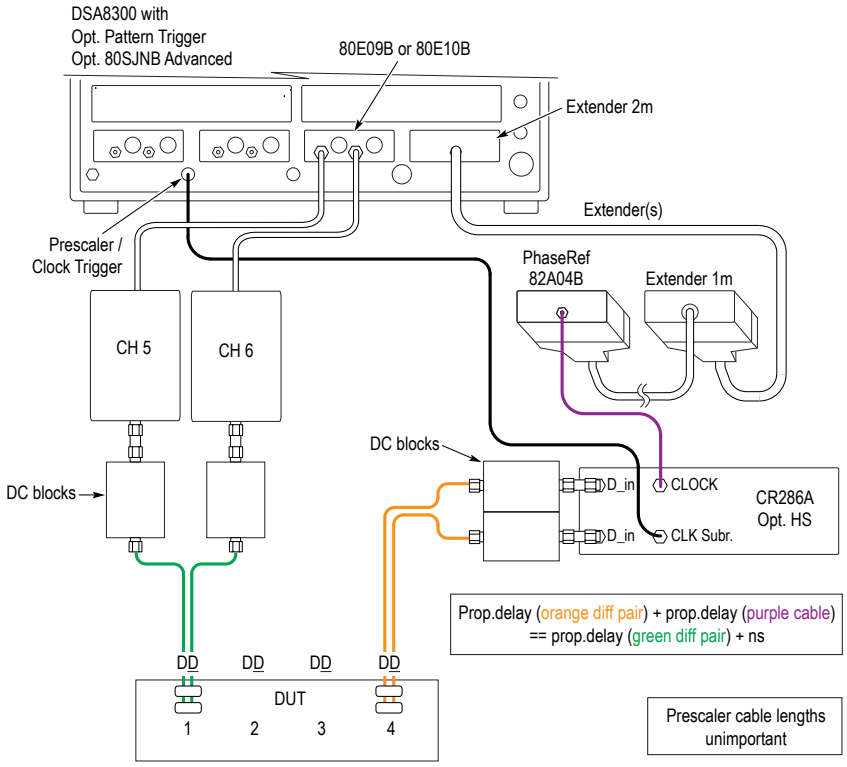

Figure 2. Measurement setup with HW Clock Recovery based on adjacent channel. Note the lack of divider in the Data path. Also note that it is necessary to first prove that the adjacent channel used to drive the CRU has the same uncorrelated jitter as the signal from acquired channel.

4.1. Clock Recovery considerations

A typical setup with an explicit HW clock recovery unit (CRU) is shown in Figure 1. The clock recovery is required by standards and emulates the behavior of the physical receiver.

The divider in the Data path must be carefully considered, see section “5 Interconnect Component”. The divider can be avoided in several cases:

- When the system under test has a clock signal that is sufficiently close to the CRU tracked clock. This might be the case, for example, when there is no Periodic Jitter (PJ) in the system.
- When another path can be used to source signal for clock recovery. This is shown in Figure 2. There are some conditions to this setup – the jitter on DUT channels has to be similar and in phase, for example. Erroneous assumptions result in a pessimistic (increased) jitter results.

4.2. Experiments without Clock Recovery

In practical terms the CR is not necessary in cases of simple testes of devices that do not include a retimer; for example, if testing a simple buffer amplifier we can reasonably drive the buffer amplifier directly from a BERT, and drive the clock of the sampling oscilloscope directly from the BERT – without using the CRU. The fact that a CRU is not tracking the timing changes of the DUT (buffer amplifier) is a pessimism (some of the jitter might not be tracked by the CR, so a larger jitter result will appear), and this pessimism will be very small in the case of a short (in propagation delay) DUT that doesn’t have its own re-timer.

5. Interconnect Components

Overview:

DC Block: some SerDes will be damaged when loaded with 50 Ohm DC to ground. In that case a DC Block is the preferred way to separate the DC loading from the test and measurement equipment.

Note that the DC block is not always necessary – sometimes the DUT doesn't require it, or some form of AC Coupling is already included as a part of the fixture. If in doubt, verify with the SerDes manufacturer or designer.

Deskew hardware: Most oscilloscopes include built-in de-skew. In the case of a Tektronix DSA8300 the deskew is built into the sampling strobe path, rather than the signal path, so there is no impact in signal quality from the Deskew function. Note: for historical reasons the naming is confusing: the "Deskew" function of DSA8300 is actually the wrong choice; you mustn't use it for serial data (it's effectively a multi-acquisition timebase setting meant originally for TDR). In the DSA8300 the correct dial is labeled "Delay".[3]

The BERT's error detector requires precise HW deskew; but due to difficult-to-meet requirements on bandwidth and jitter floor, the existing BERTs are not commonly used for precise jitter and/or bathtub analysis.

The HW Deskew will still be needed in the clock recovery path or the error detector; this is certainly true if the skew between Data and Data is a significant fraction of the UI, but the sensitivity here is much lower than for the deskew in the Acquisition path, and for this reason a well-designed system typically can be used without HW Deskew in the CRU path.

Divider or a "Trigger Pick-off T" for clock recovery

As discussed above in *4.1 Clock Recovery considerations*, in some cases the divider can be avoided and if so we do recommend that.

If the divider is necessary, the following possibilities and their trade-offs should be considered:

5.1. Trigger Pick-off T[4]

Advantages: best flatness, best (lowest) loss.

Disadvantages: the input and output characteristic impedance of fastest devices is lower than 50 Ohm, so DUTs with a low tolerance for reflections and/or poor S11 should not use this method alone; adding a 3 dB attenuator to the input path relieves the concern.

Example: Picosecond Pulse Labs PN 5361 with a risetime of ca. 7ps in the main path. Typical configuration 5361-237-14DB (all 2.4 mm)

Female port 1 (input), Male port 2 (high power split), Female port 3 (low power split).

[3] i.e., Setup->Vertical->[selected channel]->Delay. For practical purposes it's better to always adjust the even channel (although the HW allows either).

[4] In general the difference between a (trigger) pick-off T and a divider is that in a divider the two (or more) outputs are as-much-as possible of the same RF quality. In a pick-off the designer typically assumes intentionally different tasks for each path, and some design trade-off s can be made based on this assumption. Both are reciprocal devices (unlike e.g. directional couplers).

5.2. Matched Trigger Pick-off T[4], or a 20-80 divider

Advantages: good impedance matching; lower loss in the main path than a matched 50-50 divider.

Disadvantages: no known device on the market has sufficient bandwidth[5]; also, bandwidth flatness doesn't match that of a non-matched trigger pick-off .

Example: Picosecond Pulse Labs PN 5372; typical configuration 5372-112 (SMA or 2.4 mm by request)

Female port 1 (input), Male port 2 (high power split), Female port 3 (low power split).

5.3. Matched Divider, or a 50-50 divider

Advantages: good impedance matching; lower loss in the trigger path than the trigger pick-off T.

Disadvantages: higher loss in the through path; worse loss delta between DC and the highest frequency (than the loss delta of a trigger pick-off T).

Example: Picosecond Pulse Labs PN 5350 with risetime of ca. 8 ps in the main path. 5350-237 2.4 mm,Female port 1, Male port 2, Female port 3; (all ports are electrically equivalent)

Example: Anritsu V240C 'V' (1.85 mm) matching 65 GHz power divider, Female all 3 ports, if needed add an Anritsu 34VV50 65 GHz Male to Male adapter.

5.4. DC Block

We've found several good DC blocks on the market without significant trade-offs.

Example: Marki DCZM24F24 DC block 4 kHz-65 GHz (sic) 2.4 mm conn M/F; Example: Picosecond Pulse Labs DC block PN 5509-205-224 2.4 mm 40 GHz DC block

5.5. Cables

Cables that do not mode at very high frequencies share the problem of connectors: the inner diameter of the outside conductor has to be smaller than in lower bandwidth cables. Given fixed impedance, this leads to a smaller diameter of inner conductor as well, and that in turn leads to higher losses – that is, higher losses than lower bandwidth cables even at low frequencies.

This is the main reason why we recommend remote head oscilloscopes for accurate signal capture; the remote head limits –ideally to 0 - the amount of cable necessary.

Example: Gore TEK67HF06PS 152 mm (6") Male "V" both ends, 67 GHz cable, match for pair skew < 5 ps

Example: Tektronix PN 174-6424-xx, CABLE, COAXIAL, FLEX, 2.4mm Male both ends(5 cm), 7016-xxx by SV MICROWAVE INC, match for pair skew < 5 ps.

Cable skew: oscilloscope channels are deskew-capable. The CRU is not deskew-capable, but its sensitivity to skew is small.

5.6. Connector Adapters from {1.85 mm, 2.4 mm} to 2.92 mm

The adapter is necessary in cases when e.g. the signal source is connectorized with 2.92 mm connector.

Additionally both BERTScope and the CRU use Crown adapters which can be ordered in 2.4 mm.

Example: Marki ADPM24F29 adapter, (M) 2.4mm to (F) 2.92mm

Example: Tektronix PN 011-0187-00 adapter, (M) 2.4mm to (F) 2.92mm, i.e. Rosenberger Adapter, RF, PRCN; 2.4mm OR 1.85mm M TO 2.92mm F

Example: Crown 2.4 mm for BERTScope or CR286A CRU

Example: Aeroflex PN 7005A-12, 2.4mm Crown connectors: Part Number 7005A-12 2.4mm Female

[5] To the best of our knowledge no device with a t_r <8ps exists. If this is not correct I would much appreciate an update, pavel.zivny@tek.com.

5.7. Sampling Module Extenders

Sampling module extender cables are “2m Sampling Module Extender cable, Tek 80X02”, and “1m Sampling Module Extender cable, Tek 80X01” (80X02 is aka 80N01).

5.7.1 Sampling Module Extenders if remote head sampling modules are used for acquisition

If sampling modules with remote heads are used (80E09B, 80E09, 80E10B, 80E10) as shown in all setup illustrations in this note), the 82A04B or 82A04 PhaseRef module needs to be put on an extender as shown in the illustrations.

5.7.2 Sampling Module Extenders if monolithic sampling modules are used for acquisition

If a monolithic sampling module is used (e.g. 80E11) consider placing it on a 1m or a 2m extender. If the module is on 2m extender then the delays should be as shown in the examples already given here.

If the 80E11 would be used with a 1m extender cable, then the delay in the PhaseRef’s extender cable needs to be reduced by 1m. (e.g. where there is a 2m+1m extender specified for the remote head modules, only a 2m extender would be used if the 80E11 is on a 1m extender).

If the 80E11 is not on an extender cable then the delay in the PhaseRef’s extender cable needs to be reduced by 2m (relative to what is shown throughout this note).

6. Practical Recommendation for Interconnect at 2.4 mm

Besides the discussion above, the following parts were selected as the basic recommended equipment, and are orderable as a Tektronix 80A08 kit. Here is the partial partlist as of 2013/11, note that further improvements might change some of the part numbers.

6.1. Interconnect

Single-lane listed, please double for differential setup

- DC Block
  PSPLabs 5509-205-224 16 V max. 2.4 mm F to 2.4 mm M
- CRU Data Pick-off: a pick-off T
  Picosecond Pulse Labs Trigger Pick-off T (ca. 7 ps risetime), 5361-237-14DB 2.4 mm jack (f) plug (m) jack (f) Resulting CRU Sensitivity ≤ 160 mV_{diff} [with CR286 Opt. HS]
- Connector Adapters from {1.85 mm, 2.4 mm} to 2.92 mm
  Tektronix PN 011-0187-00 adapter, (M) 2.4mm to (F) 2.92mm, i.e. Rosenberger Adapter, RF, PRCN; 2.4mm OR 1.85mm M TO 2.92mm F
- Connection from the divider T to the CRU:
  cable, ca. 2ns (40cm, i.e. 2”) 2.4 mm / 60GHz rated cables Tek PN 174-6425-xx with 2.4 mm M to 2.4 mm M, 5 ps match. Into Crown 2.4 mm (for BERTScope or CR286A CRU): Aeroflex PN 7005A-12 Tek PN 131-9164-xx
- Connection to a 2.4 mm connectorized DUT:
  cable, ca. 5cm (2”; i.e. very short) 2.4 mm / 60GHz rated cables Tek PN 174-6425-xx with 2.4 mm M to 2.4 mm M, 5 ps match.

6.2. Sampling Module Extenders

Supply:

- 2m Sampling Module Extender cable, Tek 80X02;
- 1m Sampling Module Extender cable, Tek 80X01.

Note that these modules will be supplied automatically with the 82A04B modules.

[3] i.e., Setup->Vertical->[selected channel]->Delay. For practical purposes it’s better to always adjust the even channel (although the HW allows either).

6.3. Sampling Module Extenders if monolithic sampling modules are used for acquisition

If a monolithic sampling module is used (e.g. 80E11) consider placing it on a 1m or a 2m extender. If the module is on 2m extender then the delays should be as shown in the examples already given here.

If the 80E11 would be used with a 1m extender cable, then the delay in the PhaseRef's extender cable needs to be reduced by 1m. (e.g. where there is a 2m+1m extender specified for the remote head modules, only a 2m extender would be used if the 80E11 is on a 1m extender).

If the 80E11 is not on an extender cable then the delay in the PhaseRef's extender cable needs to be reduced by 2m (relative to what is shown throughout this note).

7. Minimizing the Interconnect between the DUT and the Measurement Devices

The photo in Figure 3 is an example of a chip characterization board connected to a sampling oscilloscope (Tek DSA8300) and its sampling module's (Tek 80E09B) remote heads.

The board is connectorized with SMP-M (aka Mini-SMP) connectors. The connectors are cabled vertically with a ca. 30 mm "SMP-M to mm" matched cables pair which is connected to a pick-off 'T'. Blue cables exiting the photo to the left connect to the CRU; the CRU itself is visible in the background.

The weight of the Sampling Remote heads is carried by Tek Probe Holder "PPM203B" articulated arms, one per sampling head (the black arm above the module).

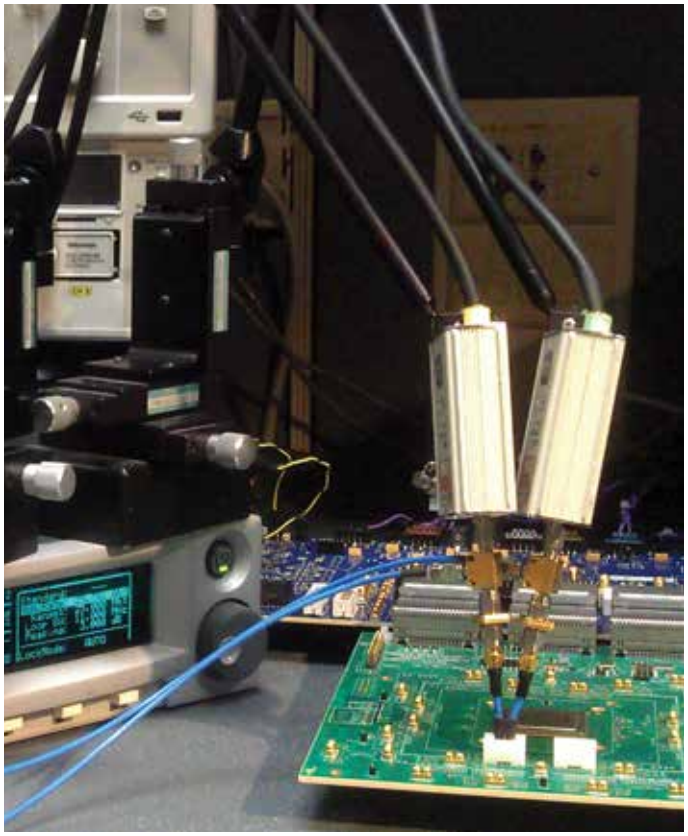

Figure 3. Example of remote head used for short interconnect length.

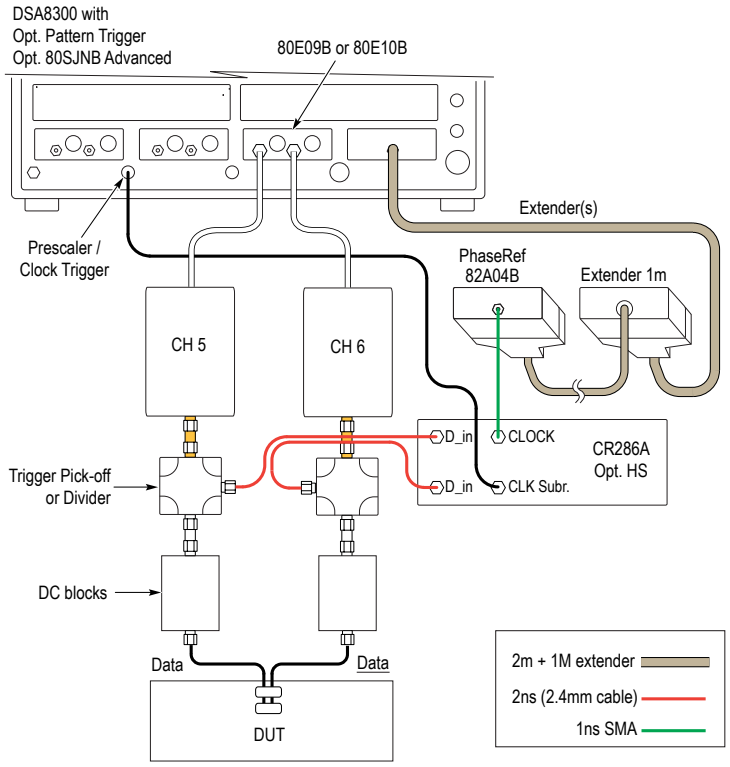

Figure 4. Cable Delays for Measurement setup with direct HW Clock Recovery. Color connections are delay-critical.

8. Data path and Clock path Delay Matching

8.1. The need for Data and Clock path delay matching

The two requirements placed on the interconnect are:

A. The high-speed data path should be of as limited length as possible

B. The data should be acquired based on timing derived from the clock recovered with near-zero delay from the data.

In a setup for a sampling oscilloscope the two requirements are in conflict with each other: the CR and its interconnect insert a non-zero propagation delay that doesn't exist in the data path. In a real-time oscilloscope this can be handled in software by inserting a delay in the data path, but in a sampling oscilloscope a hardware delay in the data path would seem necessary; however a hardware delay line in the data path would violate the requirement "A".

The solution lies in delaying not the data path, but instead in delaying the timing reference to the PhaseRef module – the module which acquires the phase clock generated by the clock recovery, and thus the precise timing between data and clock. This is emphasized in Figure 4 in red; all cables shown in red are length-critical for the proper matching of the timing between the data acquisition point and the clock acquisition point.

Depending on the amount and frequency of uncorrelated jitter, an error in this delay matching between the data acquisition path and the clock acquisition path will impact the results of Periodic Jitter, Random Jitter, and NP-BUJ (Non-Periodic Bounded Uncorrelated Jitter). In typical 25 Gb/s systems the matching has to be performed to better than +/- 500 ps between the data and the acquisition path for the jitter result not to be impacted[6].

The impact of improper matching between the clock and the data acquisition paths is typically pessimistic (larger jitter results than what is correct), since the CRU's tracking of the jitter of the DUT is captured (by the clock acquisition path) out-of-phase relative to the jitter present on the data at the data acquisition.

[6] This depends on amount of jitter measured and required. Here we are assuming the performance of the transmitter devices is on the order of 100 fs to 300 fs.

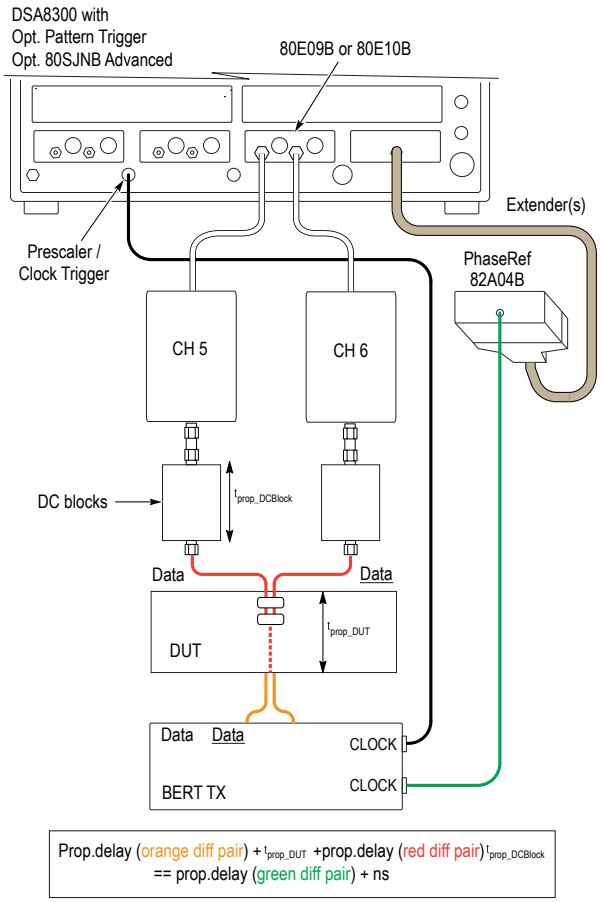

Figure 5. Measurement setup with HW Clock Recovery based on signal in an adjacent channel. Note the lack of divider in the Data path. Color connections are delay-critical.

A different consideration needs to be given to cable delays in setups without CRU (Clock Recovery Unit). This is shown below in Figure 5; the propagation delay of the Data path includes the DUT interconnect and the DUT, the propagation delay of the clock path is now just the delay of the clock interconnect.

An important point in all of the setups discussed so far is the electrical length of the Remote Head cables and the Extender cable. The Remove Head cables are designed for a 10 ns propagation delay, as is the 2m Extender cable.

9. Vertical Calibration and Deskew

9.1. Importance of Vertical Calibration:

If the signal from the DUT has to pass through the DC Block and through the divider / “T”-pick-off, then it is necessary to calibrate the final vertical sensitivity.

In a system with either the DC Block or the CRU connected to the Data path it is necessary to calibrate with an AC signal. We recommend using a square-wave signal and calibrating within a window of at most 0.1 us around the transition (e.g. a risetime).

This way the droop of a typical AC coupling will not impact the calibration result.

9.2. General comments on Vertical Calibration Procedure

Vertical calibration can be performed by connecting the sampling module to an AC waveform source that is not precisely known but is stable.

In the first step the Sampling module is used to determine the amplitude of the signal from the stable calibration source.

In the second step the calibration source is connected to the oscilloscope via the CRU signal pickup (pick off T or a divider), if used, and via the AC Coupling, if used; and the vertical gain corrections factor is adjusted to match the original amplitude from the calibration source.

Since the amplitude from DSA8300’s own front panel AC signal source, the TDR Clock OUT SMA, is too large to be directly measured by most of the modules, it is necessary either to attenuate this signal, use another signal, or, finally, use the Vertical Offset to capture the signal in two steps – the Low level and the High level.

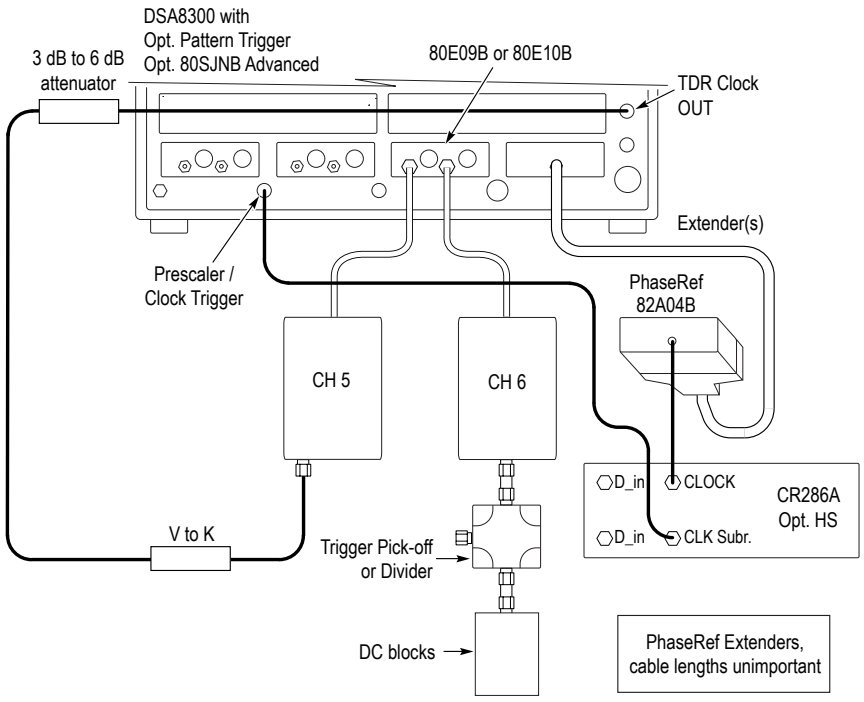

Figure 6. System Setup for Vertical Calibration, step B. Calibration signal highlighted in ochre.

9.3. Vertical Calibration

If your setup will be using the signal divider and/or the DC block, calibrate the vertical amplitude as follows:

9.3.1 Vertical Calibration, Step A: basic oscilloscope setup

- Perform Default Setup (e.g. from the Front Panel)
- Perform Setups->Mode/Trigger->Trigger Source: TDR
- Select (enable) C5 (Channel 5).
- Set Horizontal Scale time/div to 1us/div
- Set Setups->Horz-> Record Length > 1000 [S(amples)]
- Setups->Disp->Style: Show Vectors
- Make sure the Oscilloscope Run/Stop state is Run.
- Setups->Acq->Acquisition Mode: Average (the default 16 samples Average is sufficient).

9.3.2 Vertical Calibration, CH5, Step B: measure Reference Amplitude

- Select (enable) C5 (Channel 5) (if not already enabled).
- Connect the input to the Oscilloscope Channel 5 directly[7] via cable to the “TDR Clock OUT” SMA on the front panel of the oscilloscope. See Figure 8.

[7] directly: there should be no DC block, no divider or “T”-pick-off. The V-connector (aka 1.85mm connector) to K/SMA adapter should be used as needed; see “Figure 8 System Setup for Vertical Calibration, step A”, and see Annex on Pg. 5.

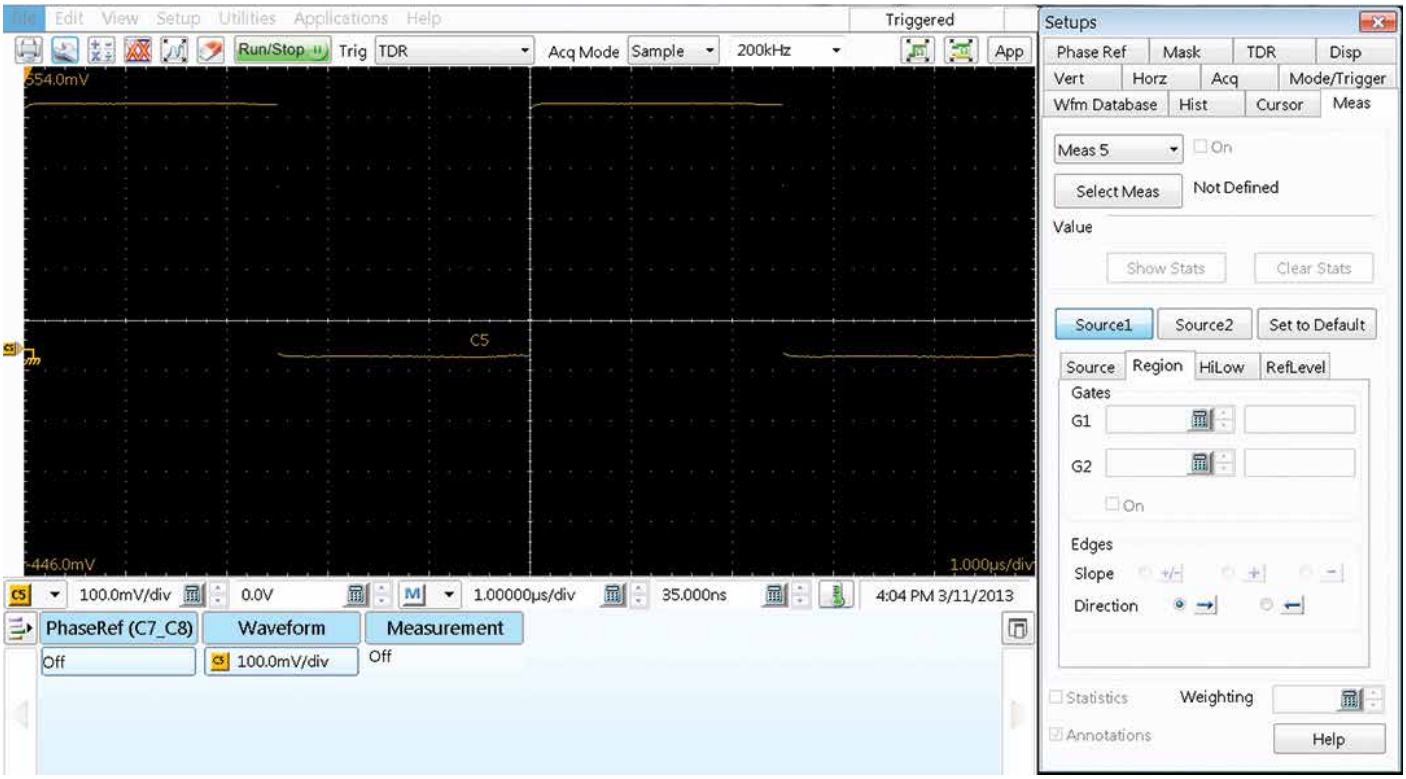

Figure 7. The TDR Clock OUT signal via attenuator.

- The screen should show a square wave, as in Figure 7.
- Depending on the attenuation factor and the sampling module it might necessary to move the signal fully into the amplitude range of the module with its Vertical Offset, e.g.

  Setups->Vertical->Channel: Offset (on C5) : set to 200 mV

  Set a measurement Meas1 of the Amplitude of the step signal around its rise-time:

  Setups->Meas->Signal Type: Pulse

  Setups->Meas->Source: C5

  Setups->Meas->Pulse Amplitude: Amplitude

  Setups->Meas->Meas1: check On
  (The oscilloscope creates this as Meas1).

  Setups->Meas->Region: On

  Setups->Meas->Region: Gates G1: 46%

  Setups->Meas->Region: Gates G1: 54%

  Setups->Meas->Annotations: On ; observe the measurement of pulse amplitude.

Note: We are using a short window around the rise-time only due to effects the DC Block might have on the leveled parts of the signal.

Note (write down) the amplitude reported as Meas1, e.g. 496.2 mV;this is the *Amplitude Referenced*.

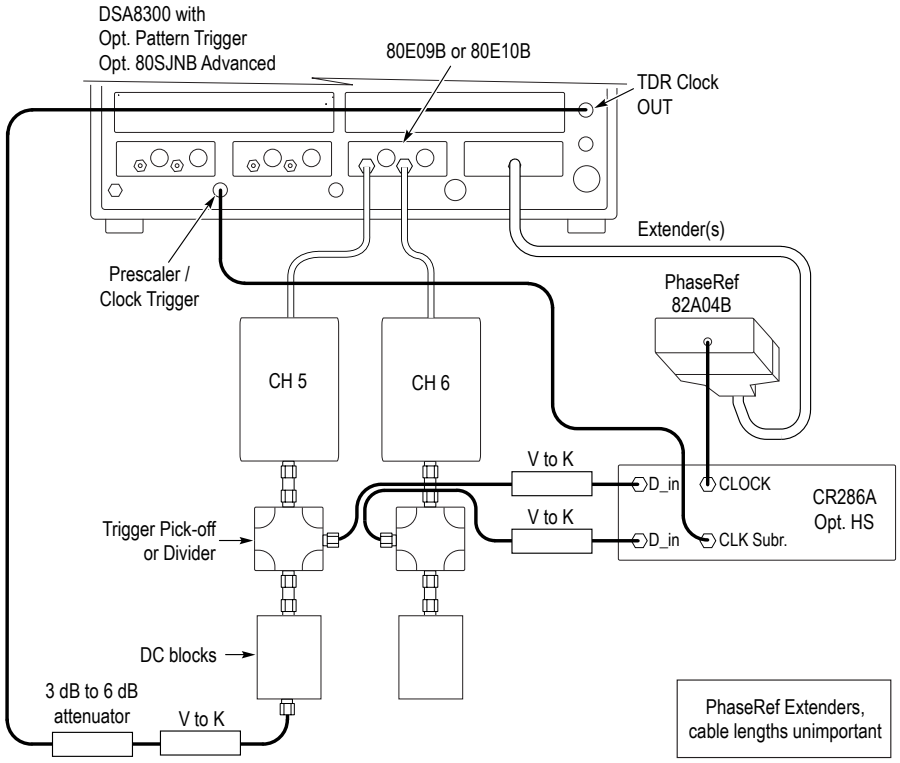

Figure 8. System Setup for Vertical Calibration, step C.

9.3.3 Vertical Calibration, CH5, Step C: measure Apparent Amplitude

- Connect the oscilloscope's C5 if the DC Block (if using the DC Block) and with the Trigger Pick-off T (if using the Trigger Pick-off T) as in Figure 8 .

  Setups->Vertical->Channel: Offset (on C5) : set to 0 V (if previously set away from 0 V).

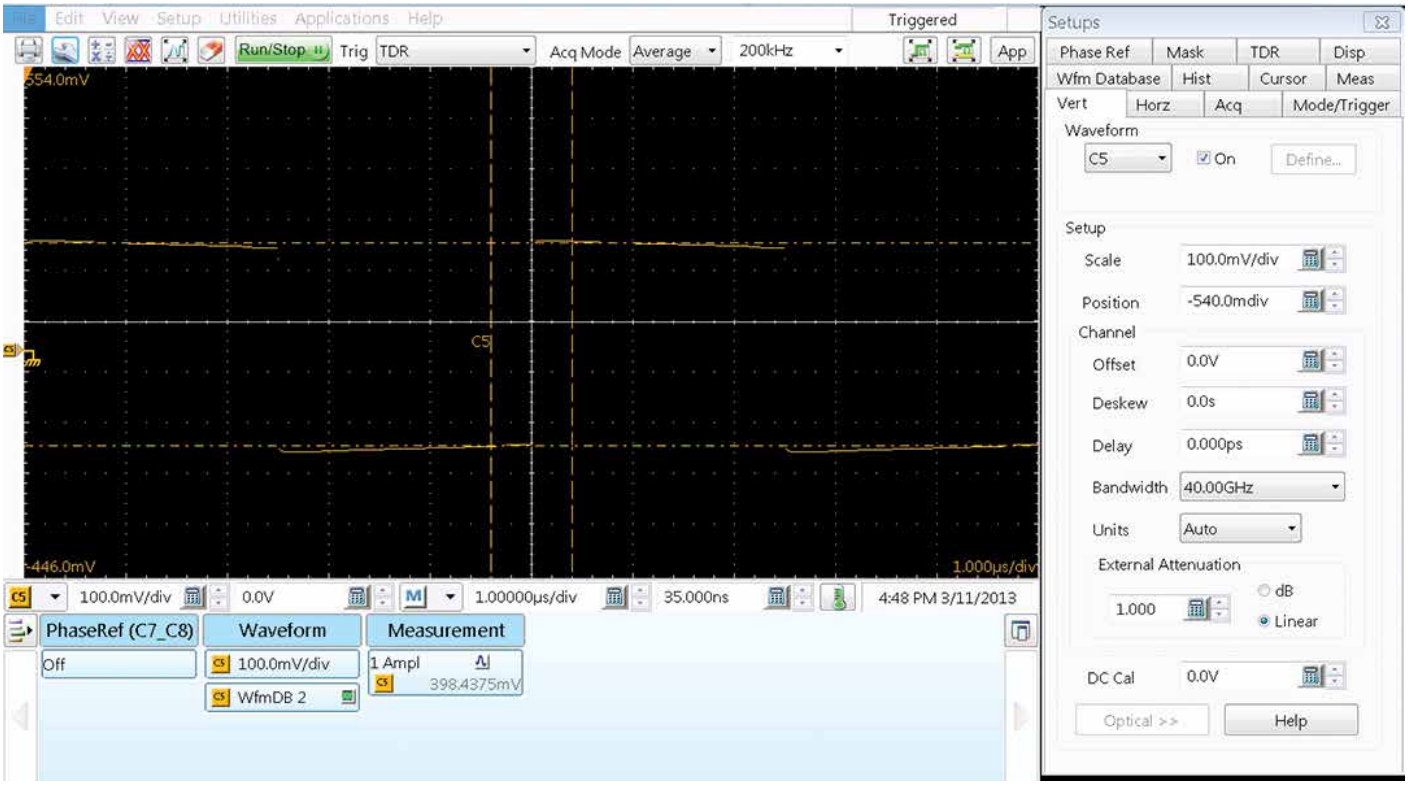

Figure 9. The TDR Clock OUT signal via DC Block.

Again note (write down) the amplitude reported as Meas1; e.g. 398.4 mV, this time smaller due to losses in the Divider and possibly in the DC Block as well. This is the Amplitude Apparent, with all the losses included.

Note that the square-wave might have noticeable slope on high and low levels; this is a function of the size of the capacitor in the DC Block and will be different depending on DC Block used. (This picture is taken with a Marki DC block mentioned in the parts list).

9.3.4 Vertical Calibration, CH5, Step D: Set External Attenuation Factor

- Calculate Gain Correction Factor:=

  < Amplitude Referenced TDR CLOCK OUT> / < Amplitude Apparent TDR CLOCK OUT>, e.g. 1.245 [-].

This is the correction factor for the gain of C5. Write the correction factor into C5 Vertical Attenuation correction as follows:

- Setups->Vertical (C5) ->External Attenuation (Linear): <Gain Correction Factor>.
- This concludes the Vertical Gain Calibration of C5.

9.3.5 Vertical Calibration, C6, Step B, C, D:

- Repeat steps above for C6.
- This concludes the Vertical Gain Calibration of C6.
- Keep the values for External Attenuation written down.
- Set the Setups->Mode/Trigger->Trigger Source: Clock
- Set Horizontal Scale time/div to 40 ps/div
- Make sure the Oscilloscope Run/Stop state is Run.
- Set Setups->Acq->Acquisition Mode: Sample
- This concludes the Vertical Calibration of C5 and C6. Save the setup, and continue to Deskew.

9.4. Deskew of C5 to C6

Deskew Assumption:

- we assume that the DUT signals should be optimally de-skewed at the measurement device.
- In steps A though D we are not attempting to measure the deskew, but rather to optimize it at the measurement device input with a simple procedure that is tolerant of large skew.
- As soon as the skew is less than ½ UI, the method given in 9.6 “Deskew of C5 to C6: Step E: Refine the Deskew by minimizing the interval between eye crossings” should be followed for optimal result. Also see Deskew Note 3.

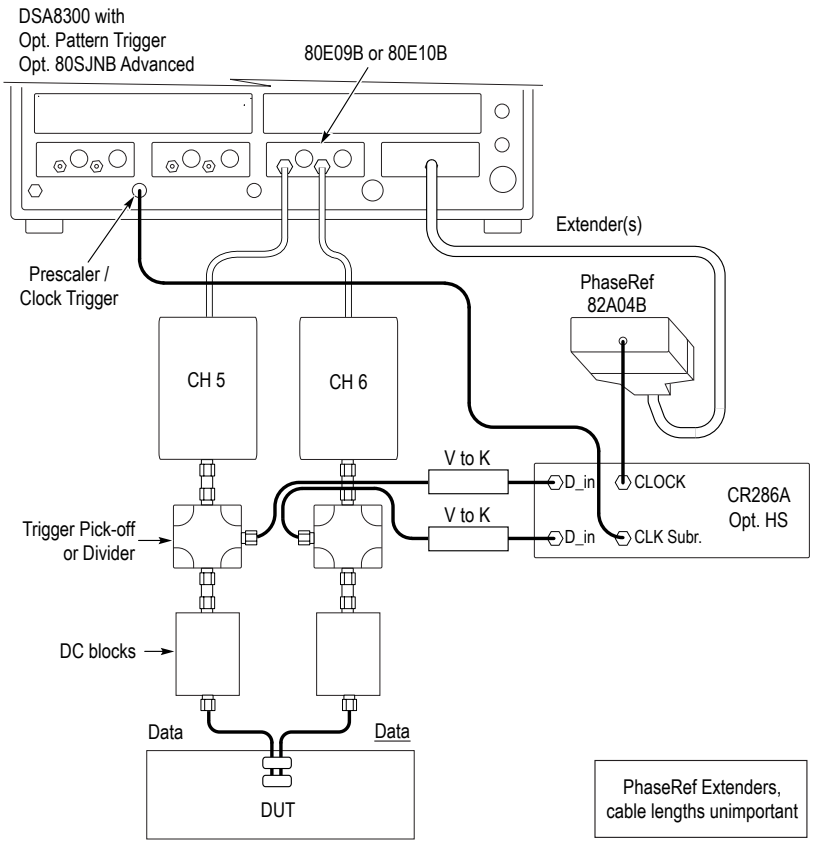

Figure10. Block diagram of system interconnect.

9.4.1 Step A: setup

Connect the oscilloscope to the DUT as for the DUT's signal measurements:

- On DUT:

  Enable the DUT output for standard operation.

  Set the DUT to generate a short pattern (e.g. PRBS9).

- On oscilloscope:

  Perform Setups->Mode/Trigger->Trigger Source: Clock Clock/Prescale

  Select (enable) C6 (Channel 6), turn OFF any other channel.

  Setup->Acq->Acquisition Mode: Sample

  Setup->Disp->Style: uncheck Show Vectors

  In Setups->Meas, unclick On for all measurements

  Set Horizontal time/div to approximately 1 UI/div (e.g. 40 ps for 25Gb/s)

  Set Setup->Horz-> Record Length -> 1000 [S(amples)]

  Open Utilities->Autoset Properties: Uncheck Options: Horizontal, click Autoset. Close Autoset Properties.

  Make sure the Oscilloscope Run/Stop state is Run.

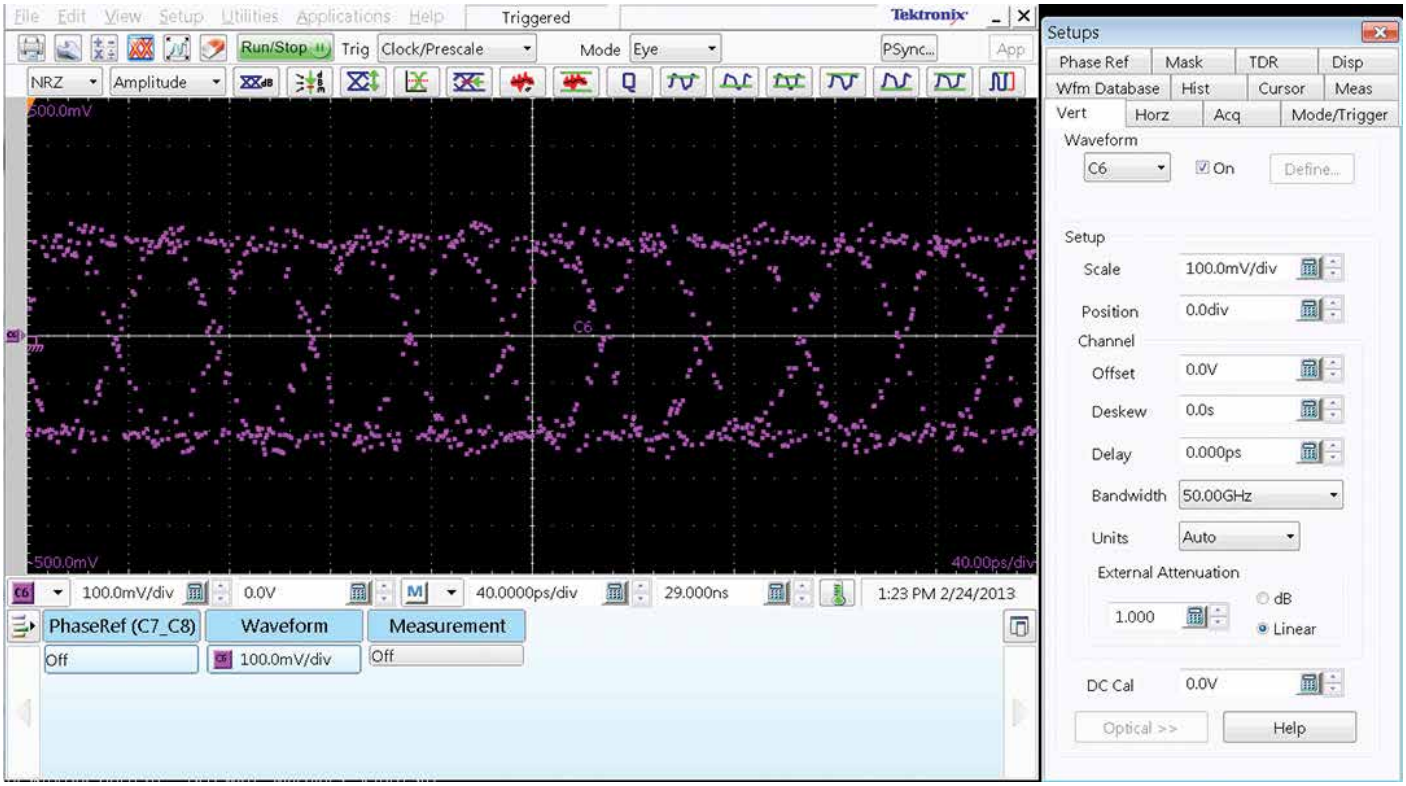

Figure 11. Figure 11. Eye diagrams Autoset, Vectors off. (sample dots enhanced in this picture)

Observe that dimly visible eye diagrams appear on the screen. If not, manually manipulate C6 V/div and Vertical Position and Vertical Offset to achieve a trace in the middle of the screen. See Figure 11.

Select Setups->Vert->Waveform: C5

If following a standard that mandates certain BW (e.g. 40 GHz Bessel-Thompson filter) for electrical acquisition, set the BW appropriately; e.g. for 100GBASE-KR4 Backplane Ethernet:

- Set Setup->Vert (Waveform C6): Bandwidth to 40 GHz. Set the same BW for C5:
- Set Setup->Vert (Waveform C5): Bandwidth to 40 GHz.
- Verify that both C5 and C6 have the proper External Attenuation determined in step 9.3 “Vertical Calibration”.

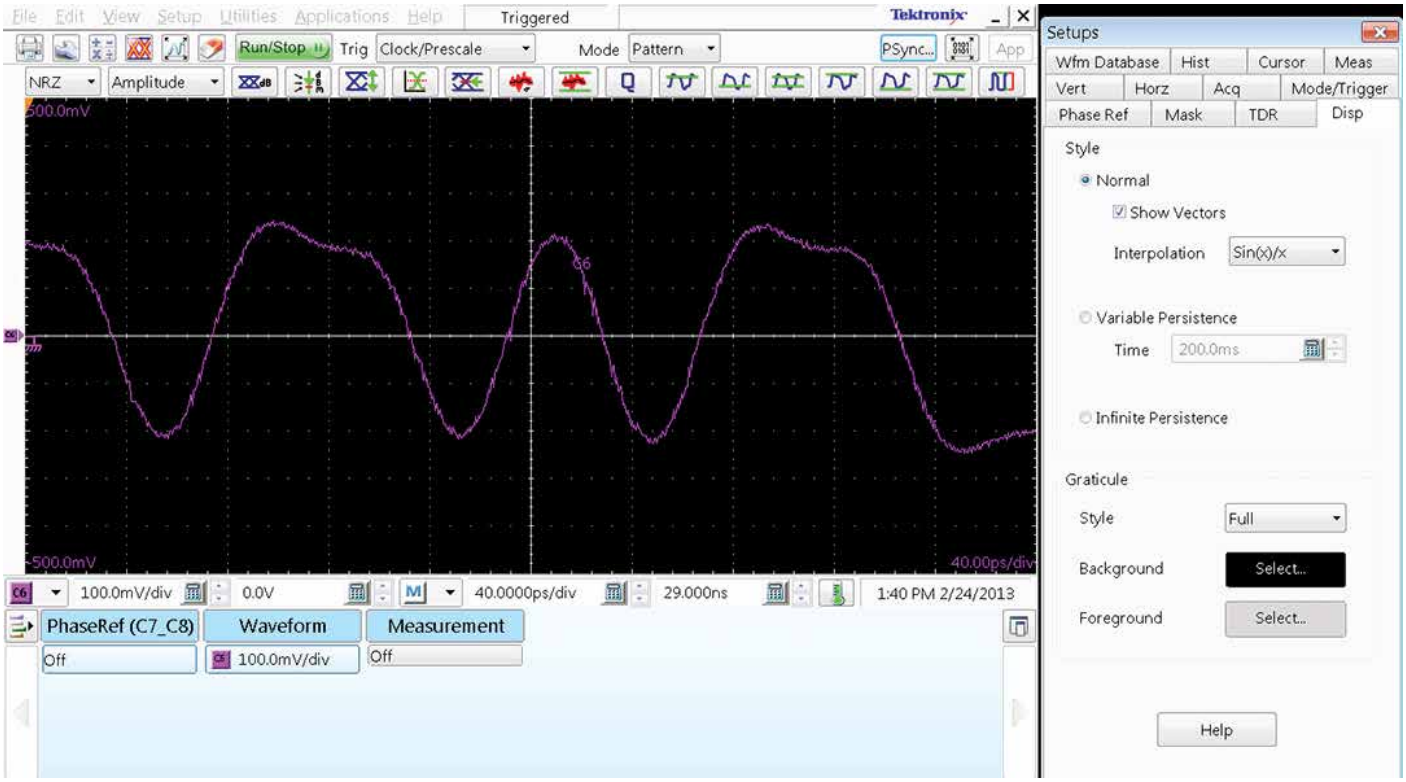

Figure 12. After Pattern Sync is achieved.

9.4.2 Step B: Trigger on pattern

Open Pattern Sync dialog (top-right of the tool-bar; or, in Setups->Mode/Trigger).

Unclick “Data Rate”, fill in Data Rate (e.g. 25.781Gb/s).

Click “AutoSync to Selected Waveform.

Setup->Disp->Style: check Show Vectors

If a trace similar to that of Figure 12 is not present, troubleshoot the setup.

Enable C6.

Select Setups->Vert->Waveform: C6

Set Vert Bandwidth as above for C5.

Open Utilities->Autoset Properties

Click Mode: Period, uncheck Horizontal, click Autoset (all in the Autoset Properties). Close Autoset Properties.

Observe both C5 and C6 displayed mid-screen, w/o clipping.

Both signals should be of similar amplitude – if not, troubleshoot the interconnect to the DUT.

Position the screen such that multiple zero-crossings are seen

Alternative: slow down time/div such that the longest run-length in the pattern would be no more than 1/3 of the screen – e.g. if the pattern is PRBS9, longest run-length is 9 bits; if the UI is 40 ps, then the duration of longest RL is 40*9 -> 360 ps. Set the time/div to 3*360/10, i.e. approx. 110 ps/div).

Define Math: M2:=C5+C6

Observe the common-mode waveform as the white trace.

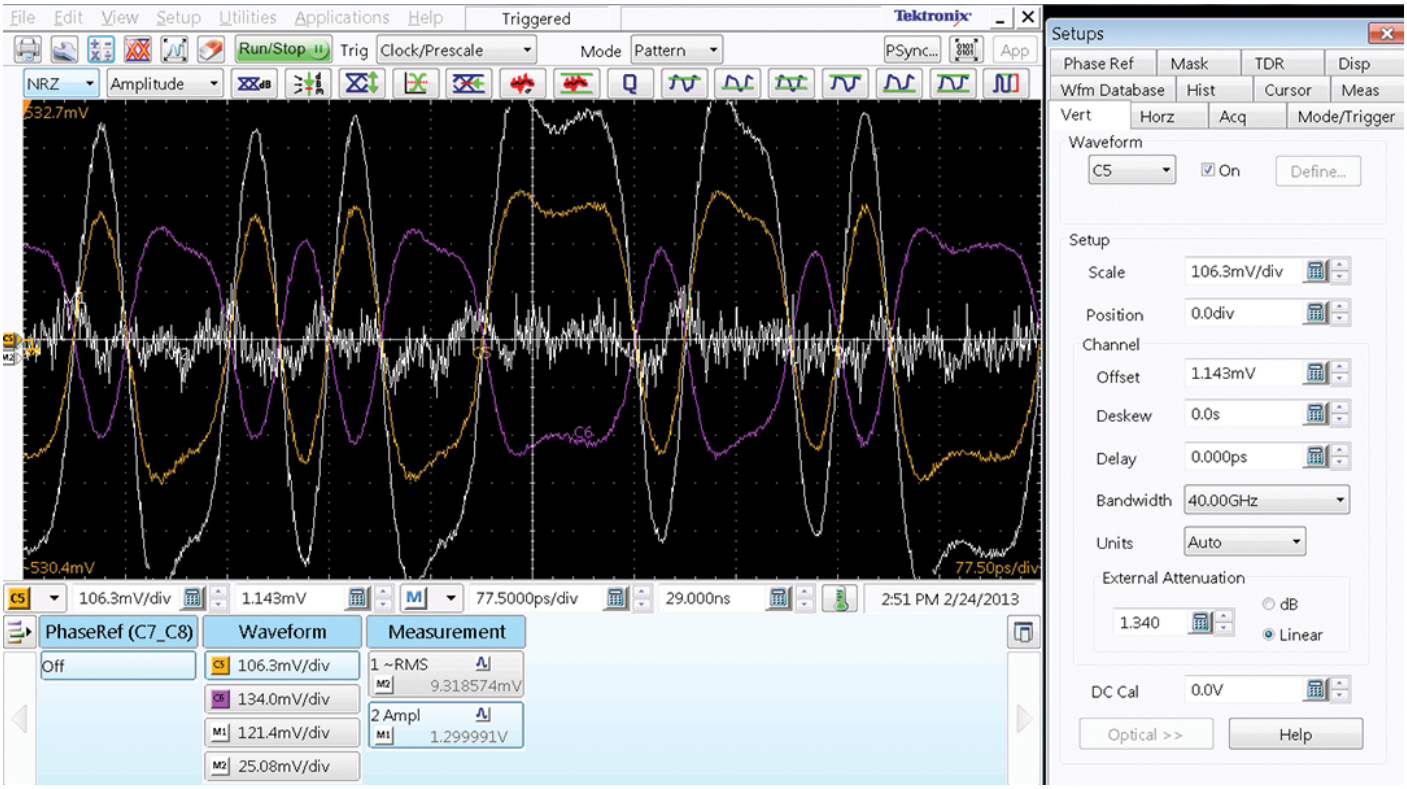

Figure 13. Example of Deskewed signals. Note External Attenuation and Delay values have been filled.

9.4.3 Deskew of C5 to C6: Step C: Deskew

Set a measurement Meas1 of the AC RMS level of the common mode signal:

Setups->Meas->Signal Type: Pulse

Setups->Meas->Source: M2

Setups->Meas->Pulse Amplitude: AC RMS

Setups->Meas->Meas1: check On
(The oscilloscope creates this as Meas1).

Select Setups->Vert->Waveform: C6

Adjust Channel: Delay to minimize the size of the M2 (white trace). Use the Front Panel Fine button and the Front Panel knob, or type values into the Delay window.

Alternative: Adjust Channel: Delay to minimize the value of Meas1 (AC RMS of Math2).

Define Math: M1:=C5-C6

Observe deskewed differential signal. Adjust M1 V/div if desired.

Also: review Deskew Note for quality of Deskew. If desired enable diff. signal Amplitude measurement:

Setups->Meas->Signal Type: Pulse

Setups->Meas->Source: M1

Setups->Meas->Pulse Amplitude: Amplitude

Setups->Meas->Meas2: check On

9.4.4 Deskew of C5 to C6: Step D

Remove M2 (Math2), Remove C5.

In Setups->Meas, unclick On for all measurements.

Store the setup (File->Save Setup As…) for later recall; this procedure uses the name “VertCalAndDeskew.stp”.

Review Deskew Note 3 and step 9.6. If step 9.6 is not needed, this concludes the Deskew process.

9.5. Deskew Notes

9.5.1 Deskew Note 1

The DSA8300 offers two Deskew mechanisms:

- a SW deskew (in Setups->Vert-> Channel: Deskew) and
- a HW deskew (in Setups->Vert-> Channel: Delay).

Except in TDR operation, do NOT use Setups->Vert-> Channel: Deskew.

9.5.2 Deskew Note 2

When deskewed, a clean system with low common mode noise typically has common mode AC RMS below 2% of the differential amplitude.
i.e. Amplitude(C5-C6) > 50* AC_RMS(C5+C6).

9.5.3 Deskew Note 3

In preceding procedure we achieved Deskew by minimizing the energy of a Common mode waveform. This method is less sensitive to large skews, but can provide multiple minima. Contending method is minimizing the eye-crossing to eye-crossing[8] delay, given below in 9.6. This method fails for large initial skew, but if the initial skew is less than ½ UI it provides the best result. Thus the best result is obtained by following the two procedures in the order given here. An informed user can select just one or the other, depending on the need or on the setup at hand.

[8] At high speed such as 25 Gb/s it is less reliable to Deskew by minimizing the an edge-to-edge delay, since different edges often exhibit different skew.

9.6. Deskew of C5 to C6: Step E: Refine the Deskew by minimizing the interval between eye crossings

This is the fine deskew procedure of minimizing the eye-crossing to eye-crossing delay.

Select (enable) C5 (Channel 5).

Set Setups->Horz-> Bit Rate to the DUT's bit rate (e.g. 25.781 Gb/s)

Set Setups->Horz-> Record Length > 1000 [S(amples)]

Setups->Mode/Trigger->Scope Mode: Eye

Setups->Wfm Database:

- select Source: C5, check Display[9]; check Persistence Variable, Waveforms 500, Display Option: check Intensity
- Make sure the Oscilloscope Run/Stop state is Run.
- Autoset

Observe that the screen spans slightly more than one UI, and duration of more than one eye diagram is visible; correct any settings if needed.

Select (enable) C6 (Channel 6).

Setups->Wfm Database:

- select Source: C6, check Display9 ; check Persistence Variable, Waveforms 500
- Autoset

Observe that the screen displays both eye diagrams.

Setup a Delay measurement between the C5 eye crossing and C6 eye crossing:

Setups->Meas->Signal Type: NRZ

Setups->Meas->Source: C5 on Main

Setups->Meas->NRZ Timing: Delay

Setups->Meas->Meas1: check On

Setups->Meas->Source2

Setups->Meas->Source2: C6 on Main

Setups->Meas->Source1

Adjust the horizontal position so crossing on both C5 and C6 is at least a division from the left edge of the screen.

The skew between C5 and C6 is reported as Meas1.

Select Setups->Vert->Waveform: C6

Adjust Channel: Delay to minimize the size of Meas1. Use the Front Panel Fine button and the Front Panel knob, or type values into the Delay window. Make sure to keep the changes in Delay value well below ¼ UI.

Remove C5, Remove C6,

In Setups->Meas, unclick On for all measurements.

In Setups->Wfm Database:

Database WfmDB<1> through <4>: uncheck On

Store the setup (File->Save Setup As…) for later recall; this procedure uses the name "VertCalAndDeskew.stp".

This concludes the Deskew process.

[9] If the channel is already used with a waveform database, find which database is the channel connected to and use it.

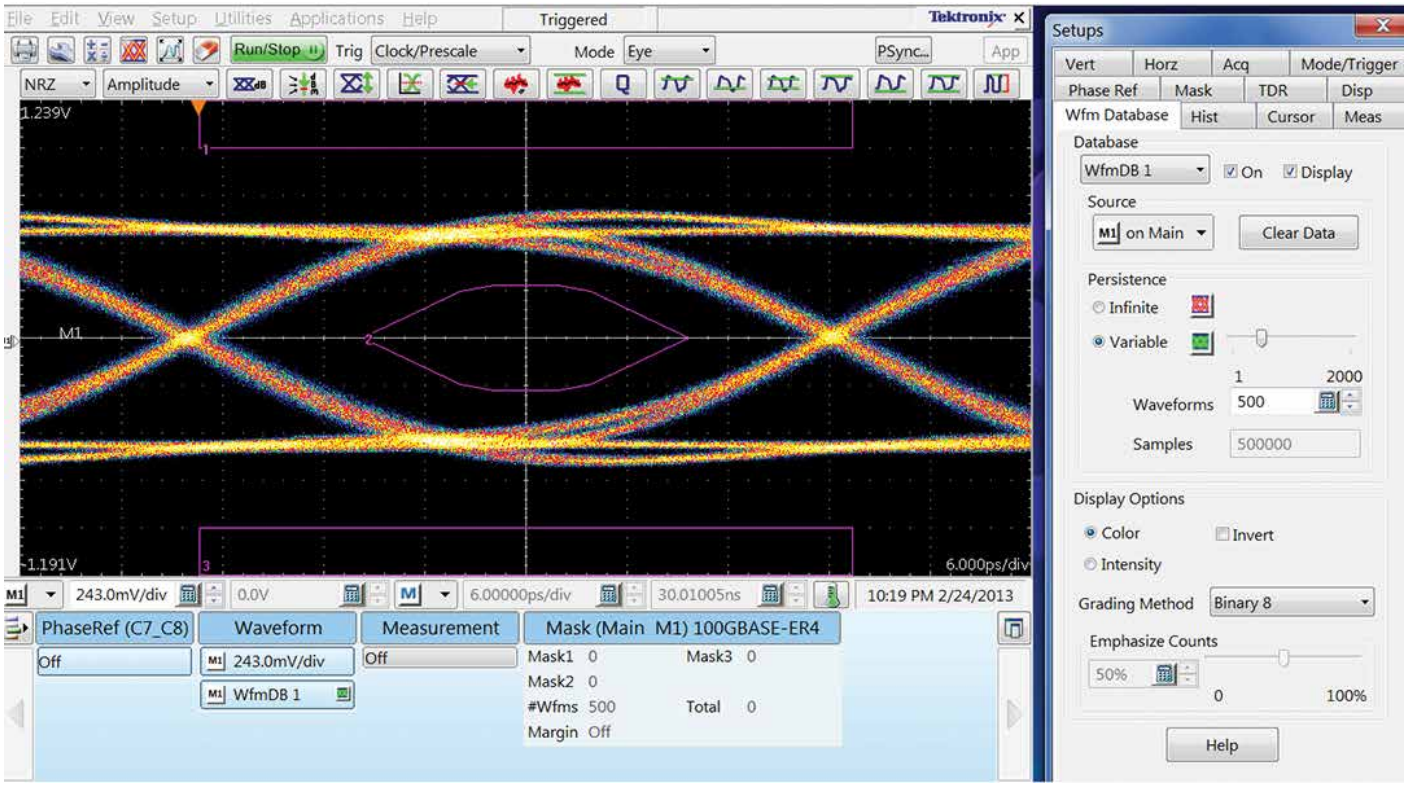

Figure 14. Eye Diagram view.

10. Measurements

10.1. Perform basic system measurements

Recall the VertCalAndDeskew.stp setup (File->Recall Setup)

Observe the waveforms for Deskew (the C6 “Delay” was determined in the Deskew procedure above).

Verify the External Attenuation for both C5 and C6 is still set.

Disable all channels except M1.

Remove all measurements.

Setups->Mode/Trigger->Scope Mode: Eye

Set Setups->Horz-> Record Length > 1000 [S(amples)]

Setups->Wfm Database:

- check Display ; check Persistence Variable, Waveforms 500, Display Option: check Color
- Recall a mask, e.g. 100GBASE-ER[10].
- Select Setups->Mask->Source: M1 on Main
- Click Autoset
- Observe an eye diagram similar to Figure 14.

[10] The example is an optical mask for 25.781 Gb/s. For many electrical tests (e.g. for 100GBASE-KR4) there is no eye diagram mask test, in which case set Setups->Horz-> Bit Rate to the DUT’s bit rate (e.g. 25.781 Gb/s).

If a practical mask is needed and it is not available in the Sampling Oscilloscope’s Mask menu, a mask file can be obtained from Tektronix for appropriate mask. Load a mask file with File->Import Custom Mask. Enable a mask file with Setups->Mask->File Based/Customs.

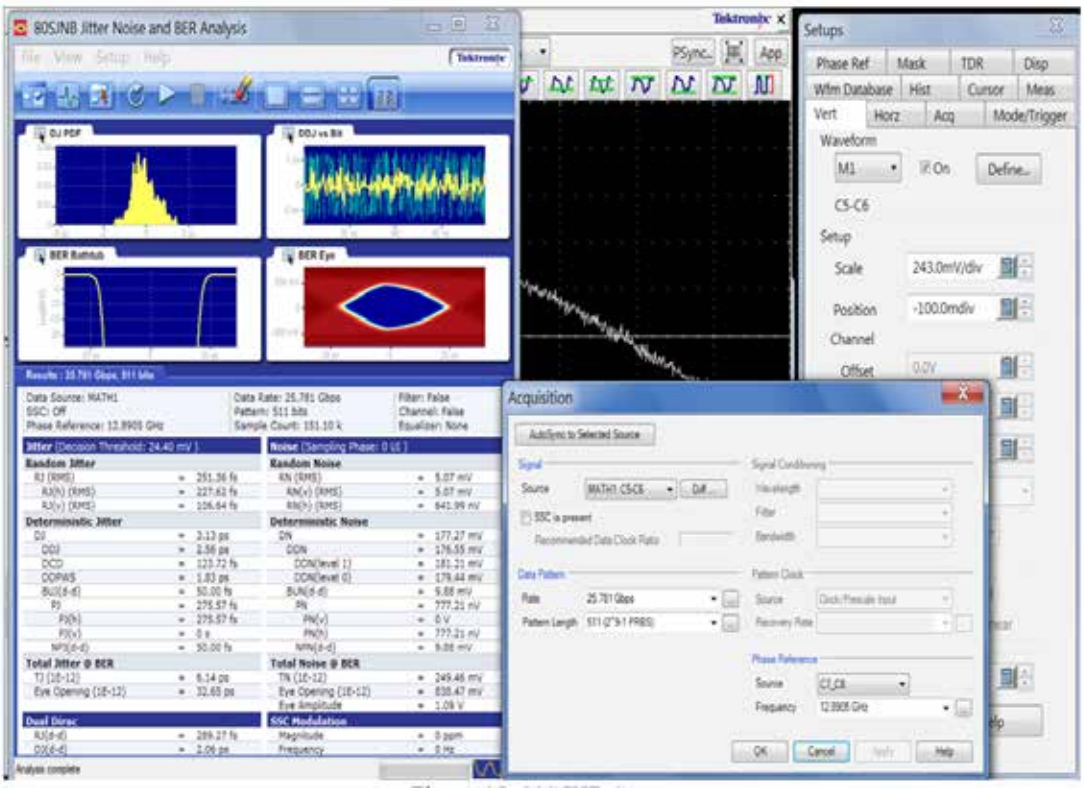

Figure 15. 80SJNB Setup.

10.2. Perform Jitter Analysis

10.2.1 Setup the oscilloscope

Recall the VertCalAndDeskew.stp setup[11] (File->Recall Setup).

Observe the waveforms for Deskew

Verify the External Attenuation for both C5 and C6 is still set.

Disable all channels except M1.

Remove all measurements.

10.2.2 Start 80SJNB

Select Applications->80SJNB (or 80SJNB Advanced if that entry is listed)

When 80SJNB starts (a splash screen should appear immediately, the tool itself in less than 1 min.), select 80SJNB Setup->Acquisition, or select the left-most tool bar button Acquisition ; an Acquisition pane will open up.

In the Acquisition pane (see Figure 1580SJNB Setup) select

- Signal Source MATH1:C5-C6; then select AutoSync to Selected Source .
- The Data Pattern: Rate and Data Pattern: Pattern Length should pre-fill with the values from the oscilloscope; if not, enter the values manually.
- Select Phase Reference Source that is relevant to the position of 82A04 or 82A04B in the mainframe.
- Select Phase Reference Frequency and enter the frequency of the PhaseRef clock.

NOTE: for frequencies above 14.1 GHz the CRU CR286C and the CRU CR175 both generate ½ clock (that is, for 25.781 Gb/s Data Rate, the CRU's main clock out is at 12.8905 GHz).

So if the bit rate is e.g. 25.781 Gb/s, the Phase Reference Frequency should be set to 12.8905 GHz.

In case of any measurement difficulties, disable the Phase Reference and verify that the 80SJNB jitter analysis works properly; if yes then debug the Phase Reference in the oscilloscope environment (not in the 80SJNB environment).

[11] as per the procedure above in "9. Vertical Calibration and Deskew", the setup stored deskewed and vertically calibrated C5 and C6, and defined the diff waveform M1:=C5-C6.

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