Technical Reference

MIPI® M-PHY* Measurements & Setup Library

Methods of Implementation (MOI) for Verification, Debug, Characterization, Compliance and Interoperability Test

DPOJET Opt. M-PHY

077-0518-01

www.tektronix.com

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MODIFICATION RECORD

Jul 13, 2010 (Version 0.1) Initial Document with two measurements

Jul 13, 2010 (Version 0.2) Initial Document with two measurements and Test Procedure

Aug 10, 2010 (Version 0.3) Removed all PWM and SYS measurements, ready with 10 setup files

Sep 28, 2010 (Version .0.4) Updated screen shot for slew rate

Jan 24, 2011 (Version 0.5) Added TX_EYE and will be added SJT/LJT, limit files

Apr 18, 2011 (Version 0.6) Added PSD measurement

Sep 14, 2012 (Version 0.7) Rewritten MOI for new setup files and added measurements

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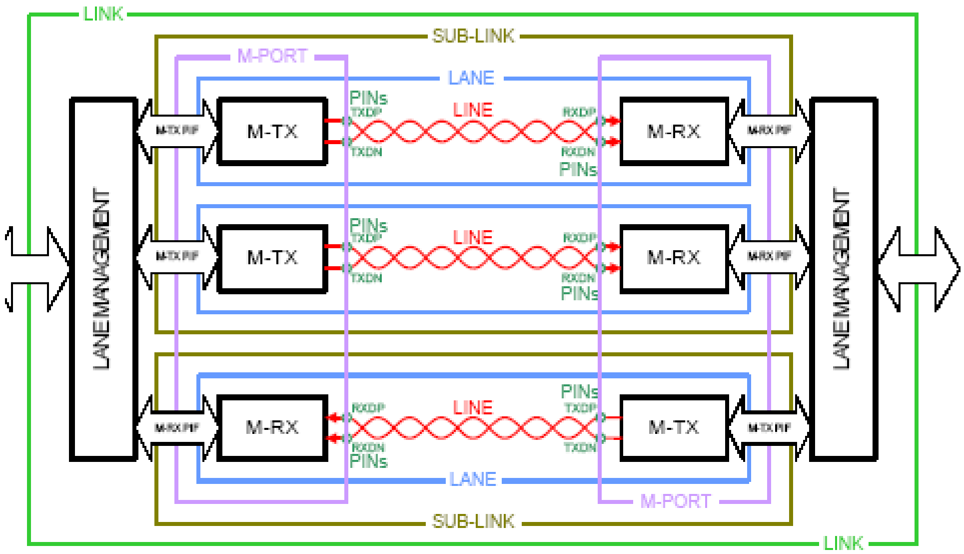
INTRODUCTION

M-PHY enables faster data transfer rates with the help of an embedded clock, and is capable of transmitting signals both in the burst mode and in the differential mode of data transfer. Different data rates gave flexibility to operate at low speed as well as high speed and speed ranges defined in different gears enable it suit for many application . M-PHY works either with an independent clock embedded at the Transmitter and the Receiver and also supported reference clock configuration

The interface is electrical but also optical friendly and enable optical data transport inside the interconnect module. The interface can be single lane or multiple lanes gave flexibility to configure and support multiple protocol

A block diagram of a typical link is as shown below [1]:



Multiple lanes in each direction are incorporated at both Transmitter (TX) and Receiver (RX), which results in a link achieving the required data rate.

A LANE consists of a Single TX, RX and line that connect TX and RX using a differential wire corresponding to two signaling wires DP and DN.

M-PHY Test Specifications are defined at the PINS of the M-TX and M-RX. The transmission lines between the two points are called TX lines. A line may contain a converter for other media such as Optical fiber.

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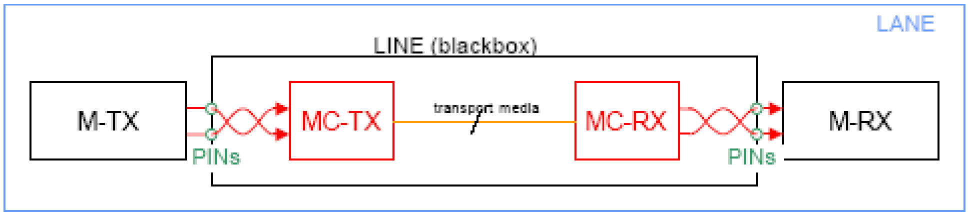
For advanced configuration, module and media converters supported are as follows [1]:



An interface based on M-PHY technology shall contain at least one LANE in each direction; there is no symmetry requirement from an M-PHY prospective.

All lanes in a signal link are called SUB links. Two sub links of opposite directions provide bi-directional transport and additional LANE management called LINK. A set of M-TX and M-RX in a device that composes one interface port is denoted as M-Port.

LINE state

Positive differential voltage driven by M-TX is denoted by LINE state DIF-P, a negative differential voltage driven by M-TX is denoted by LINE state DIF-N, and a weak zero differential voltage is maintained by M-RX.

Differential LINE Voltage	M-TX Output Impedance	M-RX Input Impedance	LINE State set by	LINE State Name
Positive	Low	Any	M-TX	DIF-P
Negative	Low	Any	M-TX	DIF-N
Zero	High	Any	M-RX	DIF-Z
Unknown or floating	High	Any	None	DIF-Q

Table1: Line State

Termination

M-TX terminates both wires with characteristic impedance during any DIF-P or DIF-N state. M-RX does not terminate the LINE and does so optionally. In case of M-RX, the option of Terminating or not terminating with characteristic impedance is interchangeable.

Swing

M-TX supports two drive strengths. When configured for Large Amplitudes (LA), it supports 400 mv PK NT (roughly 200 mVPKRT), while when configured for Small Amplitudes (SA) it will be 240 mV_NT (120mVPK-RT), Default will be large amplitude.

*: Other names and brands may be claimed as the property of others.

References

[1] MIPI Alliance Specification for M-PHY, v1.00.00

[2] M-PHY Physical Layer Conformance Test Suite, Version 0.80

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1. Accessing the DPOJET M-PHY Essentials Measurements

On a supported Tektronix oscilloscope TekScope menu, go to Analyze -> MIPI M-PHY Essentials, and click on it to invoke (see Figure 1-1)the M-PHY setup library in DPOJET standards tab. Figure 1-2 shows the DPOJET standards menu.

Figure 1-1: TekScope Analyze Menu

*: Other names and brands may be claimed as the property of others.

Figure 1-2: DPOJET M-PHY Standard Menu

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2. List of Transmitter Tests

The table 2 below describes the list of CTS measurements for transmitter testing, and the corresponding test subgroupings used in this document. Figure 2 shows the Setup Files folder for M-PHY.

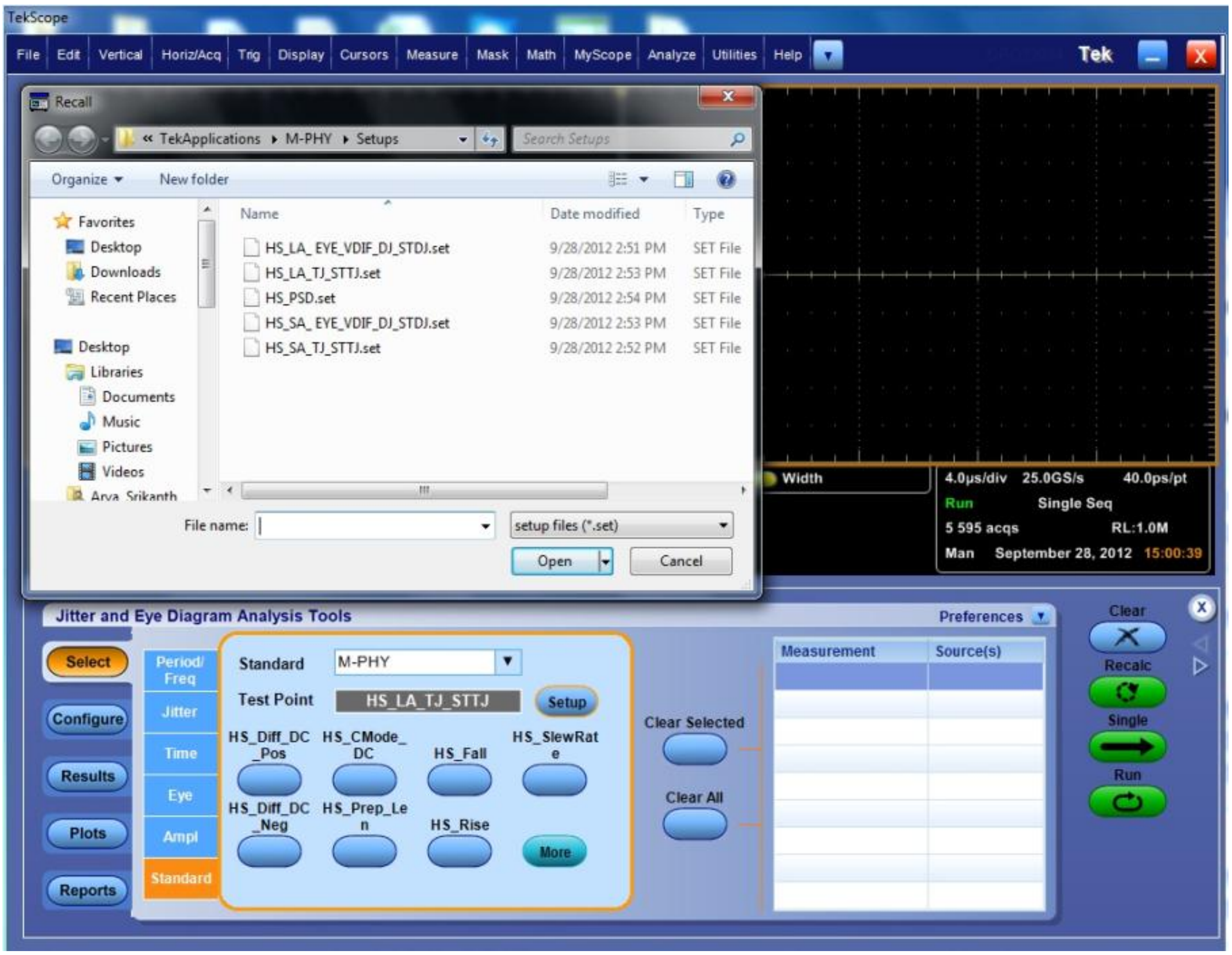

Figure 2: M-PHY Setup files

*: Other names and brands may be claimed as the property of others.

Group1: HS-TX Requirements	Reference in this Document
1.1.1 Unit Interval and frequency offset	HS Tests Subgroup 4(THS-PREPARE,VCM-TX,VDIF-DC-TX,TR-HS-TX,TF-HS-TX,SRDIF-TX)
1.1.2 Common mode AC power spectral magnitude limit	HS Tests Subgroup 3 (PSDCM-TX)
1.1.3 PREPARE length	HS Tests Subgroup 4(THS-PREPARE,VCM-TX,VDIF-DC-TX,TR-HS-TX,TF-HS-TX,SRDIF-TX)
1.1.4 Common mode DC output voltage amplitude	
1.1.5 Differential DC output voltage amplitude	
1.1.6 Minimum differential AC Eye opening	HS Tests Subgroup 2 (TEYE-TX, VDIF-AC-TX, DJTX, STDJTX)
1.1.7 Maximum differential AC output voltage amplitude	
1.1.8 20/80% Rise and Fall Times	HS Tests Subgroup 4(THS-PREPARE,VCM-TX,VDIF-DC-TX,TR-HS-TX,TF-HS-TX,SRDIF-TX)
1.1.9 Lane to lane skew	
1.1.10 Slew Rate	
1.1.11 Slew Rate State Monotonicity	
1.1.12 Slew Rate State Resolution	
1.1.13 Intra Lane Output Skew	
1.1.14 Transmitter Pulse Width	
1.1.15 Total Jitter	HS Tests Subgroup 1 (TJTX, STTJTX))
1.1.16 Short Term Total Jitter	
1.1.17 Deterministic Jitter	HS Tests Subgroup 2 (TEYE-TX, VDIF-AC-TX, DJTX, STDJTX)
1.1.18 Short Term Deterministic Jitter	

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Group2: PWM-TX Requirements	**Reference in this Document**
1.2.1 PWM-TX Transmit Bit Duration (T_{PWM-TX})	PWM Tests (All)
1.2.2 PWM-TX Transmit Ratio (k_{PWM-TX})	
1.2.3 PWM-TX PREPARE Length ($T_{PWM-PREPARE}$)	
1.2.4 PWM-TX Common Mode DC Output Voltage Amplitude (V_{CM-TX})	
1.2.5 PWM-TX Differential DC Output Voltage Amplitude ($V_{DIF-DC-TX}$)	
1.2.6 PWM-TX 20/80% Rise and Fall Times ($T_{R-PWM-TX}$ and $T_{F-PWM-TX}$)	
1.2.7 PWM-TX G1 Transmit Bit Duration Tolerance ($TOL_{PWM-G1-TX}$)	
1.2.8 PWM-TX G0 Minor Duration ($_{TPWM-MINOR-GO-TX}$)	

Table 2: List of tests

*: Other names and brands may be claimed as the property of others.

3. Test Setup

The Figure 3 below depicts the setup to test a single Lane. The differential positive and negatives lines at the Transmitter (Tx) output are connected to Ch1 and Ch2 of the oscilloscope respectively.

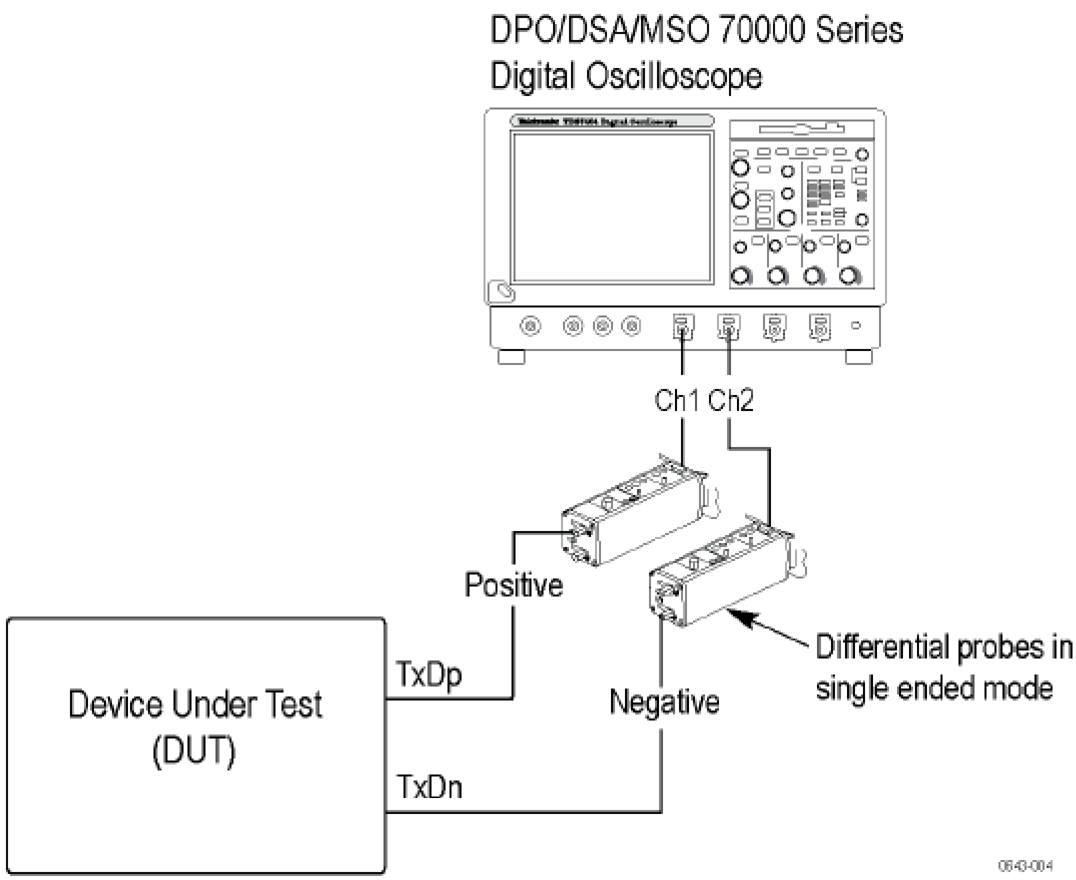

Figure 3: Opt.M-PHY Test Setup

*: Other names and brands may be claimed as the property of others.

4. HS Tests Subgroup 1 (TJ_{TX}, $STTJ_{TX}$)

Purpose

To verify the following Measurements

(a) Test 1.1.15-HS-TX Total Jitter(TJ_{TX})
(b) Test 1.1.16-HS-TX Short-Term Total Jitter($STTJ_{TX}$)

Discussion

UI_{HS} is the Unit interval in high speed mode based on gear. For all combinations of supported.

Amplitudes, Terminations, LANEs, and HS GEARs, the value of TJ_{TX} must be less than 0.32*UI_{HS} in order to be considered conformant.

Similarly, $STTJ_{TX}$ for all combinations, must be less than 0.2*UI_{HS}

Setup File

(a) HS_LA_TJ_STTJ.set for Large Amplitude (Un-terminated-NT) case

(b) HS_SA_TJ_STTJ.set for Small Amplitude (Un-terminated-NT) case

(c) For RT (terminated) use-cases of LA and SA, the above setup file(s) configurations remain unchanged, except that the eye-mask needs to be edited in the above setup files appropriately by the user.

Test Procedure

1. Connect the DUT as described in section 3.Test Setup.
2. Open DPOJET application and recall the appropriate setup file based on LA or SA
3. Click Single to capture and run the measurements. If need be adjust the trigger level to capture the waveform. Expect a result shown in Figure 4 below.
4. Total Jitter (See Result 'TJBER-Test 1.1.15' in the Figure) should be less than 0.32*UI_{HS} for a pass
5. Short-Term Total Jitter (See Result 'TJBER-Test 1.1.16' in the Figure) should be less than 0.2*UI_{HS} for a pass
6. The result example in the Figure 4 is for a Gear1A signal. UI_{HS} for Gear1A = 800 psec.

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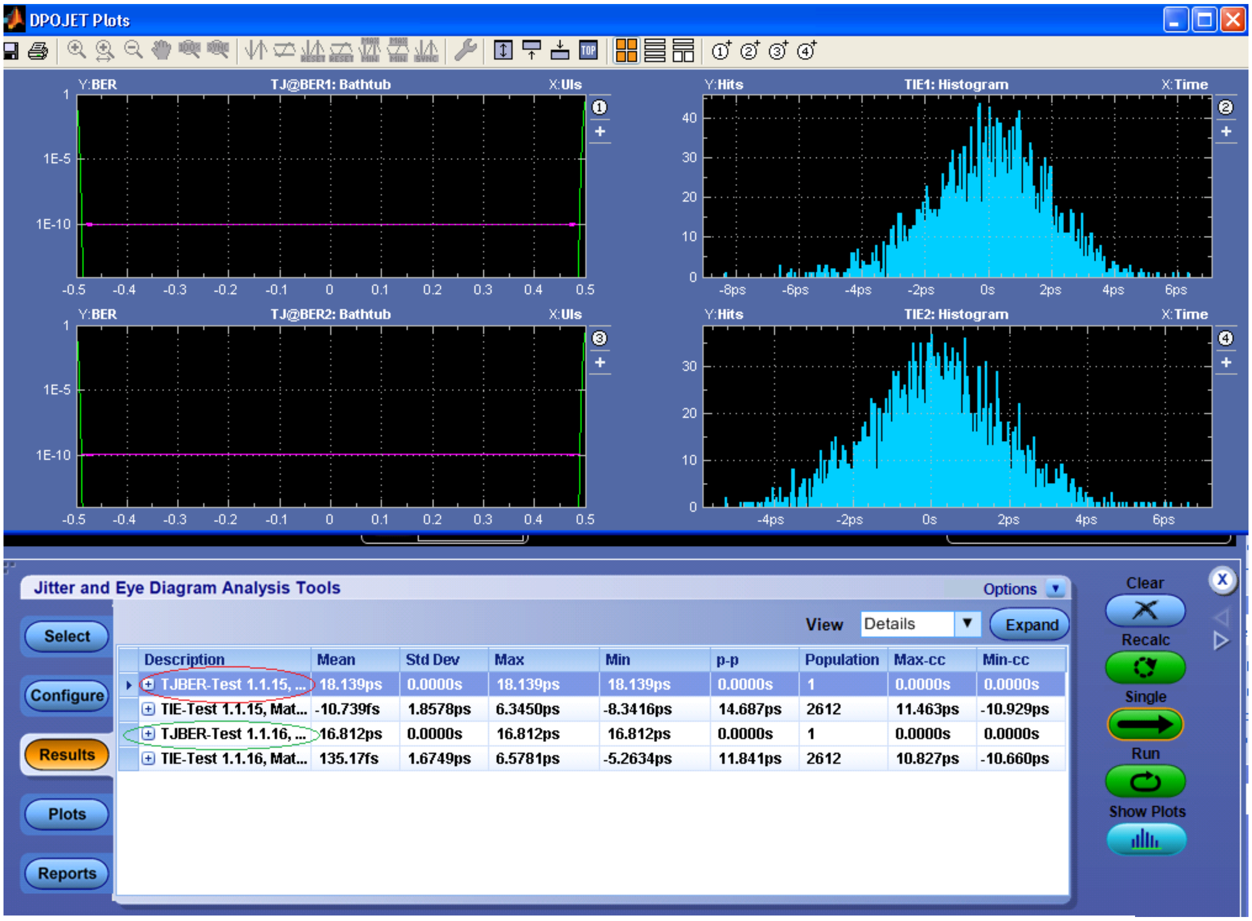


Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
TJBER-Test 1.1.15, ...	18.139ps	0.0000s	18.139ps	18.139ps	0.0000s	1	0.0000s	0.0000s
TIE-Test 1.1.15, Mat...	-10.739fs	1.8578ps	6.3450ps	-8.3416ps	14.687ps	2612	11.463ps	-10.929ps
TJBER-Test 1.1.16, ...	16.812ps	0.0000s	16.812ps	16.812ps	0.0000s	1	0.0000s	0.0000s
TIE-Test 1.1.16, Mat...	135.17fs	1.6749ps	6.5781ps	-5.2634ps	11.841ps	2612	10.827ps	-10.660ps

Figure 4 Total Jitter

*: Other names and brands may be claimed as the property of others.

5. HS Tests Subgroup 2 (T_{EYE-TX}, $V_{DIF-AC-TX}$, DJ_{TX}, $STDJ_{TX}$)

Purpose

To verify the following Measurements

(a) Test 1.1.6-HS-TX Minimum Differential AC Eye Opening(T_{EYE-TX})
(b) Test 1.1.7-HS-TX Maximum Differential AC output voltage amplitude($V_{DIF-AC-TX}$)
(c) Test 1.1.17-HS-TX Deterministic Jitter (DJ_{TX})
(d) Test 1.1.18-HS-TX Short term Deterministic Jitter($STDJ_{TX}$)

Discussion

Differential AC amplitude limits are defined for amplitude and termination use-cases are defined in Table below [1].

Table 1.1.7-1: AC Amplitude Parameter Summary

Parameter	Amplitude	Termination	Reference Load	Conformance Min	Conformance Max
$V_{DIF-AC-LA-RT-TX}$	Large	Terminated	R_{REF-RT}	140mV	250mV
$V_{DIF-AC-SA-RT-TX}$	Small	Terminated	R_{REF-RT}	80mV	140mV
$V_{DIF-AC-LA-NT-TX}$	Large	Unterminated	R_{REF-NT}	280mV	500mV
$V_{DIF-AC-SA-NT-TX}$	Small	Unterminated	R_{REF-NT}	160mV	280mV

Transmit eye opening TEYE-TX for all combinations must be greater than $0.2*UI_{HS}$. All combination encompasses – all supported amplitudes, terminations, LANEs, and HS-Gears.

An AC amplitude reference mask to test 'HS-TX Minimum Differential AC Eye Opening' can be defined based the Minimum of Differential AC amplitude.

Also another reference mask to test 'HS-TX Maximum Differential AC output voltage amplitude' can be defined based on Maximum of Differential AC amplitude.

Deterministic Jitter DJ_{TX} for all combinations must be less than $0.15*UI_{HS}$.

Short-term Deterministic Jitter DJ_{TX} for all combinations must be less than $0.10*UI_{HS}$.

Setup File

(a) HS_LA_ EYE_VDIF_DJ_STDJ.set for Large Amplitude (Un-terminated-NT) case
(b) HS_SA_ EYE_VDIF_DJ_STDJ.set for Small Amplitude (Un-terminated-NT) case
(c) For RT(terminated) use-cases of LA and SA, the above setup file(s) configurations remain unchanged, except that the eye-mask needs to be edited in the above setup files appropriately by the user.

*: Other names and brands may be claimed as the property of others.

Test Procedure

1. Connect the DUT as described in section Test Setup.
2. Open DPOJET application and recall the appropriate setup file based on LA or SA.
3. Click Single to capture and run the measurements. If need be adjust the trigger level to capture the waveform.Expect a result shown in Figure 5below.
4. **T_{EYE-TX}**: See Result ‘MASKHITS-Test 1.1.6’. The number of Mask hits should be zero for a pass.
5. **$V_{DIF-AC-TX}$**: See Result ‘MASKHITS-Test 1.1.7’. The number of Mask hits should be zero for a pass.
6. **DJ_{TX}**: See Result ‘DJDIRAC1-Test 1.1.17’. The deterministic jitter should be less than $0.15*UI_{HS}$.
7. **$STDJ_{TX}$**: See Result ‘DJDIRAC1-Test 1.1.18’. The short-term deterministic jitter should be less than $0.10*UI_{HS}$.
8. The result example in the Figure 5 is for a Gear1A signal, Large Amplitude and Un-terminated use-case.

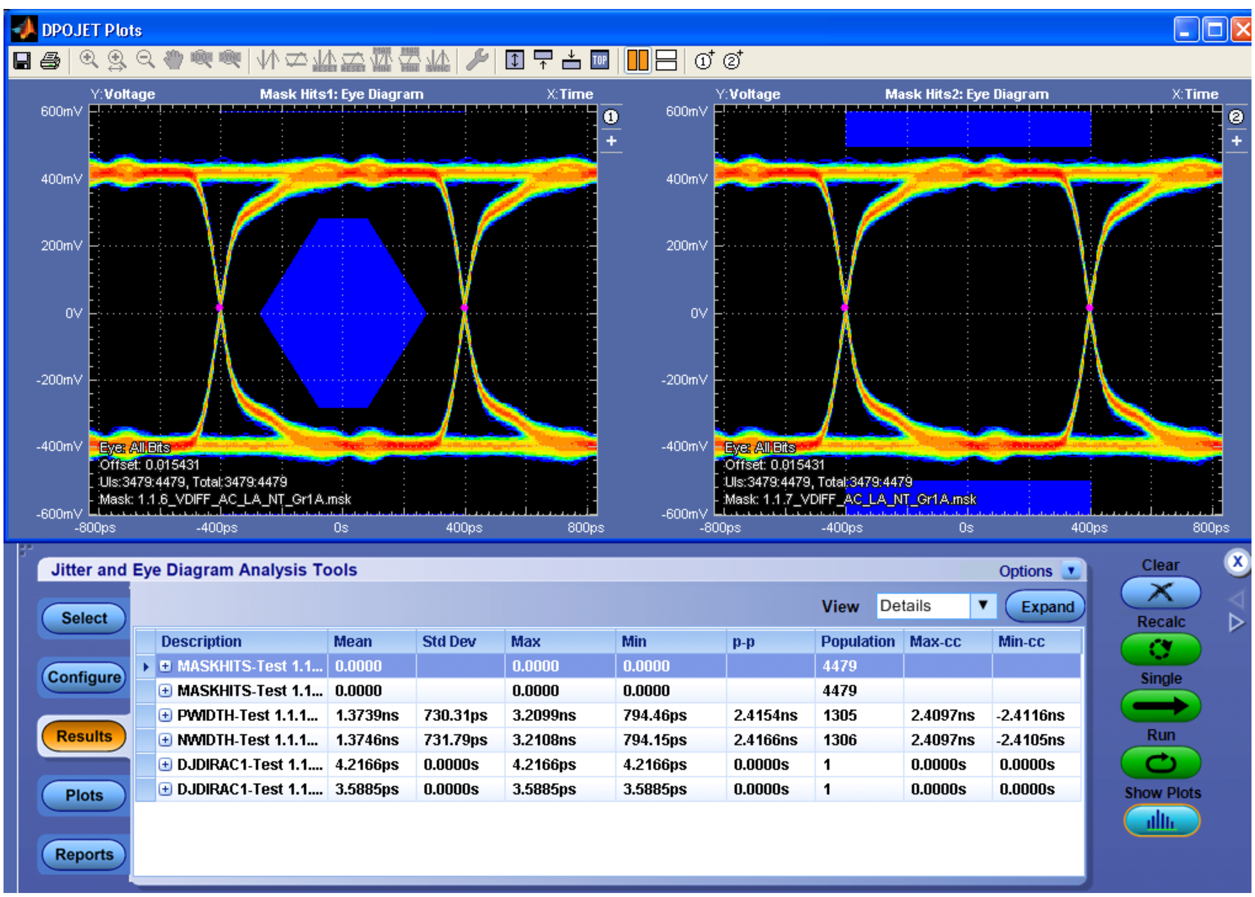


Figure 5-1: Deterministic Jitter

*: Other names and brands may be claimed as the property of others.

6. HS Tests Subgroup 3 (PSD_{CM-TX})

Purpose

To verify the following Measurements

(a) Test 1.1.2 - HS-TX Common-Mode AC Power Spectral Magnitude Limit ($PSDC_{M-TX}$)

Discussion

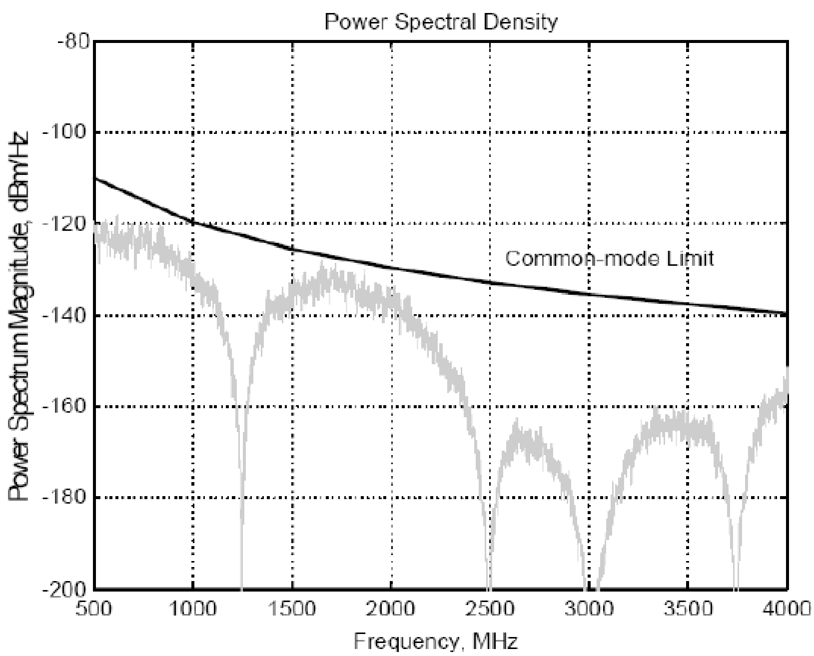
This measurement is performed on the Common mode signal.

Spectral magnitude of the common mode signal is computed. Hamming window is employed for this.

Common mode PSD limit is specified by the following equation

CM Mask = -180 - (14.3*ln (f_MHz) - 159) dBm/Hz over 500-3000 MHz.

Figure 6-1 below show an example PSD, Limit line and the limit table.



Common-Mode Limit

F, MHz	Limit, dBm/Hz
500	-109.9
1000	-119.8
1500	-125.6
2000	-129.7
2500	-132.9
3000	-135.5
3500	-137.7
≥4000	-139.6

Figure 36 Common-mode Power Spectral Magnitude Limit

Figure 6-1: Common Mode PSD

Setup File

(a) HS_PSD.set

*: Other names and brands may be claimed as the property of others.

Test Procedure

1. Connect the DUT as described in section Test Setup.
2. Open DPOJET application and recall the setup file – *PSD.set*
3. Note the Setup configuration. Math1 computes the common mode signal. Math2 computes the Spectral magnitude.
4. A PSD limit file can be pre-created as a waveform file and used for comparison.
5. Click Single to capture and run the measurements. Expect a result shown in Figure 6-2below.
6. The result example in the Figure 6-2 is for a Gear1A signal. In this the pre-created Gear1A limit file is loaded on the Ref1 (white line in the Figure).

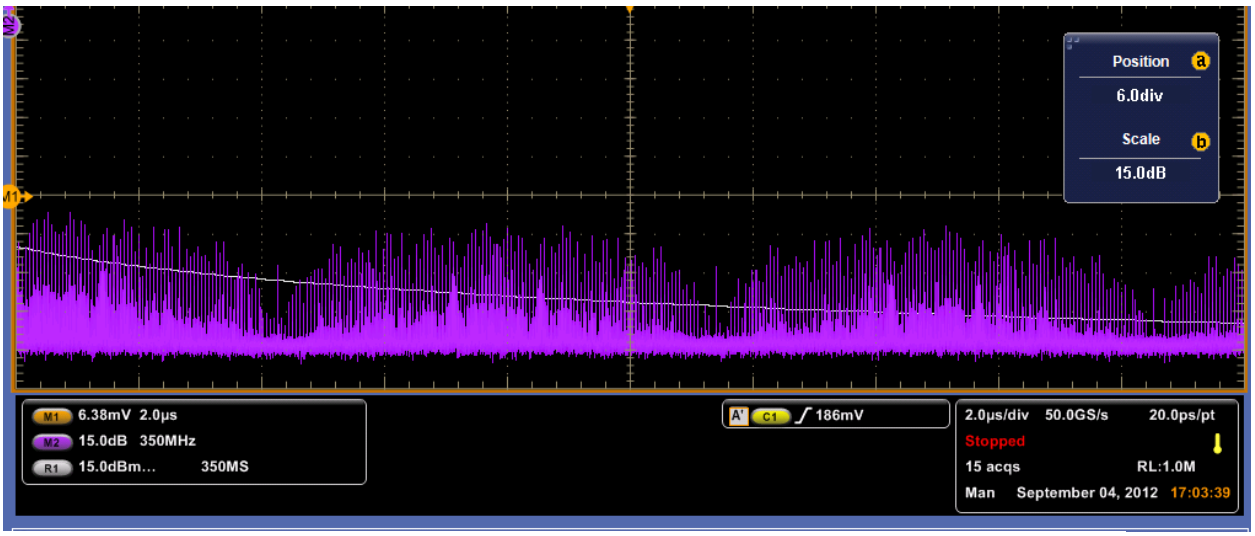


Figure 6-2: PSD

*: Other names and brands may be claimed as the property of others.

7. HS Tests Subgroup 4($T_{HS-PREPARE}$, V_{CM-TX}, $V_{DIF-DC-TX}$, $T_{R-HS-TX}$, $T_{F-HS-TX}$, $S_{RDIF-TX}$)

Purpose

To verify the following Measurements

(a) HS-TX PREPARE Length ($T_{HS-PREPARE}$)
(b) HS-TX Commonmode DC Output Voltage Amplitude (V_{CM-TX})
(c) HS-TX Differential DC Output Voltage Amplitude ($V_{DIF-DC-TX}$)
(d) HS-TX 20/80% Rise and Fall Times ($T_{R-HS-TX}$ and $T_{F-HS-TX}$)
(e) HS-TX Slew Rate ($S_{RDIF-TX}$)

Discussion

HS-TX PREPARE Length ($T_{HS-PREPARE}$)

TX_HS_PREPARE_LENGTH attribute determines the value of $T_{HS-PREPARE}$ and this would be the expected values. The measured value should be within +/- 1UI of the expected value.

HS-TX Common-Mode DC Output Voltage Amplitude (V_{CM-TX})

Table 7-1 given below lists the conformance minimum and maximum.

Parameter	Amplitude	Termination	Reference Load	Conformance Min	Conformance Max
$V_{CM-LA-TX}$	Large	Terminated and Unterminated	R_{REF-RT} and R_{REF-NT}	160mV	260mV
$V_{CM-SA-TX}$	Small	Terminated and Unterminated	R_{REF-RT} and R_{REF-NT}	80mV	190mV

Table 7-1: DC Common Mode Amplitude Requirement Summary [2]

HS-TX Differential DC Output Voltage Amplitude ($V_{DIF-DC-TX}$)

Table 7-2 given below lists the conformance minimum and maximum for all combinations

Parameter	Amplitude	Termination	Reference Load	Conformance Min	Conformance Max
$V_{DIF-DC-LA-RT-TX}$	Large	Terminated	R_{REF-RT}	160mV	240mV
$V_{DIF-DC-LA-NT-TX}$	Large	Unterminated	R_{REF-NT}	320mV	480mV
$V_{DIF-DC-SA-RT-TX}$	Small	Terminated	R_{REF-RT}	100mV	130mV
$V_{DIF-DC-SA-NT-TX}$	Small	Unterminated	R_{REF-NT}	200mV	260mV

Table 7-2: DC Differential Mode Amplitude Requirement Summary [2]

HS-TX 20/80% Rise and Fall Times ($T_{R-HS-TX}$ and $T_{F-HS-TX}$)

Rise and Fall times should be greater than $0.1*UI_{HS}$ to be conformant.

*: Other names and brands may be claimed as the property of others.

HS-TX Slew Rate ($S_{RDIF-TX}$)

One of the Slew Rate supported must meet the conformance as specified in the Table 7-3 below.

Parameter	Amplitude	Termination	Reference Load	Conformance Min	Conformance Max
$SR_{DIF-SA-RT-TX}$[MAX]	Small	Terminated	R_{REF-RT}	0.90 V/ns	n/a
$SR_{DIF-SA-RT-TX}$[MIN]	Small	Terminated	R_{REF-RT}	n/a	0.35 V/ns
$SR_{DIF-LA-RT-TX}$[MAX]	Large	Terminated	R_{REF-RT}	1.665 V/ns	n/a
$SR_{DIF-LA-RT-TX}$[MIN]	Large	Terminated	R_{REF-RT}	n/a	0.6475 V/ns

Table 7-3: Slew Rate Requirement Summary [2]

Setup File:

Not-Applicable, as the measurements in this sub-group are made available as click buttons as shown below.

Figure 7-1 below refers to remaining tests of the M-PHY HS measurements, as described in the CTS [2]. And the following Table 7-4 provides a brief description of these remaining measurements.

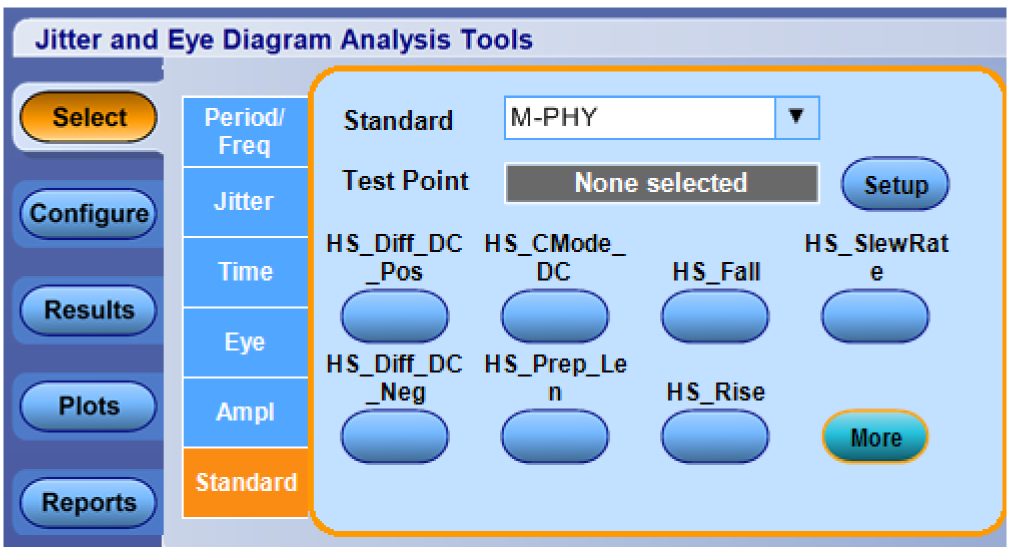


Figure 7-1: DPOJET Snapshot –M-PHY – HS

*: Other names and brands may be claimed as the property of others.

Measurement Name	Test	Detail
HS_Prep_Len	HS-TX PREPARE Length ($T_{HS-PREPARE}$)	Computes prepare length($T_{HS-PREPARE}$) in UI
HS_CMode_DC	HS-TX Commonmode DC Output Voltage Amplitude (V_{CM-TX})	Computes the average of the Common mode DC voltage for the DIF-P(PREPARE) State and DIF-N(STALL) State
HS_Diff_DC_Pos and HS_Diff_DC_Neg	HS-TX Differential DC Output Voltage Amplitude ($V_{DIF-DC-TX}$)	Computes Differential DC voltage for the DIF-P(PREPARE) State - HS_Diff_DC_Pos Computes Differential DC voltage for the DIF-N(STALL) State - HS_Diff_DC_Neg
HS_Fall and HS_Rise	HS-TX 20/80% Rise and Fall Times ($T_{R-HS-TX}$ and $T_{F-HS-TX}$)	Computes Rise and Fall time in UI
HS_SlewRate	HS-TX Slew Rate ($S_{RDIF-TX}$)	

Table 7-4: HS Tests Subgroup 4 Measurement Details

Test Procedure

1. Given that the DIF-P and DIF-N are connected to scope. To perform measurements on differential signal set Math1 = Ch1-Ch2.
2. All the measurements except, Common Mode DC voltage Measurements can be performed on Math1.
3. For Common Mode DC Voltage measurements feed two sources Ch1 and Ch2.
4. Based on the HS gear, sampling rate and record length needs to be set so as to capture at-least one complete burst.

8. PWM Tests (All)

Purpose

To verify the following Measurements

(a) PWM-TX Transmit Bit Duration (T_{PWM-TX})
(b) PWM-TX Transmit Ratio (k_{PWM-TX})
(c) PWM-TX PREPARE Length ($T_{PWM-PREPARE}$)
(d) PWM-TX Common Mode DC Output Voltage Amplitude (V_{CM-TX})
(e) PWM-TX Differential DC Output Voltage Amplitude ($V_{DIF-DC-TX}$)
(f) PWM-TX 20/80% Rise and Fall Times ($T_{R-PWM-TX}$ and $T_{F-PWM-TX}$)
(g) PWM-TX G1 Transmit Bit Duration Tolerance ($TOL_{PWM-G1-TX}$)
(h) PWM-TX G0 Minor Duration ($T_{PWM-MINOR-GO-TX}$)

Discussion

PWM-TX Transmit Bit Duration (T_{PWM-TX})

Transmit bit duration limits for different PWM gears and in Table 8-1.

PWM Gear	Conformance Min	Conformance Max	Units
$T_{PWM-G0-TX}$	1/3	100	µs
$T_{PWM-G1-TX}$	1/9	1/3	µs
$T_{PWM-G2-TX}$	1/18	1/6	µs
$T_{PWM-G3-TX}$	1/36	1/12	µs
$T_{PWM-G4-TX}$	1/72	1/24	µs
$T_{PWM-G5-TX}$	1/144	1/48	µs
$T_{PWM-G6-TX}$	1/288	1/96	µs
$T_{PWM-G7-TX}$	1/576	1/192	µs

Table 8-1: Summary of TPWM-TX **Conformance requirements (usec) [2]**

PWM-TX Transmit Ratio (k_{PWM-TX})

Transmit ratio is the ratio of Major and Minor durations. This is computed for PWM-Bit0 [k (0)] and PWM-Bit1 [k(1)] respectively.

For PWM-Bit0, k(0) = MAJOR(0) / MINOR(0)

Both the transmit ration should be between 1.7027 and 2.5714.

PWM-TX PREPARE Length ($T_{PWM-PREPARE}$)

TX_LS_PREPARE_LENGTH attribute determines the value of TPWM-PREPARE and this would be the expected values. The measured value should be within +/- 1UI of the expected value.

*: Other names and brands may be claimed as the property of others.

PWM-TX Common Mode DC Output Voltage Amplitude (V_{CM-TX})

Refer to Table 7-1, in section 7.Test Subgroup 3 – HS

PWM-TX Differential DC Output Voltage Amplitude ($V_{DIF-DC-TX}$)

Refer to Table 7-2, in section 7.Test Subgroup 3 – HS

PWM-TX 20/80% Rise and Fall Times ($T_{R-PWM-TX}$ and $T_{F-PWM-TX}$)

Rise and fall times should be less than 0.07*T_{PWM-Tx} to be conformant.

PWM-TX G1 Transmit Bit Duration Tolerance ($TOL_{PWM-G1-TX}$)

Transmit Bit Duration for each bit will first be measured based on the time difference between the falling edges of the PWM signal. Also the Average bit duration is computed.

$TOL_{PWM-G1-TX}$ (i) value for each bit will be computed = T_{PWM-TX} (i)/Average;

Both the maximum and minimum values of $TOL_{PWM-G1-TX}$ must be between 0.97 and 1.07 in order to be considered conformant.

PWM-TX G0 Minor Duration ($T_{PWM-MINOR-GO-TX}$)

This is applicable only for Gear0. $T_{PWM-MINOR-TX}$ intervals will be measured, separately for PWM-Bit0 and PWM-Bit1. The minimum of the minors (both) should be within 1/27 and 1/9 us for conformance.

Setup File:

Not-Applicable, as all the measurements in the PWM group are made available as click buttons as shown below.

*: Other names and brands may be claimed as the property of others.

Figure 8-1 below refers to all the M-PHY PWM measurements, as described in the CTS [2]. And the following Table 8-2 provides a brief description of these PWM measurements.

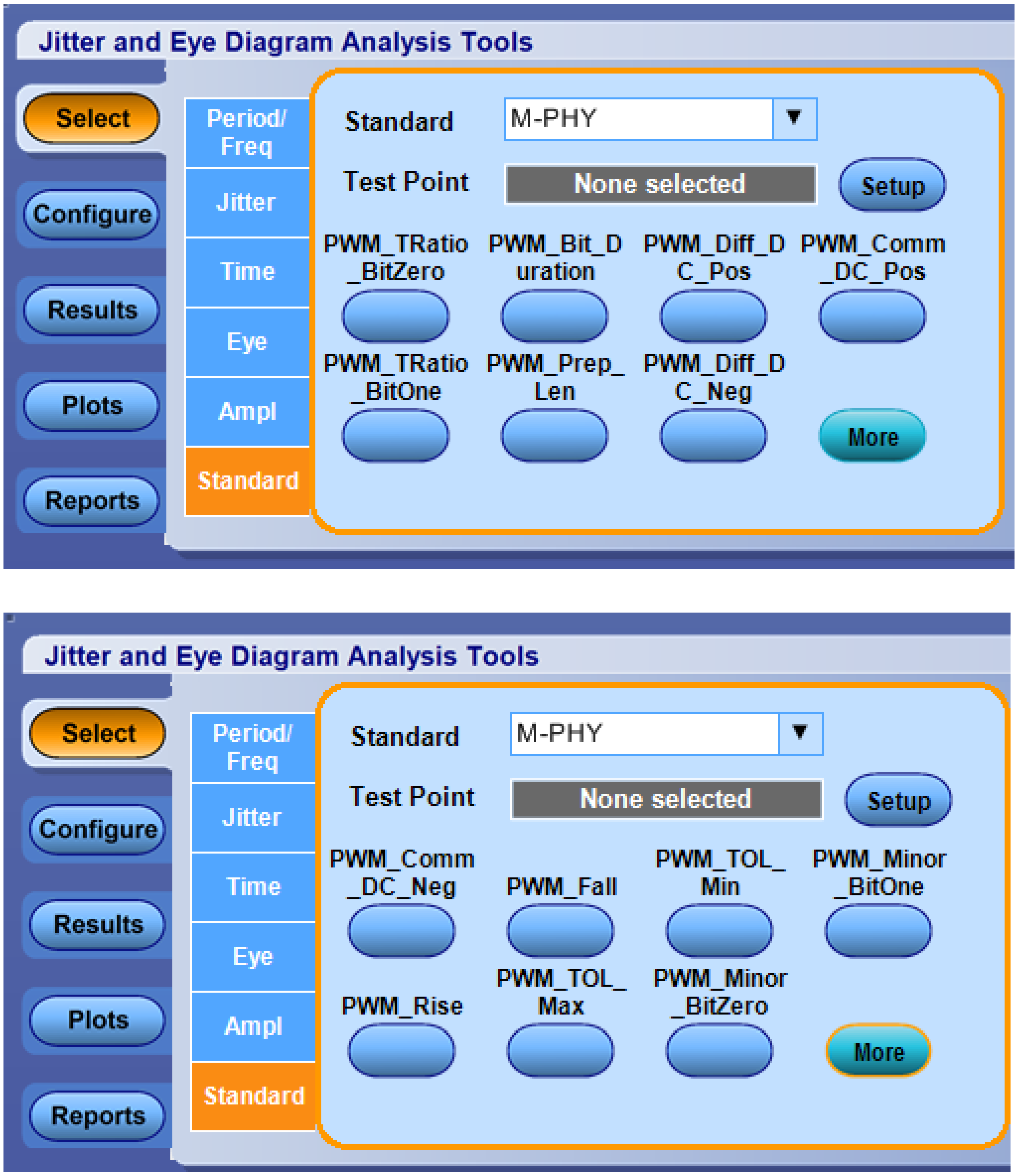


Figure 8-1: DPOJET Snapshot –M-PHY - PWM

*: Other names and brands may be claimed as the property of others.

Measurement Name	Test
PWM_Bit_Duration	PWM-TX Transmit Bit Duration (T_{PWM-TX})
PWM_Tratio_BitZero and PWM_Tratio_BitOne	PWM-TX Transmit Ratio (k_{PWM-TX})
PWM_Prep_Len	PWM-TX PREPARE Length ($T_{PWM-PREPARE}$)
PMW_CMode_DC_Pos and PWM_CMode_DC_Neg	PWM-TX Common Mode DC Output Voltage Amplitude (V_{CM-TX})
PWM_Diff_DC_Pos and PWM_Diff_DC_Neg	PWM-TX Differential DC Output Voltage Amplitude ($V_{DIF-DC-TX}$)
PWM_Rise and PWM_Fall	PWM-TX 20/80% Rise and Fall Times ($T_{R-PWM-TX}$ and $T_{F-PWM-TX}$)
PMW_TOL_Min and PWM_TOL_Max	PWM-TX G1 Transmit Bit Duration Tolerance ($TOL_{PWM-G1-TX}$)
PWM_Minor_BitOne and PMW_Minor_BitZero	PWM-TX G0 Minor Duration ($T_{PWM-MINOR-GO-TX}$)

Table 8-2: PWM Tests – All Measurements Details

Test Procedure

1. Given that the DIF-P and DIF-N are connected to scope. To perform measurements on differential signal set Math1 = Ch1-Ch2.
2. All the measurements except, Common Mode DC voltage Measurements can be performed on Math1.
3. For Common Mode DC Voltage measurements feed two sources Ch1 and Ch2.
4. Based on the PWM gear, sampling rate and record length needs to be set so as to capture at-least one complete burst. For example, a sampling rate of 625MHz is sufficient of PWM–Gear 0, 1, 2 & 3.

*: Other names and brands may be claimed as the property of others.

APPENDIX A – RESOURCE REQUIREMENTS

1. **Real-time Digital Oscilloscope (any one of the following instruments)**
   (a) DPO/DSA/MSO 70604B/C/D or above for HS-GEAR1
   (b) DPO/DSA/MSO70804B/C/D or above for higher up to HS-GEAR2
   (c) DPO/DSA/MSO72004B/C/D or above for up to HS-GEAR3

2. **Probes (Any one of the following probes pair for HS-GEARs)**
   (a) 2Qty P7360A / P7380A/ P7313/ P7506/ P7508/ P7513A/ P7516/ P7520 for HS-GEAR1
   (b) 2Qty P7313/ P7513A / P7516/ P7520 for up to HS-GEAR2
   (c) 2Qty P7520 for up to HS-GEAR3
   (d) 2Qty P3xx for all PWM-Gears

3. **Software**
   DPOJET Advanced (Option DJA) enabled with Option M-PHY

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