Tektronix®

SDLA Visualizer
Serial Data Link Analysis Visualizer Software
Printable Application Help

076-0173-06

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Serial Data Link Analysis Visualizer Software
Printable Application Help

Supports SDLA Visualizer Firmware V2.0.1 and above

www.tek.com
076-0173-06

Contacting Tektronix

Tektronix, Inc.
14150 SW Karl Braun Drive
P.O. Box 500
Beaverton, OR 97077
USA

For product information, sales, service, and technical support:

- In North America, call 1-800-833-9200.
- Worldwide, visit *www.tek.com* to find contacts in your area.

Table of Contents

GPIB remote control

Welcome

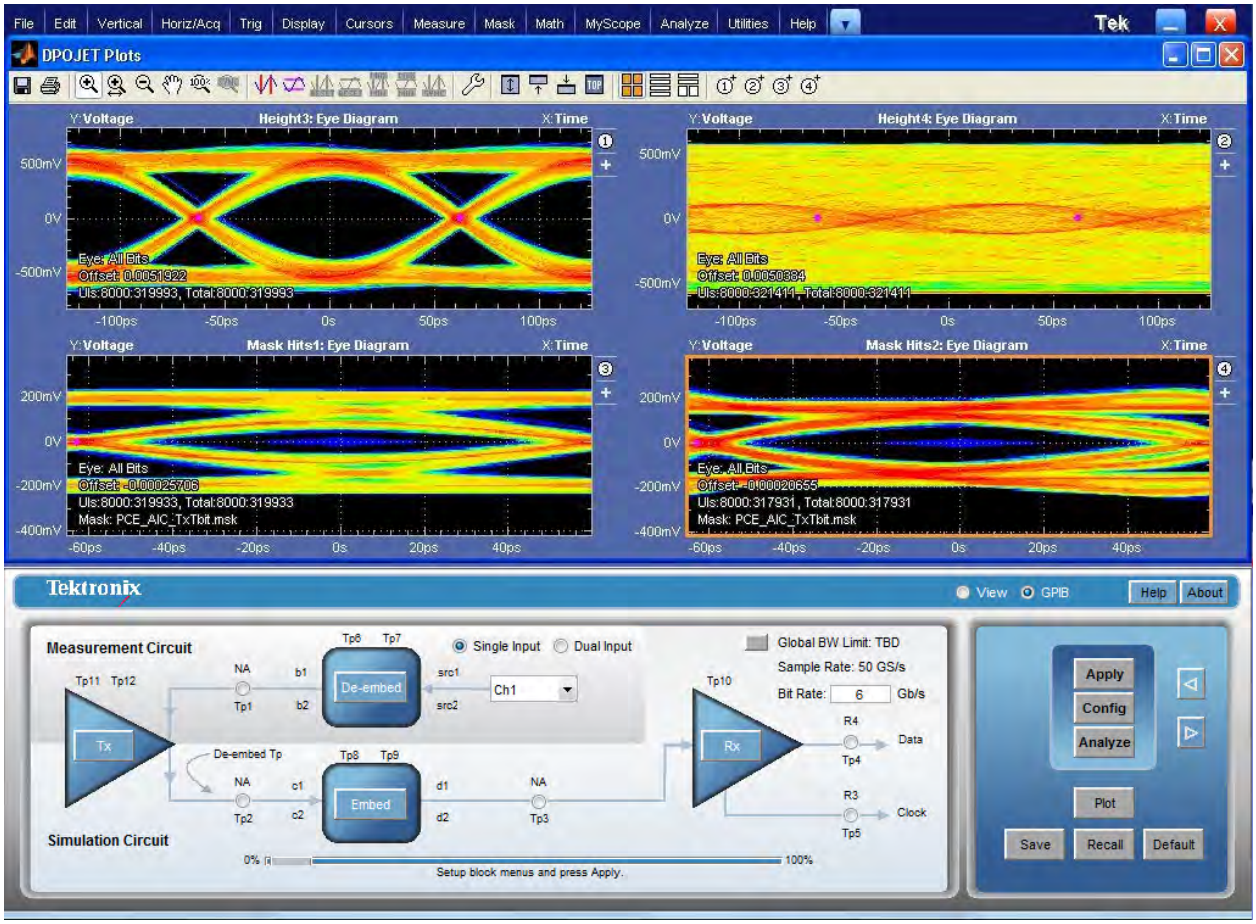


Figure 1: The Tektronix SDLA Visualizer offers a powerful, flexible set of modeling tools for de-embedding, embedding and equalizing high speed serial signals. Using a simple user interface with many configurable features, you can model a measurement circuit to de-embed the effects of scopes, probes, fixtures, cables and other equipment from the acquired scope waveform back to the transmitter block. Likewise, you can model and embed a simulation circuit from the transmitter block that simulates possible effects upon the signal. Both single and dual waveform input modes are available.

Getting started

Software updates from the Tektronix web site

Periodic software upgrades may be available from the Tektronix Web site.

To check for upgrades:

1. Go to the Tektronix Web site (*www.tektronix.com*).
2. Press on **Support** and select the item **Downloads, Manuals & Documentation**.
3. Enter "**SDLA**" in the **MODEL OR KEYWORD** text box.
4. Select **Software** in the **SELECT DOWNLOAD TYPE** drop-down list.
5. Press **Go** to find the available software upgrades.
6. Press the appropriate software title. Read the application information to be sure that it is compatible with your instrument model.
7. Press **Login to access this content** and log in to access the download.
8. Press the **Download File** link.

Requirements and installation

The SDLA Visualizer application is installed on the following instruments:

- Tektronix DPO/DSA/MSO70000/C/D/DX Series oscilloscopes before they leave the factory
- Tektronix DSA8300 sampling oscilloscopes

The installation provides ten free uses of the full featured SDLA Visualizer application.

Requirements for Proper Operation

RT oscilloscope: The SDLA Visualizer application requires a Tektronix DPO/DSA/MSO70000/C/D/DX Series Oscilloscope with a single shot bandwidth ≥4.0 GHz.

To perform jitter and timing analysis, it also requires the following:

- RT oscilloscope: Tektronix DPOJET Jitter and Eye-diagram Analysis software
- Sampling oscilloscope: Tektronix 80SJNB Jitter, Noise and BER Analysis software

To ensure accurate acquisitions, be sure to properly calibrate your oscilloscope by running the signal path compensation. The length of time between SPC and temperature changes at the instrument location dictate when this should be done.

Software Compatibility

Refer to the product Release Notes or the Optional Applications Software Installation manual for the compatible versions of oscilloscope software and for DPOJET (RT oscilloscopes) and for 80SJNB (sampling oscilloscopes).

Option Key Requirement

You must have a valid option key for the application. Without the key, there are free trials. Consult with your Tektronix Applications Engineer or Account Manager for details.

Reinstalling the SDLA Visualizer Software

To install the latest version of SDLA Visualizer software, press *Software Updates From the Tektronix Web Site*.

Conventions

The online help uses the following conventions:

- DUT refers to the Device Under Test.
- When a step requires a sequence of selections, the > delimiter indicates the path from menus to sub-menus and to menu options.
- The directory path to support files is C:\Users\Public\TekApplications \SDLA.
- (RT only) indicates a feature available on real-time oscilloscopes, but not available on sampling oscilloscopes.

Application file types and locations

The software uses the following file types and locations. The support files are arranged in folders with descriptive names at C:\Users\Public\Tektronix \TekApplications\SDLA:

- Input filters – FIR and IIR filter files
- Input S-parameters – Touchstone 1.0 version
- Output filters – where the software stores generated FIR filters when the **Apply** button is pressed. The filenames are overwritten each time you click the **Apply** button. You can rename the filter files to save a set of FIR filters for later use.

  These filters are stored in the directory entitled C:/users/public/Tektronix/ TekApplications/SDLA/output filters.

  Default naming conventions:

  For Single Input mode, the filenames are:

  Sdlatp1.flt, sdlatp2.flt, …. Sdlatp<n>.flt where n is the test point number.

  For Dual Input mode: folders named

  Tp1, Tp2, … Tp<n>

  are created, where n is the test point number. Inside each folder is the set of files.
- Save recall – temporary location where software stores the SDLA Visualizer setup configuration files.
- Example waveforms (RT only) – Example waveform files to help you learn the application.

Your custom S-parameter files and filter files can reside at any path accessible to the instrument.

Moving between applications

The quickest way to move between software applications is to hold down the keyboard Alt key and tap the Tab key to pick an application.

An alternative is to use the triangle buttons on the right side of the Main Menu to switch between the SDLA Visualizer, TEKScope and DPOJET/JNB applications:

- Press the left triangle to bring the oscilloscope waveform display to the foreground.
- Press the right triangle to bring the oscilloscope waveform display into view with SDLA Visualizer application still in the foreground. This option is handy when also using the DPOJET/JNB application.

You may bring all the SDLA Visualizer windows to the foreground by first pressing the minimize button at the upper right corner of the oscilloscope window to collapse it to the Windows tool bar. Then press the right triangle on SDLA to expand the scope back to full screen with SDLA in the foreground.

Online help

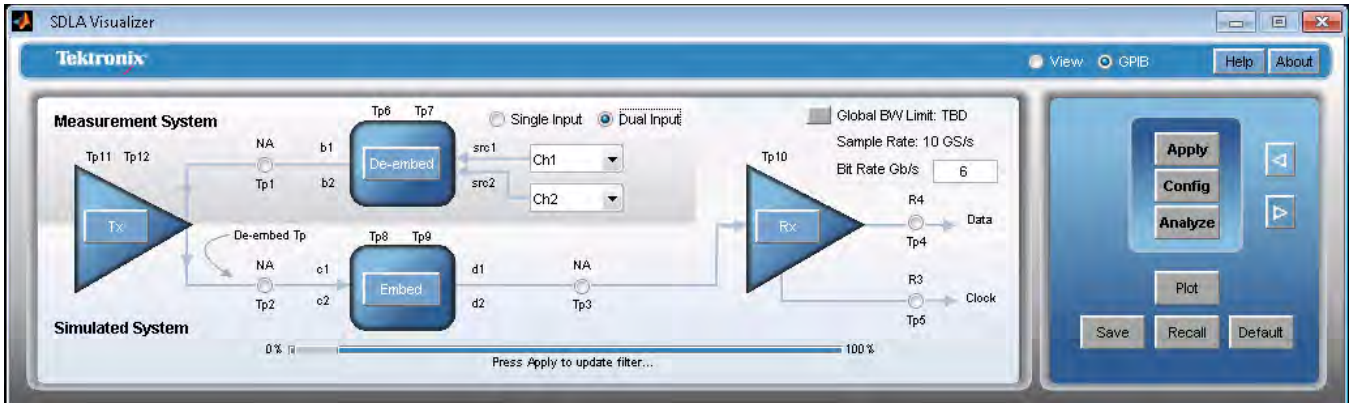
Help in Different Languages

If you would like to download a .PDF file of the Online Help that has been translated into Japanese, simplified Chinese, or Korean, visit www.tektronix.com and press on “Change Country” at the top. Then enter the search term “SDLA Visualizer”.

Press the **Help** button in the upper right corner of the SDLA Visualizer Main Menu to bring up the online Help system. Pressing the **F1** key at any time also brings up the Online Help system.

Product overview

SDLA visualizer product overview



The Tektronix SDLA Visualizer offers a powerful, flexible set of modeling tools for de-embedding, embedding and equalizing high speed serial signals. Using a simple user interface with many configurable features, you can model a measurement circuit to de-embed the effects of scopes, probes, fixtures, cables and other equipment from the acquired scope waveform back to the transmitter block. Likewise, you can model and embed a simulation circuit from the transmitter block that simulates possible effects upon the signal. (RT only): Both single and dual waveform input modes are available.

SDLA Visualizer offers full 4-Port S-parameter modeling support that takes into account the Tx and Rx impedance models, along with all transmission line characteristics. The signal path is fully represented by a unique cascading S-parameter feature; if any parameter changes anywhere in the cascade, it affects all test points in the cascade.

With the ever increasing data speeds for high speed serial links, PAM-4 is gaining popularity as the new signaling of choice to double the date rate without doubling the bandwidth of the delivery network. SDLA now supports PAM-4 Rx modeling in its Rx Block, including PAM-4 aware clock date recovery and equalization methodology.

Many standards require that equalization is applied to the signal before measurements are taken. SDLA Visualizer provides CTLE, FFE and DFE equalization modeling tools with support for serial standards such as PCI Express 3.0/4.0, USB 3.0/3.1, Thunderbold 10G/20G, and SAS. Also available is an IBIS-AMI model (RT only) that lets you use equalization files supplied by a chip vendor.

Validation is simplified with a rich set of plotting tools, including S-parameter plots, time domain plots, Smith chart, and overlay tools. These plots are available starting with the cascade block configuration stage, providing confidence that the input models (i.e. S-parameters) are correct.

After the circuits are defined, SDLA Visualizer provides the ability to observe the signal via 12 user-defined test points, including 4 that are movable within the De-embed and Embed Blocks. You may view multiple test points simultaneously, and observe areas of the signal that you could not probe otherwise. Up to four math and two reference waveforms are visible on the scope graticule at one time. You are able to see the differential, common mode, or individual inputs of the signal at once, without having to create multiple models for each option. You can also create test point filter (transfer function) plots that allow for verification of the system setup. Magnitude, Phase, Impulse and Step plots are available.

SDLA is intended to be used along with Tektronix DPOJET Real-time Jitter and Timing Analysis software (RT scopes) or JNB Jitter, Noise, and BER Analysis software (sampling oscilloscopes). Together, these tools provide deep insight and analysis capabilities so that you can visualize an entire signal processing path and accurately measure the true signal from the DUT.

Some tasks you can accomplish using SDLA Visualizer

- Remove the effects of reflections, cross-coupling, and loss caused by non-ideal probe points, fixtures and cables
- Remove the effects of interposers using 3, 4, or 6-port S-parameter models
- Simulate and measure at test points using actual captured waveforms where physical probing is not practical
- Observe the signal at the end of the link by embedding user-defined channel models into the waveform at the transmitter
- Add or remove transmitter equalization, using 2 or 3-tap filter coefficients or FIR filter
- Open closed eyes using CTLE, clock recovery, DFE and FFE equalization
- Model silicon-specific receiver equalization algorithms using IBIS-AMI models (RT only), so you can virtually view the signal inside of the receiver
- De-embed high impedance or SMA probes
- Model RLC, TDT waveforms, and lossless transmission lines in the absence of S-parameters
- Create S-parameter plots, time domain plots, and Smith Chart plots for quick verification of S-parameters and test point transfer functions
- Perform quick analysis of jitter and timing parameters using integrated DPOJET/JNB support
- Work with DDR and next generation serial standards including PCI Express 3.0/4.0, USB 3.0/3.1, Thunderbolt 10G/20G, SAS 6G, SATA, and DisplayPort (including interposer model)

For more information:

Understanding the System

Using DPOJET and SDLA Visualizer together

Using JNB and SDLA Visualizer together

Running a Test: Recommended Order

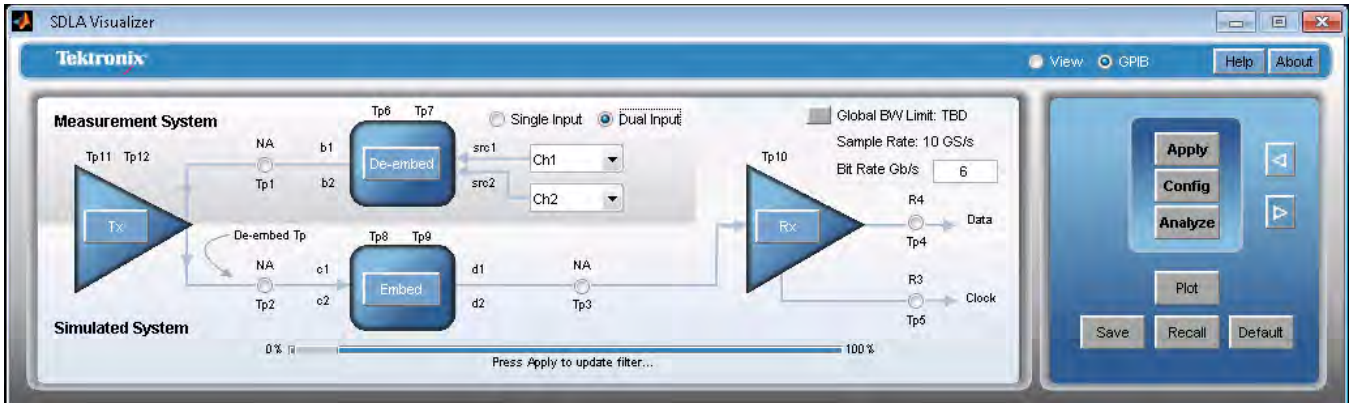
NOTE. *Pressing the F1 key at any time brings up the Online Help system.*

NOTE. *If you would like to download a .PDF file of the Online Help that has been translated into Japanese, simplified Chinese, or Korean, visit www.tektronix.com and press on "Change Country" at the top. Then enter the search term "SDLA Visualizer".*

SEE ALSO:

- *Main Menu in Detail*
- *Examples of Tasks and Troubleshooting*

Understanding the system



SDLA Visualizer requires you to define two circuit models, the Measurement Circuit and the Simulation Circuit, that both connect to the **Tx Block**. The Tx Block makes use of Thevenin equivalent voltage to provide a point where the acquired waveform is passed into the simulation side of the system. (Thevenin's Theorem states that it is possible to simplify any linear circuit, no matter how complex, to an equivalent circuit with just a single voltage source and impedance.)

The Measurement Circuit

The upper part of the Main Menu diagram stemming from the Tx Block represents the Measurement Circuit: the probes, scope, fixtures and the portion of the channel between the Tx and the fixture. (Note that this diagram changes, reflecting whether Single or Dual Input mode is specified.) This is where the S-parameter models that represent the physical test and measurement system used to acquire the signal need to be defined and loaded into the **De-embed Block**. In the absence of S-parameters, you can use RLC or lossless transmission line models.

The **test points** in this circuit represent simulated probing locations that allow visibility of the link at multiple test locations, including two movable test points within the De-embed Block. The software derives the transfer function(s) and creates FIR filters for each test point. When the filters are applied to the waveform(s) acquired from the scope, SDLA produces waveforms at the desired test points. The waveform with the loading of the Measurement Circuit can be viewed at **Tp1**, **Tp6**, or **Tp7**.

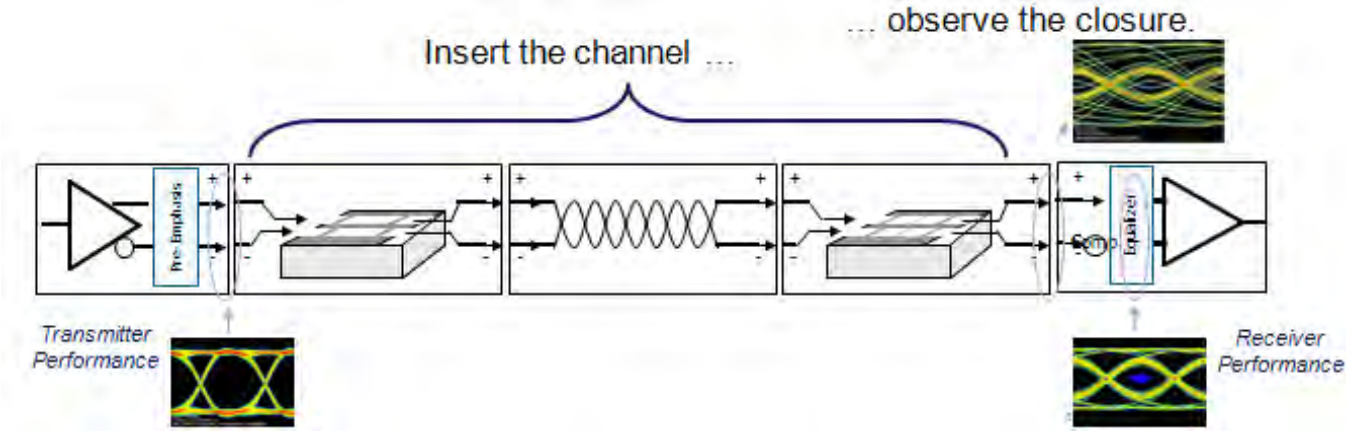
The Simulation Circuit

The lower part of the Main Menu diagram stemming from the Tx Block represents the Simulation Circuit. Now that the waveforms have been de-embedded back to the Tx Block, the Simulation Circuit is used to embed a simulated channel to the Tx Block. The S-parameter models for the link you would like to simulate need to be defined and entered into the **Embed Block**. Again, you may use an RLC or a lossless transmission line models when S-parameters are not available. The load of the receiver is also modeled in the Embed Block. The **Rx Block** allows you to specify Rx equalization. The **test points** in this circuit allow visibility in between link components, including two movable test points within the Embed Block. **Tp2** shows the Tx output waveform without the loading of the Measurement Circuit, but with the loading of Simulated Circuit.

NOTE. *The arrows on the Main Menu circuit diagram show the order in which SDLA processes the transfer functions. For the Measurement Circuit part of the diagram, the ACTUAL signal flow is in the opposite direction of the arrows. For the Simulation Circuit, the actual signal flow direction is the same as the signal processing flow arrows.*

Using the Embed Block to Close the Eye and Rx Block to Open the Eye

The Embed Block lets you “insert” a simulated channel so that you can observe the closed eye (viewable at **Tp3**):



Now, you can use the Rx block to open the eye and observe the signal after CTLE **(Tp10)** or after FFE/DFE **(Tp4)** as been applied. The **Rx Block** allows you to specify Rx equalization. Serial data receivers typically contain three kinds of equalizers: a continuous-time linear equalizer (CTLE), a feed-forward equalizer (FFE), and decision feedback equalizer (DFE)). CTLE, clock recovery, DFE and FFE equalizers are available in the Rx Block; alternatively, IBIS-AMI models (RT only) can be used to model silicon specific equalization algorithms. Also, three test points are available in the **Rx Block**. These allow for visibility of the waveform after CTLE and/or after FFE/DFE and recovered clock, or an IBIS-AMI model has been applied.

Test Points

With 12 test points, SDLA Visualizer gives you visibility over multiple test points simultaneously, providing virtual "observation points" of the signal that you could not probe otherwise. You can view the transmitter signal with the loading of the measurement circuit at **Tp1**, and at the same time, view the de-embedded measurement circuit at **Tp2** with an ideal 50 Ohm load. You have many flexible options for labeling test points, and for mapping test points to math waveforms. It is easy to put the test point labels onto the scope waveform display, so you can tell which waveform is which, and easy to apply the data to DPOJET/JNB, so that you know which waveform you're doing the measurement on. A **Delay** feature lets you move the waveforms in time with respect to each other. (By default, the delay is removed from the test point filters, so that events are close to being time-aligned.)

SDLA Visualizer provides up to 6 waveforms (four math and two reference) that are simultaneously visible on the scope graticule at one time, allowing visibility of the link at different locations. (You use the Test Point and Bandwidth Manager to map the SDLA test points to the math and reference waveforms.) The software allows for dynamic configuration of test points in order to best utilize the scope math channels (i.e. after de-embedding, CTLE, etc.) Also, four test points can be moved on the De-embed and Embed Menu cascade diagrams, providing maximum flexibility. Press here for a *deeper understanding of how test points work*.

Once the simulation and measurement circuits have been defined, you can easily save test point filters that can be used with the scope math system. For details, see *Saving Test Points*.

Modeling Block View

Another way to view the system is as a series of modeling blocks for de-embedding the effects of the waveform acquisition hardware setup, and modeling blocks for embedding link components that are not represented physically.

These diagrams illustrate the entire S-parameter processing path.

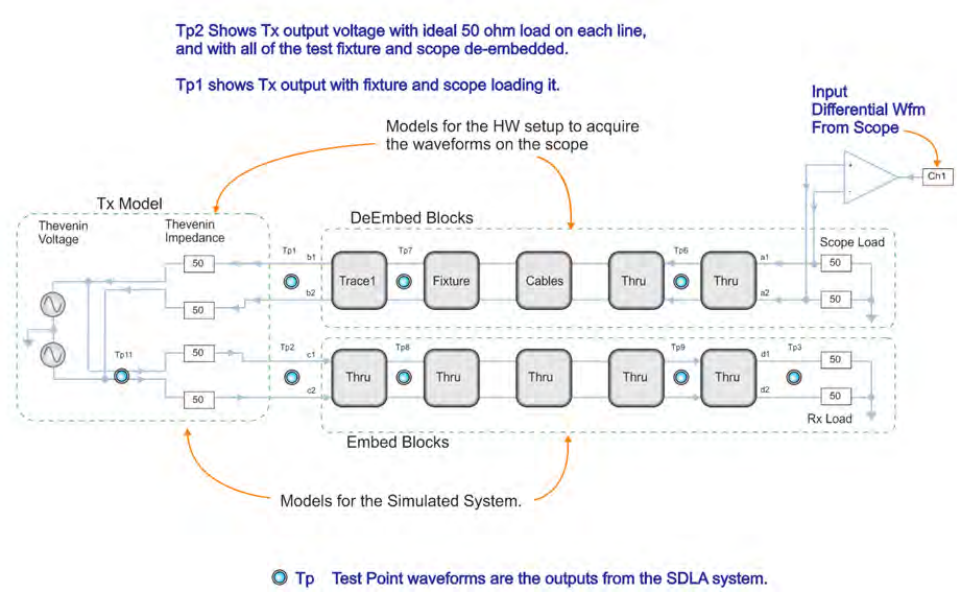


Figure 2: Single Input Mode

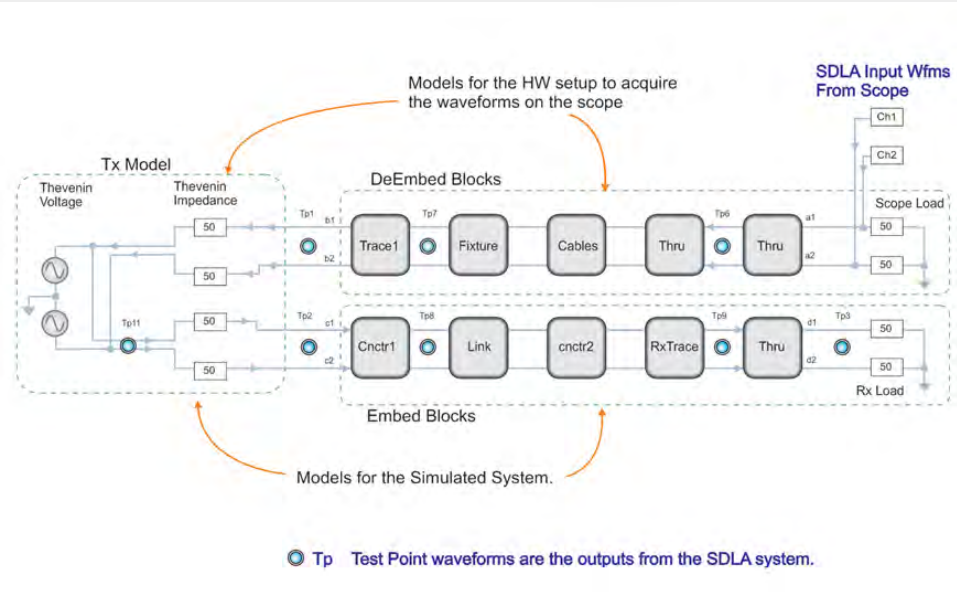


Figure 3: Dual Input Mode

Dual and Single Input Modes

In some cases, it is desired to process each leg of the signal individually through the network, in order to completely take into account differences in the two sides of the signal. SDLA Visualizer offers a choice of Dual Input (RT only) or Single Input modes on the Main Menu. In Single Input mode, the differential signal may be viewed at each test point. Dual Input mode (RT only) allows the viewing of individual inputs, differential, or common mode. For additional information, see *Full 4–port Modeling.*

Algorithms, theory and math derivations

For in-depth information on several advanced SDLA topics, including algorithms, theory, math derivations for re-normalizing S-parameters and converting single-mode S-parameters to mixed mode, see technical papers located at www.tek.com/sdla.

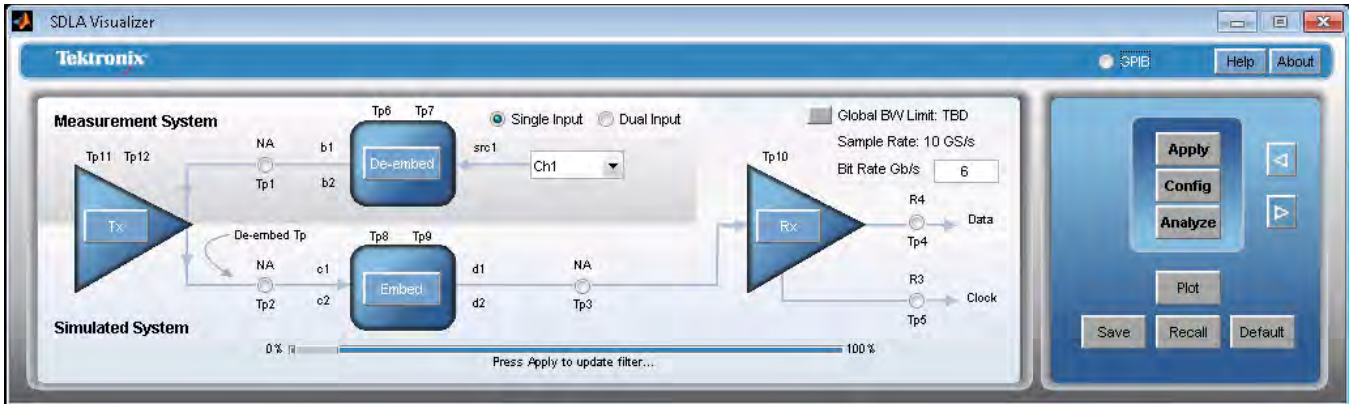
SEE ALSO:

- *Using DPOJET and SDLA Visualizer Together*
- *Product Overview*

Understanding test points

Test points output waveforms that represent the signal at a particular position in the system circuit diagram. Each test point waveform is obtained by applying at least one filter to the input waveform(s) acquired by the oscilloscope.

SDLA Visualizer provides up to 12 test points (when using the REF waveforms). Up to 6 test point outputs are viewable on the scope graticule at one time: four math and two reference. The SDLA processing and analysis operate only on waveforms that have been turned on and are displayed on the oscilloscope.



Press here for a Table of Test Point Descriptions.

Test point	Position	Description
Tp1	Main	Measurement circuit loading the Tx block output
Tp2	Main	Simulation circuit loading the Tx block output, measurement circuit de-embedded
Tp3	Main	Rx block input. Simulation circuit loading the Tx block output, measurement circuit de-embedded
Tp4	Rx Eq Data	Data output of the Rx block after equalization
Tp5	Rx Eq Clock	Test point for the recovered clock output of the Rx block
Tp6	De-embed Block	Movable test point with the measurement circuit loading the Tx block output
Tp7	De-embed Block	Movable test point with the measurement circuit loading the Tx block output
Tp8	Embed Block	Movable test point with the simulation circuit loading the Tx block output, measurement circuit de-embedded
Tp9	Embed Block	Movable test point with the simulation circuit loading the Tx block output, measurement circuit de-embedded
Tp10	CTLE	CTLE output
Tp11	Tx	Thevenin equivalent voltage of the Transmitter model
Tp12	Tx	Test point for the output of the Tx Emphasis block (if on)

Test Point and Bandwidth Manager

Pressing on a test point on the Main Menu brings up the **Test Point and Bandwidth Manager**, which is used to configure test points and modes (Dual Mode only) and to save test point filters. For details, see *Test Point and Bandwidth Manager*.

How Test Point Filters are Applied

The test point filters are derived from the S-parameter models that are contained in the De-embed, Tx, and Embed Blocks. These filters are of type FIR, which are convolved in the time domain with the source waveforms acquired on the oscilloscope. Press here for details on what generally happens when test point filters are applied.

Real-Time Scopes

1. First, you have to enter the S-parameters or models that will determine S-parameters for each of the blocks and terminations throughout the system using the Tx Block and De-embed/Embed Menu.
2. You also need to turn on and define the desired test points by pressing on a test point on the Main Menu and using the Test Point and Bandwidth Manager.
3. Finally, you press the **Apply** button in the SDLA Visualizer Main Menu. The software computes the filters (transfer functions) for each test point that has been turned on using the Test Point and Bandwidth Manager. These filters are then stored in the directory entitled C:/users/public/Tektronix/TekApplications/SDLA/output filters. (You may also save the filters from the Test Point and Bandwidth Manager into files using your own names or folder.)

   Default Naming Conventions

For Single Input mode, the filenames are:

Sdlatp1.flt, sdlatp2.flt, …. Sdlatp<n>.flt where n is the test point number.

For Dual Input mode: folders named

Tp1, Tp2, … Tp<n>

are created, where n is the test point number. Inside each folder is the set of files.

At the same time, SDLA loads the filters that have been turned on into the oscilloscope math menu, and creates a math expression that will display live waveforms for the selected test points on the oscilloscope graticule.

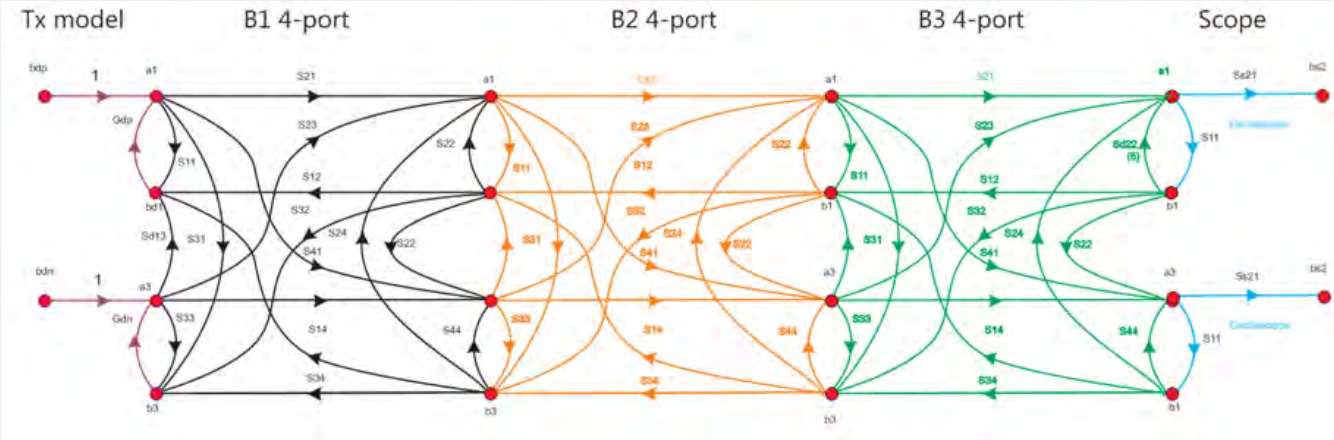
Sampling Scopes

The above holds for sampling scopes except that only Single Input mode is available.

Crosstalk and Reflection Handling

SDLA Visualizer uses all elements of the S-parameter models to compute the transfer functions for test points. Press here for an illustration of the signal flow graph.

Shown below is an example of the signal flow graph for three cascaded 4-port networks. This illustrates the effects that cross-talk paths, transmission paths, and reflection paths have on the overall transfer function from one point in the network to another point in the network. SDLA Visualizer uses all of these S-parameter paths to compute the transfer functions for test points.



Full 4-port Modeling

This system maintains full 4-port modeling. Therefore, the test points are differential, and each contains a set of four possible waveforms (test point modes) to view.

Dual input mode (RT only)

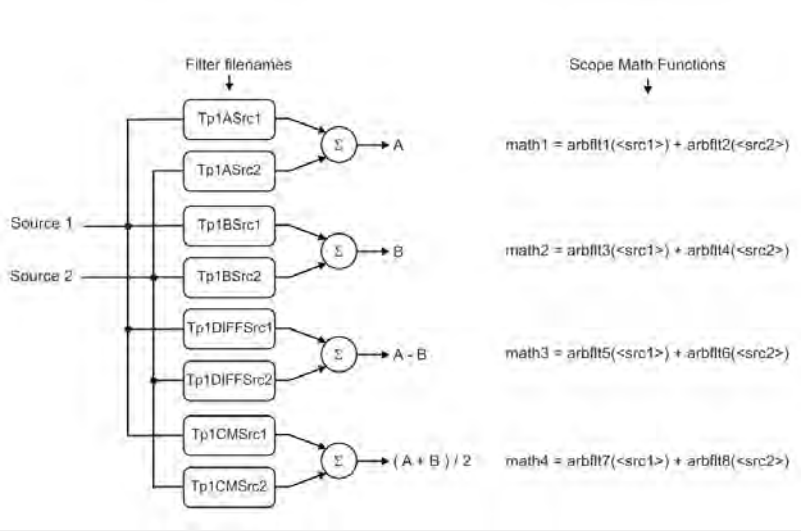
- Dual input selection takes two waveforms from two channels, math functions or reference waveforms in the oscilloscope, and processes them through the 4-port system to obtain test point waveforms. When Dual Input mode has been selected on the Main Menu, the Test Point and Bandwidth Manager will show the options for **Select Test Point Mode**. The options are:
  - **A**: the waveform on the upper line of the test point
  - **B**: the waveform on the lower line
  - **A – B**: the differential waveform and
  - **(A + B)/2**: the common mode waveform.

  In Dual Input mode, **each test point can output waveforms for all four modes described above**. Each of these four modes requires two filters applied to the two input waveforms. Press here for example math expressions that SDLA might set up in the oscilloscope Math menu.

An example math expression that SDLA might set up in the oscilloscope Math menu:

Math1 = arbflt1(ch1) + arbflt2(ch2)

Mathematically, only four filters are required for a differential test point. However, this would require two filters each for A and B modes, and all four filters for differential and common modes. In order to simplify to only two filters for any mode, an additional four filters are created from linear combinations of the four basic filters. Thus SDLA creates eight filters for each test point, as shown below:



Single Input mode

- **Real-Time Scopes**

  When Single Input mode is selected on the Main Menu, an assumption is made that a differential input waveform of form A – B is acquired on a single source of the oscilloscope (Src1). SDLA then splits this waveform mathematically into an exactly balanced A and B signal, which is then processed through the 4-port cascaded system.

  For Single Input operation, **the test points throughout the system only utilize the A – B Mode** (differential waveform as output). Only one filter is required, and is applied to the input source waveform to obtain the output test point waveform. An example math expression that SDLA might set up in the Math oscilloscope menu:

  Math1 = arbflt1(ch1)

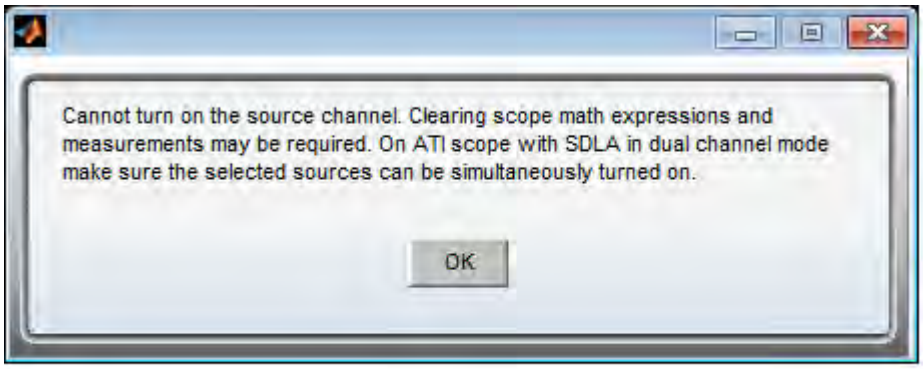
- **Sampling Scopes**

  Sampling scope waveforms are not acquired by SDLA.

Run SDLA on SX oscilloscope

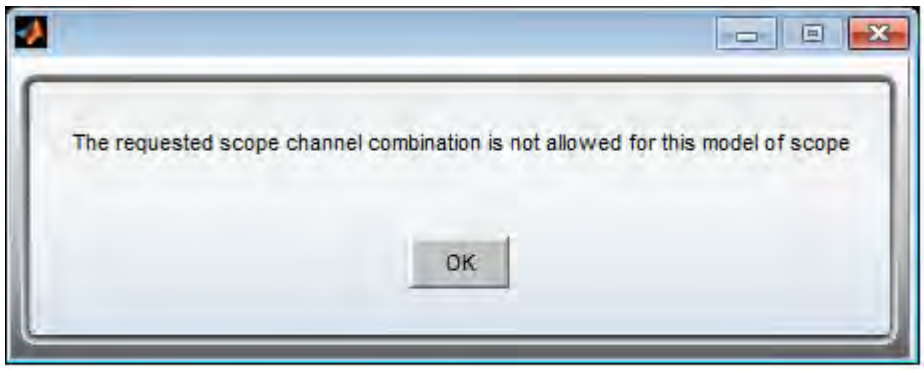
- **Single input**

  SX oscilloscopes allow three live channels: ch1, ch2 and ch3. Selecting channel 4 will display the following error message.



- **Dual Input**

  SX oscilloscopes don't allow mixing ATI and non-ATI channels in Dual Input case. Either two ATI channels or two TekConnect channels can be used as the input source; otherwise an error message is shown:



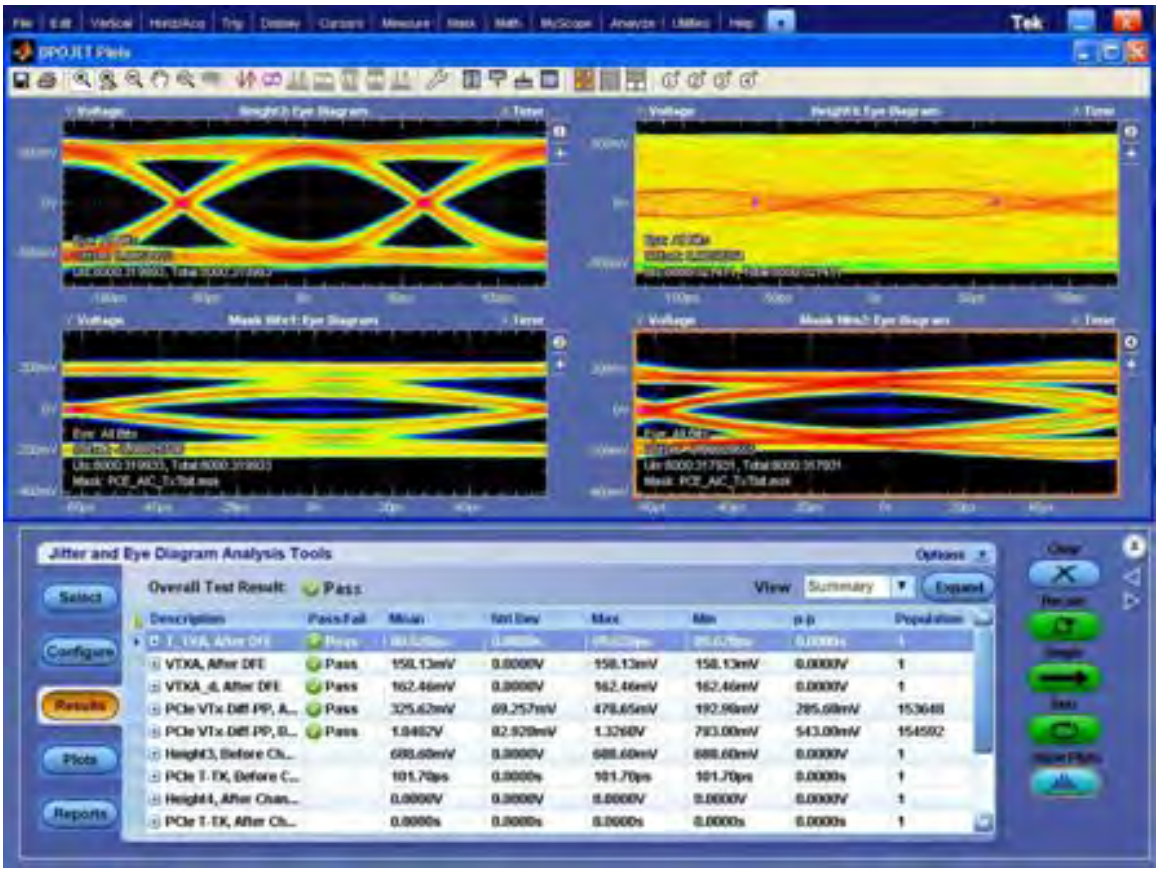
SEE ALSO:

- *Test Point and Bandwidth Manager*
- *Saving Test Points*
- *Main Menu in Detail*
- *Product Overview*.

Using DPOJET and SDLA visualizer together

Together, SDLA Visualizer and DPOJET provide a complete solution for high-speed serial measurement and analysis. DPOJET operation is integrated right into the SDLA Visualizer Main Menu **Analyze** and **Config** buttons. DPOJET gives you the flexibility to analyze and compare the results at multiple points on the link. What's more, it allows multiple measurement configurations; for example, you could easily compare standard-specific vs. silicon-specific clock recovery measurement parameters.

The figure below shows an example where the Analyze button has been configured to automatically run DPOJET without changing the SDLA setup. Here, the PCI Express 3.0 configuration has been defined by the user. Notice how using DPOJET and SDLA Visualizer together gives you full link visibility of the eye diagram and associated measurements for each of the desired test points. The eye diagram on the top left shows the acquired waveform and the input into SDLA. The eye diagram on the top right shows the Simulation Circuit loading the Tx block output **(Tp3)**. The eye diagrams on the bottom show the signal after CTLE **(Tp10)** and after FFE/DFE **(Tp4)**.



To switch between SDLA Visualizer and DPOJET, use the Alt Tab keyboard combination or the navigation buttons (< and >) on the SDLA Main Menu. Use the TekScope application minimize button to minimize the scope window to view the DPOJET and SDLA applications.

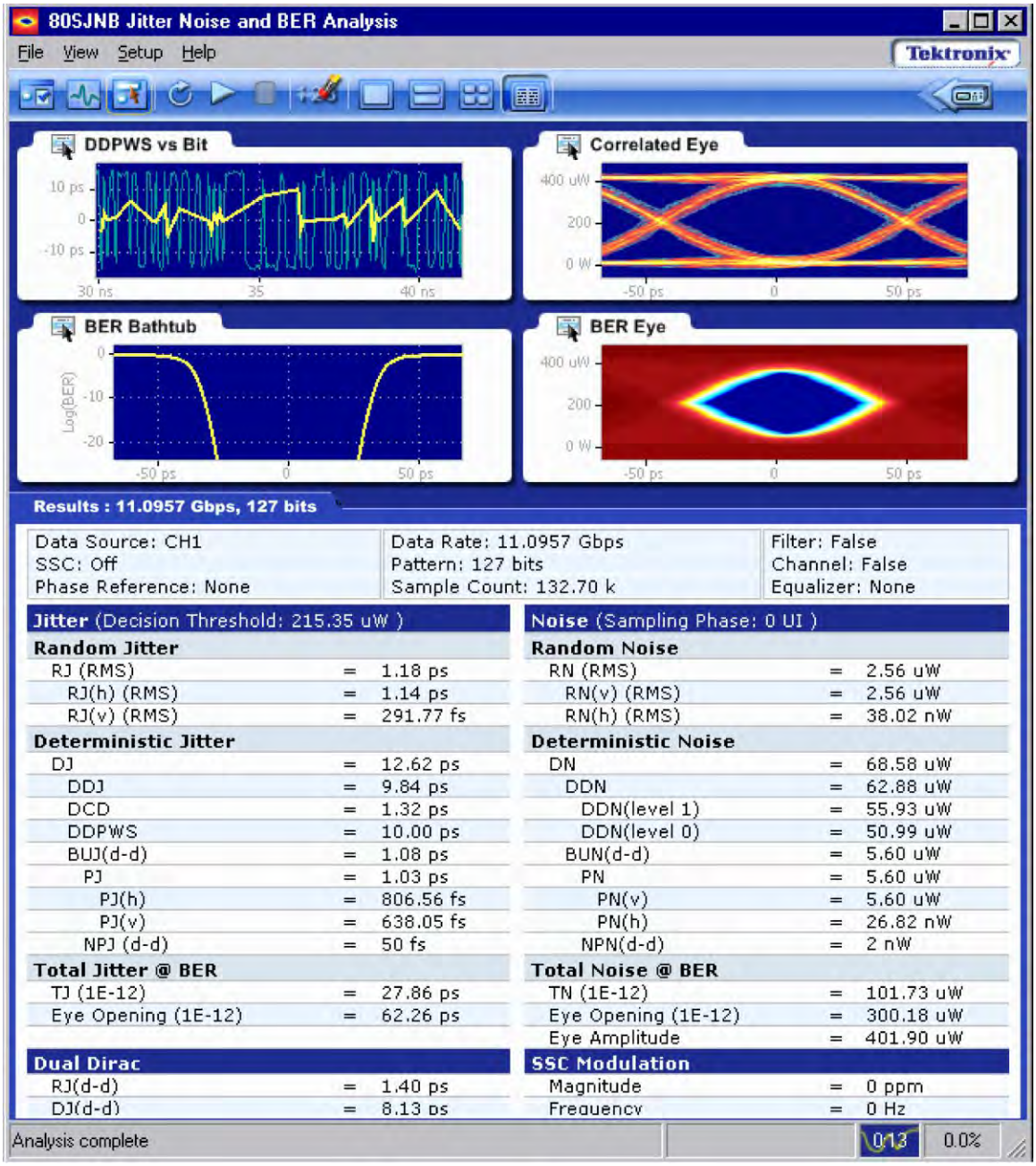
SEE ALSO:

- *Configure Actions for Apply and Analyze Buttons*
- *Product Overview*
- *Understanding the System*

Using JNB and SDLA Visualizer together

Together, SDLA Visualizer and JNB provide a complete solution for high-speed serial measurement and analysis. JNB operation is integrated into the SDLA Visualizer Main Menu **Analyze** button. JNB gives you the flexibility to analyze and compare the results at multiple points on the link.

SDLA Visualizer combines all its inputs into one filter, launches JNB and passes its filter to JNB. The figure below shows the JNB display. Notice how using JNB and SDLA Visualizer together gives you full link visibility of the eye diagram and associated measurements for the desired test points.



To switch between SDLA Visualizer and JNB, use the Alt Tab keyboard combination or the navigation buttons (< and >) on the SDLA Main Menu. Use the TekScope application minimize button to minimize the scope window to view the JNB and SDLA applications.

SEE ALSO:

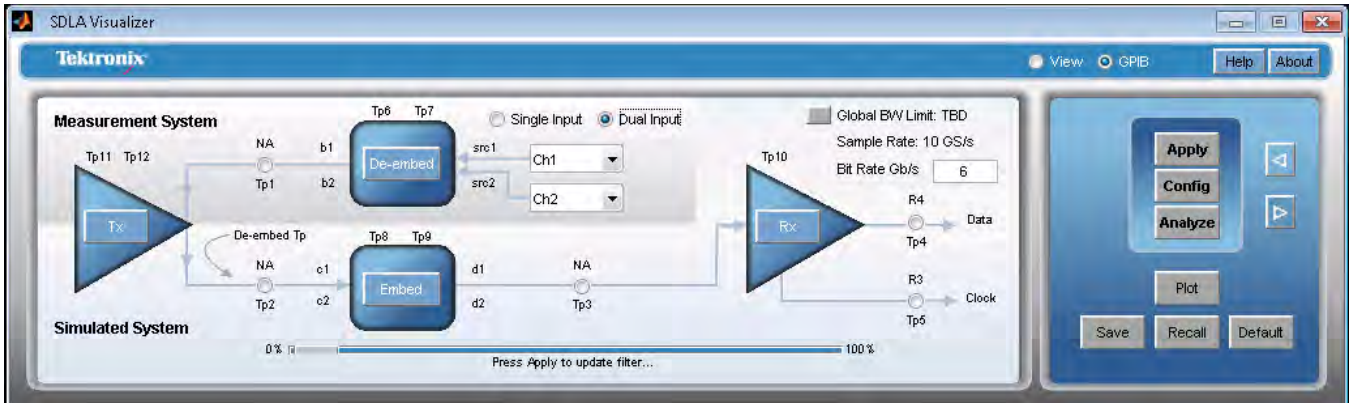
- *Configure Actions for Apply and Analyze Buttons*
- *Product Overview*
- *Understanding the System*

Components and menus

Main menu in detail

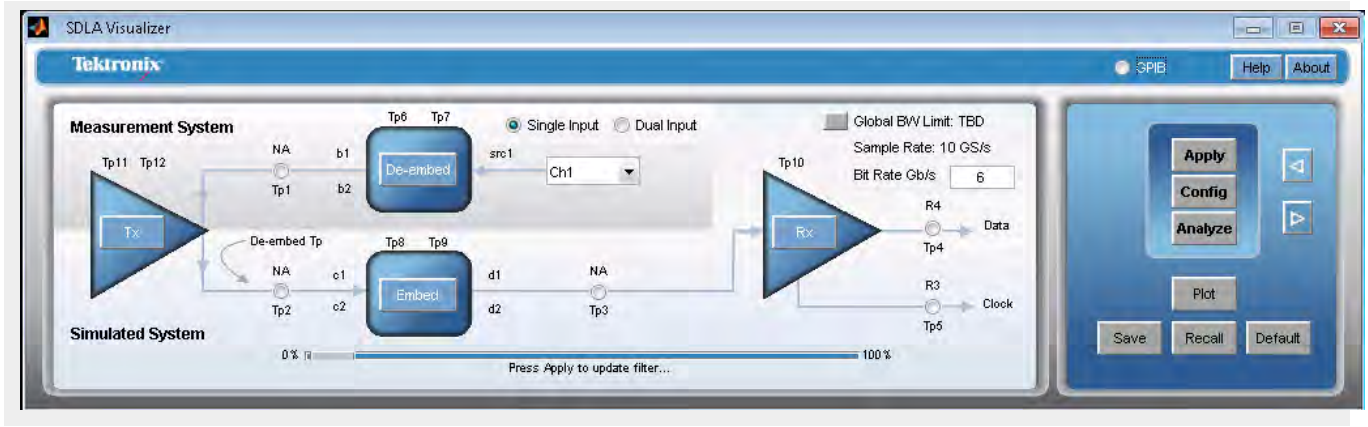
Use the SDLA Visualizer **Main Menu** to configure the blocks, models, and test points, and to apply, plot and analyze the data.

The upper part of the circuit diagram shows the Measurement Circuit model, and the lower part shows the Simulation Circuit model. The arrows show the order in which SDLA processes the transfer functions. Note that for the Measurement Circuit part of the diagram, the ACTUAL signal flow is in the *opposite direction of the arrows*. For the Simulation Circuit, the actual signal flow direction is the same as the signal processing flow arrows.



Inputs

You can use either one or two inputs with SDLA Visualizer by selecting either Single Input or Dual Input mode. Changing these radio buttons will change the configuration panels here and elsewhere. The image above displays Dual Input mode. Press here to view Single Input mode.



Global BW Limit

This displays the current bandwidth. Pressing on the **BW** button brings up the *Test Point and Bandwidth Manager*, where you can set and *create custom BW limit filters*.

Sources

The SDLA processing and analysis operate only on waveforms that are displayed on the oscilloscope. You can select from actively acquired channel signals, Math waveforms or reference waveforms. For a live acquired waveform, select its channel number. To recall a reference waveform, select **File>Reference Waveform Controls** in the oscilloscope menu. Then press **Recall** in the Reference menu to bring up the Recall browser.

De-embed Block

The De-embed Block contains the circuit models that represent the actual hardware probe, fixtures, etc. that were used to acquire the waveforms with the oscilloscope acquisition system. Here, you can define the effects of the fixture, probe, scope and other acquisition and measurement hardware upon the DUT signal, re-normalize the S-parameter reference impedance, perform singled-ended to mixed mode conversion, reach the Block Configuration menu for Thru, File, RLC and T-line options, add and configure High Z, SMA probes, or interposer, and many other tasks. For more information, see the *De-embed/Embed Menu*.

Test Points

Test points output waveforms that are displayed live on the oscilloscope. You may bring up the **Test Point and Bandwidth Manager** by pressing a test point on the system circuit diagram on the Main Menu. From here, you can configure the individual output waveforms and save test point filters. (When Dual Input mode has been selected on the Main Menu, you can also select test point modes.) You can also set a Global BW limit and create a custom BW limit filter. For more information, see *Test Point and Bandwidth Manager*.

Tx Block (Transmitter Modeling Block)

The Tx Block represents the model of the serial data link transmitter that is driving both the Measurement Circuit model and the Simulation Circuit model. Pressing **Tx** on the Main Menu brings up the Tx Configuration Menu, where you can select files and view plots. It also gives you access to the Tx Emphasis Menu, where you can select emphasis, de-emphasis or pre-emphasis filters, read from FIR filters and make other choices. For more information, see the *Tx Block Overview*.

Embed Block

The Embed Block allows the user to "insert" the channel based on its S-parameters, as a lossless transmission line, or as an RLC model, in order to observe the waveforms at the various test points on the Simulation Circuit model. Pressing **Embed** on the Main Menu brings up the *De-embed/Embed Menu,*. Use this for the same tasks as the De-embed Block above, except you cannot configure a probe.

Rx Block (Receiver Modeling block)

The Rx Block represents the model for the serial data link receiver for the simulation side of the circuit drawing. Pressing **Rx** on the Main Menu brings up the Rx Configuration Menu. Here, you may apply CTLE equalization, perform clock recovery, and apply FFE/DFE equalization. You also configure PAM-4 versus NRZ Rx modeling in this block. Alternatively, you may set up an AMI model that uses imported equalization files to emulate actual silicon. For more information, see the *Rx Block Overview*. Note: the Rx load is defined in the Embed Block, not the Rx Block.

Apply, Config and Analyze buttons

Apply

By default, this computes test point filters and applies them to the scope. If any SDLA configuration is changed, run Apply to get updated results. Some configuration options are available, as described below.

Analyze

Pressing **Analyze** performs waveform analysis with the DPOJET/JNB application. The SDLA application is put into a sleep state and then the DPOJET/JNB application is started with the test point signal(s), and the recovered data and clock signals selected for analysis. The SDLA software may configure (RT only) the DPOJET application to analyze the link quality with eye diagrams and jitter measurements. Note that you must first press the **Apply** button and wait for filter processing to complete before pressing the **Analyze** button. The DPOJET/JNB application must be installed for this transfer to work.

Config

This button (RT only) lets you configure the action of the Apply button as well as the Analyze button with DPOJET, and to determine whether to use a new or a previously acquired waveform. *Press here for Apply and Analyze button configuration options*.

Plot button Press to show the results of running the enabled test points. *Press here for more about plots.*

Default button Press to restore the SDLA Visualizer system to its default settings.

Save button Press to save the current SDLA Visualizer setup to a file with a .sdl file extension in the directory SDLA\Save recall.

NOTE. *Only the SDLA setup is saved and recalled, not the entire oscilloscope setup.*

Recall button Press to recall saved setup files and to return the software to a previous configuration.

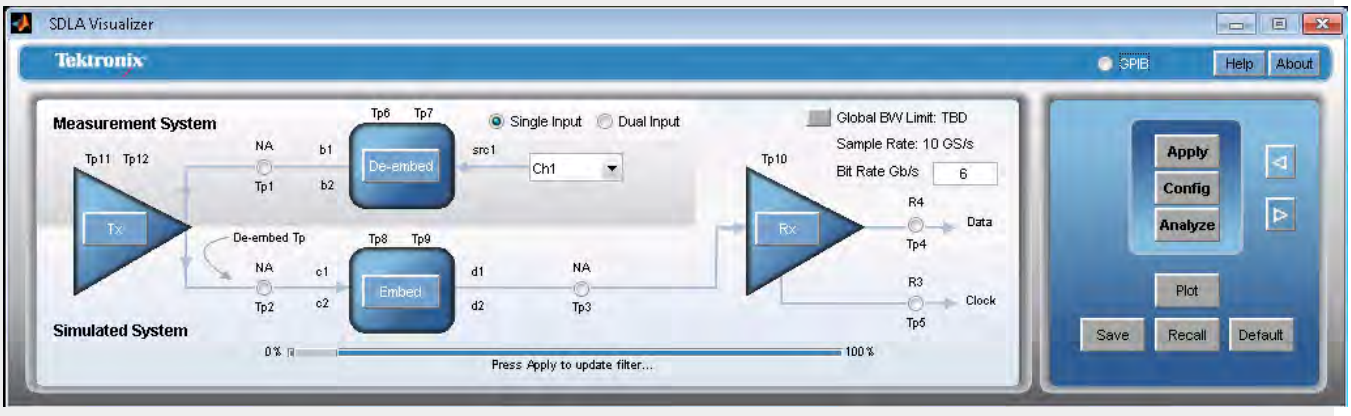
SEE ALSO:

- *Product Overview*
- *Running a Test: Recommended Order*
- *Solving Problems with SDLA Visualizer*

Test points

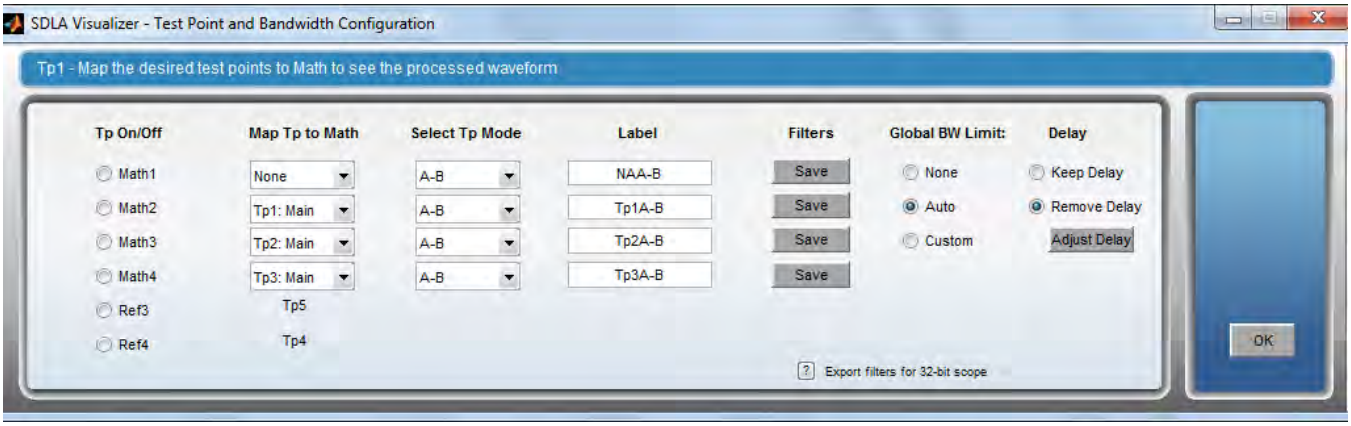
Test point and bandwidth manager (RT only) SDLA Visualizer provides up to 12 test points (when using REF for two), including four test points that can be moved on the schematic drawing. Up to six test point outputs are viewable on the scope graticule at one time (math plus reference). Press here for a Table of Test Point Descriptions.

NOTE. *For a conceptual overview of how test points work, see Test Point Locations.*



Test point	Position	Description
Tp1	Main	Measurement circuit loading the Tx block output
Tp2	Main	Simulation circuit loading the Tx block output, measurement circuit de-embedded
Tp3	Main	Rx block input. Simulation circuit loading the Tx block output, measurement circuit de-embedded
Tp4	Rx Eq Data	Data output of the Rx block after equalization
Tp5	Rx Eq Clock	Test point for the recovered clock output of the Rx block
Tp6	De-embed Block	Movable test point with the measurement circuit loading the Tx block output
Tp7	De-embed Block	Movable test point with the measurement circuit loading the Tx block output
Tp8	Embed Block	Movable test point with the simulation circuit loading the Tx block output, measurement circuit de-embedded
Tp9	Embed Block	Movable test point with the simulation circuit loading the Tx block output, measurement circuit de-embedded
Tp10	CTLE	CTLE output
Tp11	Tx	Thevenin equivalent voltage of the Transmitter model
Tp12	Tx	Test point for the output of the Tx Emphasis block (if on)

The Test Point and Bandwidth Manager is reached by pressing any test point on the Main Menu. Use this to configure the individual output waveforms, to save test point filters, to set the Global BW limit or to create a custom BW limit filter. You can also select test point modes if Dual Input is selected on the Main Menu. (If Single Input is selected, the **Select Tp Mode** column will not appear.) Scroll down for descriptions of each feature.



Tp On/Off. Controls which of the six (4 math and 2 reference) active test point waveforms are on or off. Each radio button lists the name of one of the available Math functions or a Ref memory waveform in the oscilloscope. If the button is off, then the waveform on the oscilloscope screen is turned off. If the button is on, then the waveform on the oscilloscope screen is turned on.

Map Tp to Math. This drop-down menu allows a specific test point to be assigned to a math function of Math1, Math2, Math3, or Math4. The same test point may be assigned to more than one math slot.

NOTE. *SDLA only processes and creates test point filters for the enabled test points. An enabled test point is a Tp that has been mapped to a Math or Ref waveform, and the corresponding Math or Ref is turned on.*

Select Tp Mode. This column is only visible when **Dual Input** has been selected on the Main Menu. Press here for more information.

This system maintains full 4-port modeling. Therefore, the test points are differential, and each contains a set of four possible waveforms (test point modes) to view. The options are:

- **A**: the waveform on the upper line of the test point
- **B**: the waveform on the lower line
- **A – B**: the differential waveform and
- **(A + B)/2**: the common mode waveform.

Label. A label for the test point waveform can be entered into this box. It will appear on the oscilloscope screen along with the waveform.

Save Filters. You can save each test point filter into the file folder you specify by pressing the **Save** button next to the test point label. For more information, see, *Saving Test Points*.

Filter Scaling Factor. Filter Scaling Factor is located at the bottom of the configuration menu in the single input case only. It scales the test point filter coefficient according to the value.

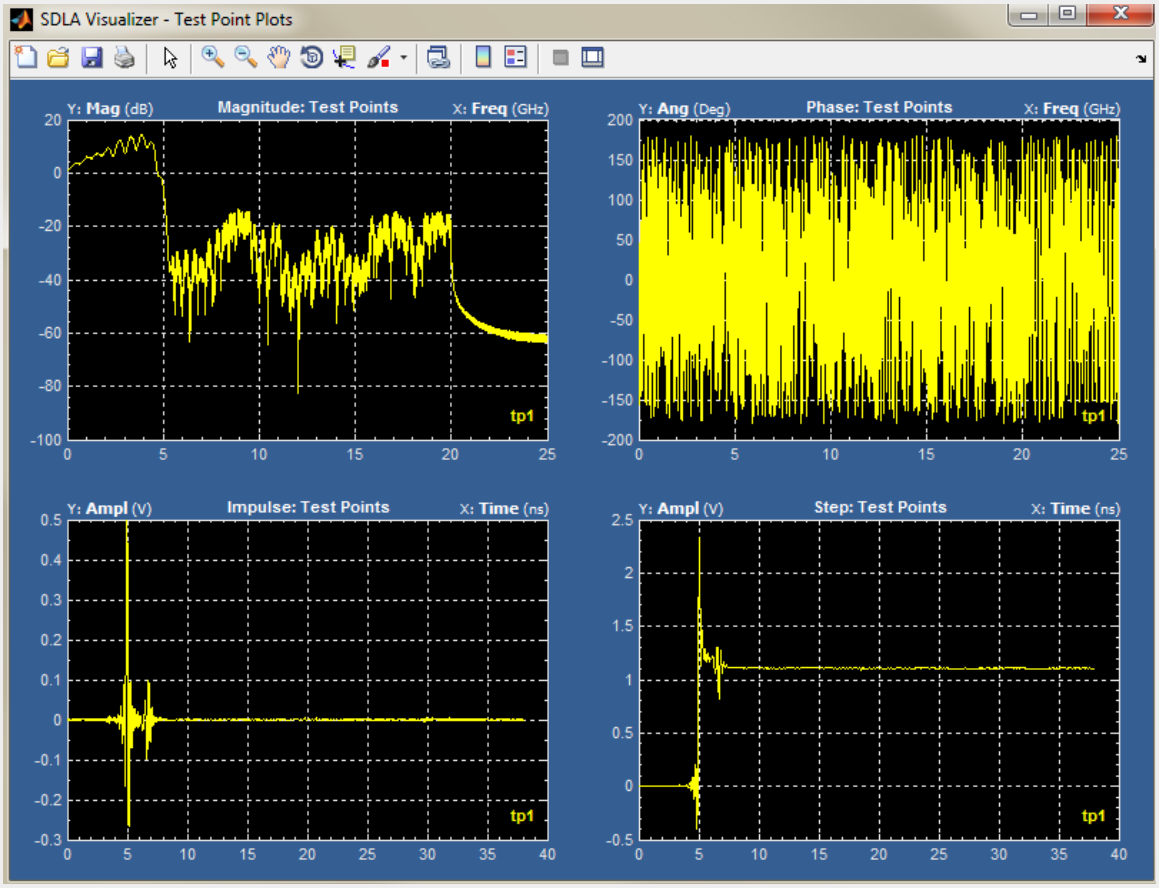
The small square check box is used to enable or disable the Scaling Factor. The Scaling Factor value is not effected whether the check box is on or not.

After the scaling factor is enabled and the main menu Apply is finished, the scaled filter coefficient value can be saved. The range of the scaling factor is between 20% to 200%. The default is 90%.

Plotting Test Points. To plot test point transfer functions, return to the Main Menu and press **Plot**. Magnitude, Phase, Impulse and Step graphs are available. Press here for more information.

It is useful to always check these plots AFTER the **Apply** button on the Main Menu has been pressed, in order to verify that the results appear as expected. This helps ensure that no errors were made in setting up the configuration of the S-parameter blocks throughout the system.

For cases where the auto bandwidth limit setting has been used (see below), the plot will reveal whether or not the auto bandwidth limit is sufficient. If not, you may select **Custom** bandwidth and specify a more appropriate bandwidth limit filter. Then press **Apply** once more, and re-check the plots.



Global Bandwidth Limit. This allows you to set up how the global BW limit filter will be applied to all test point waveforms. Under the **Global Bandwidth Limit** label, three options are available, including the option to create a custom filter. Press here for more information..

- **None.** No bandwidth limit filter will be applied to test points.
- **Auto.** All test point transfer functions will be checked. The one that crosses the -14 dB point at the lowest frequency will be determined. The bandwidth limit filter cutoff frequency will be set to that value.
- **Custom.** Allows you to create a bandwidth limit filter. The Custom option is most useful when the Auto bandwidth filter is not appropriate for your input data, or your test has specific bandwidth requirements. For more information, see *Creating a Custom Bandwidth Filter*.

Delay. This allows you to control how SDLA Visualizer handles absolute and relative delay for the test points. By default, the absolute delay is removed.

Keep Delay: The absolute delay between all test point waveforms is maintained.

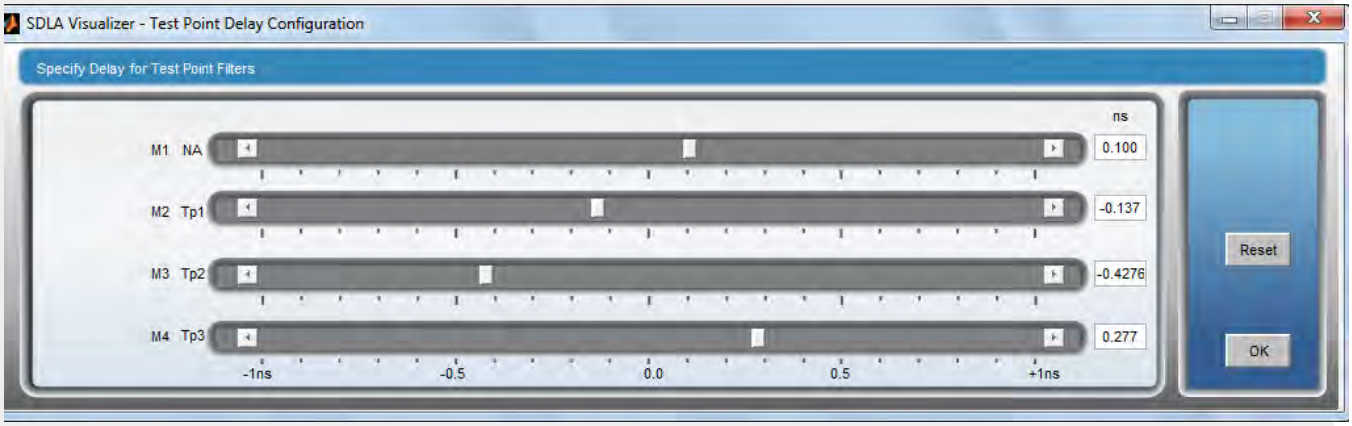
Remove Delay: This is the default setting. The absolute delay of the test point filters is removed, so that the test point waveforms all have the same events close to being aligned in time.

Adjust Delay: This button is only visible when the **Remove Delay** radio button is selected. Pressing that will bring up the Test Point Filter Delay Slider.

Test Point Filter Delay Sliders

The Delay Slider menu allows the relative delay of each test point filter applied to Math to be adjusted over a range of -1 ns to +1 ns.

There are four delay sliders, one for each math waveform on the oscilloscope display.



There are several ways to control the relative delay using a slider:

- enter a number in the text edit box next to the slider
- drag the slider button with a mouse
- fine position by pressing or holding down the arrow buttons
- course position by pressing or holding down on the space between the arrow button and the slider button.

Sliders that are assigned to the same test point will operate together, with their delays set to the same value.

As the delay is adjusted, the test point filters will be recalculated and will update live on the oscilloscope display. Hint: to obtain a more lively interaction, you can make the record length shorter temporarily while setting up delay.

SEE ALSO:

- *Understanding Test Points*
- *Creating a Custom Bandwidth Limit Filter*
- *Saving Test Point Filters (Transfer Function)*

Test point and bandwidth manager (Sampling only)

SDLA Visualizer provides up to 12 test points (when using REF for two), including four test points that can be moved on the schematic drawing. Up to six test point outputs are viewable on the scope graticule at one time (math plus reference). Press here for a Table of Test Point Descriptions.

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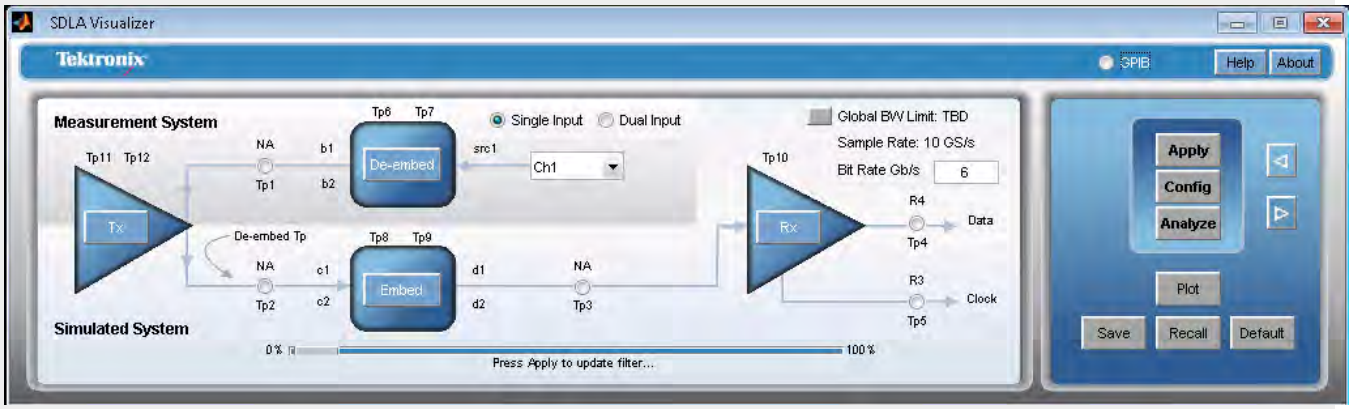

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Test point	Position	Description
Tp10	CTLE	CTLE output
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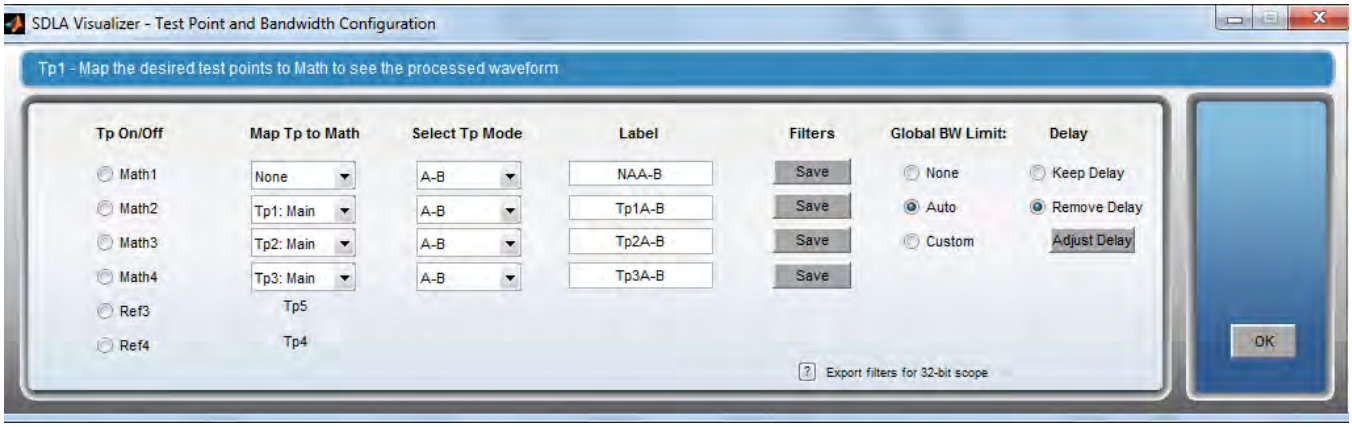

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- **A**: the waveform on the upper line of the test point
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Label. A label for the test point waveform can be entered into this box. It will appear on the oscilloscope screen along with the waveform.

Save Filters. You can save each test point filter into the file folder you specify by pressing the **Save** button next to the test point label. For more information, see, *Saving Test Points*.

Filter Scaling Factor. Filter Scaling Factor is located at the bottom of the configuration menu in the single input case only. It scales the test point filter coefficient according to the value.

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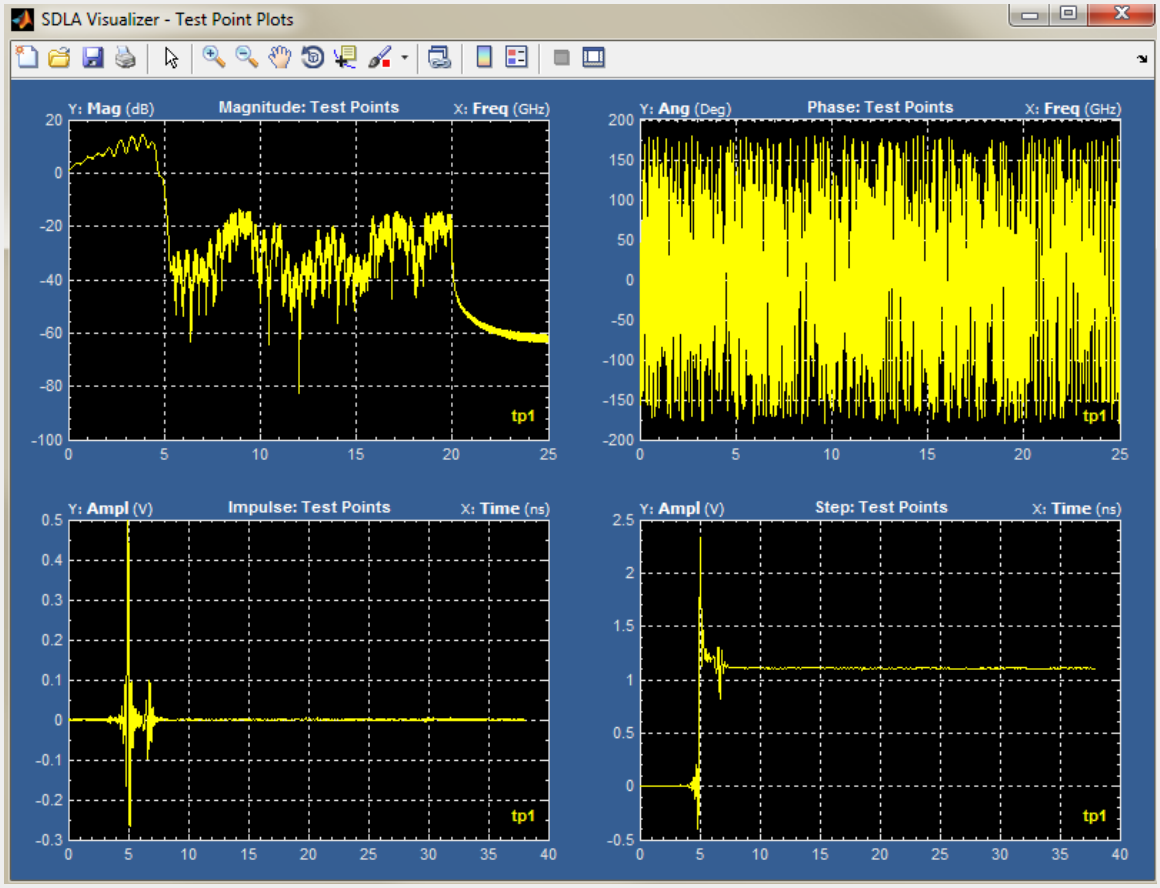

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Adjust Delay: This button is only visible when the **Remove Delay** radio button is selected. Pressing that will bring up the Test Point Filter Delay Slider.

Test Point Filter Delay Sliders

The Delay Slider menu allows the relative delay of each test point filter applied to Math to be adjusted over a range of -1 ns to +1 ns.

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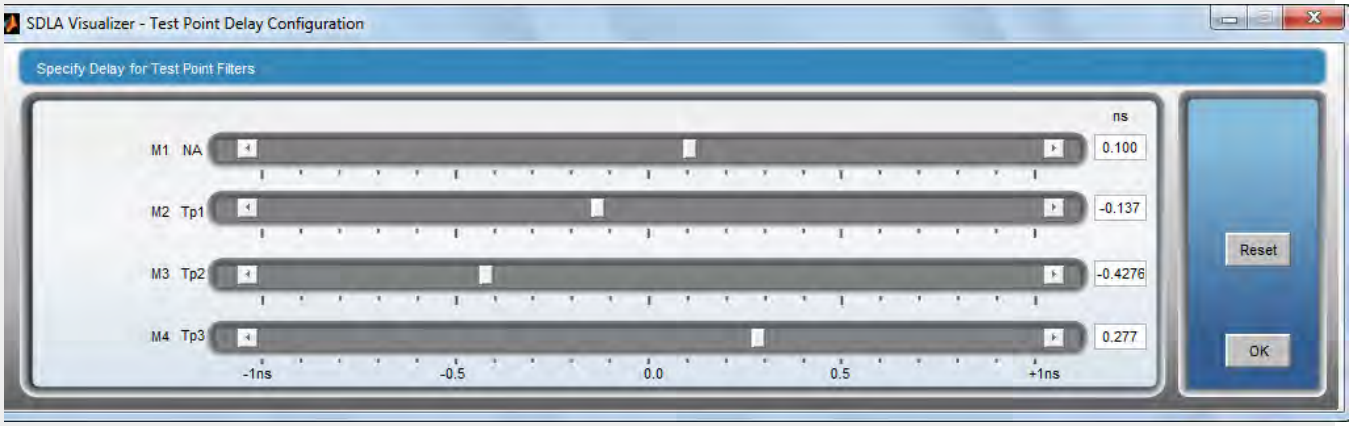

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Sliders that are assigned to the same test point will operate together, with their delays set to the same value.

As the delay is adjusted, the test point filters will be recalculated and will update live on the oscilloscope display. Hint: to obtain a more lively interaction, you can make the record length shorter temporarily while setting up delay.

SEE ALSO:

- *Understanding Test Points*
- *Creating a Custom Bandwidth Limit Filter*
- *Saving Test Point Filters (Transfer Function)*

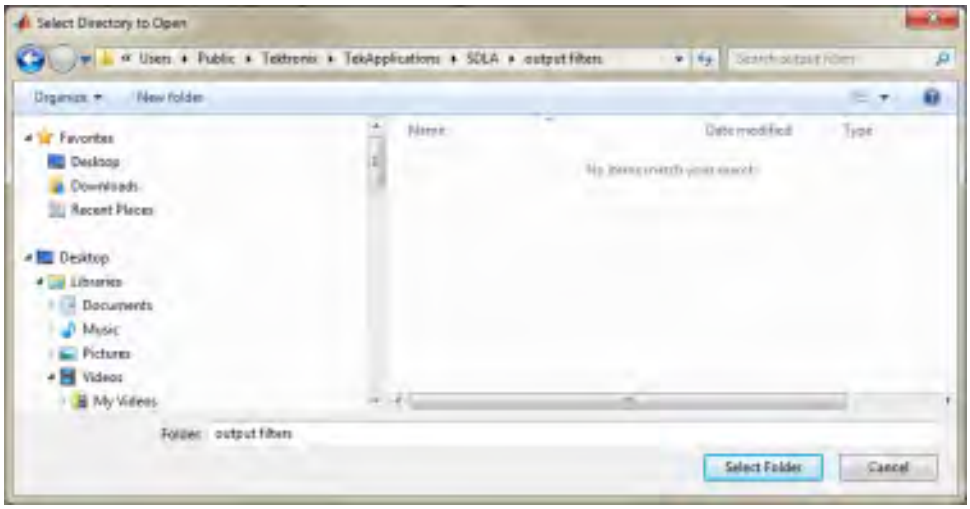
Saving test points

There is a separate **Save** button on the Test Point and Bandwidth Manager that is associated with each of the four possible test points that may be active. Simply press on **Save** next to the test point you are interested in.

In order to save a test point that was not enabled before Applying the model, you must return to the Main Menu and press **Apply** to recompute the test point filters.

NOTE. *Test point filters are intended to work on oscilloscopes that have a 64-bit processor. However, if you wish to export these filters for use with a scope that has a 32-bit processor, then you'll need to edit the file to make it compatible. For more information, see* *Exporting filters for use with a 32-bit oscilloscope**. You can also press ? on the Test Point and Bandwidth Manager.*

Pressing any **Save** button in the Test Point and Bandwidth Manager will open up a folder browser. You may then either select a folder or specify a new folder:



Dual Input Mode (RT only). If you have selected **Dual Input** on the Main Menu, then SDLA Visualizer will save 9 files into the specified folder. Eight of the files will each contain one of the test point filters. One of the files will contain all eight of the filters. If using math as the input source, make sure the test point is output to a different math.

The test point filter filename convention for Dual Input mode is:

<foldername>_Tp<X><mode><source>.flt. File details.

<Foldername>: entered by user

<X>: test point number

<mode>: either A, B, Diff, or Cm

<source>: either Src1 or Src2, where Src1 relates to **src1** on the Main Menu, and Src2 relates to **src2**.

A test point single file contains ASCII characters. The first character is "#" to identify a comment line. Numerous comments can be included. Variables and parameters can be included in comment lines of these forms:

TpX differential test point filters

[DELAY] 1e-09 is the delay parameter same as current arbflt format.

[SAMPLERATE] 50e9

Eight lines contain the coefficients for the 8 filters, i.e.:

Line 1: TpXASrc1

Line 2: TpXASrc2

Line 3: TpXBSrc1

Line 4: TpXBSrc2

Line 5: TpXDiffSrc1

Line 6: TpXDiffSrc2

Line 7: TpXCMSrc1

Line 8: TpXCMSrc2

NOTE. *For future releases of scope firmware it is planned that this file may be loaded into a new math function that can apply the filters according to the selected mode and sources.*

Single Input Mode. For Single Input mode, only one filter file is saved for each test point when you press **Save** on the Test Point and Bandwidth Manager. This is for mode **A-B, differential**. You may save test point filters to a file with the following name format: <filename>.flt.

The ASCII file format contains comment lines that start with a "#". A line with **[DELAY] <value>** may be present in the file. The filter line contains a sample rate number followed by a ";" and the coefficients separated by commas.

SEE ALSO:

- *Exporting Filters to Use with a 32-bit Oscilloscope*
- *Test Point and Bandwidth Manager*
- *Understanding Test Points*

Exporting filters for use with a 32-bit sampling oscilloscope

Test point filters are saved to an arbflt ASCII file format, in order to allow them to be loaded into the oscilloscope's arbflt function in the math menu. There is a slight difference between filters used by RT (64-bit) scopes and filters used by sampling (32-bit) scopes. SDLA automatically selects the appropriate type of filter based on whether the Source selection on the main menu specifies Sampling.

However, if you later wish to use filters created for a RT scope on a sampling scope you'll need to edit the file to make it compatible.

The file format contains lines with comments preceded by the # symbol.

Next, there is a line that contains the sample rate value for the first entry, followed by ";" followed by the filter coefficients for the remaining entries separated by commas. (For further information on the filter file format, see *Understanding Test Points*.)

NOTE. *If the radio button is selected on the Test Point and Bandwidth Manager, then the waveform timing may be off by one sample period.*

To edit the file:

1. Open it up using Windows Notepad.
2. Add a comment line at the top of the file in order to document what sample rate the filter was designed to operate at. Enter **# <sample rate value>** where the sample rate value is the first element of the filter coefficient line.
3. Next, on the filter coefficient line, edit the first sample rate number to be an @ symbol. The @ symbol indicates that the filter will operate at all sample rates with the same set of coefficients.

Make sure that if you use this filter on a 32-bit scope, that the oscilloscope is set to the sample rate specified in the comment line above. The arbflt math function was designed to run only at the sample rate in the coefficient line and will normally blank out the waveform if the oscilloscope sample rate is changed to some other value. However, when the @ symbol is present, then the filter will run at all sample rates, but its response will be normalized to the sample rate. In other words, the filter will only work as desired when the scope is set to the sample rate the filter was designed for.

For example:

Tp1 filter

sample rate 50GS/s

@ <coeff**1**>, <coeff**2**>, <coeff**3**>, ... <coeff**n**>

CAUTION. *Note that if you are using this filter with a scope with a 32-bit processor, and the scope is operated in IT mode (interpolated sample rate), then the sample rate readout on the screen is not actually the interpolated sample rate, but rather is the base sample rate before the interpolation. The filter would be operating at the interpolated sample rate.*

In order for the filter with an @ as the sample rate to operate with the correct response, the interpolated sample rate must be set to the rate for which the filter was designed. The user must manually do this when exporting to a scope using a 32-bit processor. You may determine the IT sample rate by computing 1 divided by the sample interval readout in seconds per point on the scope display.

Save test point filters for multiple sample rates (RT only)

On real-time scopes, there may be a need to save a single Test Point Filter to cover multiple sample rates. SDLA can create one Test Point Filter for one sample rate. The following steps can be used to combine multiple Test Point Filters for each sample rate to a single Test Point Filter that covers all the sample rates that are needed.

To cover m number of sample rates SR1, SR2, …., SRm:

1. Set the sample rate of SDLA input to SR1, run SDLA to create the Test Point Filter for Tp<x>. Rename it to sdlaTpxxxx.flt.
2. Set the sample rate of SDLA input to SR2, run SDLA to create the Test Point Filter for Tp<x>. Copy the sample rate and coefficient part of sdlaTp<x>.flt and paste it to the end of sdlaTpxxxx.flt.
3. Repeat Step 2 for the remaining sample rates. The final Test Point Filter covering all the sample rates will look like:

tp1 filter coefficients

5.000000E+10; <coeff1>, <coeff2>, <coeff3>, ... <coeffn1>,

1.000000E+11; <coeff1>, <coeff2>, <coeff3>, ... <coeffn2>,

2.000000E+11; <coeff1>, <coeff2>, <coeff3>, ... <coeffn3>,

.

.

.

SRm; <coeff1>, <coeff2>, <coeff3>, ... <coeffnm>,

SEE ALSO:

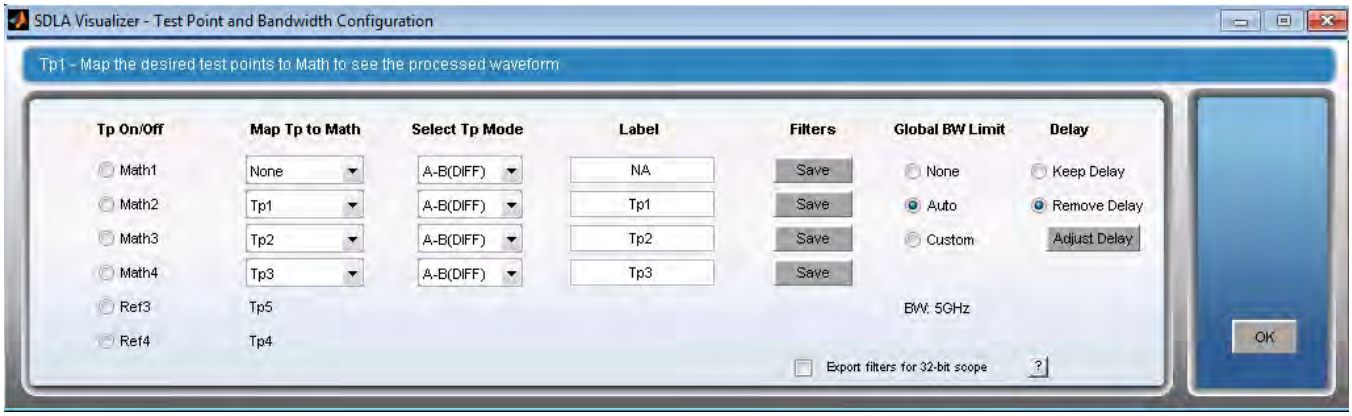
- *Test Point and Bandwidth Manager*
- *Understanding Test Points*
- *Saving Test Points*

Creating a custom bandwidth limit filter

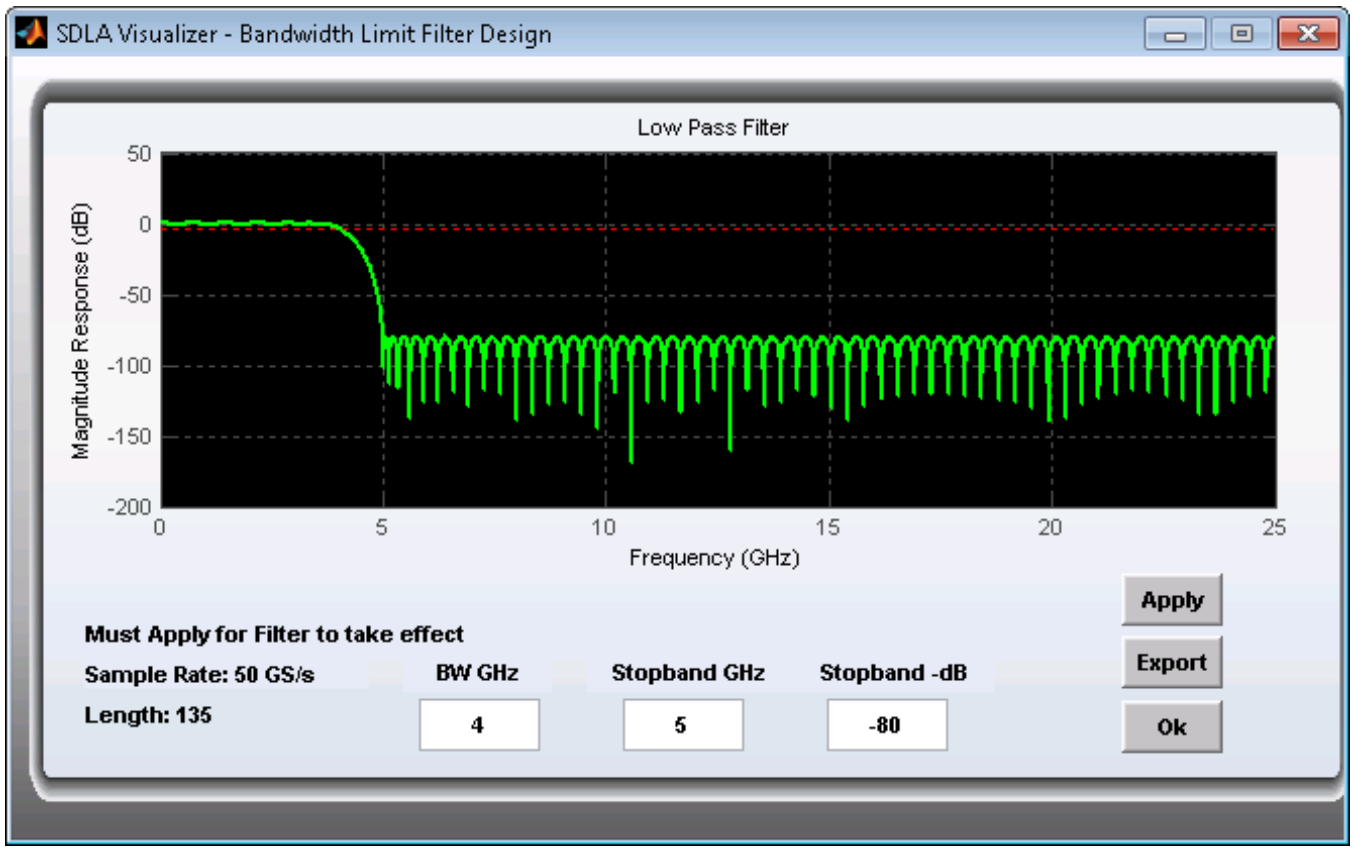
When de-embedding fixtures, cables or other equipment, a bandwidth limit filter is usually necessary to obtain a usable result. In such cases, a bandwidth limit filter can reduce the gain on noise by filtering out the high frequency components. SDLA Visualizer gives you control over the pass band, transition band and stop band responses, which affect noise attenuation, rise time, preshoot and overshoot.

Follow these steps to create a custom filter:

1. Press a test point on the Main Menu to bring up the Test Point and Bandwidth Manager. (Pressing **Global BW** on the Main Menu also brings up the Test Point and Bandwidth Manager.)



2. Under **Global BW Limit**, select **Custom** and then press **Setup BW**. This brings up the **Bandwidth Limit Filter Design Menu**.



3. Set values in the BW GHz, Stopband GHz and Stopband dB fields.
4. Press **Apply** to generate the bandwidth filter and save it for use in SDLA's internal data base. The filter response is plotted for review. Optionally, press the **Export** button to save the filter to a file for uses outside SDLA.
5. Press **Close** to return to the Test Point and Bandwidth Manager.

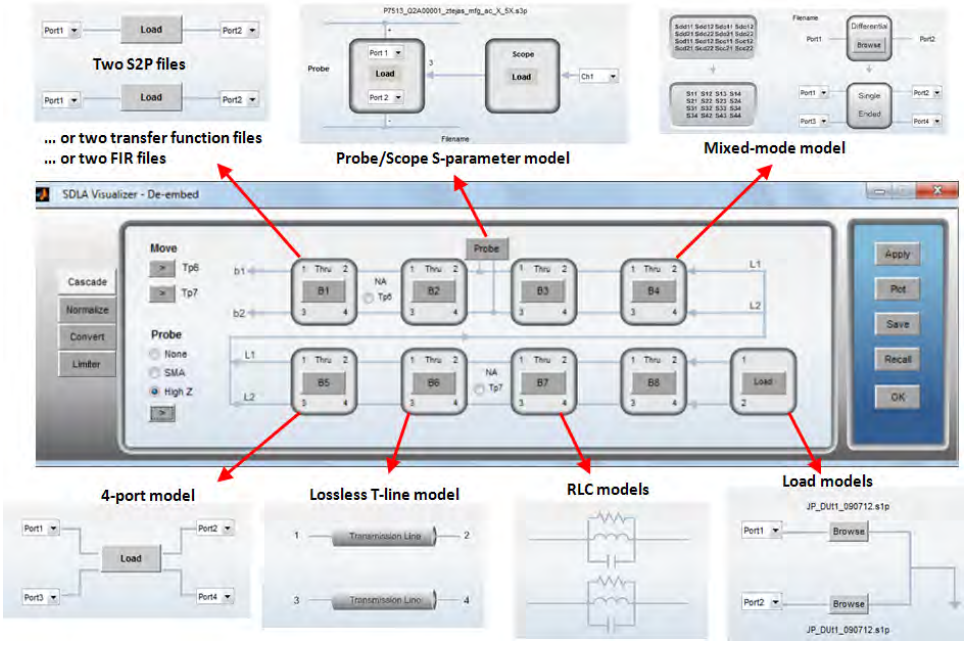
SEE ALSO:

Test Point and Bandwidth Manager

De-embed block

De-embed block overview

The **De-embed Block** contains the Measurement Circuit models that represent the actual hardware probe, fixtures, etc, used during waveform acquisition. Press **De-embed** on the Main Menu to bring up the *De-embed Menu*, which represents a cascade of 4-port S-parameters. These menus provide multiple ways to model the blocks, as shown below:



NOTE. *SMA and High Z Probe support is for RT only.*

NOTE. *If the DUT has large attenuation, de–embedding results will have limited bandwidth, ringing, and slower rise-time. If you increase the bandwidth limit filter transition band, it can reduce ringing at the expense of phase and magnitude error at the higher frequencies, and at the expense of increased noise.*

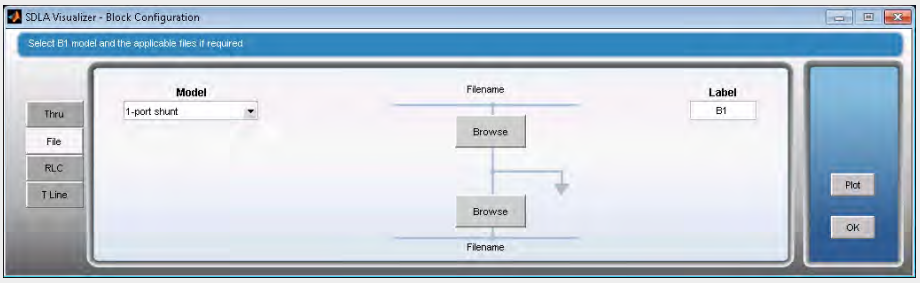
SDLA Visualizer handles *cross-talk and reflections* in both directions through the cascade.

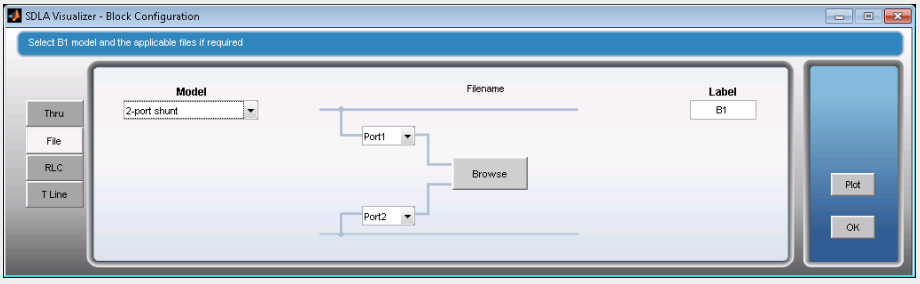
The De-embed Block lets you model a variety of different configurations. Here are some possibilities.

De-embed Block – Possible Configurations

- 4-port single-ended S-parameter file
- 4-port differential S-parameter file
- Two 2-port S-parameter files

- FIR filter files (time domain)
- Transfer function files (frequency domain)
- High-Z probe
- TDT Waveform
- 6-port Single-ended
- 8-port Single-ended
- 12-port Single-ended
- 16-port Single-ended





- SMA probe model (RT only)
- Interposer/probe/scope model
- Mixed-mode S-parameter files
- Various RLC series or parallel configurations
- Lossless Transmission line model
- 3-port probe model file
- 1-port load S-parameter file
- 2-port load S-parameter file
- Nominal load values
- TDT waveform

NOTE. *For step-by-step examples of de-embedding and embedding, see* *Examples and troubleshooting (RT only) on page 149.*

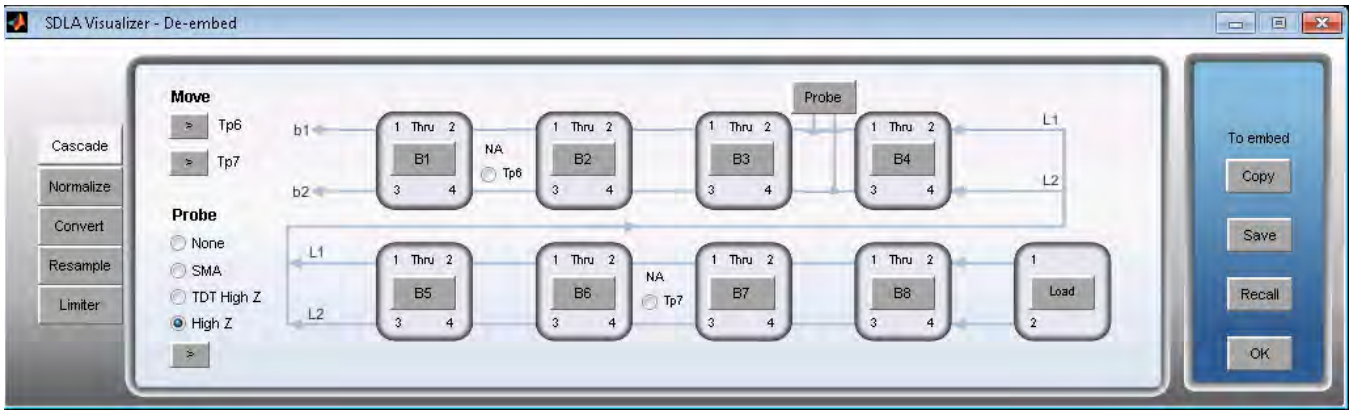
SEE ALSO:

- *De-embed/Embed Menu*

De-embed-Embed menu

The De-embed/Embed Menu allows you to define where the acquired waveforms enter the signal flow path of the system.

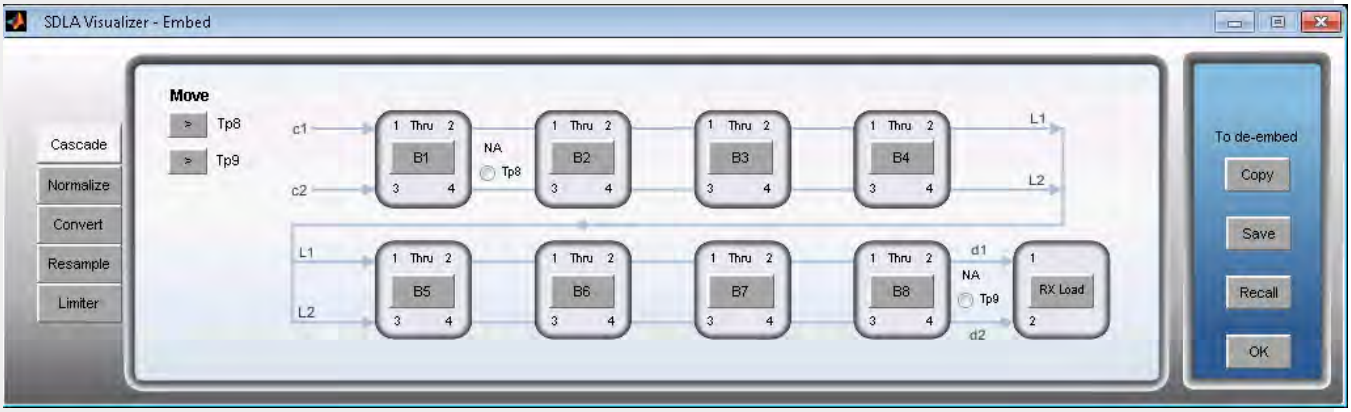
NOTE. *For step-by-step examples of de-embedding and embedding, see* *Examples of Tasks and Troubleshooting*.



Pressing **De-embed** on the Main Menu brings up the De-embed Menu; pressing **Embed** brings up the Embed Menu. These menus display a diagram of 8 cascaded 4-port S-parameter block models, plus a load model at the end, which you may configure, plot and save. You may also select the locations of two movable test points, configure the load, and configure probes (de-embed menu only).

NOTE. *Parameter changes in the De-embed Block may affect all test points in the De-embed Block as well as in the Embed Block. However, parameter changes in the Embed Block cannot affect test points in the De-embed Block.*

Differences between De-embed Menu and Embed Menu. In the De-embed cascade model diagram, shown above, note that the processing arrows in the diagram flow from right to left. In the Embed cascade model diagram, shown here, the arrows flow from left to right. Also, the De-embed Menu includes probe options, while the Embed Menu does not. Each menu has its own specialized Load Block (the final block) with a menu for configuration options. Other than that, the functionality is the same.



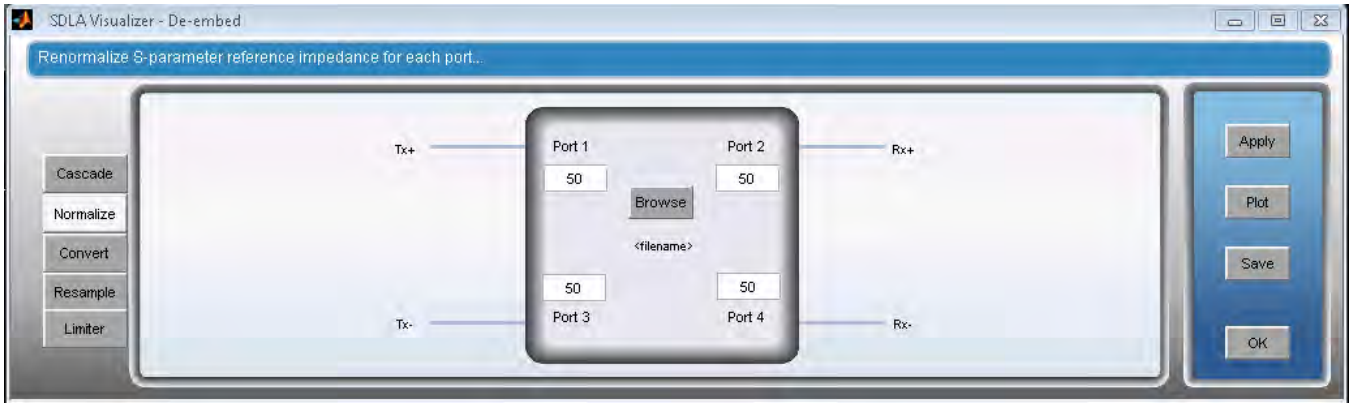
On both menus, there are four tabs on the left side of the screen:

Cascade Tab. The cascade diagrams show the S-parameter modeling blocks. The two arrow buttons under **Move** may be used to move **Tp6** and **Tp7** on the De-embed Menu, and **Tp8** and **Tp9** on the Embed Menu. Pressing on these arrows repositions the movable test points. In the De-embed Menu only, you may configure SMA or High Z probe options. For details, see *Configuring Probes*.

Pressing on any of the cascade blocks **B1-B8** brings up the individual block's configuration menu. For details, see *Block Configuration Menu*.

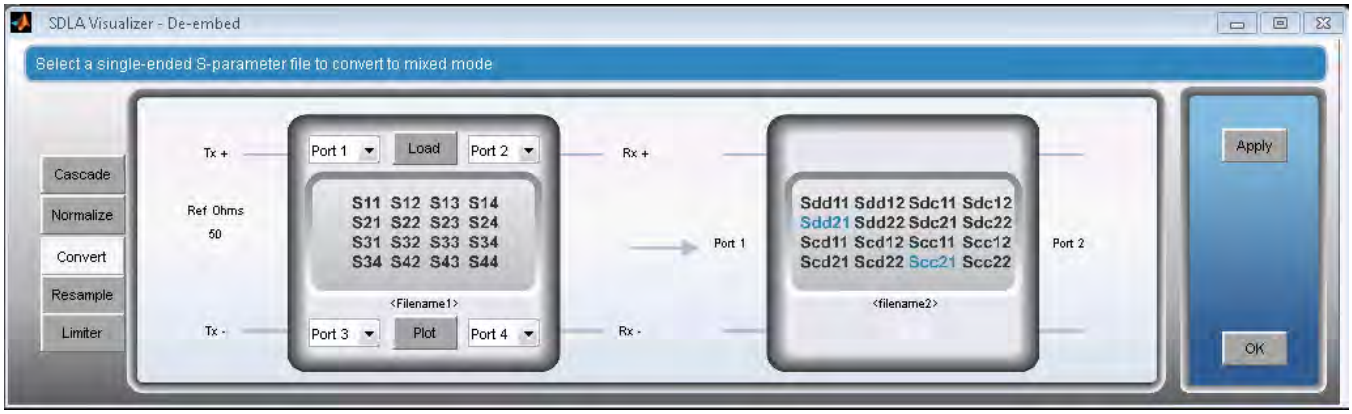
The final block of the cascade is labeled either **Scope**, **SMAProbe** or **Load** in the De-embed Menu, and labeled **Rx Load** in the Embed Menu. When you press this block, the appropriate configuration menu comes up where you may determine the load of the output ports. For details, see *Load Configuration Menu*.

Normalize Tab. SDLA requires all ports to have a reference impedance of 50 Ohms. You can use the Normalize Tab to re-normalize the S-parameters to the correct reference impedance for each port before reading them into SDLA Visualizer De-embed or Embed Blocks. For details, see *How to Renormalize S-Parameters to Different Reference Impedances*.



Convert Tab. Here, you can set up singled-ended to mixed mode S-parameter conversion. Once you load a file, the **Save** and **Plot** buttons become available.

NOTE. *It is preferred practice to leave the data in single-ended format, not mixed-mode, for uses that are internal to SDLA.*



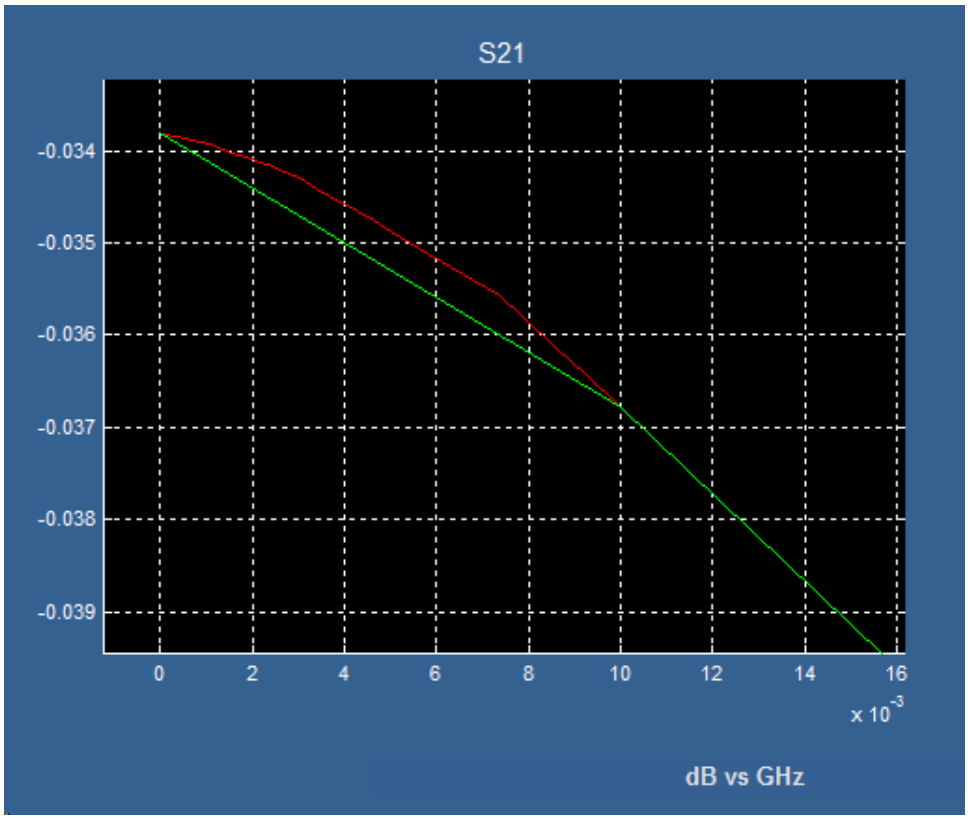
Resample Tab. SDLA requires all S-parameter files to be uniformly sampled. Files with non-uniform sampling can be resampled using the Resample tab, which works with any number of ports.

After loading a file you can change the suggested uniform sampling interval, then plot and save the uniformly sampled version of your data.

If you click the Plot button on the right, three new windows appear with the following graphs.

- dB magnitude overlays of the original and resampled data.
- Phase overlays of the original and resampled data.
- dB magnitude plots of the resampled data with the standard subsidiary plotting options.

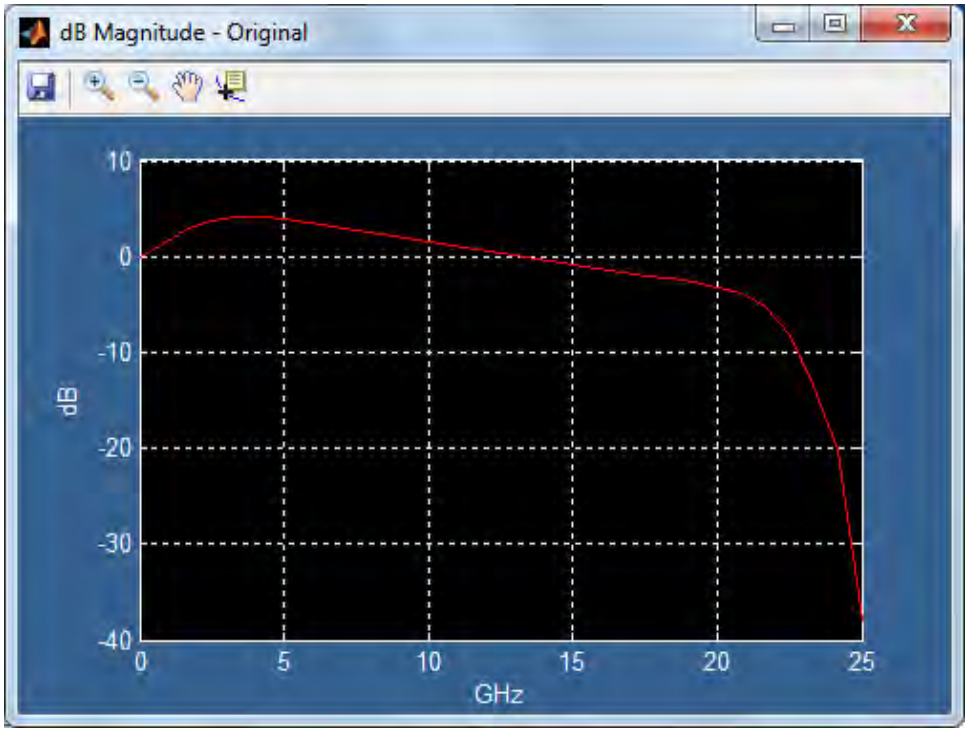
The two overlay windows display the original S-parameters in red and the resampled S-parameters in green. With a good resampling frequency spacing all the red will be covered by green. The following graph illustrates a case in which the lowest frequencies were oversampled and some information was lost in resampling. While in this graph the discrepancy is acceptably small, it demonstrates what to look for when evaluating the accuracy of the resampling.


S21
-0.034
-0.035
-0.036
-0.037
-0.038
-0.039
0
2
4
6
8
10
12
14
16
x 10-3
dB vs GHz

Limiter Tab. This tab permits simple editing of computed filters, in particular, it allows undesired peaks to be removed.

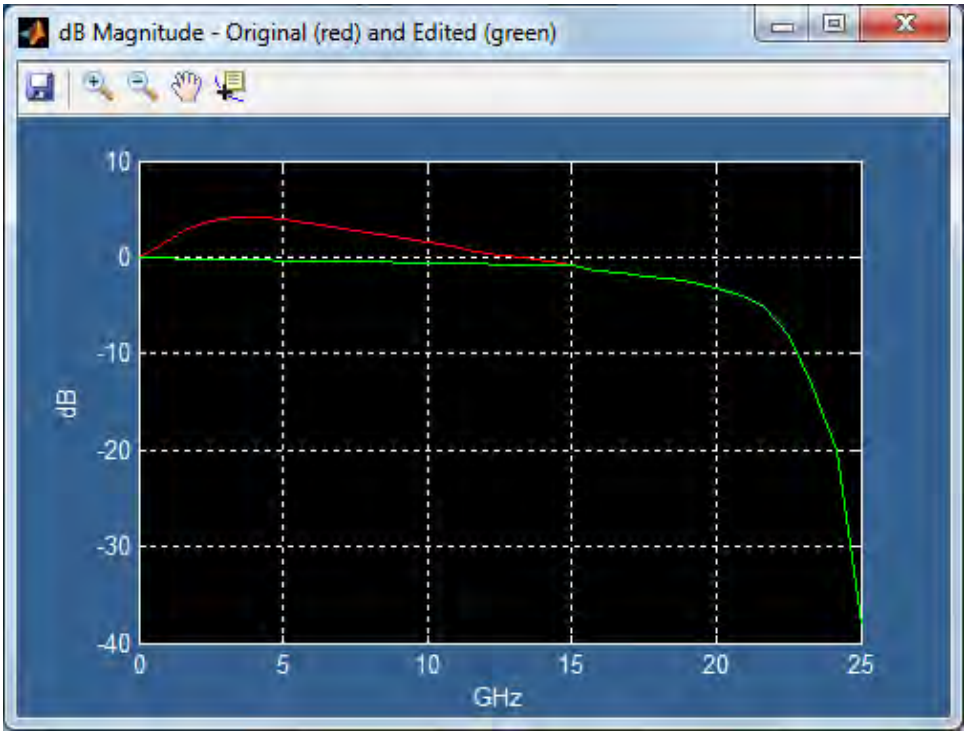
Use the following steps to use this tool.

1. Click Load to load a filter file with file extension .flt.
2. Click Plot to view the frequency space representation of the filter.



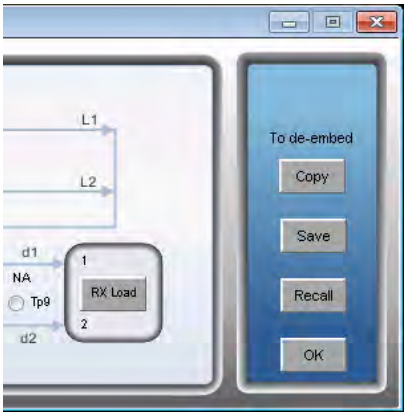
3. Enter the start and stop frequencies of the frequency range to recompute and click Apply.

4. Click Plot to display the original (red) and the recomputed (green) functions. The recomputation in the selected interval is done by linear interpolation in magnitude and phase. Because the plots show dBMagnitude instead of magnitude the interpolated values in the recomputed interval generally will not display as a straight line.



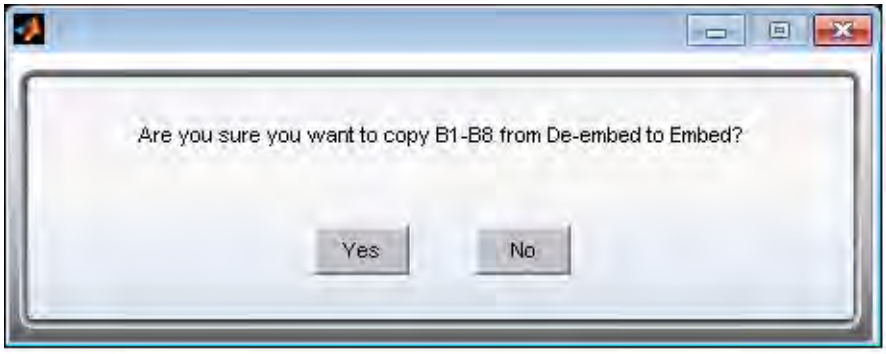
5. Click the Save button and select a file name for the edited filter.

Control Buttons. On the right side of the screen, the buttons vary depending on the context. On the Cascade Tab, these buttons appear:



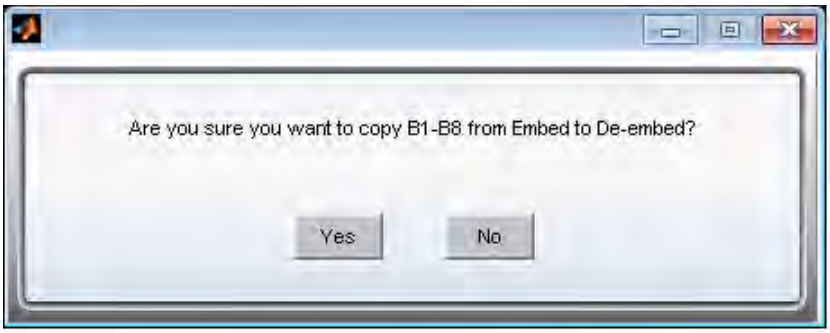
Copy: It can copy the content of block B1 to B8 from de-embed blocks to embed blocks when Copy is pressed.

The following message dialog shows up upon clicking Copy, press Yes to continue copying; press No to cancel the action.



Copy: It can copy the content of block B1 to B8 from embed blocks to de-embed blocks when Copy is pressed.

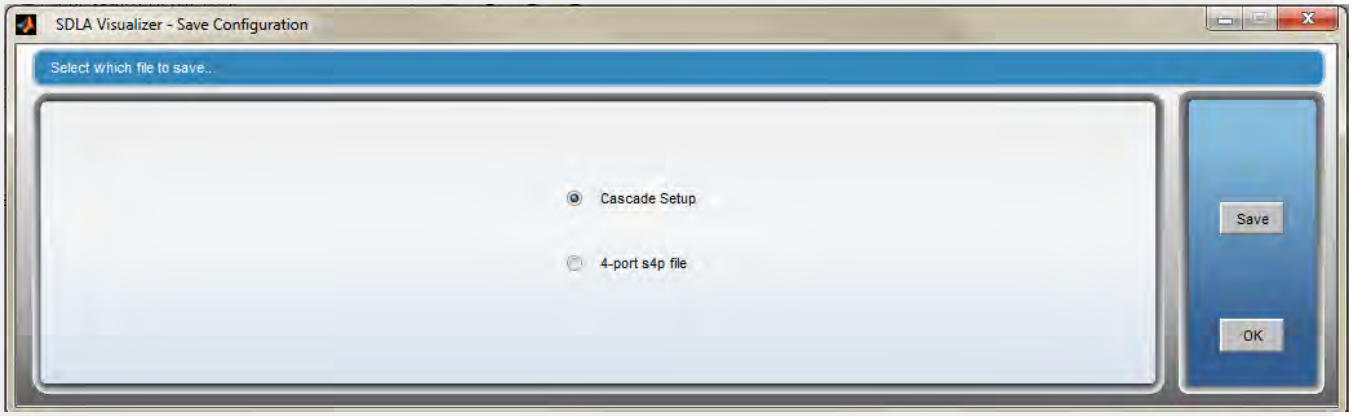
The following message dialog shows up upon clicking copy, press Yes to continue copying; press No to cancel the action.



Save

When you press **Save**, you can select from two options.

- **Cascade Setup:** Saves the parameters for the current cascade into a setup file. The cascade setup can be recalled later by pressing **Recall.** Note the cascade setup file is different from the main SDLA setup file, as the cascade setup file only contain the cascade configuration.
- **4-port s4p file:** Allows you to save a single 4-port S-parameter set for the combination of all the blocks in the cascade, excluding the load (final) block and the Tx Block. This allows for general purpose cascading of 4-port S-parameters exported to a file that may be used in other simulation tools, or may be loaded back into a cascade block in order to combine with additional blocks. This is useful if more than 8 blocks need to be combined together.



Recall. Recalls a setup file saved using the **Save** button.

OK. Returns you to the Main Menu.

SEE ALSO:

- *Block Configuration Menu*
- *Load Configuration Menu*
- *De-embed Block Overview*
- *Embed Block Overview*

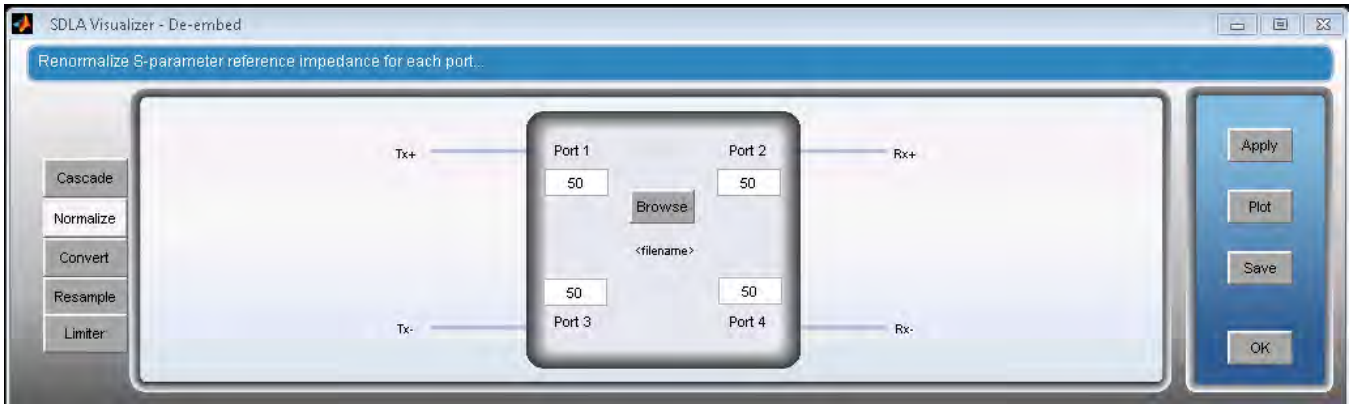
How to re-normalize S-Parameters to different reference impedances

Use the **Normalize Tab** on the *De-embed/Embed Menu* to take an S-parameter set that was not normalized to 50 Ohms and normalize it to 50 Ohms, which is the reference impedance required by SDLA Visualizer. The reference impedance is the value that ports are loaded with at the time the S-parameters are measured. (Reference impedance should not be confused with the Load impedance in the cascade, which may be any value you desire.)

The tab may be used to normalize the port reference impedances to any value for any port for uses external to SDLA, or for analyzing the effects by looking at the plots.

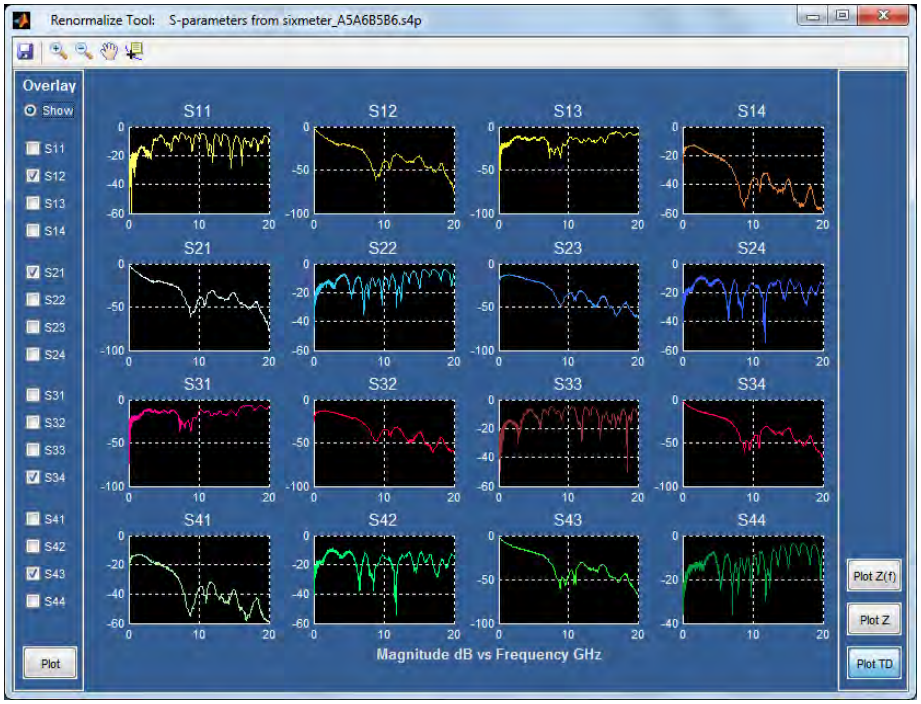
Using the Normalize Feature.

1. Press on the **Normalize** Tab.
2. Press **Browse** and select the 4-port S-parameter file that is to be re-normalized.



3. Touchstone 1.0 format only supports one impedance value for all ports. That number will be displayed in the port edit boxes. Now, edit each box to 50 Ohms for internal use with SDLA. Edit any port to desired values for external use outside of SDLA or for observing differences in the plots.
4. Press the local **Apply** button to compute the re-normalized set of S-parameters. Note that this data is not used by any SDLA blocks, unless you save the data to a file and then load it into a block in the Cascade Tab.
5. Press **Plot** to observe the original S-parameters overlaid on the re-normalized set. The plot shows the original S-parameter data in gray traces and the new re-normalized plots in various colors. Use the zoom tool on the plot tool bar

to zoom in on the detail of each individual plot. A cursor tool allows the read out of trace data. There is also a trace marking tool.



6. Press **Save** to create a Touchstone 1.0 file containing the re-normalized data. If all four ports have the same reference impedance, then a standard file will be written with that value in the option line. However, if some ports have an impedance setting that is different than the other ports, the system will place 1 as the impedance in the options line and write a comment line with

   ! [IMPEDANCE] <value1> <value2> <value3> <value4>

   You can load the re-normalized file into any block in the Cascade Tab diagram.

   If required, the re-normalized file can be read back into the tool and restored back to the original reference impedance values.

SEE ALSO:

- *De-embed/Embed Menus*

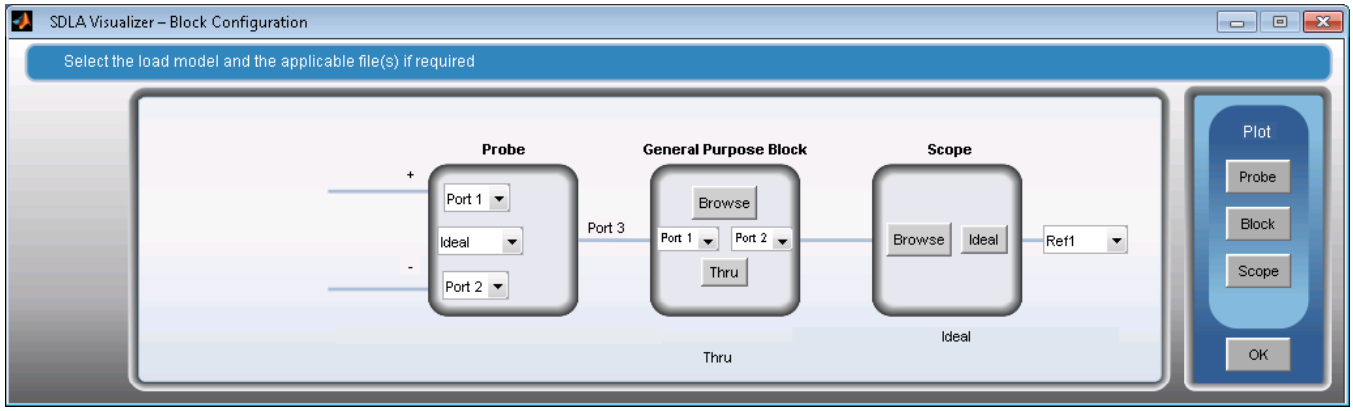
Configuring probes (RT only)

You may choose from three probe options on the De-embed Menu:

None. For this option, no probe is used. The input waveform signals from the scope are represented at the load block on the Cascade Tab diagram (the final block), and are indicated by the labels **src1** and **src2**. A typical use case might be where a fixture and two cables are attached to the transmitter in order to acquire signals into **Ch1** and **Ch2** of the oscilloscope. To model this, you would choose **Dual Input** on the Main Menu, and then select **Ch1** and **Ch2** as the waveforms that are labeled **src1** and **src2**.

SMA Probe. This option can only be selected if **Single Input** has been chosen on the Main Menu. This selection specifies that a single waveform will be obtained from an SMA probe to be input into the De-embed Block. SDLA will assume this waveform was acquired through a 3-port SMA probe which had equal but opposite polarity signals at the input to each cable. The SMA probe S-parameter set includes the cable pair that comes with the probe. The load (final) block of the Cascade Tab diagram will only allow the SMA probe model for termination of the cascade, and will be labeled "SMAProbe".

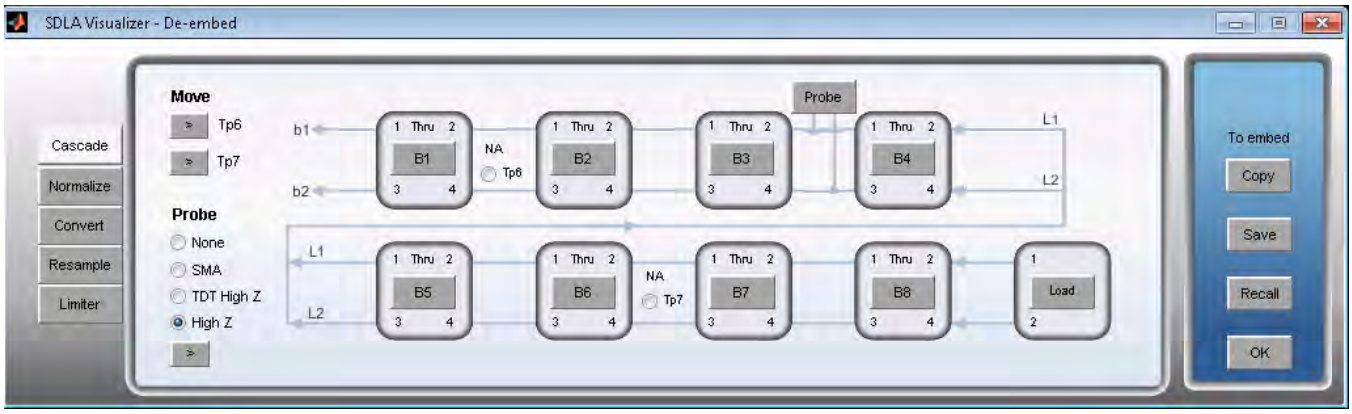
Pressing **SMAProbe** on the Load block (final block) of the De-embed Menu Cascade Tab diagram brings up this menu:



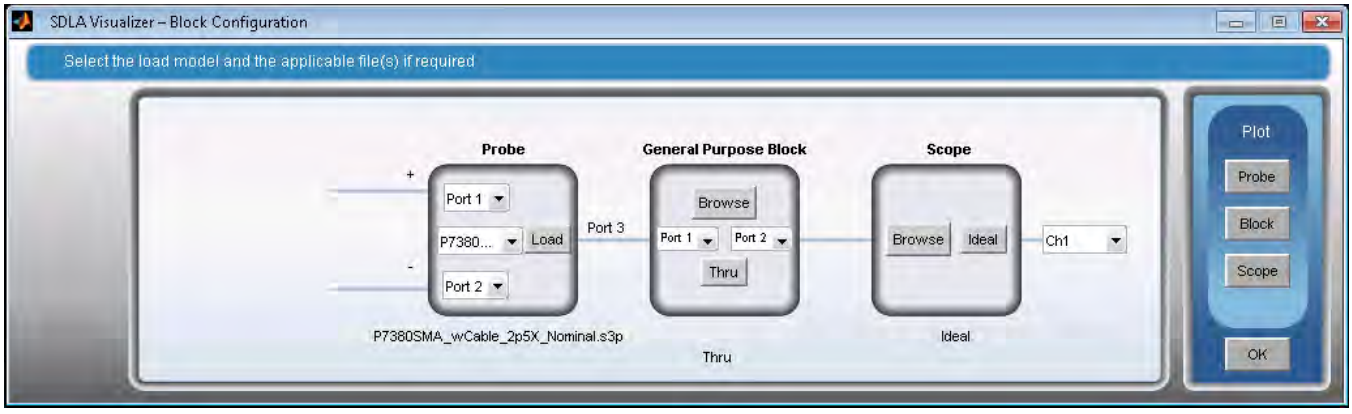
Options

- **Port Numbers:** Select the port numbers to make the correct connection polarity for the probe.
- **Probe model:** Use this drop-down menu to select the probe model that is connected to the oscilloscope. This selection will cause a file browser window to open so that the correct S-parameter file may be selected. Pressing the **Load** button on this menu will also open the file browser menu to the same folder determined by the probe model selection.
- **Scope Browse:** Press this button to load an S-parameter file for the scope. This will open a browser and the user can select the correct file according to the scope model in use.
- **General Purpose Block Browse:** Press this button to load an S2p file for the general purpose block. This general purpose block may be used to model a RF switch.
- **General Purpose Block Thru:** Press this button to make the general purpose block be ideal Thru.

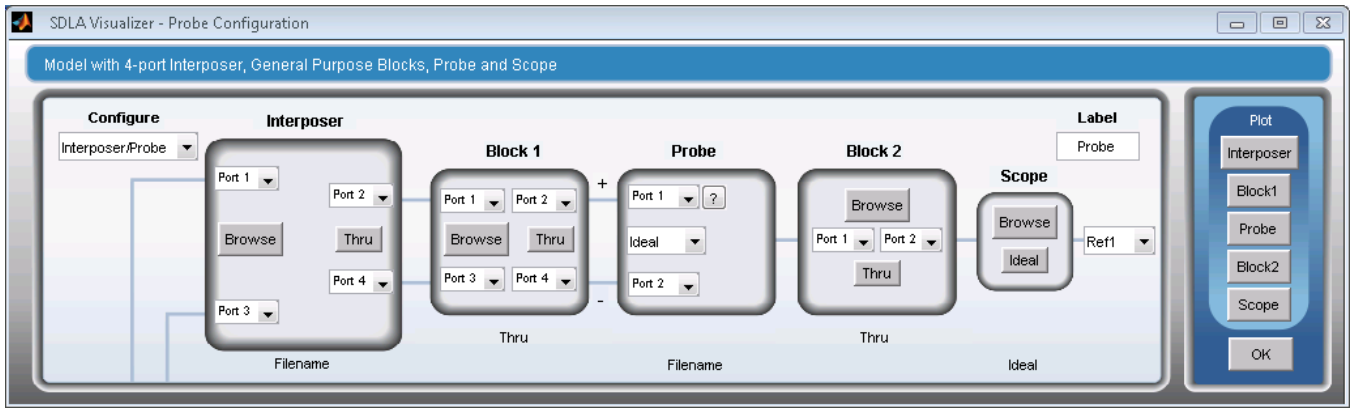
High Z Probe. This option can only be selected if the **Single Input** radio button has been selected on the Main Menu. This selection specifies that a single waveform will be obtained from a High Z probe to be input to the De-embed Block. When you press the **High Z** radio button on the left, a **Probe** button appears on the Cascade Tab diagram. A right arrow ">" button also appears below the words High Z. Pressing on the arrow button moves the probe to a different location on the diagram.



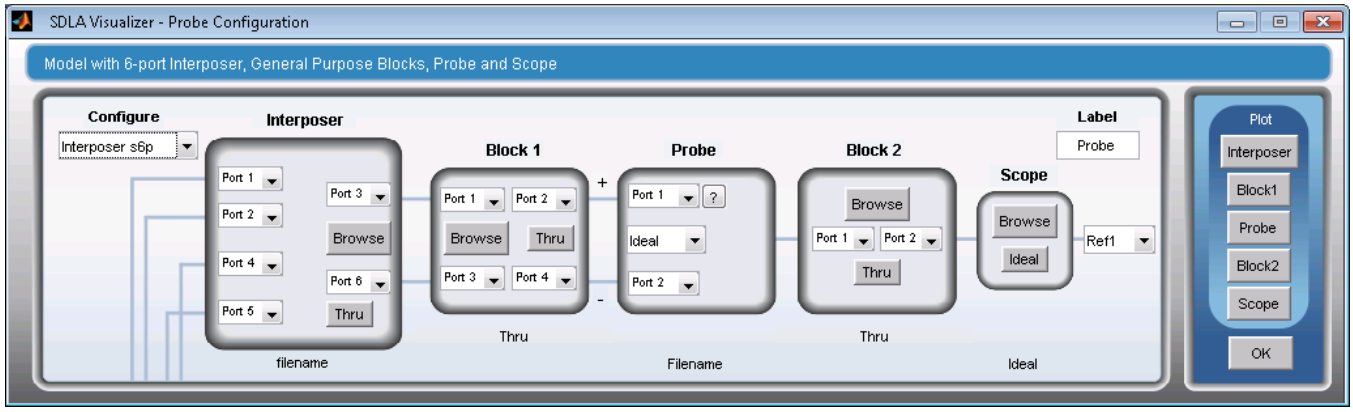
Pressing the **Probe** button on the Cascade Tab diagram brings up the Probe Path Configuration Menu:



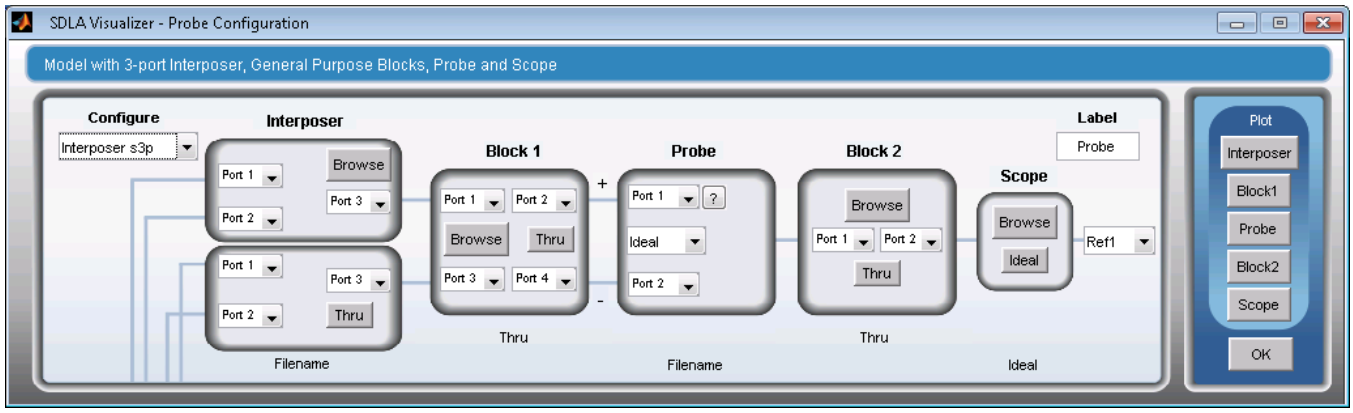
Under **Configure**, select the circuit configuration desired. There is choice of **Probe/Scope**, shown above, or **Interposer/Probe**, shown below:



Or **Interposer s6p**, shown below:



Or **Interposer s3p**, shown below:



Options

- **Probe model:** Use this drop-down menu to select the type of probe in use. This opens a file browser to the correct probe directory. The user must

then select the correct file according to the probe attenuation setting and according to the tip in use. For help selecting the correct tip name for the file, see *Probe and Tip Selection.*. You may also press the **?** button on the Probe panel.

- **Probe Load**: Press this to load a probe file according to the currently selected model.
- **Port numbers:** Select the desired port numbers to obtain the correct polarity connection for the probe.
- **Scope Browse:** Press this button to load an S-parameter file for the scope. This will open a browser and the user can select the correct file according to the scope model in use.
- **Scope Ideal:** Press this button to use an ideal 50 Ohms termination to model scope.
- **Interposer Browse:** Press this to load 4-port S-parameters for the interposer model. This supports a simplified interposer model for a differential clock or strobe line pair. Where the memory input and controller input are assumed to be one port per line, and the connect to the probe are the other two ports.
- **Interposer Thru:** Press this to set the interposer to model two isolated ideal three way line connections.
- **Interposer s6p Browse:** Press this to load 6-port S-parameters for the s6p interposer model. This supports a complete two line differential interposer model for a differential clock or strobe line pair. Where the memory input and controller input are modeled as two ports per line, and the connection to the probe are the other two ports. The port number assignments for the s6p parameter is as follows: the Tx side positive leg is connected to the top port on the left, the Tx side negative leg is connected to the second port from the bottom on the left, the Rx side positive leg is connected to the second port from the top on the left, the Rx side negative leg is connected to the bottom port on the left, the probe positive leg is connected to top port on the right, the probe negative leg is connected to the bottom on the right.
- **Interposer s6p Thru:** Press this button to set the interposer to model two isolated ideal three way line connections.
- **Interposer s3p Browse:** Press this to load 3-port S-parameters for the s3p interposer model. This supports an interposer having the same 3-port model on the positive leg and on the negative leg, and there is no coupling between the two lines. This configuration is useful for single line signaling. The port number assignments for the s3p parameter are: the Tx side line is connected to the top port on the left, the Rx side line is connected to the bottom port on the left, and the probe tip is connected to the port on the right
- **Interposer s3p Thru:** Press this button to set the interposer to model two isolated ideal three way line connections.
- **Block 1 Browse:** Press this button to load an S4p file for general purpose block 1. This general purpose block may be used to model extra probe tip resistors.
- **Block 1 Thru:** Press this button to make general purpose block 1 be ideal Thru.

- **Block 2 Browse:** Press this button to load an S2p file for general purpose block 2. This general purpose block may be used to model an RF switch.
- **Block 2 Thru:** Press this button to make general purpose block 2 be ideal Thru.
- **Label:** Edit this label to change the probe block label in the De-embed menu.
- **Filenames:** The filenames for the loaded S-parameter files are listed at the bottom of the menu.
- **Interposer in Plot:** Press this button to plot the interposer data. The interposer data could be s4p, s6p or s3p.
- **Block1 in Plot:** Press this button to plot the s4p data in Block1.
- **Probe in Plot:** Press this button to plot the s3p data of the Probe
- **Block1 in Plot:** Press this button to plot the s2p data in Block2.
- **Scope in Plot:** Press this button to plot the s1p data of the scope.

SEE ALSO:

- *De-embed/Embed Menu*

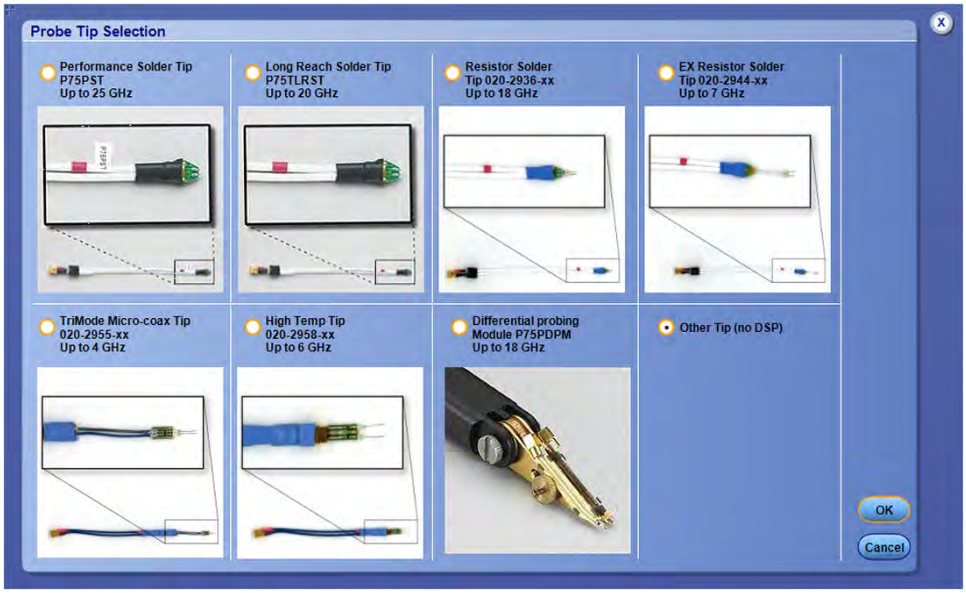
Probe and tip selection (RT only)

This topic explains how to identify probe tips and then select the proper file name for the configuration in use.

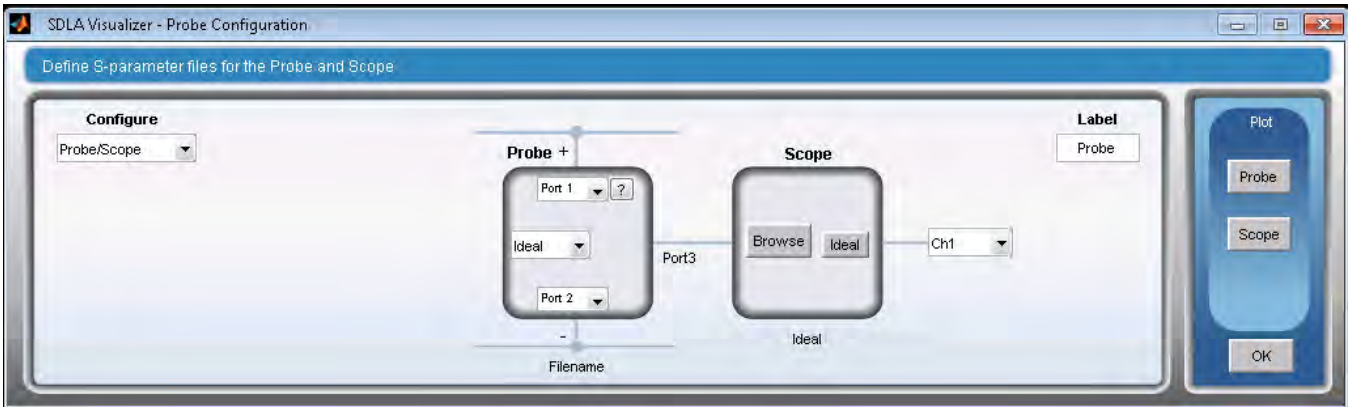
For the P7313 and 7380 probe models, the following set of tips is available; however, only four of these tips are supported with S-parameter sets. These are:

- HBW Right Angle Flex,
- HBW Straight Flex,
- Medium Flex Small Resistor,
- and Short Flex Small Resistor.

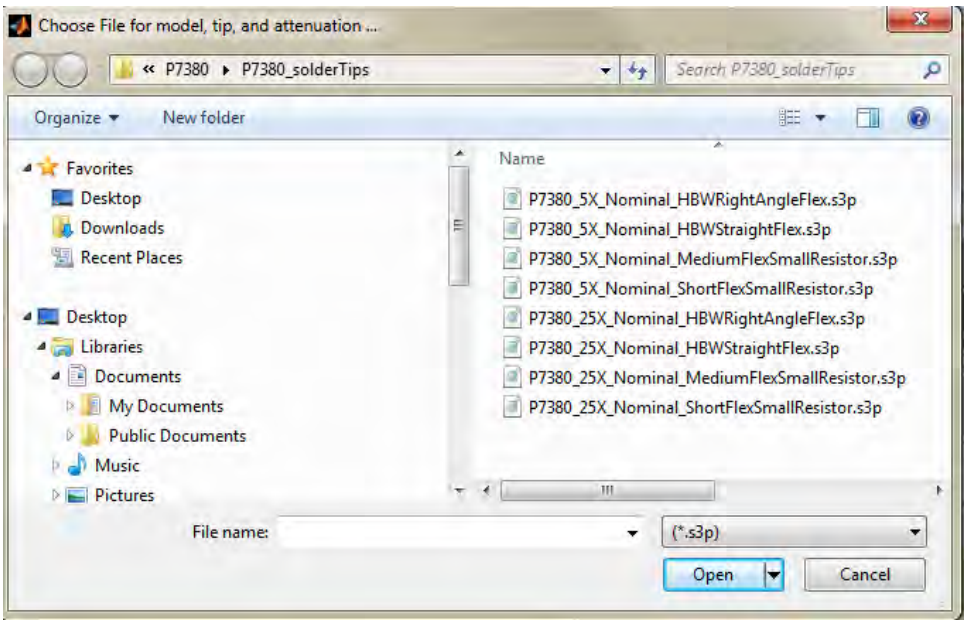
Shown below are the tips for P75xx family of probes. However, only the Performance Solder Tip is currently supported with S-parameter sets.



Choosing the correct 3-port S-parameter file. Press **De-embed** on the Main Menu. On the Cascade Tab, under **Probe**, select the **High Z** radio button. Then press the **Probe** button on the diagram. This brings up the Probe Configuration menu:



On the **Probe** drop-down menu, choose the correct model that is in use. For example, P7380 was selected in the image above. The browser will then open the correct directory for the selected probe model:



Choose the correct file for the probe's current settings. Note that the file name contains the probe model, and a gain number such as 5X or 25X, and it also contains a name for the tip that is in use. You'll need to correlate the tip name in the filename using the probe tip images shown above.

The gain setting for a probe is indicated by LEDs on the probe comp box that plugs into the oscilloscope input channel connectors.

NOTE. *Tri-mode probes, such as the 75xx models, are able to operate under 4 possible modes. However, for SDLA, the S-parameter support currently only allows a choice for differential mode, which is identified as A-B selection on the probe comp box that plugs into the oscilloscope.*

SMA Probes. The SMA probe S-parameter files include the matched pair of SMA cables that come with the probe. There are no tip selections. The attenuator choice is included in the file name and the LEDs on the probe comp box indicate which setting is in use.

Scope Settings when Using a Probe with SDLA. The oscilloscope DSP filters must be turned on while using the probe in conjunction with SDLA. To check that they are turned on, go to the oscilloscope's Vertical menu. Make sure that **Digital Filters (DSP) Enabled** radio button is selected. In addition, go to the scope's Vertical menu **Chan X** tab on the left, and select the channel which the probe is connected to. Then, on the scope menu, select **Vertical > Probe Cal**. Press the **Select** button to bring up the probe tip selection menu. Make the radio button selection in this menu match the tip that is in use on the probe. This insures that probe DSP is turned on. (Note: not all tips are supported with S-parameters, as mentioned above.)

Then, SDLA will correctly de-embed the current probe DSP response, and replace it with the probe combined with user data, and produce the results in a math waveform slot on the scope display. This way, channel X of the scope will have the nominal filter response that does not include user data for the probe connection, but the test point math waveform created by SDLA will represent the response of the system that includes both the probe and its actual connection to the DUT.

P7520A, P7625, P7630, P7633, and P77XX probes. For these probes, the S-parameters are stored internally in the probe. Therefore, they are loaded into SDLA directly from the scope. No file browser is opened. A probe must be plugged into the oscilloscope source channel in order for the S-parameter set to be loaded into SDLA.

User DATA probes. In some cases, such as for interposer setups where custom modified probe tips are sometimes used, it may be that the oscilloscope does not have nominal DSP probe data. In this case, on the scope menu, select **Vertical > Probe Cal**. Press the **Select** button to bring up the probe tip selection menu. Choose **Other Tip (no DSP)**. This way, the scope will not apply DSP for the given probe model. Instead, you may use the user probe data that is selected from the probe drop-down menu under **User**. A file browser will open, and you may load the custom probe data S-parameter set for use with the interposer. This data may be provided on a custom basis from Tektronix or from other sources, such as a custom simulation model.

NOTE. *You must have saved S-parameter data there prior to loading.*

SEE ALSO:

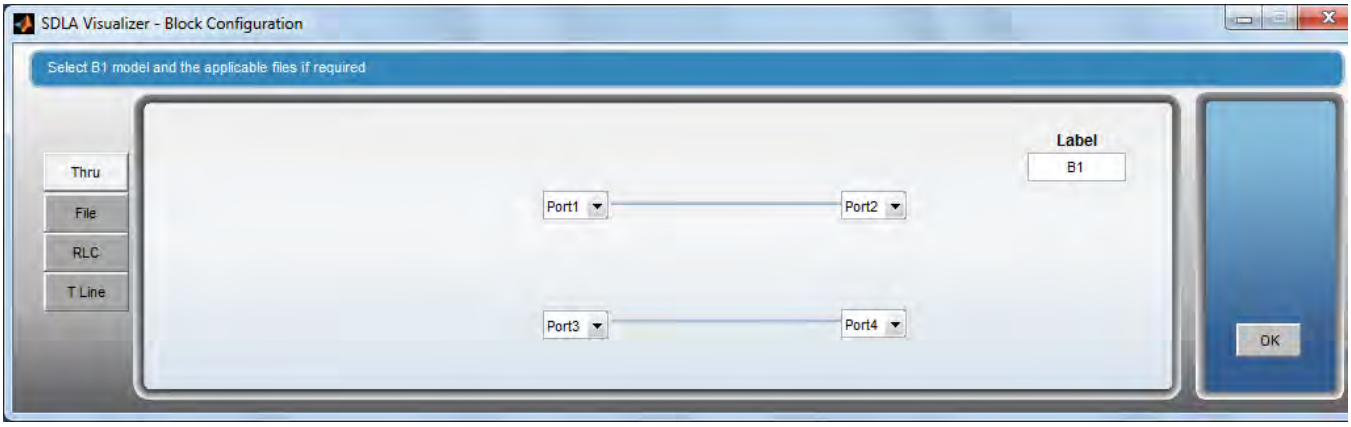
- *Configuring Probes*
- *De-embed/Embed Menu*

Block configuration menu

Use the Block Configuration menu to configure the cascaded S-parameter modeling blocks **B1–B8** in the De-embed/Embed Menu. (To configure the final block, use the *Load Configuration Menu*.)

The Block Configuration menu has four tabs that offer different categories of models:

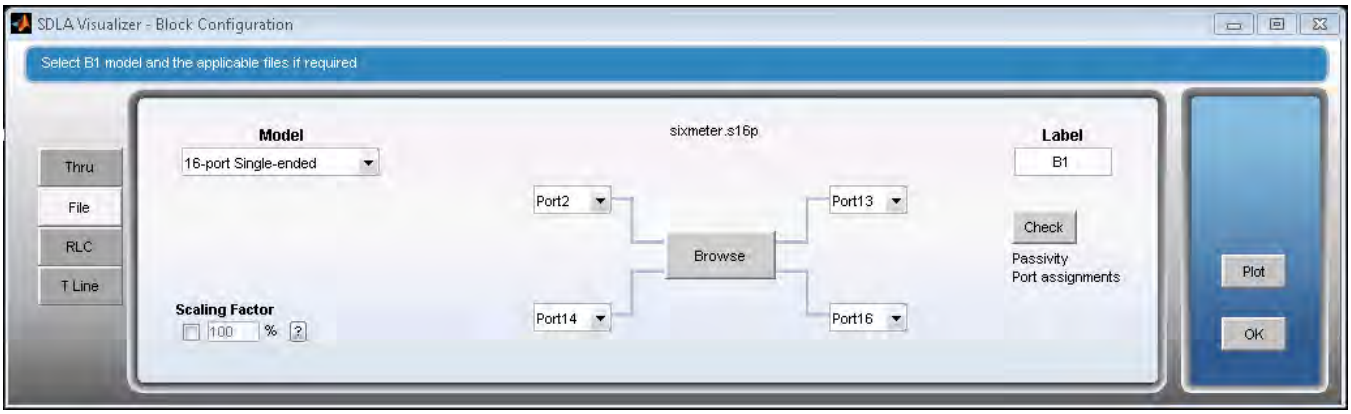
Thru Tab. The Thru block model is used when the block is not a necessary part of the cascade. It represents an ideal model that has no effect upon signals in the system.



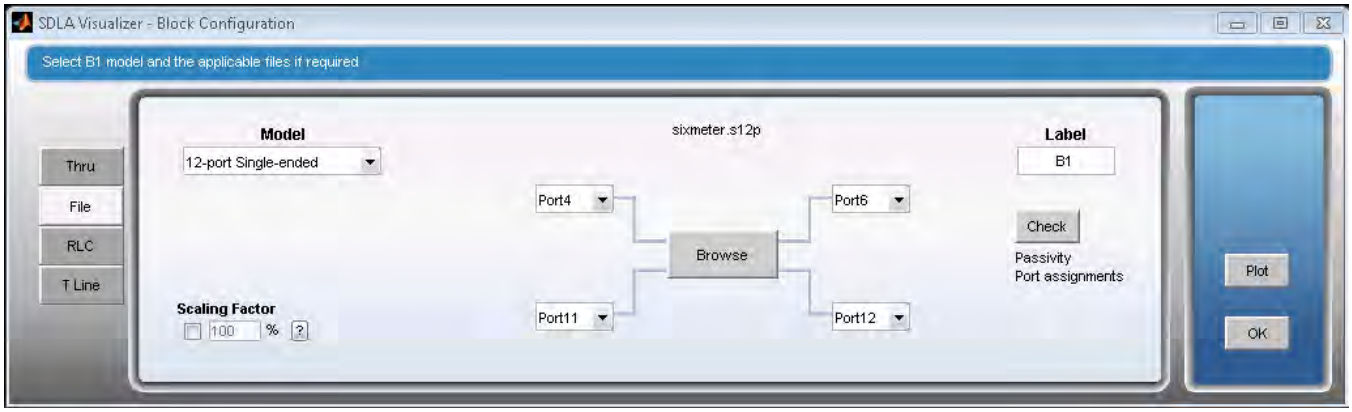
File Tab.

The File Tab allows you to choose from six models represented by data read from files:

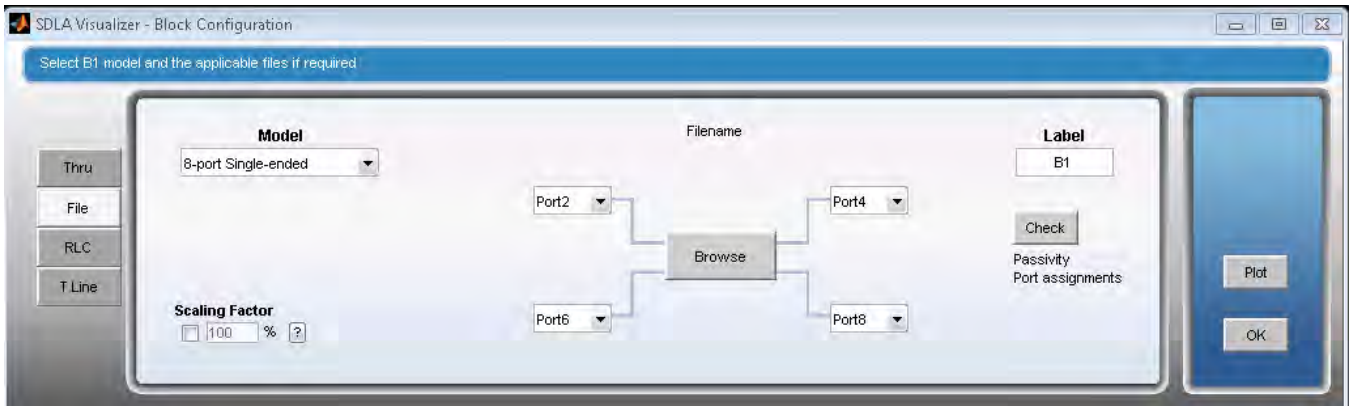
16-Port. Extract a 4- port file from a single 16-port S-parameter file. You can load a 16-port S-parameter file to represent the block. Select any four ports from the 16 ports. When apply is clicked, it plots the selected four port S-parameter. All S-parameter terms in the data are taken into account when computing test point transfer functions.



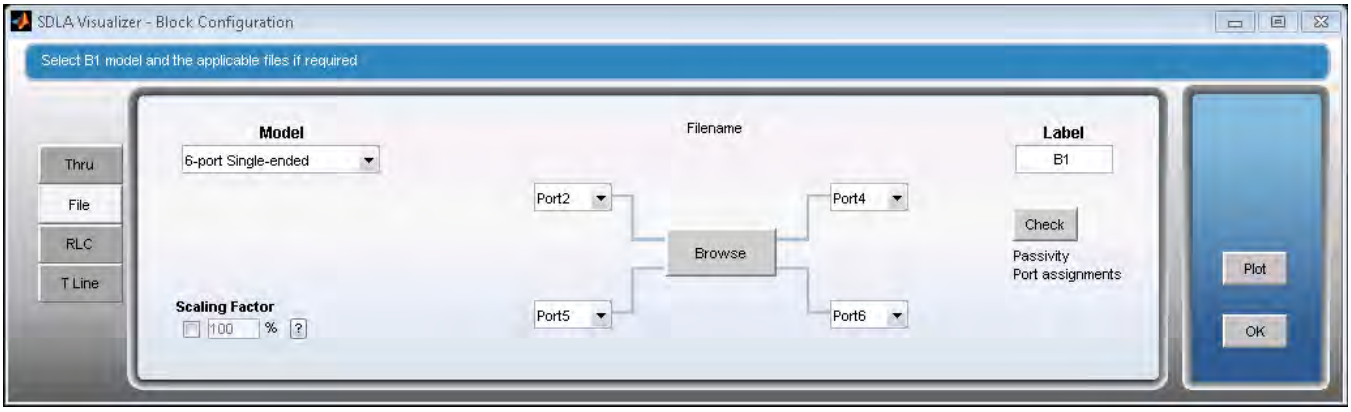
12-Port. Extract a 4- port file from a single 12-port S-parameter file. You can load a 12-port S-parameter file to represent the block. Select any four ports from the 12 ports. When apply is clicked, it plots the selected four port S-parameter. All S-parameter terms in the data are taken into account when computing test point transfer functions.



8-Port. Extract a 4- port file from a single 8-port S-parameter file. You can load an 8-port S-parameter file to represent the block. Select any four ports from the 8 ports. When apply is clicked, it plots the selected four port S-parameter. All S-parameter terms in the data are taken into account when computing test point transfer functions.



6-Port. Extract a 4- port file from a single 6-port S-parameter file. You can load a 6-port S-parameter file to represent the block. Select any four ports from the 6 ports. When apply is clicked, it plots the selected four port S-parameter. All S-parameter terms in the data are taken into account when computing test point transfer functions.



4-Port Single-ended. Models a single 4-port S-parameter set, as shown above. You can load a 4-port S-parameter file to represent the block. All S-parameter terms in the data are taken into account when computing test point transfer functions.

4-Port Differential. Models a mixed mode S-parameter set. Press here for more information.

You can load a 4-port S-parameter file that has been saved with a mixed mode format for the data. The differential block allows the filename and path for the mixed mode S-parameters to be specified using a **Browse** button. The block is shown with two differential ports, but physically it still has 4 single-ended ports. SDLA will convert the mixed mode data into a single-ended data format for use within the cascade of blocks.

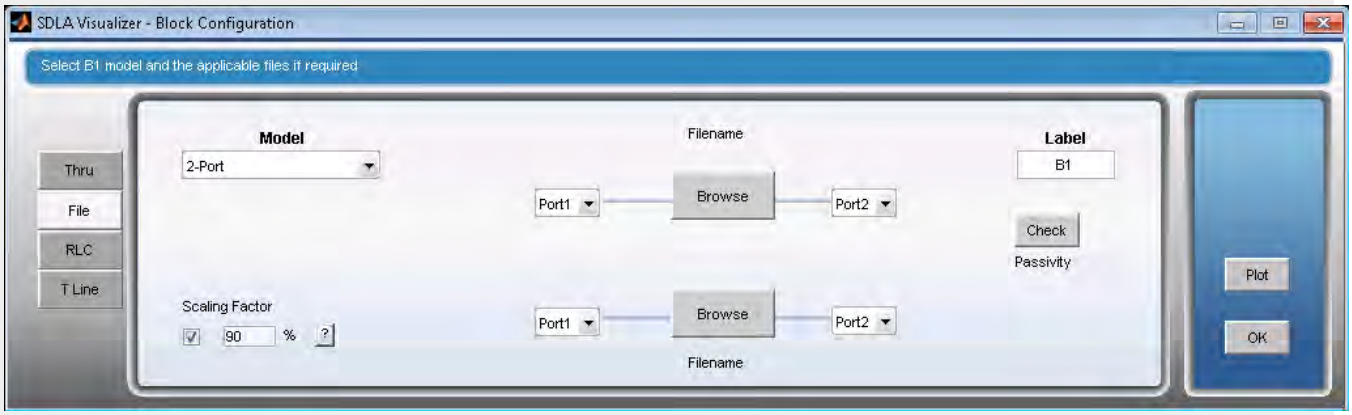
SDLA supports two ways of organizing the S-parameter data in the matrix. **Typical** shows a typical arrangement of mixed mode S-parameter data read from the file. **Alternate** provides a second arrangement.

NOTE. *The mixed mode representation of S-parameter data is not supported by the Touchstone 1.0 file format. Therefore, only two organizations of the file data is supported, as shown below:*

2-Port. Models two 2-port S-parameter sets. Press here for more information.

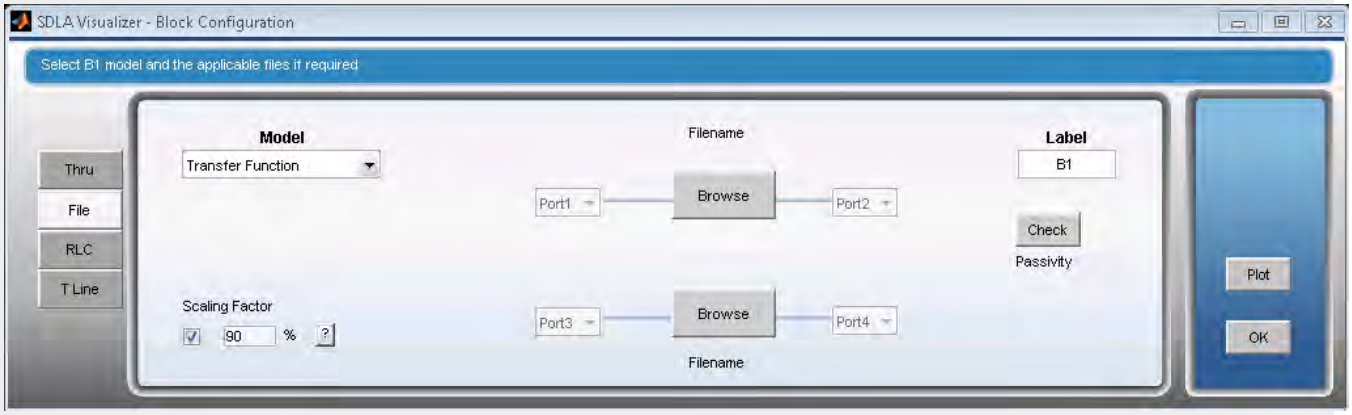
This allows two 2-port S-parameter files to be loaded into the 4-port block model. SDLA will convert these into one 4-port S-parameter set with ideal cross-coupling terms set to zero.

A common use for this choice would be to represent a pair of shielded cables connected between a fixture and the scope.



Transfer Function. Models a frequency domain set of complex data. Press here for more information.

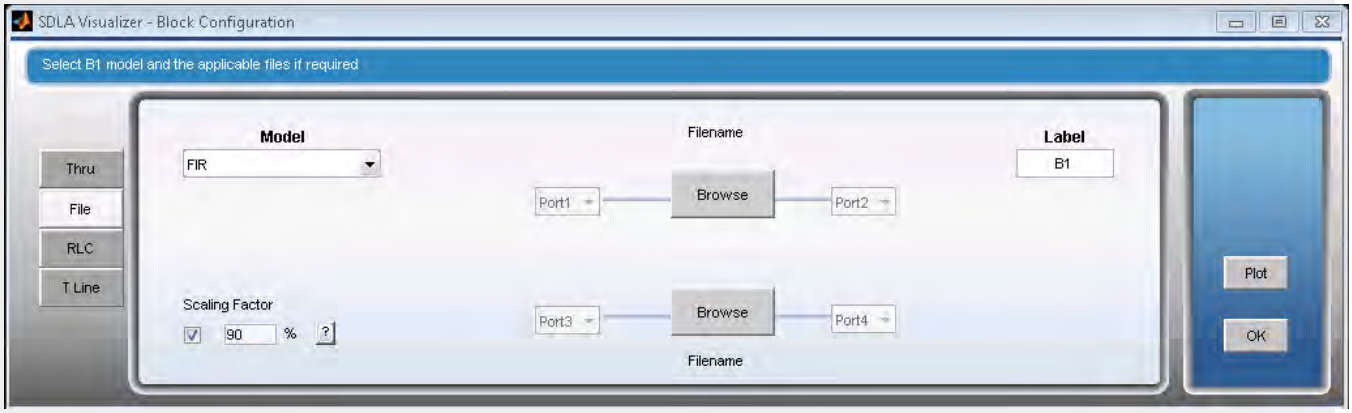
This allows two files containing transfer function data in the frequency domain to be loaded to represent the block. The file will be in the s1p Touchstone 1.0 format. This format contains a frequency column, a real or magnitude column and an imaginary or phase column. SDLA will convert these into a single 4-port S-parameter set with ideal cross-coupling and reflection coefficient terms set to zero. A common use for this choice would be to represent a pair of shielded cables connected between a fixture and the scope.



FIR. Models a time domain impulse response. Press here for more information.

This allows two files containing FIR filter coefficients data in the time domain to be loaded to represent the block. The file shall be in the oscilloscope arbflt() ASCII format. SDLA will convert these into one 4-port S-parameter set with ideal cross-coupling terms set to zero. The reflection coefficient terms are also set to zero.

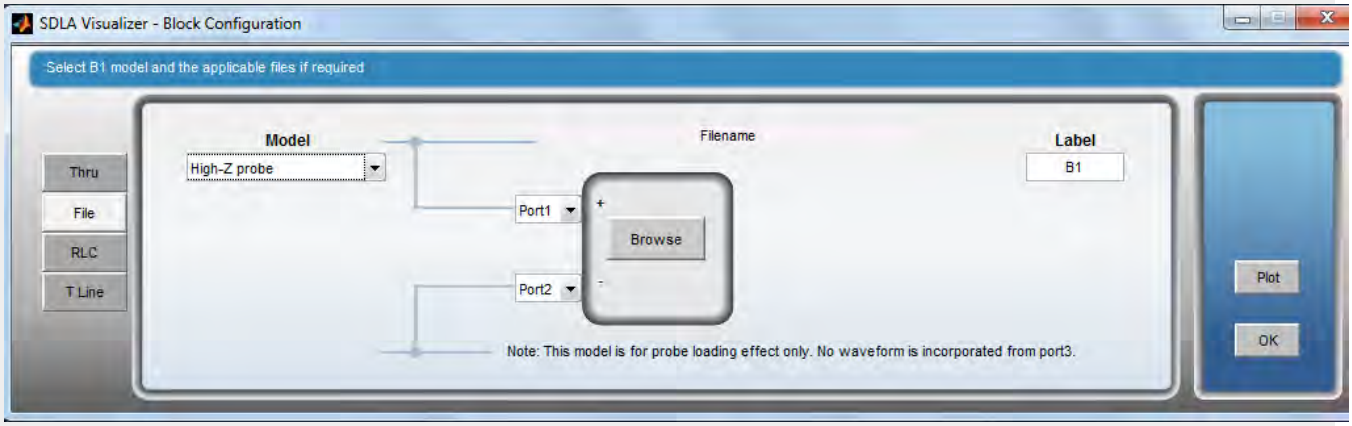
The file may contain comment lines with # as the first character. The file may contain multiple lines of filter coefficients, where the first number followed by a "**;**" is the sample rate. The remaining numbers are the filter coefficients separated by space comma.



High Z probe. Models the loading of the probe. Press here for more information.

This allows a 3-port S-parameter set representing a probe to be loaded. This model places the probe tips on line A and line B in parallel with the signal path lines. A potential use would be to observe how oscilloscope or logic analyzer probes load the system.

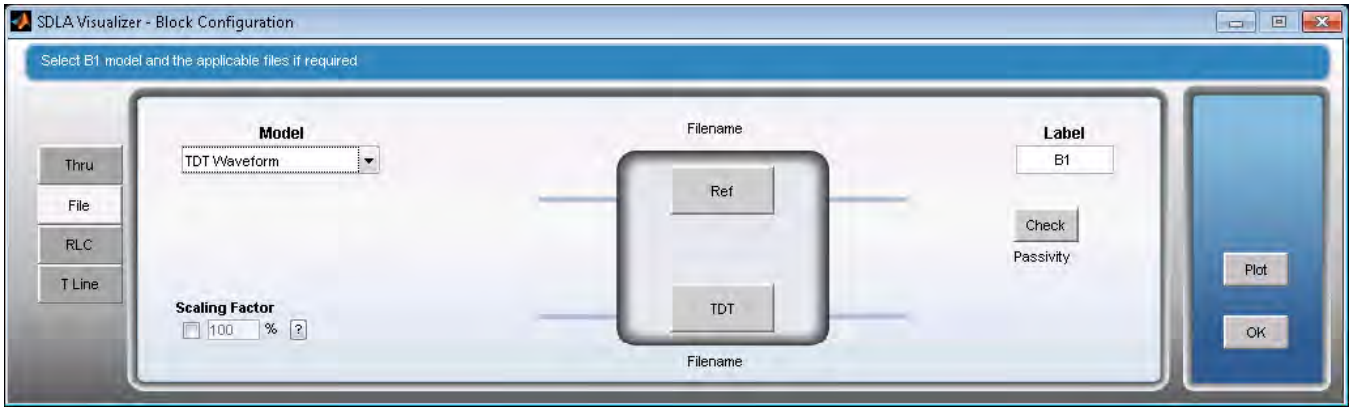
NOTE. *This model is representing probe loading effects only. There is no acquired waveform entering the simulation system from this model.*



TDT Waveforms. Models two waveforms from the TDT measurement. Press here for more information.

This allows two waveforms to be loaded as reference waveform and TDT waveform. These two waveforms are from the TDT measurement. SDLA converts these into one 4-port S-parameter set. Insertion loss term is computed from these two waveforms.

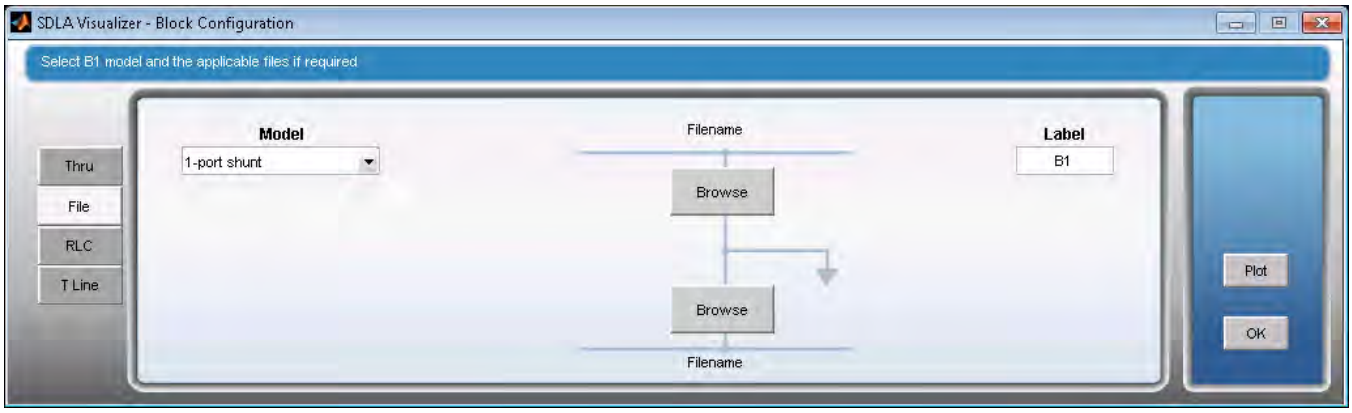
A common use for this choice would be that TDT measurement is performed and the reference waveform and TDT waveform are obtained.



1-Port Shunt. Models two 1-port S-parameter sets in shunt connection. Press here for more information.

This allows two 1-port S-parameter files to be loaded as a shunt connection. SDLA converts these into one 4-port S-parameter set in series.

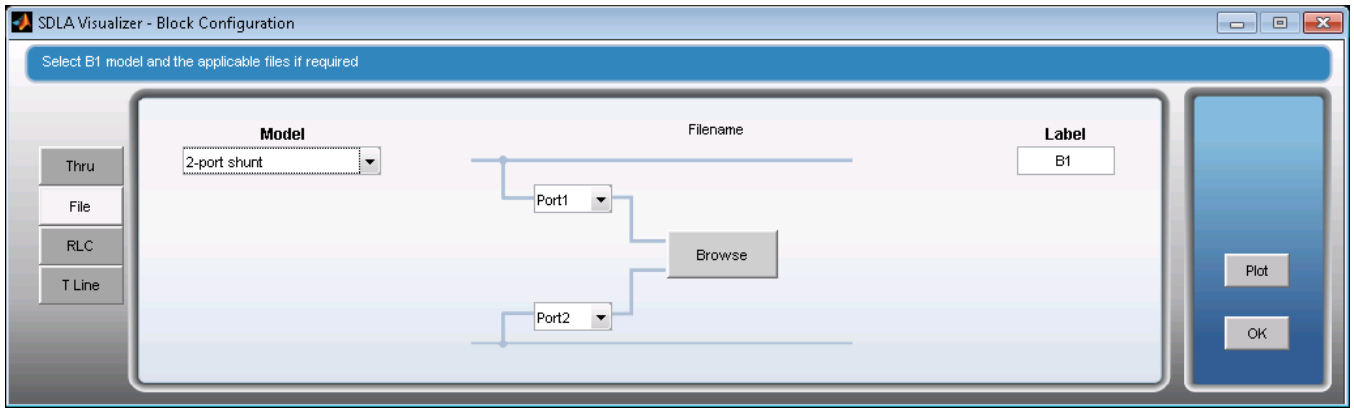
A common use for this choice would be there are shunt connections represented by two 1-port S-Parameter files.



2-Port Shunt. Models one 2-port S-parameter set in shunt connection. Press here for more information.

This allows one 2-port S-parameter file to be loaded as a shunt connection. SDLA converts these into one 4-port S-parameter set in series.

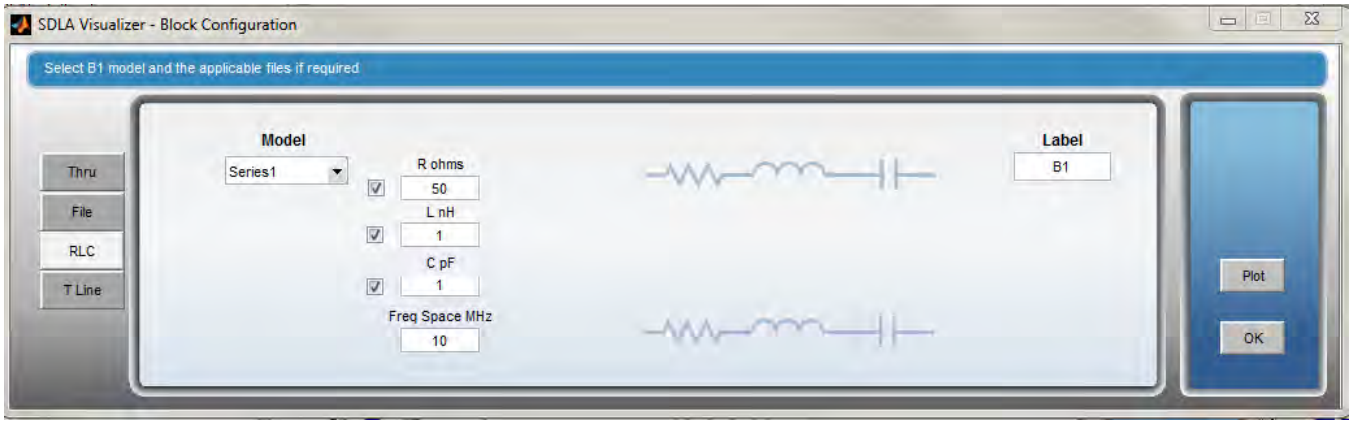
A common use for this choice would be that there are shunt connections represented by a 2-port S-Parameter file.



S Parameter Scaling. S Parameter Scaling is used to scale the S parameter. The small square check box is used to enable or disable the Scaling Factor. The Scaling Factor is not changed with it.

When enabled, the scaled S parameter is plotted and applied to the cascading. Be aware, the crossing and reflection terms are zeroed out during the scaling process, even at the 100% scaling. The default is 90%. Scaling is from 20% to 200%.

RLC Tab. This allows RLC (resistor, inductor, and capacitor) elements to be used to model the block. SDLA computes a set of 4-port S-parameters that will be used in the cascade. The cross-coupling terms will be set to zero.



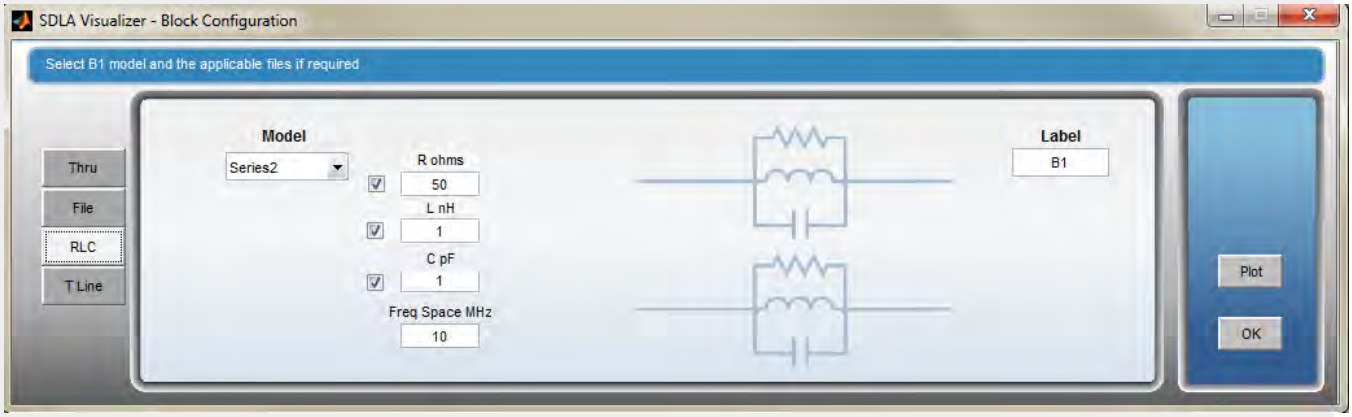
The RLC Tab **Model** drop-down menu offers six different series and shunt configurations of RLC networks. Press here for more information.

Series 1

Represents a series RLC network in series with each line (shown above).

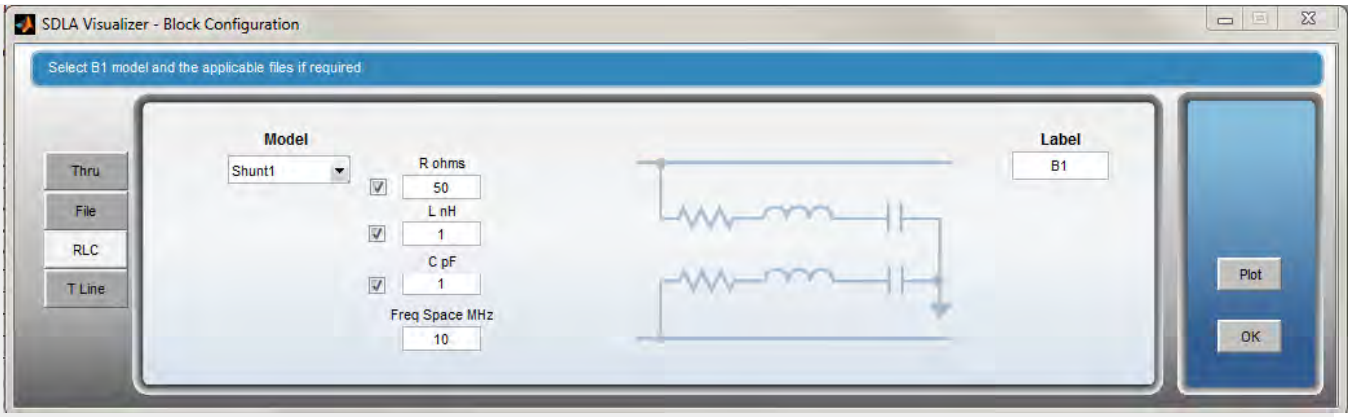
Series 2

Represents a parallel RLC network in series with each line:



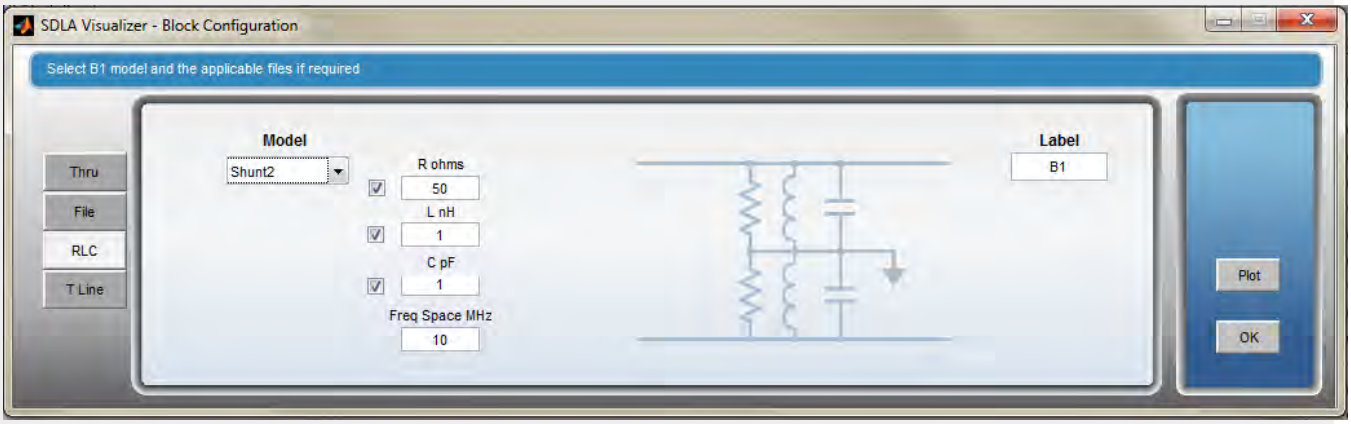
Shunt 1

Represents series RLC networks in shunt with each line:



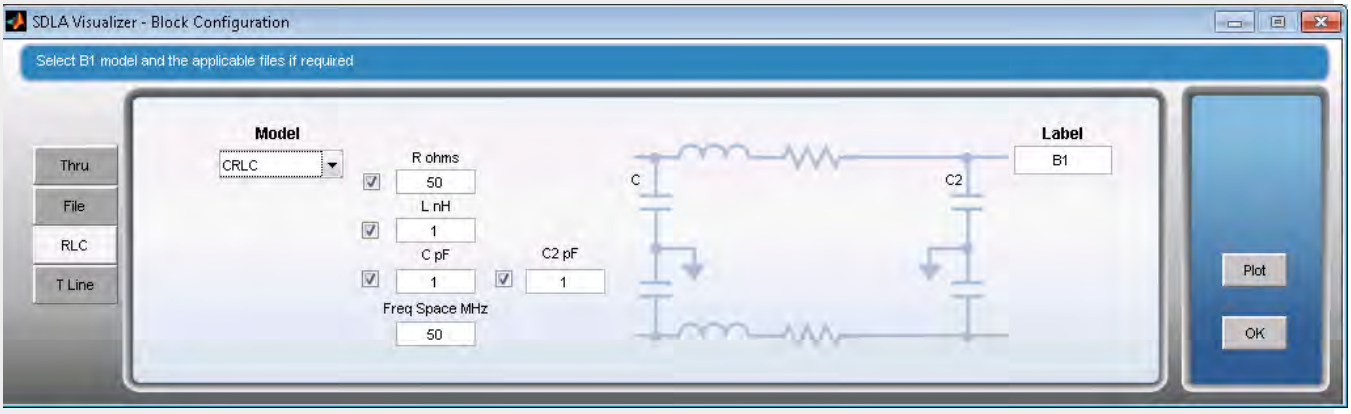
Shunt 2

Represents parallel RLC networks in shunt with each line:



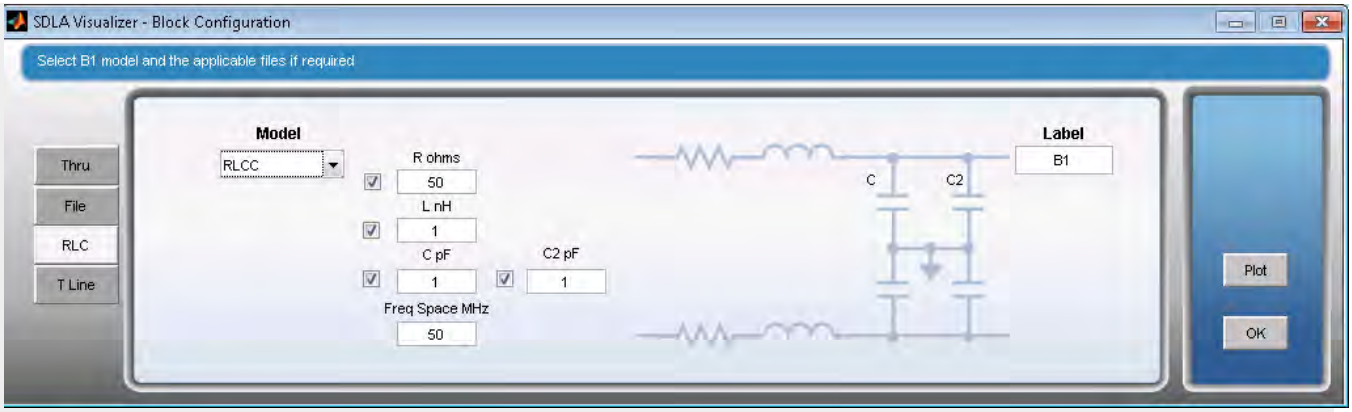
CRLC

Represents a shunt capacitor, series inductor, series resistor and a shunt capacitor with each line:



RLCC

Represents a series resistor, series inductor and two shunt capacitors with each line:



R, L, C, C2 edit boxes

These determine the values for these components.

R, L, C, C2 check boxes

When checked, the **R**, **L**, **C**, or **C2** value will be included in the circuit. When not checked, the R, L, C, or C2 element will be replaced with a short if it is a series element, or with an open if it is a shunt element.

Freq Space MHz

This edit box specifies the frequency spacing for the S-parameter set that will be computed for this network. Frequency spacing determines the time duration the S-parameter covers.

Label

This edit box determines what label will appear on the block diagram in the De-embed/Embed Menu, depending on which block this is located in.

Plot

This will open a new window containing all the plot menus for the various ways in which the 4-port S-parameter set may be viewed.

OK

This menu button closes the block menu and returns to either the Embed or De-embed menu, depending on which one was used to open the block.

T Line Tab.

This allows you to define a lossless transmission line. SDLA computes a set of 4-port S-parameters depending on the parameter settings in the edit boxes. The cross-coupling terms shall be set to zero. Press here for more information.

Z0 ohms

This allows you to specify the characteristic impedance of the transmission line pair.

Delay ns

This allows the delay through the transmission lines to be specified in ns.

Freq Space MHz

This specifies the frequency spacing for the 4-port S-parameter set that will be created for the transmission line model.

Plot

This may be used to view the characteristics.

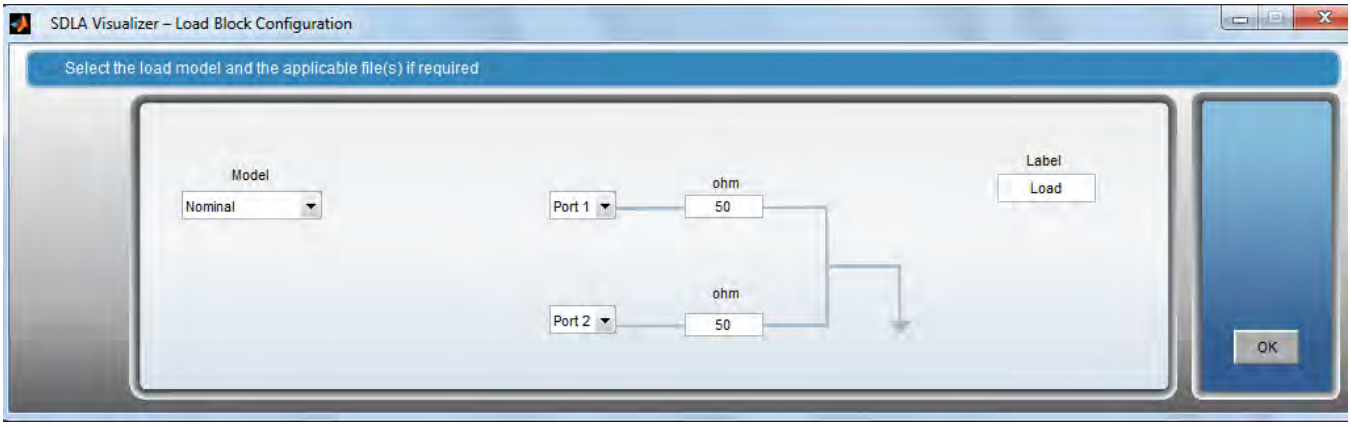
SEE ALSO:

- *De-embed/Embed Menu*
- *Load Configuration Menu*

Load configuration menu

The final block in the De-embed/Embed Menu cascade diagram is where you determine what will load the output ports of the cascaded circuit. Pressing it brings up the Load Configuration menu. (To configure blocks **B1-B8**, use the *Block Configuration Menu*.)

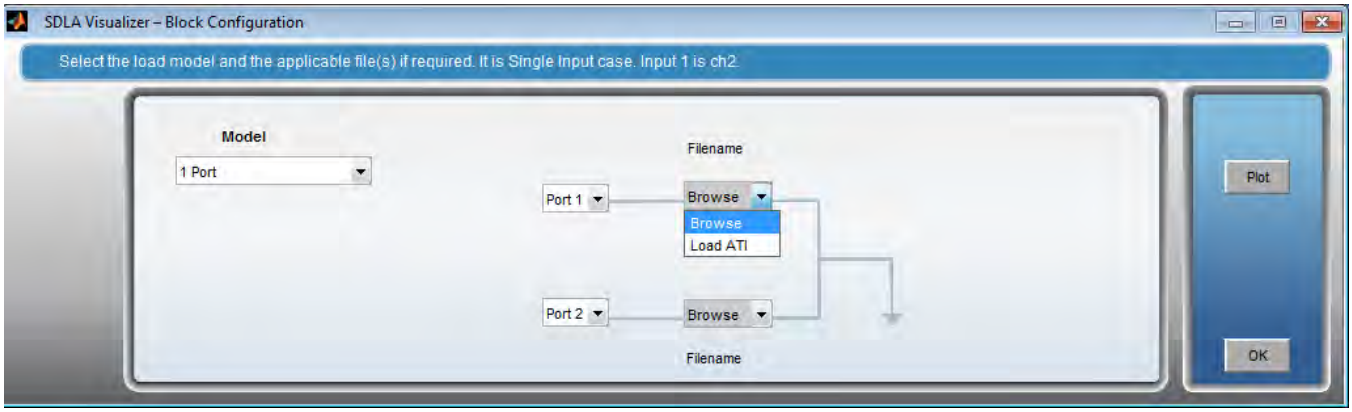
De-embed Cascade Load Block. The final block on the **De-embed Menu** cascade diagram is labeled either **Scope**, **SMAProbe** (RT only) or **Load**. When you press it, a different Load Configuration Menu will come up depending on how you have configured your model. For example, the image below shows the default menu that comes up without a probe:



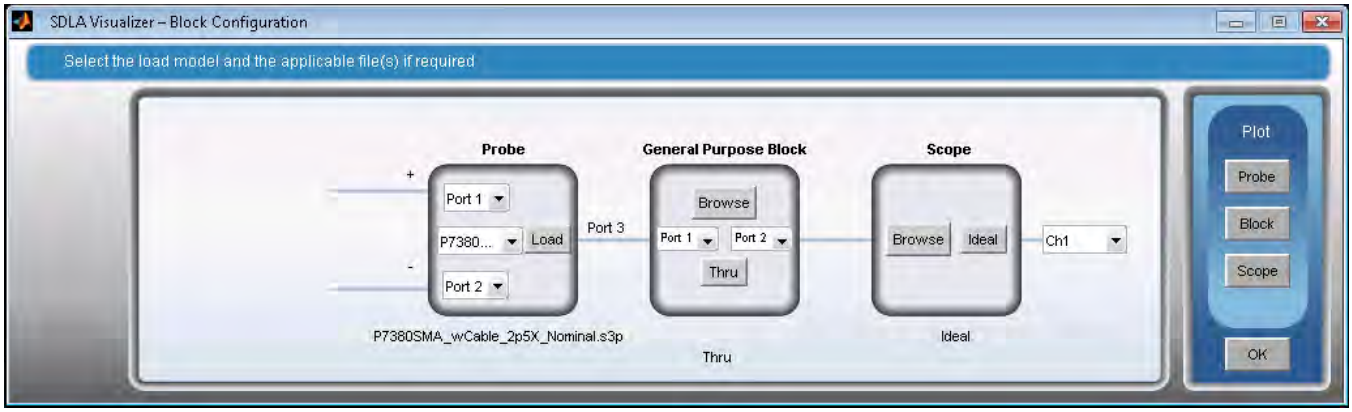
S-parameters for an ATI channel .

- **SX type scope** If the source channel is ATI, clicking the Load button in the De-embed menu will open the Load menu. After select 1-Port from Model pull down list, two options show up for file loading;

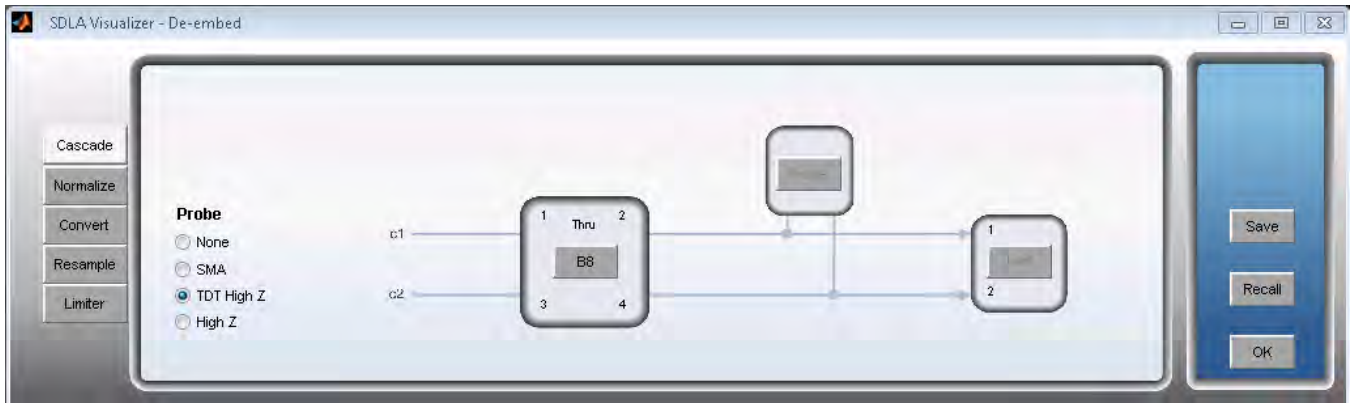
  1. Browse option lets you select any *.s1p file to load to the block.
  2. Load ATI option automatically loads the ATI channel s-parameters to the block.



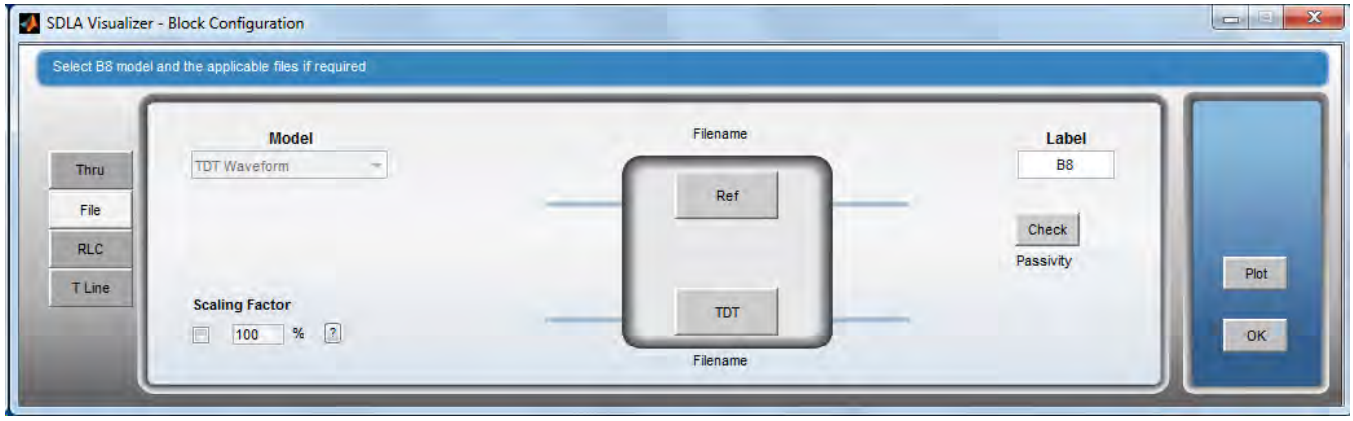
If, instead, you have configured it for an SMA Probe (RT only), the following menu comes up. The middle block allows for the effects of cabling between the probe and the scope. For further information, see *Configuring Probes*.



If you have configured it for TDT High Z the following menu comes up. Blocks B1 through B7 are ignored and B8 is defined by time domain waveforms.

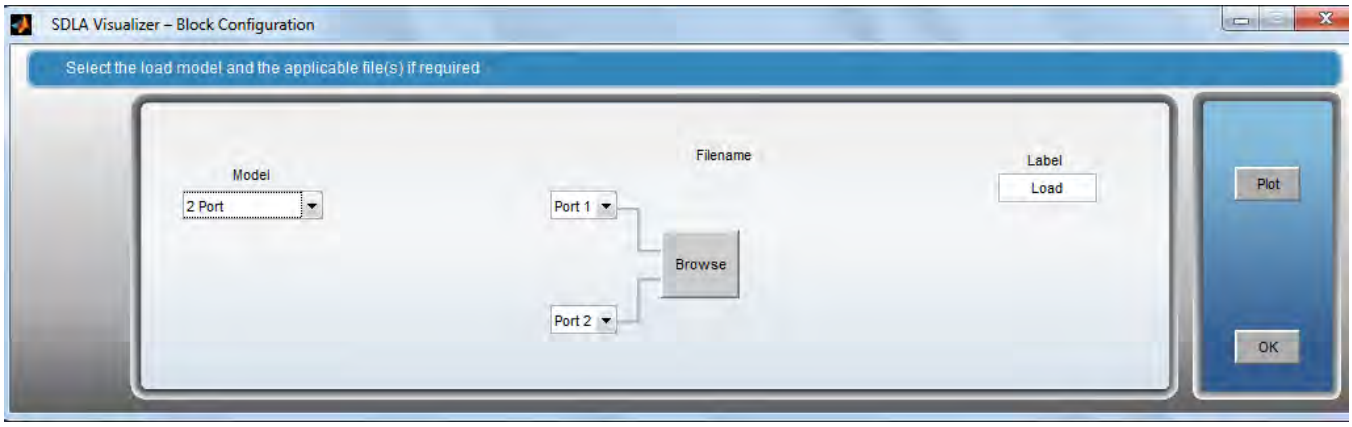


Clicking the B8 button displays the following menu in which the B8 block can be defined by a reference and a TDT waveform.



Embed Cascade Load Block. The final block on the **Embed Menu** cascade diagram is labeled **Rx Load**. Pressing on it brings up the Load Configuration Menu show below, which allows you to determine the model that will load the output ports of the simulation circuit. In many cases, this would model a physical receiver.

The impedance can be modeled as a nominal value, one 2-port S-parameter block, or two 1-port S-parameter blocks by choosing one of the options in the **Model** drop-down list. By default, SDLA assumes 50 Ohm impedance. Below is the menu that comes up with one 2-port S-parameter block:



SEE ALSO:

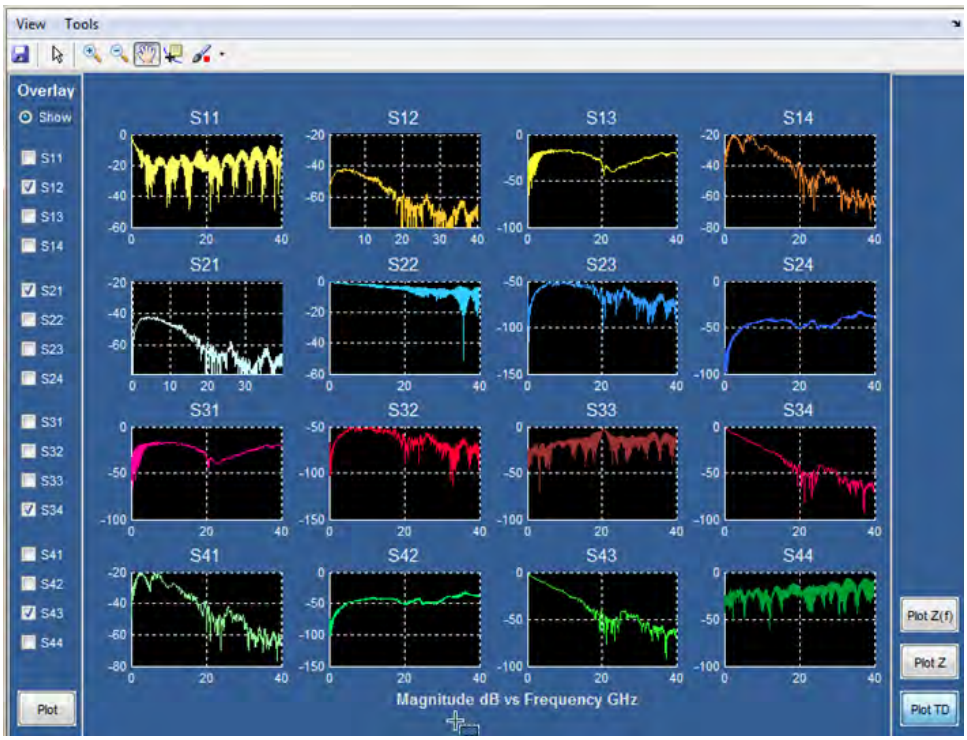
- *De-embed/Embed Menus*
- *Block Configuration Menu*

Plots

Plots

Plots are essential aids for setting up and verifying the system. SDLA Visualizer provides a variety of context-sensitive plots that show the results of running the enabled processing blocks and the test points. These can be used along with DPOJET and oscilloscope plots for tasks such as analyzing the quality of the S-parameters, verifying the configuration of each block as you configure the circuits, or determining port numbers.

Navigation features include zoom (+) and pan tools; some plots also include measurement cursor tools.



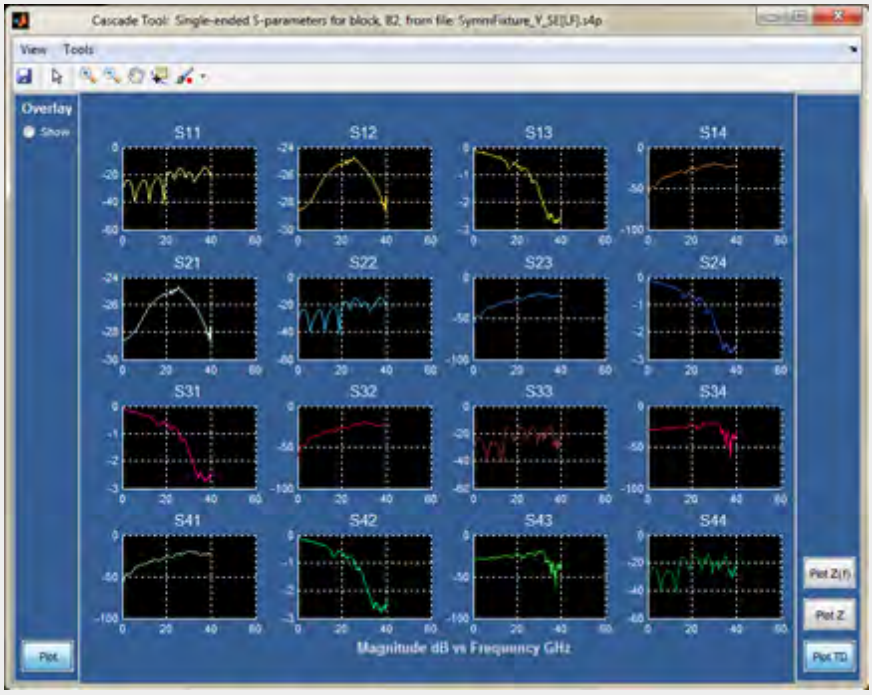
For some examples of how to troubleshoot using S-parameter plots, see *Using Plots for Troubleshooting S-parameters*.

Here are just some of the SDLA Visualizer plots available:

- **Comprehensive S-parameter plots**. Extensive plots of the S-parameters allows for full insight into the system characteristics. An **Overlay** feature is available for some plots. Some examples of S-parameter plots:
  - 6-port, 4-port, 3-port, 2-port, 1-port plots

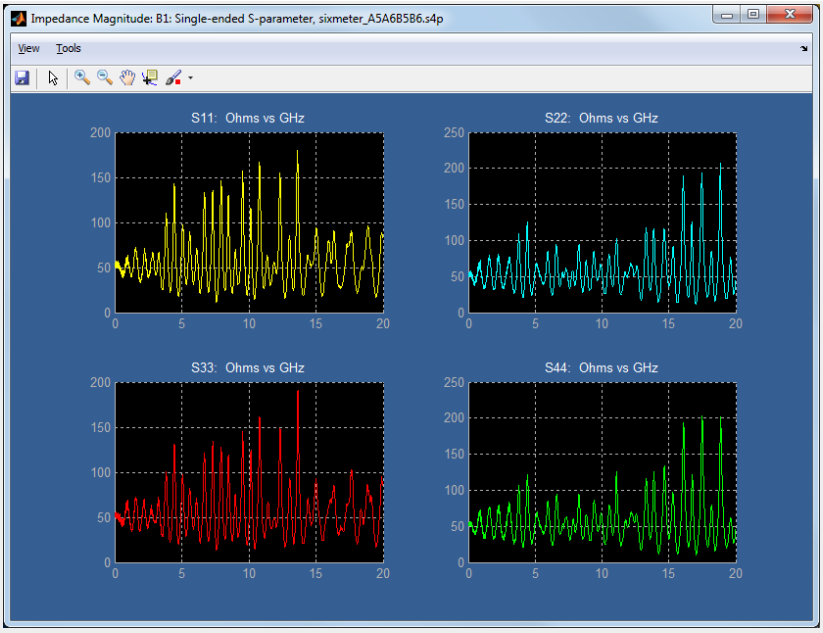
Use these plots to:

- Quickly verify port assignment. You can tell by the shape of the curve which one is insertion loss.
- Validate that the magnitude is correct. Typically, the insertion loss should be higher at high frequencies; reflection and cross talk is typically higher at higher frequencies.
- Do a passivity check. None of the S-parameters of a passive system should go above 0 dB in the frequency domain. All data can be less than 0d and yet the system may still violate passivity where the total output power is more than the input power. Note that viewing the plots is a first step only; for a more extensive check, go to a file load tab in a block menu. For cases where the S-parameter data is loaded from a file, a passivity check button becomes available.
- Check whether models are Single-ended or Mixed Mode. For a single-ended system, transmission terms such as **s21**, **s12**, **s34**, and **s43** are equal for an ideal passive system. However, if the data had been converted to mixed mode, the common mode transmission response is generally noticeably different than the differential transmission. In other words, **S34** and **S43** would equal common mode, and would look different than the differential mode response plotted in **S21** and **S12**.



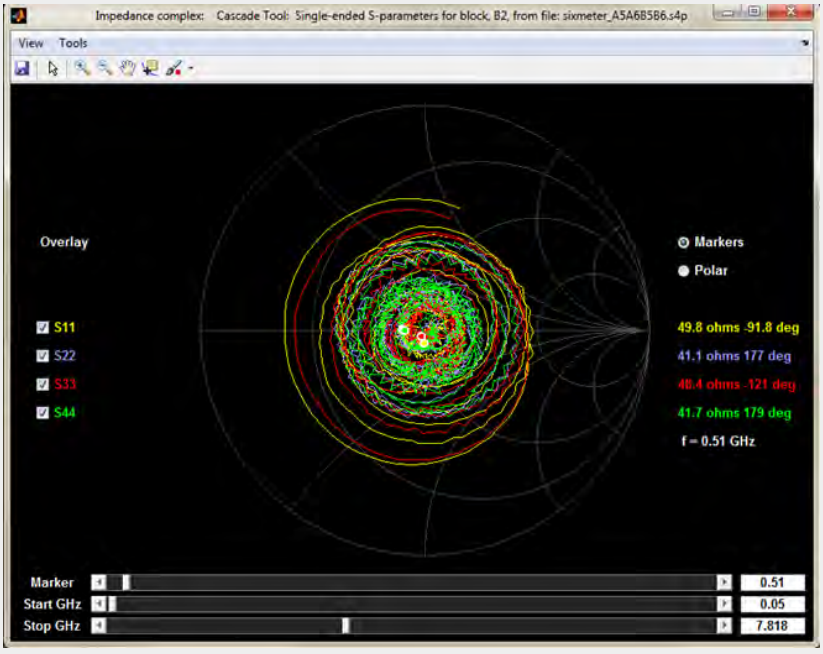
- Impedance vs. magnitude (Plot Z(f) button)

These plots let you quickly observe how impedance varies over frequency for the reflection coefficients in the S-parameter set.



- Smith Chart impedance (Plot Z button)

A Smith Chart provides impedance, phase, and magnitude information, including impedance in polar or rectangular format, markers readout, start and stop frequencies, and overlay:

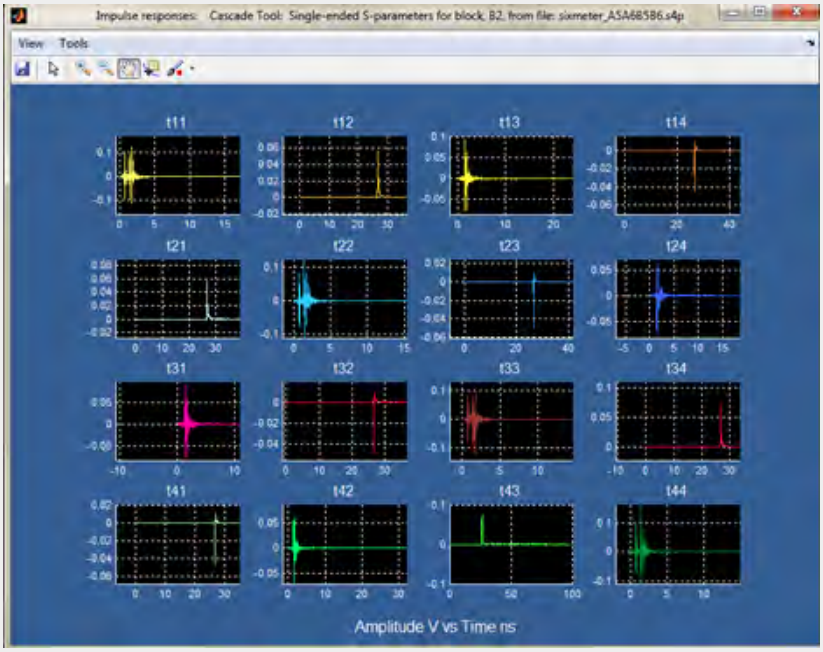


- Time Domain plots (Plot TD button), including impulse response vs. time and step response vs. time

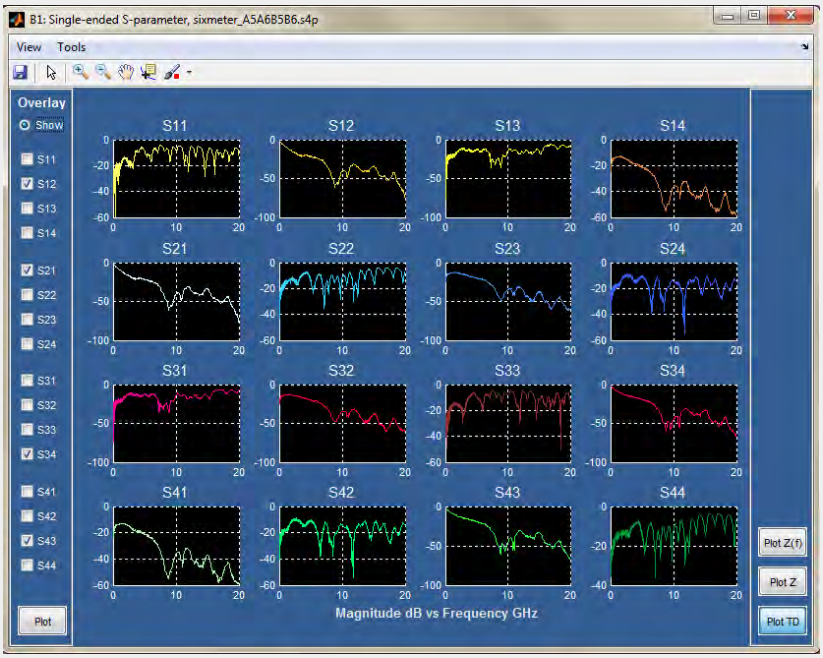
In the time domain, all the plots should be settled by the end of the time record. If not, this could mean that the measurement was performed with too short of a time interval. Note that if a pulse is close to the beginning of the record, such as a typical **t11**, then it should be expected that a portion of the non-causal response at the front is wrapped to the very end of the record. SDLA handles the wrapped-end part internally.

This non-causal part is not real for the analog circuit that was measured; it is an artifact of the band-limiting effect of performing the IFFT operation to transform the S-parameter set to the time domain.

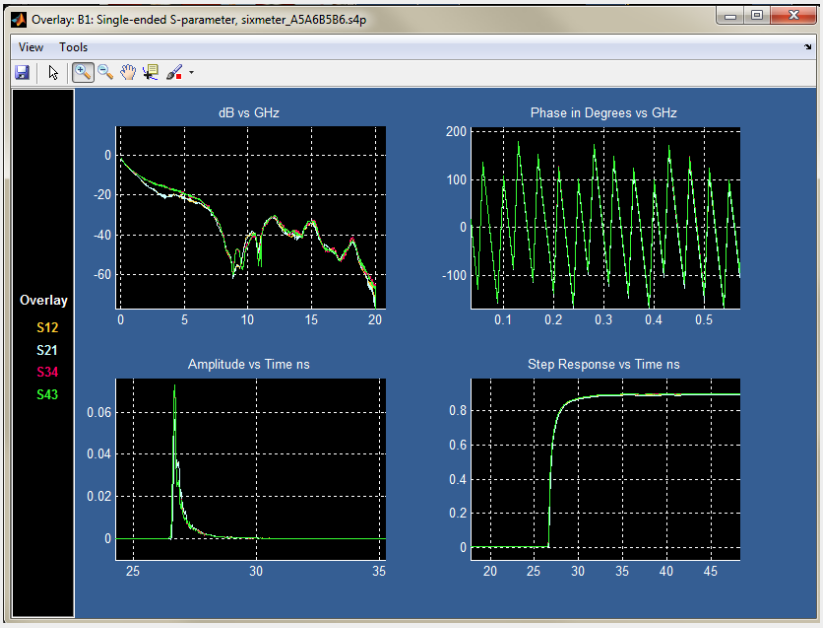
If the frequency spacing is too wide, the time domain will show aliasing where the pulse is wrapped in the time domain to an aliased position.



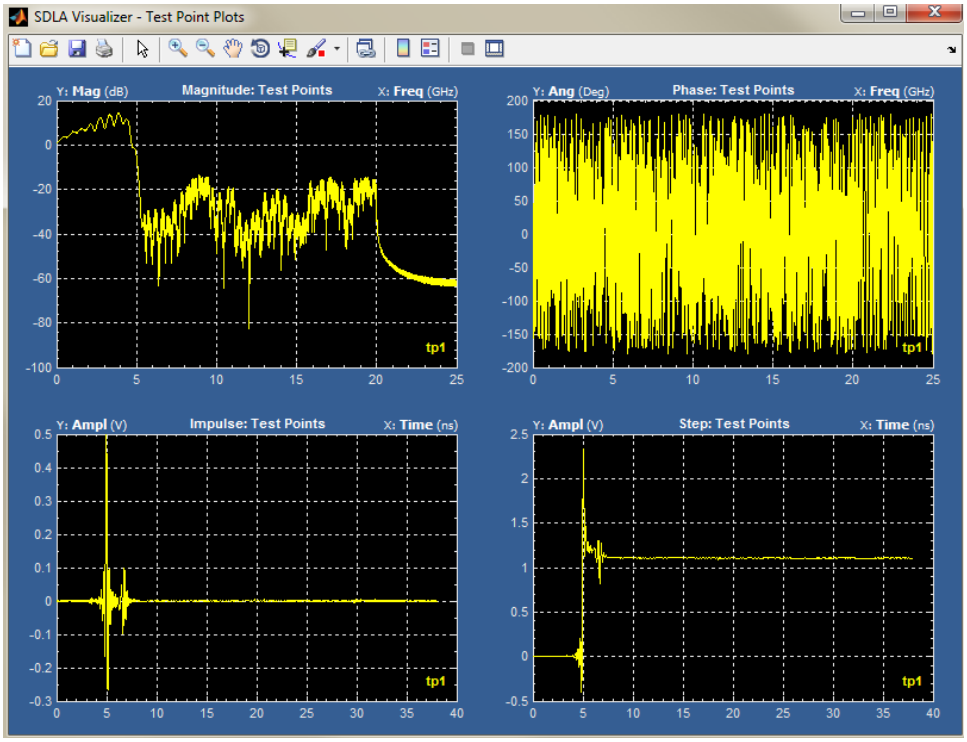
- Pressing Overlay on the left side lets you select up to 16 plots in one visual display. The overlay plot is performed on four axes: Magnitude vs. Frequency, Phase vs. Frequency, Impulse vs. Time and Step Response vs. Time:



The **Overlay Menu** is on the left side, with a **Plot** button at the bottom. Pressing **Plot** opens a window with four overlaid axes: dB vs. GHz, Phase in Degrees vs. GHz, Amplitude vs. Time, and Step Response vs. Time.



- **Test point filter (transfer function) plots**. Plots of test point filter responses allow for verification of the system setup. Any problems typically show up in the plots. Magnitude, Phase, Impulse and Step graphs are available.



- **Tx Emphasis plots.** For details, see *Tx Emphasis Menu*.

Additional plots are available via:

- **DPOJET eye diagram plots.** When the Main Menu **Config** button is set for Auto Configure, then when the **Apply** button is pressed, DPOJET will produce eye diagram plots for the test point waveforms that are turned on. These will include the source waveforms and waveforms from one or more of the test points that are enabled. DPOJET can create a maximum of four plots. Therefore, it may be necessary to go into the DPOJET menus to reassign the plots to view the waveforms desired. (To do this, from the scope menu, press Analyze>Jitter and Eye Analysis (DPOJET).)
- **JNB eye diagram plots.** JNB has an extensive collection of eye diagram plots as well as many jitter, noise, BER and spread spectrum plots, displaying up to four plots at once. it may be necessary to go into the JNB plots to reassign the plots to view the waveforms desired. (To do this, from the scope menu, press Applications > 80SJNB.)
- **Scope waveform plots.** The waveforms that represent the test points appear on the oscilloscope screen. They may be controlled for viewing by using the standard oscilloscope controls. Cursor measurements and standard measurements may also be applied.

SEE ALSO:

- *Using Plots for Troubleshooting S-parameters*
- *Understanding Test Points*

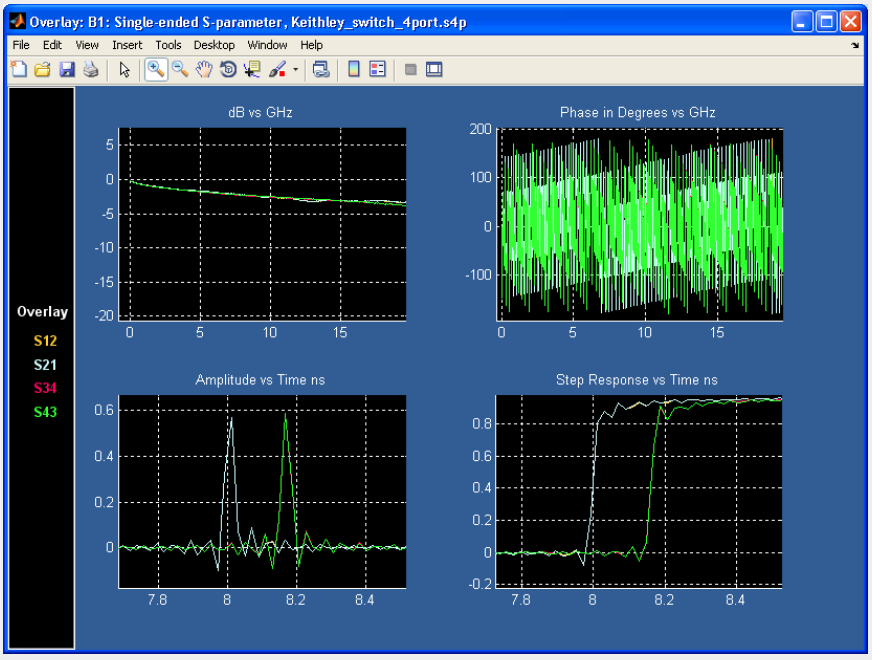
Using plots for troubleshooting s-parameters

SDLA Visualizer S-parameter plots include an Overlay tool, located on the left side, that allows you to view any selected plots on one display. This can be helpful in many scenarios, such as:

- Viewing a DUT with mismatched differential pairs

Viewing a DUT with Mismatched Differential Pairs

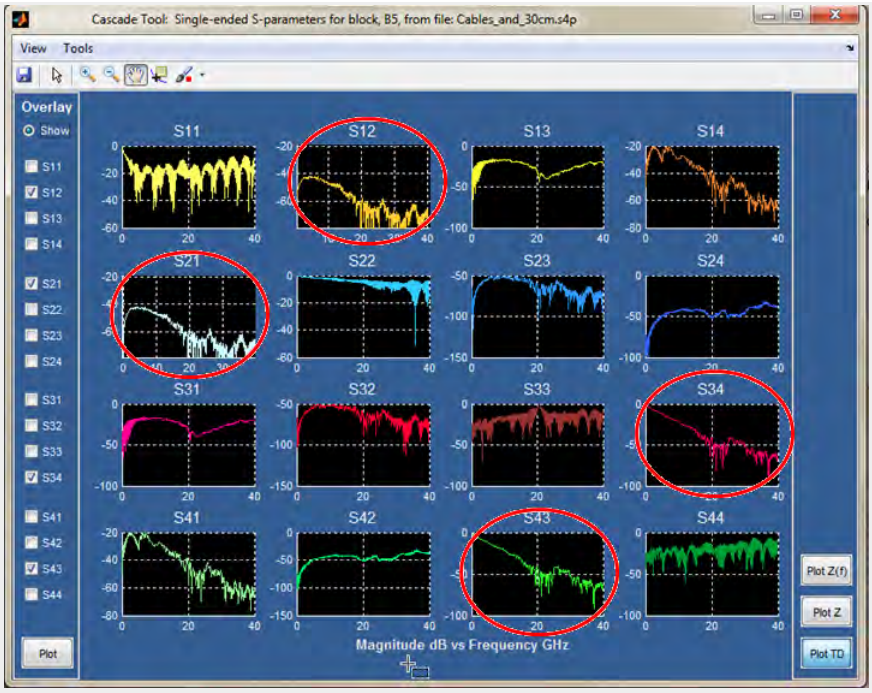
In this example, impulse plots reveal that the delay between transmission line pairs are not matched in length. In the overlay plot below, the two lines have similar magnitude responses. However, the difference in delay between the two lines shows up in the phase, impulse, and step response plots.



- Troubleshooting bad VNA measurements using overlay plots

Troubleshooting Bad VNA Measurements Using Overlay Plots

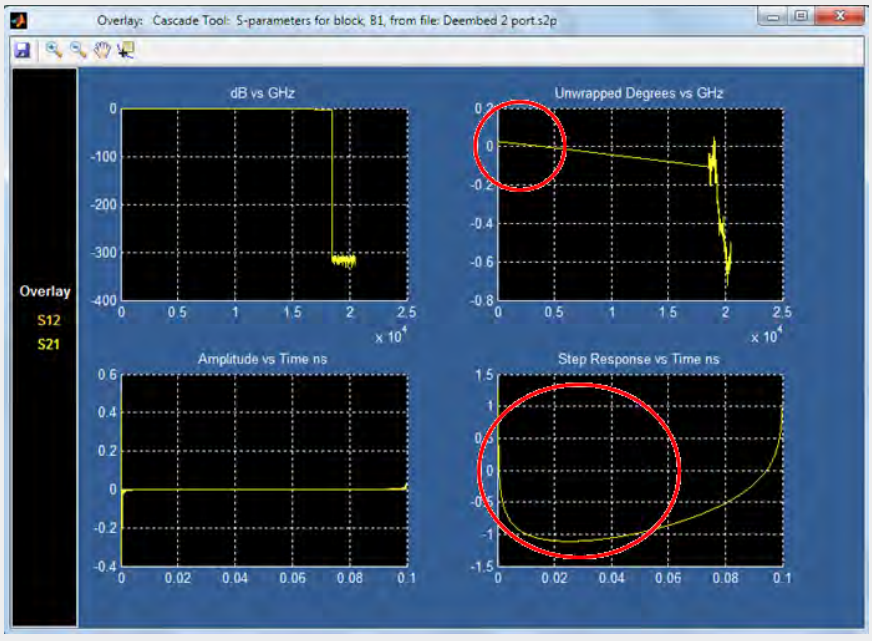
In this example, there is an open connection on one leg of the fixture and cables when measuring the S-parameters on a VNA. (Also note the bad S11 and S22.) The other leg of fixture looks okay. All four plots circled on the image below should be similar-looking for a good fixture.



- Troubleshooting bad phase response

Troubleshooting Bad Phase Response

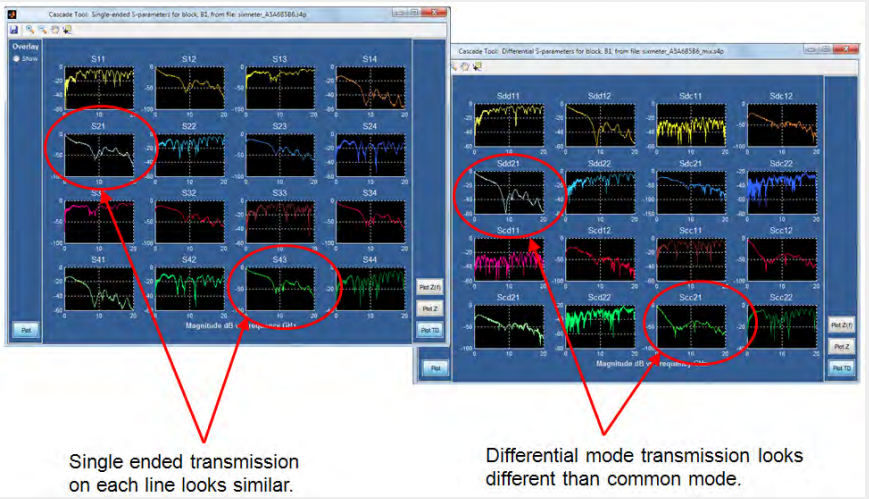
In this example, the wrong calibration kit on VNA was used, which resulted in a bad phase response. The phase did not start at zero degrees at DC. This, in turn, resulted in bad step response.



- Verifying mixed mode vs. single-ended mode

Verifying Mixed Mode vs. Single-ended Mode

You can use these plots to verify the difference between mixed mode and single-ended.

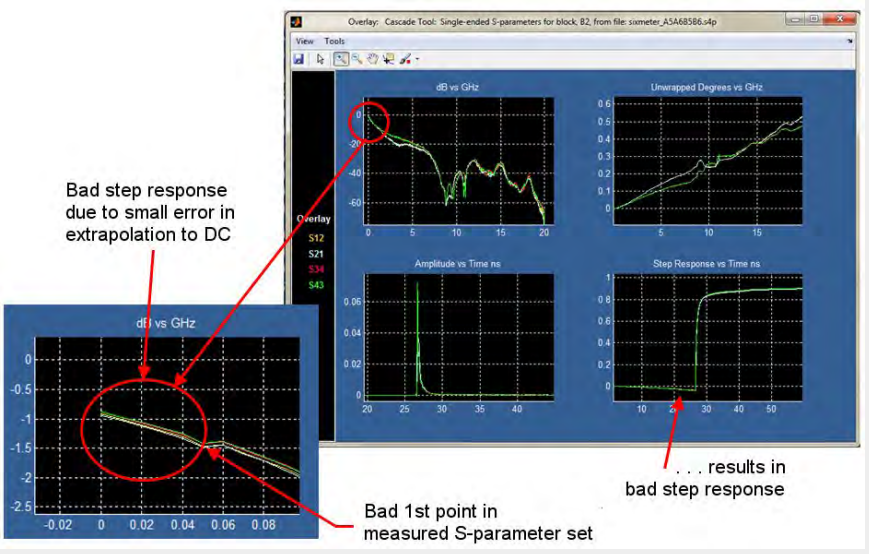


- Troubleshooting bad step response

Troubleshooting Bad Step Response

In this case, the step response has a non-casual dip before the rising edge. The cause of this is revealed by observing the magnitude response zoomed in at DC. The S-parameters commonly do not contain DC, because VNAs cannot measure it. SDLA must then extrapolate the data to DC before it can be transformed to the time domain for processing to make a transfer function filter.

Extrapolation can be problematic, as can be seen below, where the first data sample in the S-parameter set was lower than the previous one due to noise or a bad VNA measurement. This results in the extrapolated portion of the curve being slightly offset by a few tenths of a dB. This is enough to cause the pre-shoot dip in the step response, as shown below.



SEE ALSO:

- *Plots*
- *Examples of Tasks and Troubleshooting*

Tx block (Transmitter modeling block)

Tx block overview

The Transmitter Modeling Block is the only block that contains a double definition: it is defined once for the Measurement Circuit model and again for the Simulation Circuit model.

A simple model assumes a perfect 50 Ohm environment. But what if the transmitter environment is not 50 Ohm? Using the **Tx Block**, you can model different configurations, such as setting a nominal impedance. You can represent the transmitter as one 2 port S-parameter model, or as two 1-port models. You can also use it to configure **Emphasis** options.

The source impedance is specified by the user, while the Thevenin equivalent voltage is computed by the software, based on the input waveforms and system models defined by the user.

Thevenin Equivalent voltage: The Tx Block contains the Thevinin equivalent voltage, which has special importance to the system. It is the point that contains the common waveform voltage that is shared by BOTH the Measurement Circuit (de-embed) path and the Simulation Circuit (embed) path. In other words, this is the point where the acquired waveform is passed into the simulation side of the system. Since a voltage source has zero impedance, this point provides isolation that prevents the Simulation Circuit from loading the Measurement Circuit configuration.

Pressing on the Tx block brings up the *Tx Configuration Menu*. From there, you can select the **Emphasis** radio button and press on the **Emphasis** button that appears on the diagram. This brings up the *Tx Emphasis Menu*.

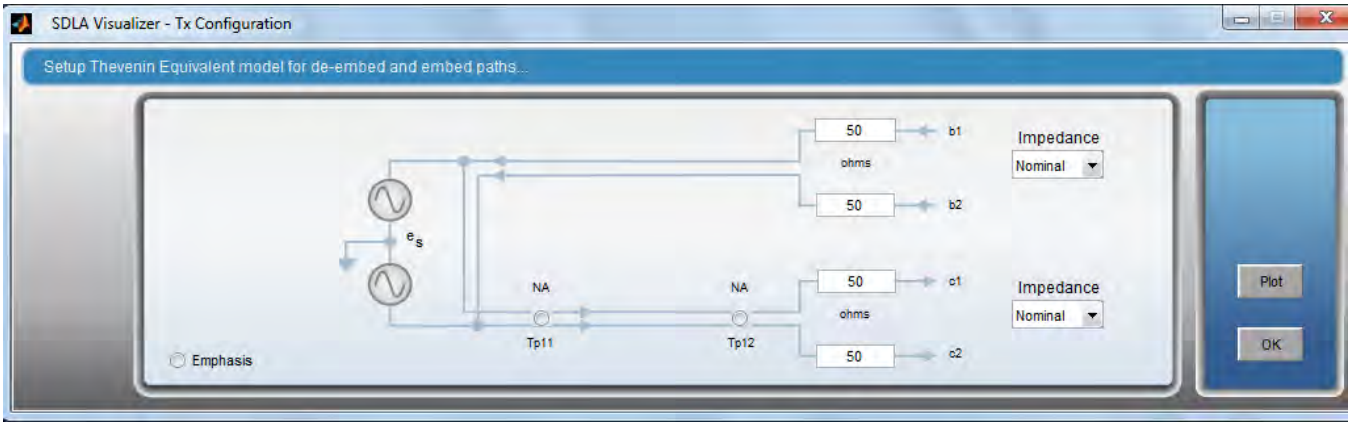
SEE ALSO:

- *Tx Configuration Menu*
- *Tx Emphasis Menu*.

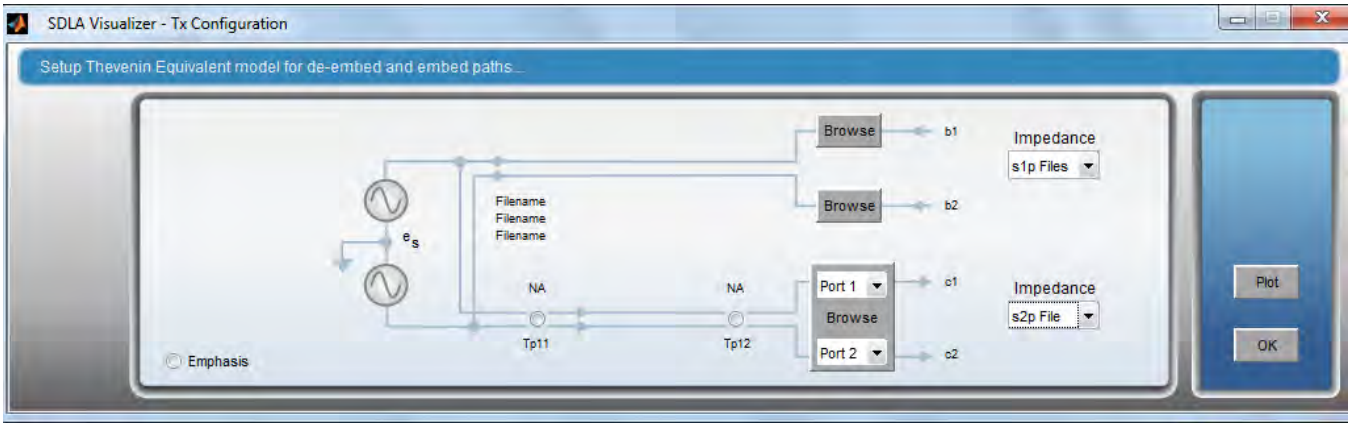
Tx configuration menu

Use this menu to model different transmitter configurations. You can reach it by pressing **Tx** on the Main Menu.

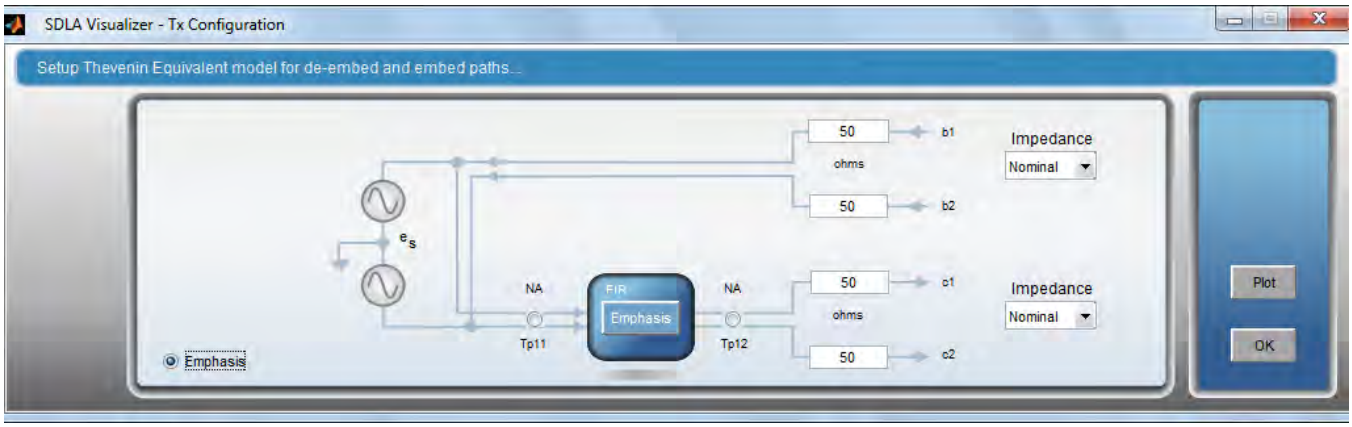
The transmitter representation is split into two Thevenin equivalent circuit models with a common differential voltage source. The top section is the side for the Measurement Circuit (de-embed) path and the bottom is for the Simulation Circuit (embed) path. For example, the graphic below shows a transmitter model using nominal impedance:



The following image represents the transmitter as one 2-port S-parameter model in the lower (embed) part of the systems, and two 1-port S-parameter blocks in the upper (de-embed) part of the system. These are shown differently to illustrate the choices; normal usage is for both the upper and lower sections to be set up as identical to each other.



Select the **Emphasis** radio button. Press the **Emphasis** button that appears in the diagram, which brings up the *Tx Emphasis Menu* :

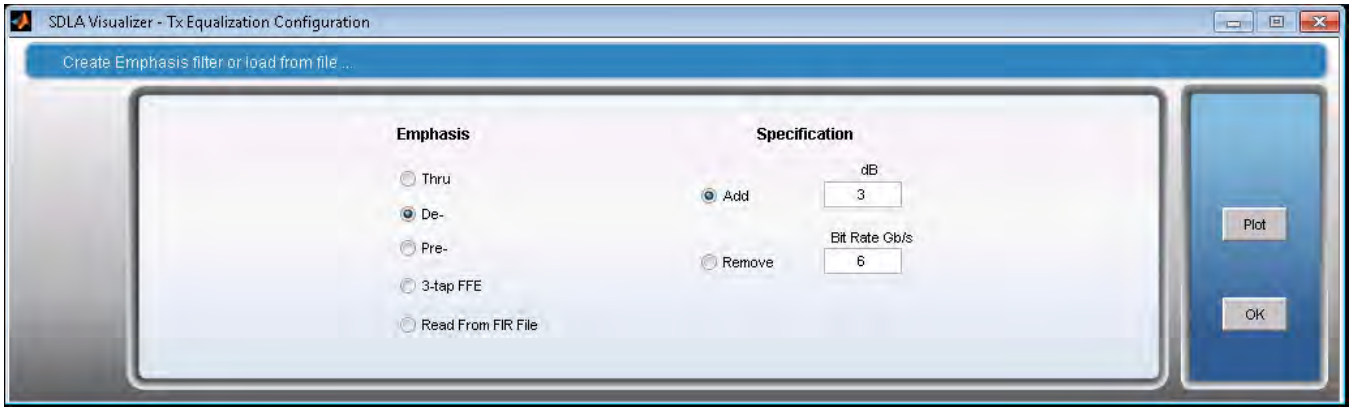


SEE ALSO:

- *Tx Block Overview*
- *Tx Emphasis Menu*.

Tx emphasis menu

The Tx Emphasis Menu lets you specify, remove or add emphasis, de-emphasis or pre-emphasis filters. You may also read data from a FIR filter file. You reach this menu by pressing **Tx** on the Main Menu, selecting the **Emphasis** radio button, and then pressing the **Emphasis** button that appears on the diagram. Note that the Emphasis feature only appears in Simulation Circuit path.



Four types of filter response are available. Each option offers the ability to either remove the effects of a component or to simulate one. The Pre/De-emphasis units are in dB. You can use the typical 3 dB setting or enter a custom dB setting. To see the results of the filter on the source signal, press **Apply** on the Main Menu to recompute the system's test point filters.

- **Thru** removes the effect of de-emphasis added by another circuit block or device.
- **De-** adds de-emphasis: it attenuates the low frequency components to compensate for high-frequency loss through the Channel. Shown in the image above.
- **Pre-** adds pre-emphasis: it amplifies the high frequency components to compensate for high-frequency loss through the Channel.
- **3-tap FFE**: High speed serial data standards require 3-tap FFE at the transmitter to compensate for the channel loss. When 3-tap FFE is selected, SDLA shows three numerical controls for the three taps c-1, c0, and c1. You can enter in values for the three taps in linear scale. When you Apply, SDLA computes the filter for the 3-tap FFE Tx equalizer. Make sure the DC term c0 is bigger than both c-1 and c+1. Otherwise the equalizer will not be stabilizing.

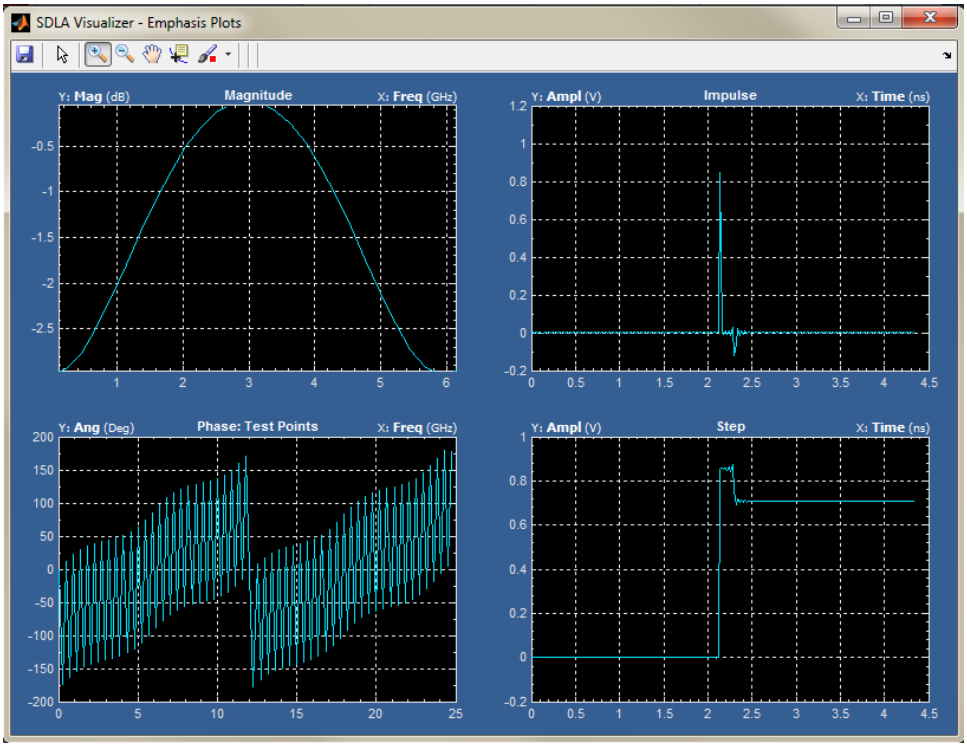
- **Read from FIR File**: The Emphasis block may be set up from a FIR filter file as follows:

  Select the **Read from FIR file** radio button. Browse to the location of your filter file. The Emphasis FIR filter is combined into the test point transfer function using the current sample rate setting of the oscilloscope. The file format contains comment lines starting with #. It then contains at least one line formatted as: <sample rate>; coef1, coef2, ... coefN.

NOTE. *The filter setup need not be an emphasis type. It may be of any type required to better simulate your system.*

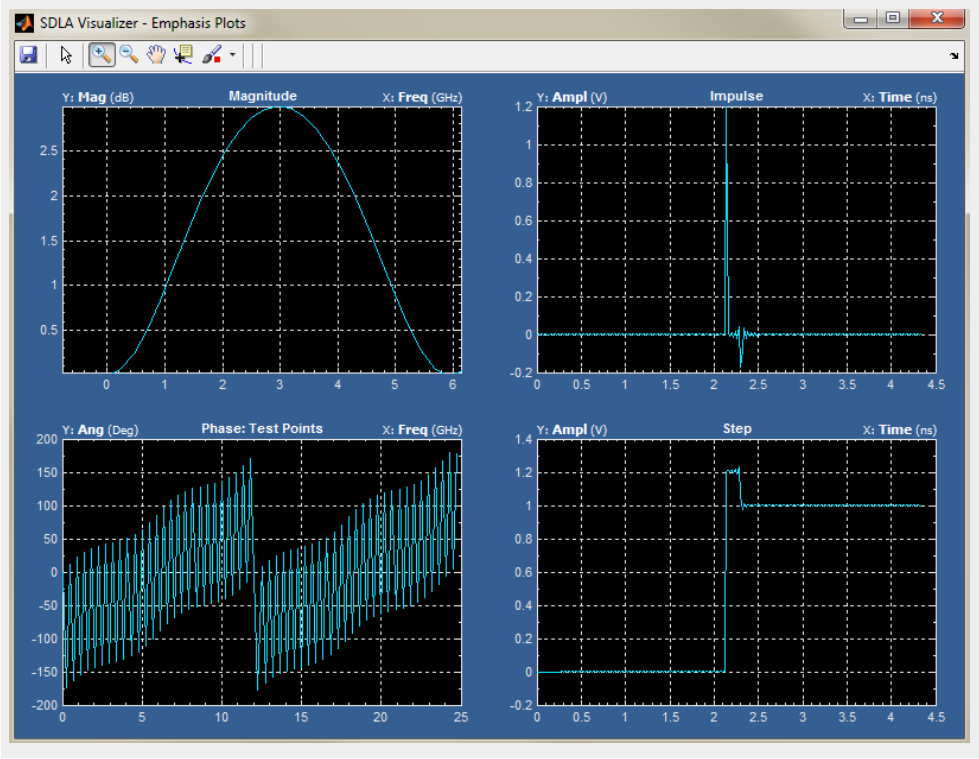
Specification Settings. Use the Specification settings that appear when you select the De- or Pre- radio button to add or remove emphasis values. The bit rate is the bit rate of the source signal. It determines the frequency range increase or decrease in the magnitude response of the emphasis filter. The magnitude frequency response is periodic, with a period determined by the bit rate. The peak value of the filter magnitude response is set by the dB value you chose.

Plot button. Pressing **Plot** opens a window that contains four graphs: Magnitude vs. Frequency, Phase vs. Frequency, Impulse Response vs. Time, and Step Response vs. Time. The image below shows a plot where de-emphasis with a setting of 3 dB was added:

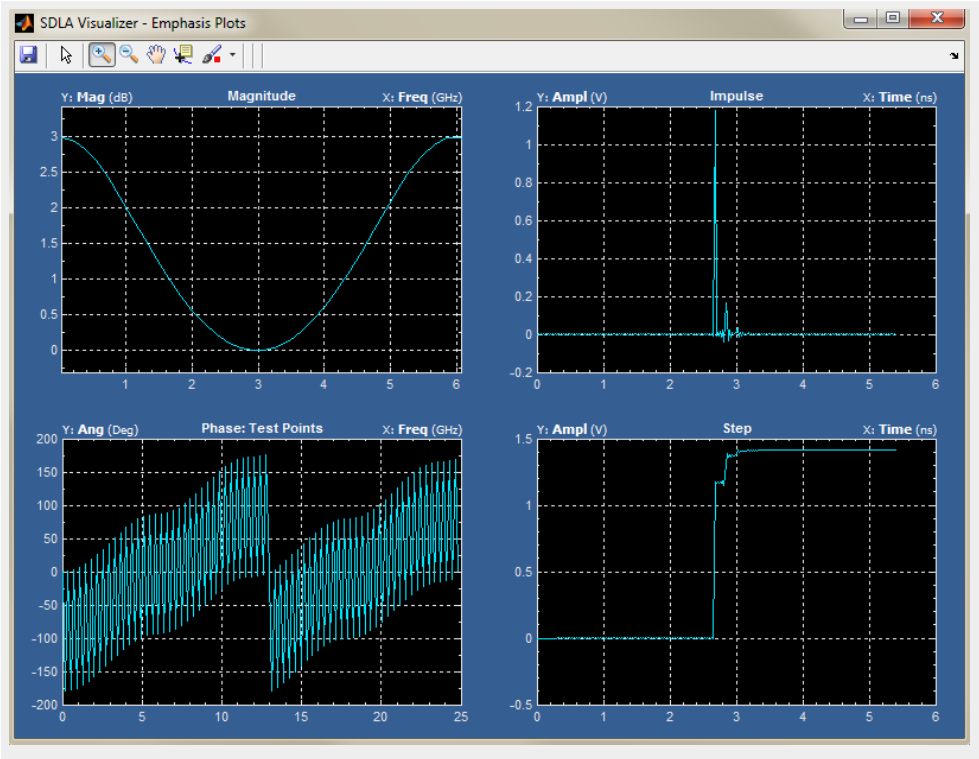


Press below for more examples of plots.

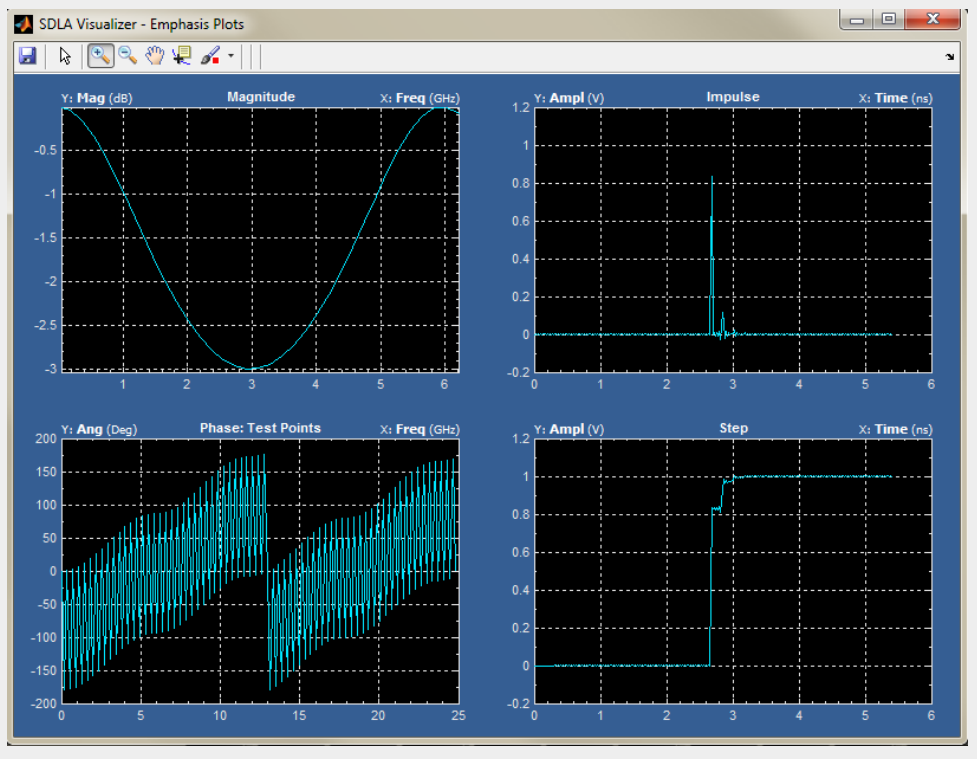
Plot with 3 dB of pre-emphasis added.



Plot with 3 dB of de-emphasis removed.



Plot with 3 dB of pre-emphasis removed.



SEE ALSO:

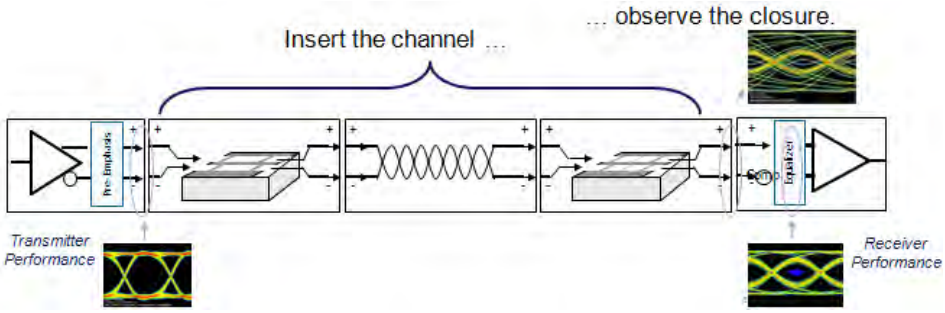
- *Tx Block Overview*
- *Tx Configuration Tool.*

Embed block

Embed block overview

The Embed Block represents a cascade of 4-port S-parameter models for simulating a desired system to be connected to the Tx model. Models can be loaded from S-parameter files as 4-port, 3-port, 2-port, 1-port, or transfer functions. Models can be created from RLC combinations, or a lossless transmission line. Probe load models are also included.

In a typical usage case, the testing of some serial standards requires the embedding of a compliance channel. But probing at the Rx pins is often not possible, requiring simulation of the channel. The Embed Block lets you "insert" a simulated channel so that you can observe the closed eye. Then, you can use the Rx Block to open the eye.

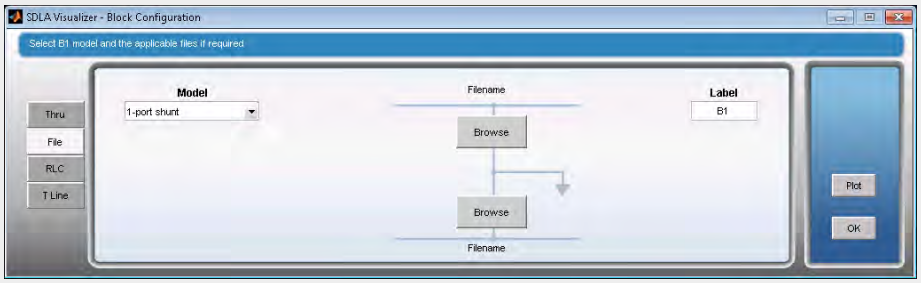


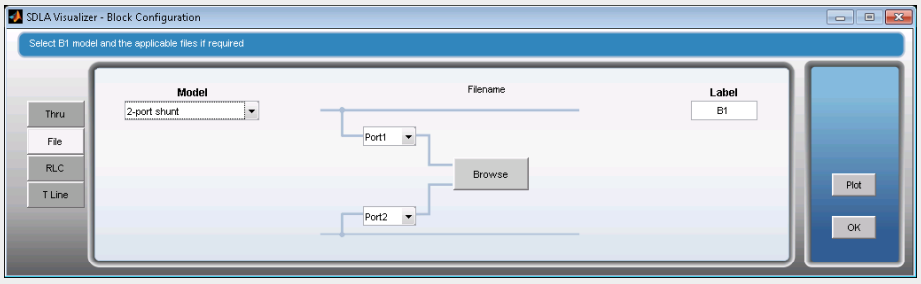
Create a simulated channel to embed by pressing **Embed** on the Main Menu. This brings up the Embed Menu. Using this, you may configure the blocks in many ways. Press here for some possible configurations. For more information, see *De-embed/Embed Menu*.

Embed Block – Some Possible Configurations

- 4-port single-ended S-parameter file
- 4–port differential S-parameter file
- Two 2-port S-parameter files
- FIR filter files (time domain)
- Transfer function files (frequency domain)
- High-Z probe
- TDT Waveform
- 6-port Single-ended
- 8-port Single-ended
- 12-port Single-ended

- 16-port Single-ended





- Various RLC series or parallel configurations
- Lossless Transmission line model
- 3-port probe load model file
- 1-port load S-parameter file
- 2-port load S-parameter file
- Nominal load impedance
- TDT waveform block

SEE ALSO:

- *De-embed/Embed Menu*

Rx block (Receiver modeling block)

Configure the Rx Block by pressing **Rx** on the Main Menu. This brings up the *Rx Configuration Menu*.

The Rx Block represents the model for the serial data link receiver for the Simulation Circuit. It restores the integrity of the data stream and recovers the embedded clock. It can serve as a "reference receiver" in that it performs at the minimal acceptable level, as defined by a standard, for a serial data receiver. (The analog part of a receiver, including the package and termination model, can be modeled using the *Embed Block,* which contains the S-parameter files, transmission line, and RLC circuit models.)

The Rx Block equalizer compensates for the loss, cross-talk, reflection or noise in the link. It attempts to optimize the signal/noise ratio of the eye opening, among other targets, in order to improve the link performance in aspects such as bit error rate. In the oscilloscope measurement context, this equalization allows you to accurately simulate the signal timing and amplitude parameters at the receiver. Sometimes, this measurement point may be referred to as a "virtual Rx", reflecting the simulated nature of the signals.

The receiver has a comparator, or "slicer", that determines whether a bit with value 0 or 1 is received in any unit interval. The exact timing at the slicer is determined by the clock recovery in the receiver. But the virtual Rx is typically not directly accessible by probing or other methods, so the Rx equalization must be simulated in order to get adequate measurements. Often the signal at the input of the equalizer will have a "closed" eye. When correctly designed, the equalization will "open" the eye and increase the eye height, width, or both.

Use the Rx Block AFTER using the Embed Block to create and insert a channel, so you can observe the eye closure at the Rx load. The Rx Block will then show what the signal will look like inside the Rx where the decision 0 or 1 is made by the comparator (aka the "slicer") after the Rx equalization.

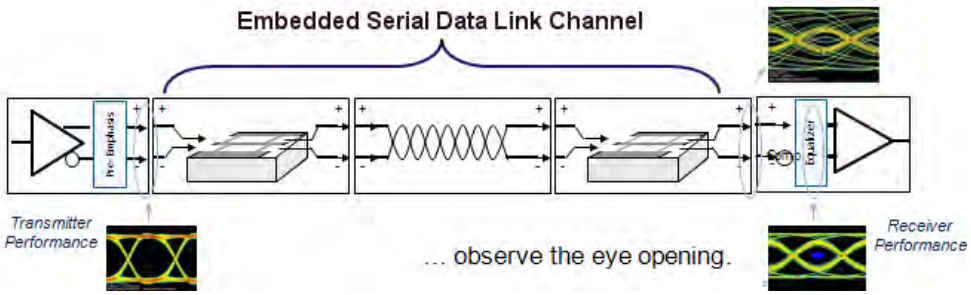
Rx block overview (RT scopes)

The Rx Block contains:

- Mode choice of User, AMI or Thru
- CTLE equalizer (User mode)
- Clock recovery (User mode)
- FFE / DFE equalizer (User mode)
- PAM-4 versus NRZ configuration (User mode)
- Output of CTLE to oscilloscope Math channel (User mode)
- IBIS-AMI model of equalizer (AMI mode)

The Rx Block provides three equalizer modes: User, AMI, and Thru. In User mode, continuous-time linear equalizer (CTLE), feed-forward equalizer (FFE), and decision feedback equalizer (DFE)) models are provided for you to try as serial data receivers typically contain them. Also, user mode supports various equalization adaptation/optimization requirements, such as the LMS-based optimization criterion from SAS 6G, and peak-to-peak based optimization criterion from PCI Express 3.0, as these standards call for "behavioral equalizers" that can be modeled using CTLE and/or DFE. Note that SDLA not only provides implementation of such behavioral equalizers for various standards, but it goes beyond them to simulate much more capable signal conditioning, and allows you to compare them.

AMI Mode is also available; this allows you to emulate IBIS-AMI models, which are descriptions of the equalizers provided by chip designers and manufacturers, as well as EDA tools that provide similar plug-in functionality. This results in more precise simulated Rx waveforms for measurements, comparison and validation.



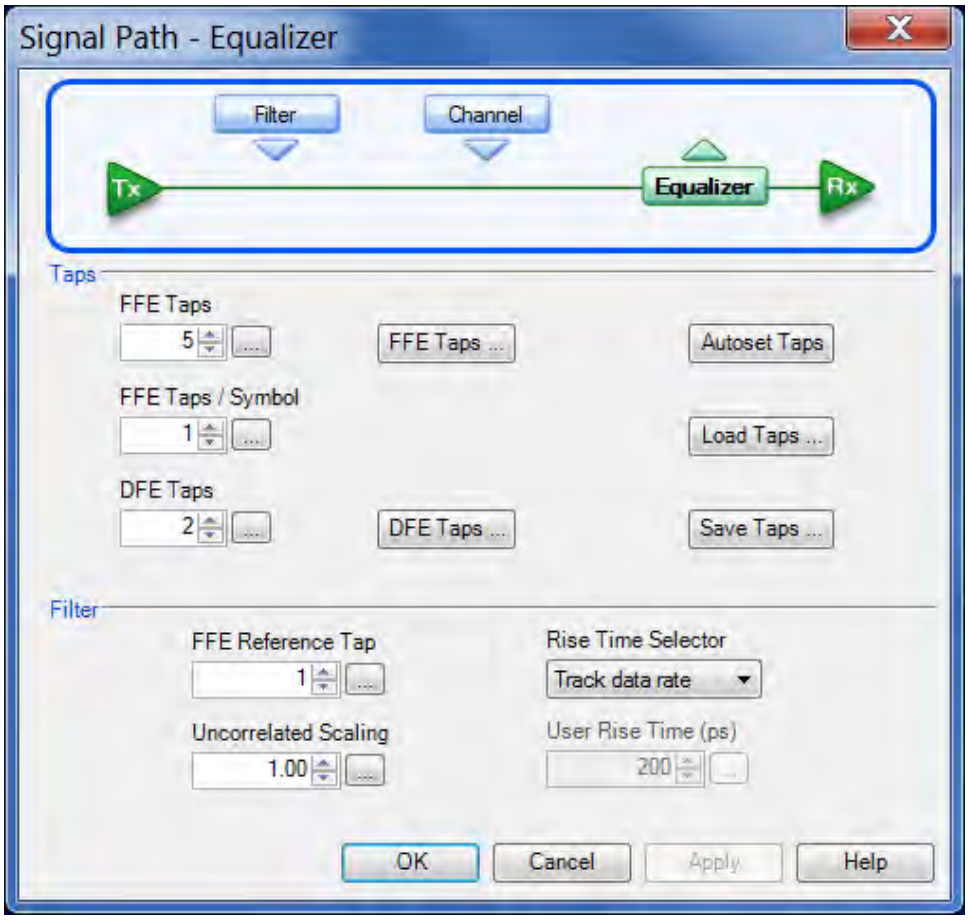
Rx block overview (sampling scopes)

The Rx Block contains:

- Mode choice of User or Thru
- CTLE equalizer (User mode)

The Rx Block provides two equalizer modes: User and Thru. In User mode, continuous-time linear equalizer (CTLE) models are provided for you to try, as serial data receivers typically contain them. Also, user mode supports various equalization adaptation/optimization requirements, such as the LMS-based optimization criterion from SAS 6G, and peak-to-peak based optimization criterion from PCI Express 3.0, as these standards call for "behavioral equalizers" that can be modeled using CTLE. Note that SDLA not only provides implementation of such behavioral equalizers for various standards, but it goes beyond them to simulate much more capable signal conditioning, and allows you to compare them.

Specifying FFE/DFE on a sampling scope is done with JNB. JNB's top level equalization menu looks as follows.



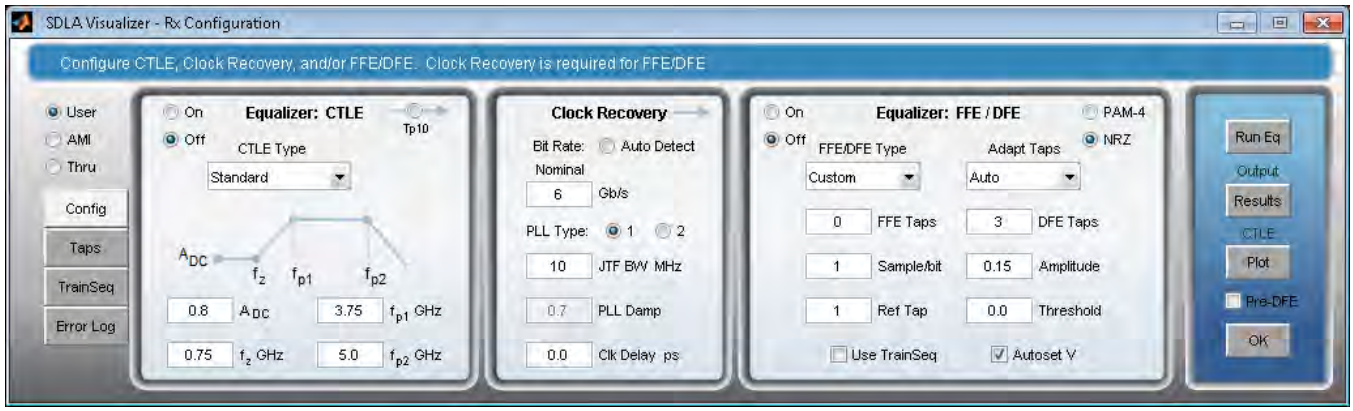
SEE ALSO:

- *Rx Configuration Menu*

Rx configuration menu

Press Rx on the Main Menu to bring up the Rx Configuration Menu. This offers you three modes in the radio buttons on the left: **User**, **AMI**, and **Thru**.

User Mode. User Mode gives you access to equalization tools and options for recovering the data stream and clock by correcting for the effects of insertion loss, cross talk, reflection, and noise. Many **CTLE, clock recovery** and **FFE/DFE** parameters can be specified, plus Taps definition and training sequence detection. This mode also implements the behavioral equalizers of PCI Express, SAS, USB, etc.



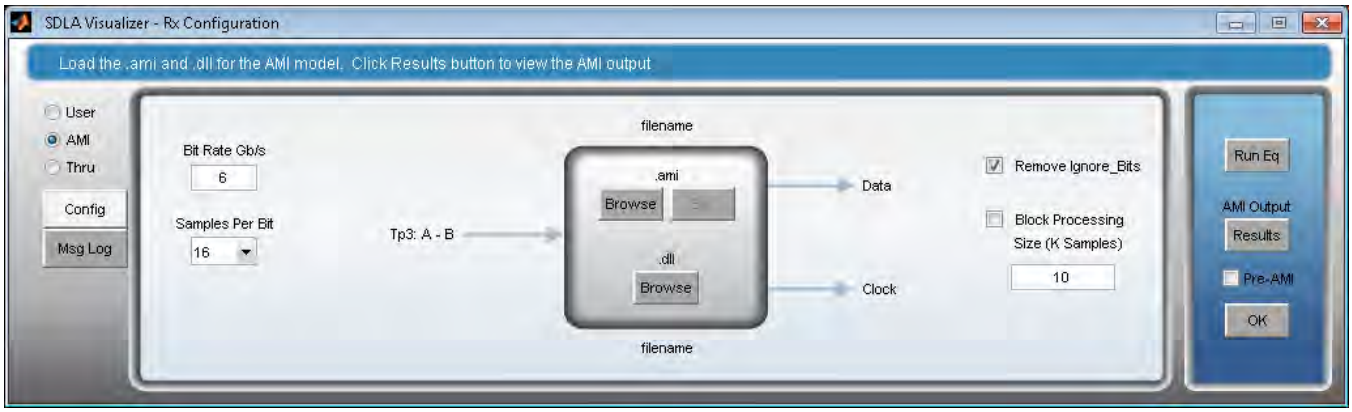
Config Tab. On the Config Tab, the equalization processing runs from left to right. The CTLE and FFE/DFE equalizers may be enabled separately. When both sets of equalizers are enabled, the CTLE equalization occurs first, followed by the FFE/DFE equalization.

The following sections provide usage details:

- *Using CTLE to Improve Signal Recovery*
- *Using PCIE/USB3.1/MIPI/CAUI-4/TBT Option in CTLE*
- *Using Clock Recovery for FFE/DFE Equalization*
- *Using FFE/DFE to Improve Signal Recovery*
- *Using PCIE/USB3.1 GEN2/MIPI/CAUI-4/TBT Option in FFE/DFE*
- *Using the Taps Tab*
- *Manual FFE/DFE configuration for PCIE/USB/MIPI/CAUI-4/TBT options*
- *Equalizing PAM-4 signals*
- *Running the Rx Equalizer in User Mode*

AMI Mode (RT only). AMI Mode allows you to emulate IBIS-AMI models, which are descriptions of the equalizers provided by chip designers and manufacturers, as well as EDA tools that provide similar plug-in functionality. Note that SDLA only emulates the digital part of the IBIS-AMI model in the Rx block. The analog part of the model is neglected in the Rx block, but can be modeled using the **Embed block**, where the S parameter file, T-line model, and RLC circuit models can be used to model the Rx package and terminations.

For more details, see *Rx AMI Mode*



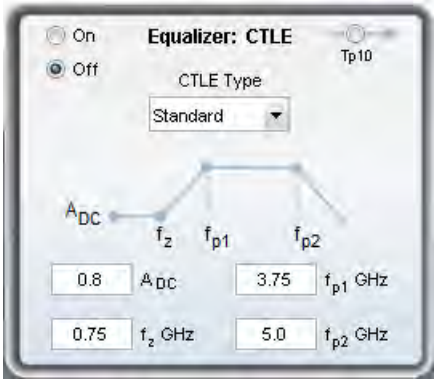
Thru Mode. When using Thru mode, the output of EQ **Tp4**, is the same as the input to EQ **Tp3**. Note that selecting **Thru** on the Rx Configuration Menu does not alter the panels displayed.

SEE ALSO:

- *Rx Block Overview*
- *Rx AMI Mode*

Using CTLE to improve signal recovery

To use the CTLE equalizer, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User**. On the **Config tab**, the **Equalizer: CTLE** panel is on the left.



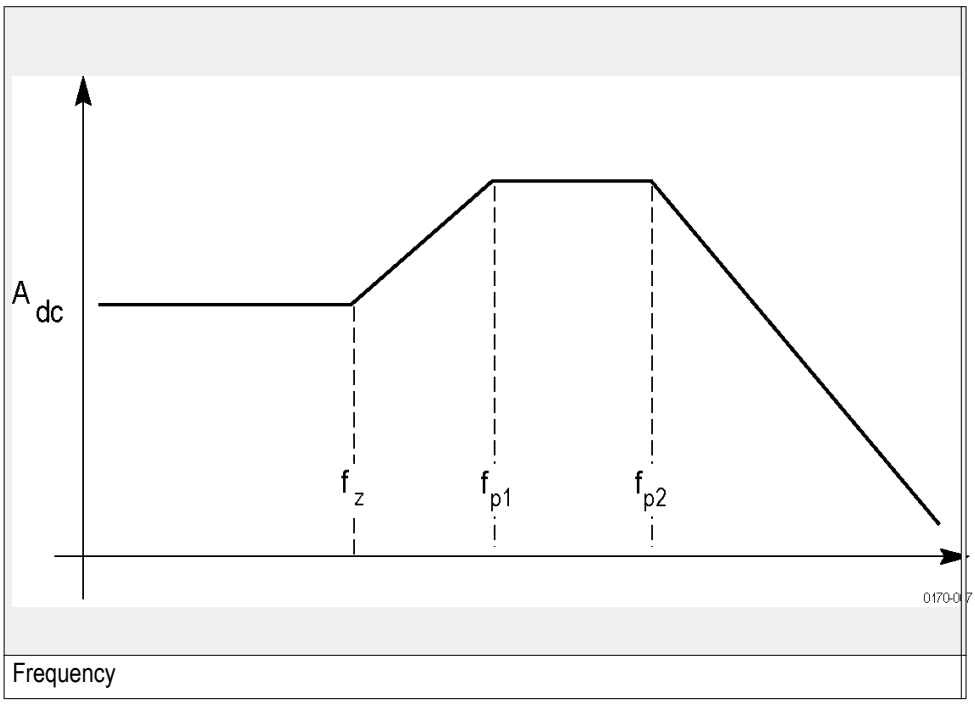
Turn CTLE on or off using the radio buttons on the left. The following CTLE types are available on the drop-down menu:

- Standard
- FIR
- IIR
- PCIe Gen3
- PCIe Gen4
- USB3.1 Gen1 Short
- USB3.1 Gen1 Long
- USB3.1 Gen2
- MIPI
- CAUI-4
- TBT (Thunderbolt) 10.3125 Gb/s
- TBT (Thunderbolt) 20.625 Gb/s

The CTLE output waveform is Tp10. Pressing **Tp10** in the CTLE panel brings up the Test Point and Bandwidth Manager, where Tp10 can be assigned to a Math channel like other test points.

You may need to adjust the CTLE settings in order to recover the data and clock signals. You can plot the CTLE by pressing the **Plot** button on the right. It shows both the frequency domain and time domain responses of CTLE.

Second-order CTLE. Many standards such as PCIE Gen3 and USB 3.0 define a second-order CTLE. The function of most of the key parameters of the second-order CTLE described here are shown in the following illustration. Refer to it as you review the parameter descriptions in the list that follows.



Most of the following parameters are defined in serial data standards.

$$H(s) = \frac{A_{dc}\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})} \qquad \text{(CTLE – 1)}$$

where $\omega_z = 2\pi f_z$, $\omega_{p1} = 2\pi f_{p1}$, $\omega_{p2} = 2\pi f_{p2}$ and

A_{dc}. This is the DC gain of the CTLE transfer function. It is a positive number in linear scale. The default value is 0.8.

F_z. This is the zero frequency of the CTLE transfer function. The value must be within the range of 1 MHz to 20 GHz. The default value is 750 MHz.

F_{p1}. This is the frequency of the first pole of the CTLE transfer function. The value must be within the range of 1 MHz to 20 GHz. The default value is 3.75 GHz.

F_{p2}. This is the frequency of the second pole of the second order CTLE transfer function. The value must be within the range of 1 MHz to 20 GHz. The default value is 5 GHz.

Another convention on the second order CTLE is used in standards such as SuperSpeed Gen 2 reference CTLE uses the following convention:

$$H(s) = A_{ac}\omega_{p2}\frac{s + \frac{A_{dc}}{A_{ac}}\omega_{p1}}{(s+\omega_{p1})(s+\omega_{p2})} \qquad \text{(CTLE – 2)}$$

where A_{ac} is the high frequency peak gain

A_{dc} is the DC gain

$\omega_{p1} = 2\pi f_{p1}$ is the first pole frequency

$\omega_{p2} = 2\pi f_{p2}$ is the second pole frequency

If the ω_z in (CTLE – 1) is set to be

$$\omega_z = \frac{A_{dc}}{A_{ac}}\omega_{p1}$$

then formula (CTLE – 1) and (CTLE -2) are identical with

$$A_{ac} = \frac{A_{dc}\omega_{p1}}{\omega_z}$$

NOTE. *Both formulas (CTLE -1 and CTLE - 2) have four independent variables to configure.*

IIR. This option, found in the **CTLE Type** drop-down menu, loads a custom IIR filter file that sets the CTLE parameters. The IIR filter file is an ASCII text file with file extension .tsf. The file uses a polynomial transfer function to define the IIR filter. There is no limit on the order of polynomials. The file uses **#** to indicate a comment line; **Numerator** as the key word for the numerator polynomial, and **Denominator** as the key word for the denominator polynomial. For example, if an IIR is a first order filter having the pole at 4 GHz, then the denominator should be written as 1, 2*pi*4*1e6.

The following is an example IIR filter file definition:

```
# IIR CTLE Filter
# defined by a polynomial transfer function
#
#       b1s^(n-1)+b2s^(n-2)+...+bn
# H(s) = - - - - - - - - - - - - - - -
#       a1s^(m-1)+a2s^(m-2)+...+am
#
#
# using the following format
#
#[Numerator]
#b1, b2, ..., bn
#[Denominator]
#a1, a2, ..., am
#
# Note that unit is radian/second, not Hz


[Numerator]
5.026548245743669e+010, 3.158273408348595e+020
[Denominator]
1, 6.283185307179587e+010, 6.316546816697189e+020
```

NOTE. *The frequency unit is radians/second, not Hz.*

SDLA generates FIR filters (based on the IIR filter definition and complete signal path) on pressing the **Apply** button in the Main Menu or the **Run Eq** button in the Rx Configuration menu. If CTLE output Tp10 is assigned to a Math waveform and turned on, then SDLA writes the **Tp10** FIR filter file (sdlatp10.flt) to C:\TekApplications\SDLA\output filters and configures the Math setup to utilize that filter.

FIR. This button opens a file browser to load a custom FIR filter to set the CTLE parameters.

PCIe Gen3/Gen4. When PCIE Gen3 option is selected (using the **CTLE Type** drop-down menu), SDLA Visualizer runs an optimization process to find the best CTLE setting to maximize the eye area, as per the PCIE Gen3 specification. For details, see *Using the PCIE Option in CTLE*.

USB3.1 Gen2. When it is selected, SDLA visualizer runs an optimization process to find the best CTLE setting to maximize the eye area.

MIPI. When it is selected, SDLA visualizer runs an optimization process to find the best CTLE setting to maximize the eye area.

CAUI-4. When it is selected, SDLA visualizer runs an optimization process to find the best CTLE setting to maximize the eye area.

TBT 10.3125/20.625 Gb/s. When it is selected, SDLA visualizer runs an optimization process to find the best CTLE setting to maximize the eye height.

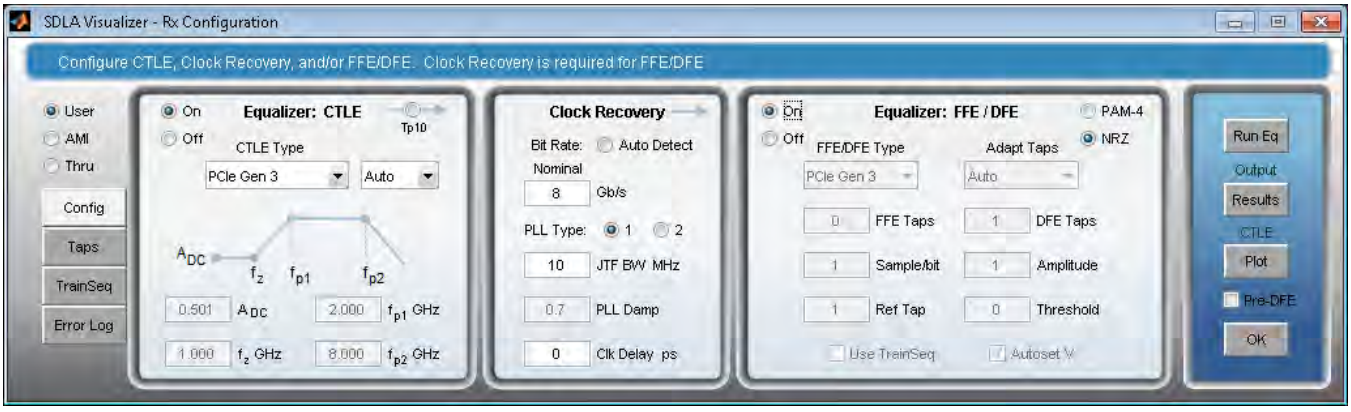
SEE ALSO:

- *Using Clock Recovery for FFE/DFE Equalization*
- *Using FFE/DFE to Improve Signal Recovery*
- *Rx Block Overview*

Using the PCIE option in CTLE

To use the PCIE option with CTLE, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User**. On the Config tab, in the Equalizer: CTLE panel, choose **PCIe Gen3** or **PCIe Gen4** from the **CTLE Type** drop-down menu.

When this option is selected, SDLA runs an optimization process to find the best CTLE setting to maximize the eye area as per the PCIe Gen3/Gen4 (whichever is applicable) specification. The PCIE specification defines 7 CTLE presets. The DC gains are -6, -7, -8, -9, -10, -11, and -12 in dB. When **PCIe Gen3** or **PCIe Gen4** is checked, the UI changes as shown in the following image.

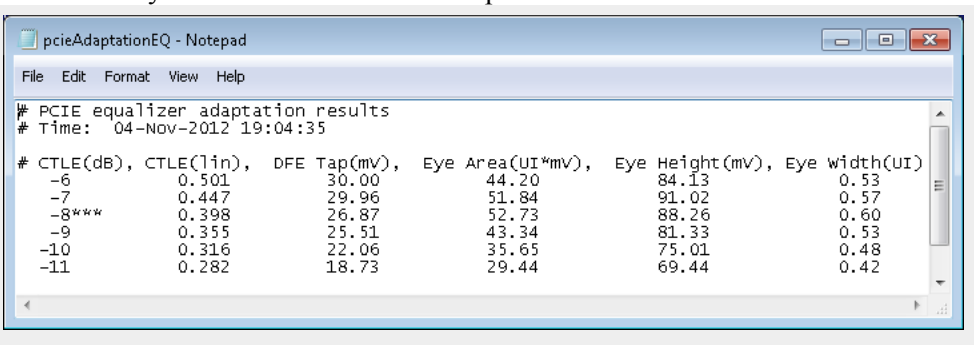


- PCIe Gen3 or PCIe Gen4 is selected in the CTLE panel **CTLE Type** drop-down menu.
- Note that Adc, fz (GHz), fp1 (GHz), fp2 (GHz) are grayed out, as they are set by the SDLA optimization routine.
- fp1 = 2 (Gen3) or 4 (Gen4) GHz, fp2 = 8 (Gen3) or 16 (Gen4) GHz, and fz = fp1*Adc. The value of Adc and fz are updated after running the CTLE optimization.
- Clock Recovery sets the **Nominal** bit rate to 8 (Gen3) or 16 (Gen4) Gb/s, PLL Type to 1, PLL BW MHz to 10.
- PCIe Gen3 or PCIe Gen4 is selected in the FFE/DFE Panel **FFE/DFE Type** drop-down menu. FFE/DFE can be turned **On** or **Off**. When FFE/DFE is turned off, it means that only CTLE is active. When FFE/DFE is turned on, it means the Rx Equalizer has CTLE plus one-tap DFE selected. (See *PCIE Option: DFE*.)
- **Auto** is selected on the **Adapt Taps** drop-down menu.

Sequence of operations when CTLE Type is set to PCIE. When PCIe Gen3 or PCIe Gen4 is selected in the **CTLE Type** drop-down menu, use this sequence of operations.

1. SDLA generates an optimal setting after the **Apply** button is pressed in the Main Menu or the **Run Eq** button is pressed in the Rx Configuration menu.
2. SDLA updates the settings of Adc, fz (GHz), fp1 (GHz), fp2 (GHz).
3. SDLA creates the file pcieAdaptationEQ.txt at C:\TekApplications\SDLA \taps.
4. When DFE is off, the DFE Tap value should be 0. When DFE is on, the DFE Tap value should be between -30 mV and 30 mV.

PCIE Output Results. Press **Results** in the far right panel to view the contents of the optimization results file pcieAdaptationEQ.txt. All 7 pre-settings are listed. The best CTLE setting is labeled with ***, where the best setting has the maximum Eye Area value. See file example.



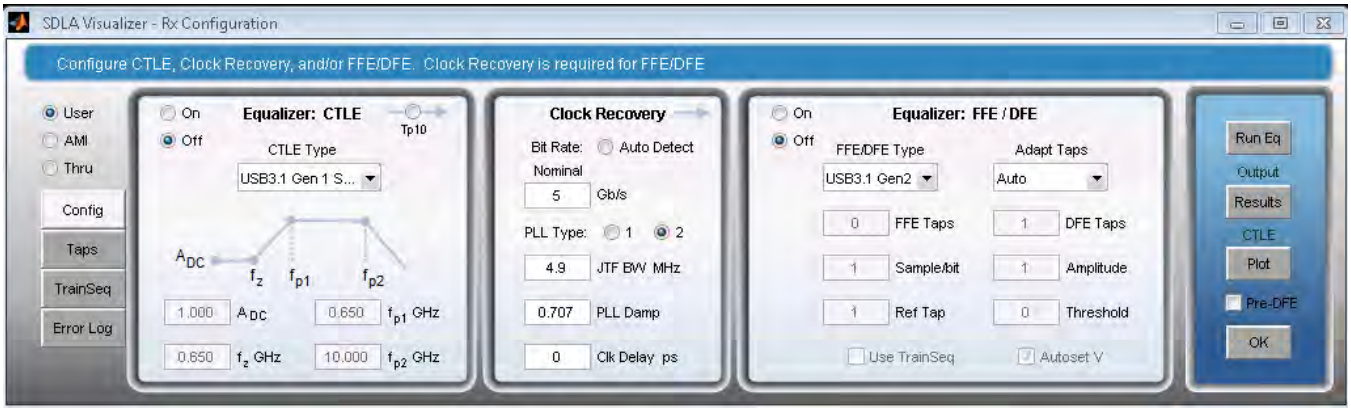
SEE ALSO:

- *Using CTLE to Improve Signal Recovery*
- *Using FFE/DFE to Improve Signal Recovery*
- *Rx Configuration Menu*
- *Rx Block Overview*

Using the USB3.1 option in CTLE

There are three USB3.1 options: USB3.1 Gen1 Short, USB3.1 Gen1 Long and USB3.1 Gen2.

When USB3.1 Gen1 Short is selected in the CTLE Type drop down menu, the menu is as follows.



CTLE settings are:

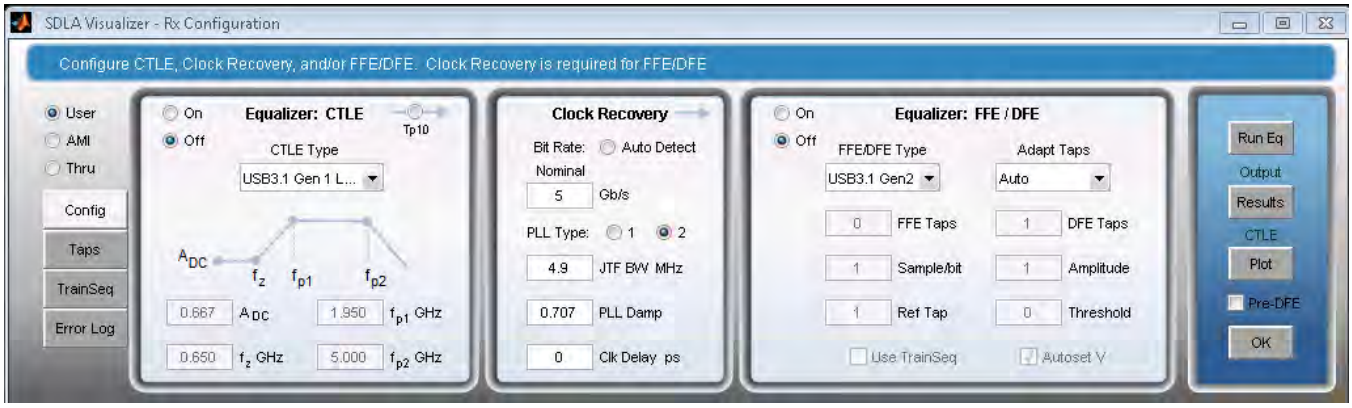
- Adc = 1.0
- fp1 = 0.65GHz

- fp2 = 10GHz
- fz = 0.65GHz

The clock recovery settings are:

- Bit Rate = 5Gb/s
- PLL type = 2
- PLL BW = 1.9MHz
- PLL Damp = 0.707
- Clock Delay = 0

When USB3.1 Gen1 Long is selected in the CTLE Type drop down menu, the menu is as follows:



CTLE settings are:

- Adc = 0.667
- fp1 = 1.95GHz
- fp2 = 5GHz
- fz = 0.65GHz

The clock recovery settings are:

- Bit Rate = 5Gb/s
- PLL type = 2
- PLL BW = 1.9MHz
- PLL Damp = 0.707
- Clock Delay = 0

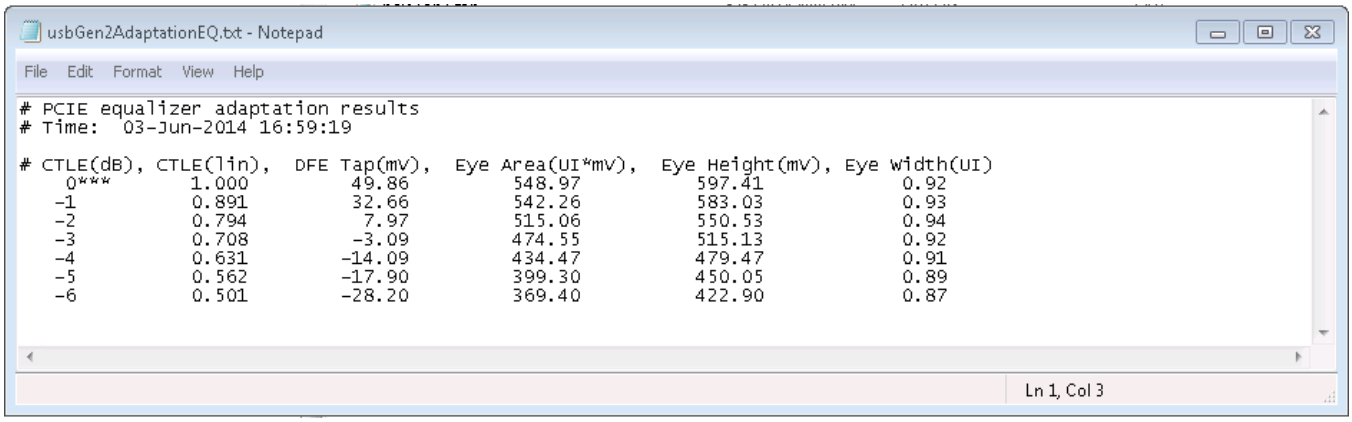
When the USB3.1 Gen2 option is selected, SDLA runs an optimization process to find the best CTLE setting to maximize the eye area as per the USB3.1 Gen2 specifications. The USB3.1 Gen2 specification defines 7 CTLE presets. The DC gains are 0, -1, -2, -3, -4, -5, and -6 in dB. When **USB3.1 Gen2** is checked, the UI changes as shown in the following image.

- USB3.1 Gen2 is selected in the CTLE panel **CTLE Type** drop-down menu.
- Note that Adc, fz (GHz), fp1 (GHz), fp2 (GHz) are grayed out, as they are set by the SDLA optimization routine.
- fp1 = 1.5 GHz, fp2 = 5 GHz, and fz = fp1*Adc. The value of Adc and fz are updated after running the CTLE optimization.
- Clock Recovery sets the **Nominal** bit rate to 10 Gb/s, PLL Type to 2, PLL BW MHz to 7.5 MHz.
- USB3.1 Gen2 is selected in the FFE/DFE Panel **FFE/DFE Type** drop-down menu. FFE/DFE can be turned **On** or **Off**. When FFE/DFE is turned off, only CTLE is active. When FFE/DFE is turned on, the Rx Equalizer has CTLE plus one-tap DFE selected. (See *USB3.1 Gen2 Option: DFE*.)
- **Auto** is selected on the **Adapt Taps** drop-down menu.

Sequence of operations when CTLE Type is set to USB3.1 Gen2. When USB3.1 Gen2 is selected in the **CTLE Type** drop-down menu, use this sequence of operations.

1. SDLA generates an optimal setting after the **Apply** button is pressed in the Main Menu or the **Run Eq** button is pressed in the Rx Configuration menu.
2. SDLA updates the settings of Adc, fz (GHz), fp1 (GHz), fp2 (GHz).
3. SDLA creates the file usbGen2AdaptationEQ.txt at C:\TekApplications \SDLA\taps.
4. When DFE is off, the DFE Tap value should be 0. When DFE is on, the DFE Tap value should be between -50 mV and 50 mV.

Click the Results button in the far right panel to view the contents of the optimization results file usbGen2AdaptationEQ.txt. All 7 pre-settings are listed. The best CTLE setting is labeled with ***, where the best setting has the maximum Eye Area value. See file example.



Using the MIPI option in CTLE

To use the MIPI option with CTLE, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User**. On the Config tab, in the Equalizer: CTLE panel, choose MIPI from the **CTLE Type** drop-down menu.

When this option is selected, SDLA runs an optimization process to find the best CTLE setting to maximize the eye area as per the MIPI specification. The MIPI specification defines 11 CTLE presets:

Adc	fz	fp1	fp2
2	0.4e9	0.401e9	10e9
1.33	0.4e9	0.6e9	10e9
1.33	0.8e9	1.2e9	10e9
1.33	1.2e9	1.75e9	10e9
1.0	0.4e9	0.8e9	10e9
1.0	0.8e9	1.6e9	10e9

Adc	fz	fp1	fp2
1.0	1.2e9	2.3e9	10e9
0.8	0.4e9	1.0e9	10e9
0.8	1.05e9	2.6e9	10e9
0.66	0.4e9	1.2e9	10e9
0.66	0.7e9	2.1e9	10e9

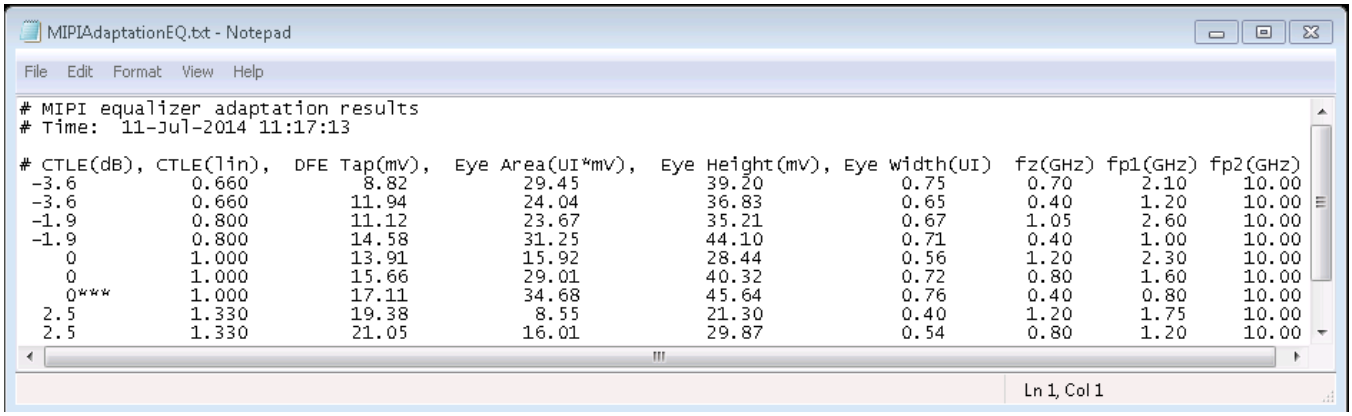
When MIPI is checked, the UI changes as shown in the following image.

- MIPI is selected in the CTLE panel **CTLE Type** drop-down menu.
- Note that Adc, fz (GHz), fp1 (GHz), fp2 (GHz) are grayed out, as they are set by the SDLA optimization routine.
- Adc = 2, fp1 = 0.4GHz, fp2 = 10 GHz and fz = 0.4 GHz to start with. The values are updated after running the CTLE optimization.
- Clock Recovery sets the **Nominal** bit rate to 10 Gb/s, PLL Type to 2, PLL BW MHz to 8 MHz, PLL damp factor is 0.707 and clock delay is 0.
- MIPI is selected in the FFE/DFE Panel **FFE/DFE Type** drop-down menu. FFE/DFE can be turned **On** or **Off**. When FFE/DFE is turned off, only CTLE is active. When FFE/DFE is turned on, the Rx Equalizer has CTLE plus one-tap DFE selected. (See *Using the MIPI option in FFE-DFE* on page 127.)
- **Auto** is selected on the **Adapt Taps** drop-down menu.

Sequence of operations when CTLE Type is set to MIPI. When MIPI is selected in the **CTLE Type** drop-down menu, use this sequence of operations.

1. SDLA generates an optimal setting after the **Apply** button is pressed in the Main Menu or the **Run Eq** button is pressed in the Rx Configuration menu.
2. SDLA updates the settings of Adc, fz (GHz), fp1 (GHz), fp2 (GHz).
3. SDLA creates the file mipiAdaptationEQ.txt at C:\TekApplications\SDLA \taps.
4. When DFE is off, the DFE Tap value should be 0. When DFE is on, the DFE Tap value should be between -30 mV and 30 mV.

Click the Results button in the right panel to view the contents of the optimization results file mipiAdaptationEQ.txt. All 11 pre-settings are listed. The best CTLE setting is labeled with ***, where the best setting has the maximum Eye Area value. See file example.



Using the CAUI-4 option in CTLE

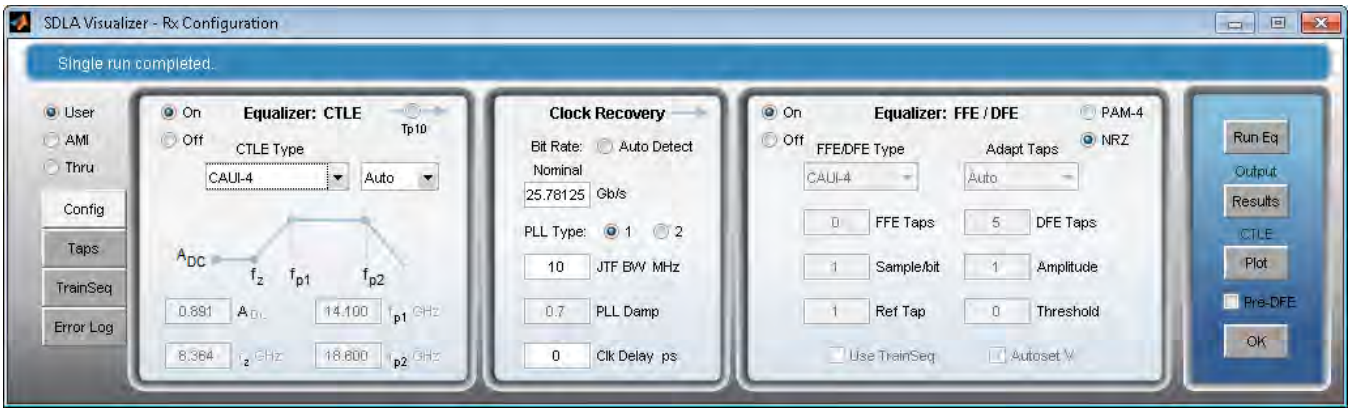
To use the CAUI-4 option with CTLE, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User**. On the Config tab, in the **Equalizer: CTLE** panel, choose **CAUI-4** from the **CTLE Type** drop-down menu.

When this option is selected, SDLA runs an optimization process to find the best CTLE setting to maximize the eye area as per the CAUI-4 specification. The CAUI-4 specification defines 9 CTLE presets:

Adc	fz	fp1	fp2
0.89125	$8.364e^9$	$14.1e^9$	$18.6e^9$
0.79433	$7.099e^9$	$14.1e^9$	$18.6e^9$
0.70795	$5.676e^9$	$14.1e^9$	$15.6e^9$
0.63096	$4.9601e^9$	$14.1e^9$	$15.6e^9$
0.56234	$4.358e^9$	$14.1e^9$	$15.6e^9$
0.50119	$3.844e^9$	$14.1e^9$	$15.6e^9$
0.44668	$3.399e^9$	$14.1e^9$	$15.6e^9$

Adc	fz	fp1	fp2
0.39811	$3.012e^9$	$14.1e^9$	$15.6e^9$
0.35481	$2.672e^9$	$14.1e^9$	$15.6e^9$

When CAUI-4 is checked, the UI changes as shown in the following image.

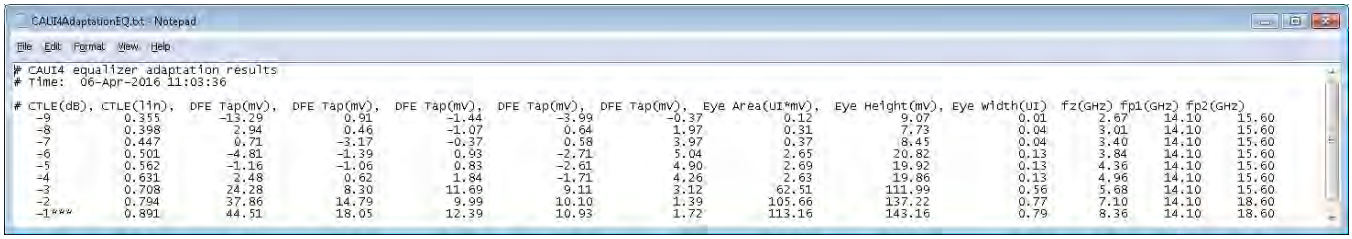


- **CAUI-4** is selected in the CTLE panel **CTLE Type** drop-down menu.
- Note that Adc, fz (GHz), fp1 (GHz), fp2 (GHz) are grayed out, as they are set by the SDLA optimization routine.
- Adc = 0.89125, fp1 = 14.1 GHz, fp2 = 18.6 GHz and fz = 8.364 GHz to start with. The values are updated after running the CTLE optimization.
- Clock Recovery sets the Nominal bit rate to 25.78125 Gb/s, PLL Type to 1, PLL BW MHz to 10 MHz, PLL damp factor is 0.7 and clock delay is 0.
- **CAUI-4** is selected in the FFE/DFE Panel **FFE/DFE Type** drop-down menu. FFE/DFE can be turned On or Off. When FFE/DFE is turned off, only CTLE is active. When FFE/DFE is turned on, the Rx Equalizer has CTLE plus five-tap DFE selected. (See *Using the CAUI-4 option in FFE-DFE* on page 128.
- **Auto** is selected on the **Adapt Taps** drop-down menu.

Sequence of operations when CTLE Type is set to CAUI-4. When **CAUI-4** is selected in the **CTLE Type** drop-down menu, use this sequence of operations.

1. SDLA generates an optimal setting after the Apply button is pressed in the Main Menu or the Run Eq button is pressed in the Rx Configuration menu.
2. SDLA updates the settings of Adc, fz (GHz), fp1 (GHz), fp2 (GHz).
3. SDLA creates the file CAUI4AdaptationEQ.txt at C:\TekApplications\SDLA \taps.
4. When DFE is off, the DFE Tap value should be 0. When DFE is on, the DFE Tap value should be between -30 mV and 30 mV.

CAUI-4 Output Results. Press **Results** button in the right panel to view the contents of the optimization results file CAUI4AdaptationEQ.txt. All 9 pre-settings are listed. The best CTLE setting is labeled with ***, where the best setting has the maximum Eye Area value. See file example.


CAUI4AdaptationEQ.txt - Notepad

File Edit Format View Help

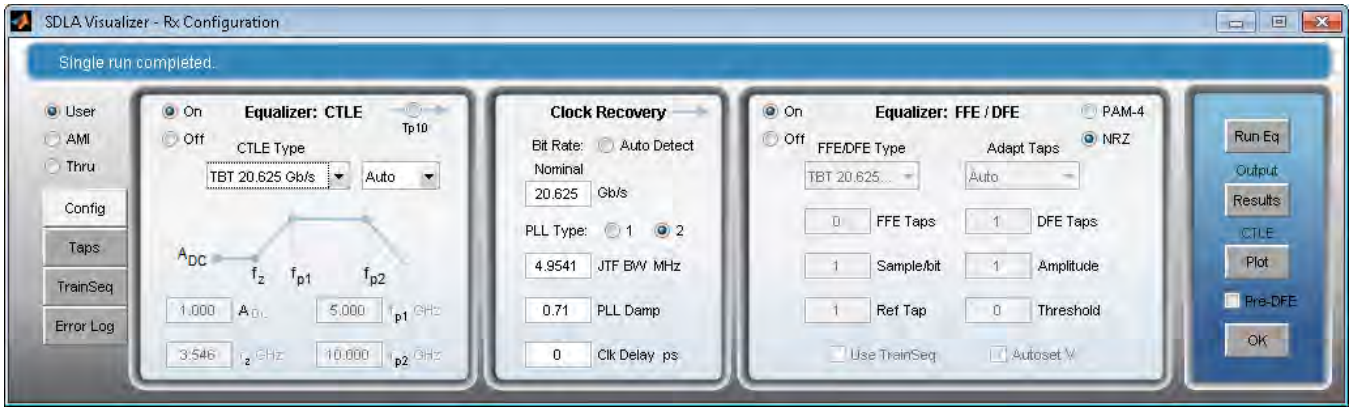
```
# CAUI4 equalizer adaptation results
# Time:  06-Apr-2016 11:03:36

# CTLE(dB), CTLE(lin),  DFE Tap(mV),  DFE Tap(mV),  DFE Tap(mV),  DFE Tap(mV),  DFE Tap(mV),  Eye Area(UI*mV),  Eye Height(mV), Eye Width(UI)  fz(GHz) fp1(GHz) fp2(GHz)
   -9        0.355       -13.29          0.91          -1.44          -3.99          -0.37          0.12           9.07          0.01          2.67    14.10    15.60
   -8        0.398         2.94          0.46          -1.07           0.64           1.97          0.31           7.73          0.04          3.01    14.10    15.60
   -7        0.447         0.71         -3.17          -0.37           0.58           3.97          0.37           8.45          0.04          3.40    14.10    15.60
   -6        0.501        -4.81         -1.39           0.93          -2.71           5.04          2.65          20.82          0.13          3.84    14.10    15.60
   -5        0.562        -1.16         -1.06           0.83          -2.61           4.90          2.69          19.92          0.13          4.36    14.10    15.60
   -4        0.631         2.48          0.62           1.84          -1.71           4.26          2.63          19.86          0.13          4.96    14.10    15.60
   -3        0.708        24.28          8.30          11.69           9.11           3.12         62.51         111.99          0.56          5.68    14.10    15.60
   -2        0.794        37.86         14.79           9.99          10.10           1.39        105.66         137.22          0.77          7.10    14.10    18.60
 -1***       0.891        44.51         18.05          12.39          10.93           1.72        113.16         143.16          0.79          8.36    14.10    18.60
```

Using the TBT (Thunderbolt) option in CTLE

To use the TBT 10.3125/20.625 Gb/s option with CTLE, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User** . On the Config tab, in the Equalizer: CTLE panel, choose **TBT 10.3125 Gb/s** or **TBT 20.625 Gb/s** from the **CTLE Type** drop-down menu.

When this option is selected, SDLA runs an optimization process to find the best CTLE setting to maximize the eye height as per the TBT specification. The TBT specification defines 10 CTLE presets. The DC gains are 0, -1, -2,-3, -4, -5, -6, -7, -8 and -9 in dB. When **TBT 10.3125 Gb/s** or **TBT 20.625 Gb/s** is checked, the UI changes as shown in the following image. Press here to see settings for the following image.



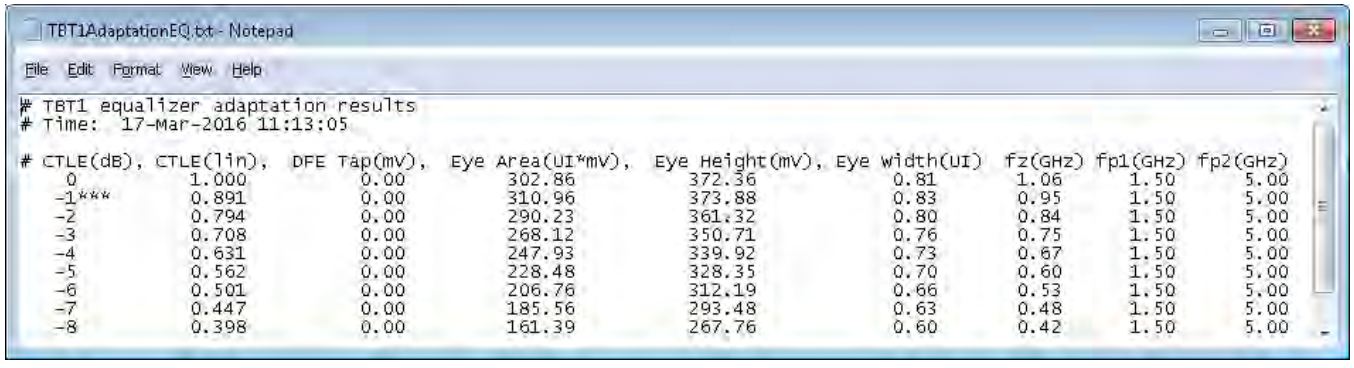
- **TBT 10.3125 Gb/s** or **TBT 20.625 Gb/s** is selected in the CTLE panel **CTLE Type** drop-down menu.
- Note that Adc, fz (GHz), fp1 (GHz), fp2 (GHz) are grayed out, as they are set by the SDLA optimization routine.

- fp1 = 1.5 (TBT 10.3125 Gb/s) or 5 (TBT 20.625 Gb/s) GHz, fp2 = 5 (TBT 10.3125 Gb/s) or 10 (TBT 20.625 Gb/s) GHz, and fz = fp1*Adc/1.41. The value of Adc and fz are updated after running the CTLE optimization.
- Clock Recovery sets the **Nominal** bit rate to 10.3125 (TBT 10.3125 Gb/s) or 20.625 (TBT 20.625 Gb/s) Gb/s, PLL Type to 2, PLL BW to 4.9858 (TBT 10.3125 Gb/s) or 4.9541 (TBT 20.625 Gb/s) MHz. PLL Damp to 0.94 (TBT 10.3125 Gb/s) or 0.71 (TBT 20.625 Gb/s).
- **TBT 10.3125 Gb/s** or **TBT 20.625 Gb/s** is selected in the FFE/DFE Panel **FFE/DFE Type** drop-down menu. FFE/DFE can be turned **On** or **Off** . When FFE/DFE is turned off, it means that only CTLE is active. When FFE/DFE is turned on, it means the Rx Equalizer has CTLE plus one-tap DFE selected. (See *Using the TBT (Thunderbolt) option in FFE-DFE* on page 129.
- **Auto** is selected on the **Adapt Taps** drop-down menu.

Sequence of operations when CTLE Type is set to TBT. When **TBT 10.3125 Gb/s** or **TBT 20.625 Gb/s** is selected in the **CTLE Type** drop-down menu, use this sequence of operations.

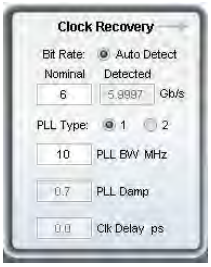
1. SDLA generates an optimal setting after the **Apply** button is pressed in the Main Menu or the **Run Eq** button is pressed in the Rx Configuration menu.
2. SDLA updates the settings of Adc, fz (GHz), fp1 (GHz), fp2 (GHz).
3. SDLA creates the file TBT1AdaptationEQ.txt or TBT2AdaptationEQ.txt at C:\TekApplications\SDLA\taps.
4. When DFE is off, the DFE Tap value should be 0. When DFE is on, the DFE Tap value should be between -50 mV and 50 mV.

TBT Output Results. Press **Results** in the far right panel to view the contents of the optimization results file TBT1AdaptationEQ.txt or TBT2AdaptationEQ.txt. All 10 pre-settings are listed. The best CTLE setting is labeled with ***, where the best setting has the maximum Eye Height value. See file example.



Using clock recovery for FFE-DFE equalization

To use the clock recovery function, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User**. On the **Config** tab, the Clock Recovery panel is in the middle.



Clock recovery is used for FFE/DFE equalization in the Rx Block. The software performs clock recovery by emulating a phase locked loop (PLL) circuit. Use the data rate defined for the serial standard you are testing. If you are testing a new serial line, you may need to measure the bit rate near the transmitter, or after some equalization (i.e., Tx emphasis equalization, Rx equalizations such as CTLE) so that the eye is opened for bit rate measurement. You can also use the **Auto Detect** option in the Clock Recovery panel to identify the bit rate.

Scroll down for information on Troubleshooting Clock Recovery.

Nominal Bit Rate. The nominal bit rate of the signal. It is typically specified by a serial data standard if the signal is generated from a device designed based on standards. If it may vary, then the **Auto Detect** option could be helpful.

NOTE. *The nominal bit rate you enter must be accurate, or you'll need to press the radio button to recover the data and clock signals.*

Auto Detect. When this radio button is selected, SDLA searches in the neighborhood of the nominal bit rate to detect the correct bit rate of the signal. After using the detect bit rate to open the eye, you can further tweak the nominal bit rate based on the detected bit rate to tune the clock recovery settings.

NOTE. *If SDLA detects spread spectrum clocking (SSC) in the input waveform, Auto Detect is turned on.*

PLL Type. The software supports Type I and Type II PLL clock recovery. Each serial standard specifies the type of PLL to use for clock recovery.

PLL BW. The loop bandwidth of the PLL is defined as the -3 dB frequency of the error transform function of the PLL. The value should be specified in the serial standard.

PLL Damp. This is the damping ratio of the Type II PLL. The value should be specified in the serial standard.

Clk Delay (ps). The clock delay is a specific delay added to the recovered clock after the PLL result. The value adjusts the clock offset to optimize the equalization result and achieve the best data recovery.

Troubleshooting Clock Recovery. If clock recovery fails, your bit rate might not be what you expect. One solution is to select **Auto Detect** in the Clock Recovery panel, as described above. Another solution is to measure the bit rate as near to the transmitter as possible. You can use the DPOJET application running on the oscilloscope to accurately measure the bit rate.

Training Sequence Functions. Another technique is to use the Training Sequence functions to help the Rx Equalizer identify the correct bit sequence before again running your test signal through the Rx Equalizer. Press here for more information.

The image below shows the **TrainSeq** tab of the Rx Configuration menu:

1. Use a signal source with the same data pattern as the signal you plan to test, but with a clean, open eye pattern. This signal could be one acquired close to the transmitter, or a slower speed version of the original signal, or the original signal compensated using Tx emphasis or Rx CTLE to improve the eye opening.
2. On the Rx Configuration menu, select the **TrainSeq** tab. Set the correct **Pattern Length** according to the standard; for example, 127 for a PRBS7 data pattern.
3. Press the **Detect** button. You should see a Bit Sequence displayed in the left field, which should be the same bit sequence as in your original signal.
4. With the correct bit sequence in place, select the **Config** tab and select the original test source.
5. Select (enable) the **Use TrainSeq** box if not already enabled. Enter the correct bit rate if you changed it in a preceding step.
6. Press the **Run Eq** button.
7. Check the results on the oscilloscope display. You should see a recovered data signal, though it may not meet the standard specifications. You may need to address other design issues to correct any problems with the recovered data.

Checking Test Point Filters. Another area for investigation is whether your test point filters are correct. Review the plots for those filters to determine whether high-frequency noise or other aberrations are corrupting the signal. Use the *global bandwidth filters* to reduce such noise.

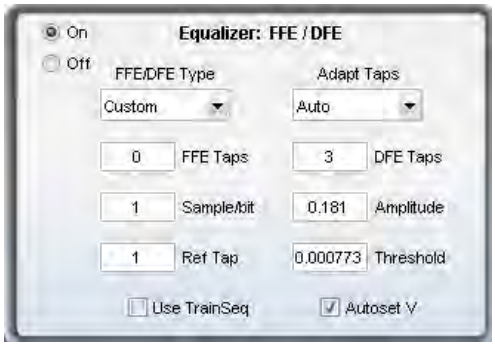
SEE ALSO:

- *Using CTLE*
- *Using FFE/DFE to Improve Signal Recovery*
- *Rx Configuration Menu*
- *Rx Block Overview*

Using FFE-DFE to improve signal recovery

To use the FFE/DFE equalizers, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User**. On the Config tab, the **Equalizer: FFE/DFE** panel is on the right.

You may adjust the Rx Equalizer settings in order to recover the data and clock signals by using many of the same techniques used to optimize a hardware receiver.



FFE/DFE Type. The following selections are available in the drop-down menu:

- **Custom:** You may configure every parameter in the FFE/DFE panel.
- **PCIe Gen3:** This is a special DFE option defined in the PCIe Gen3 specification. For details, see *Using the PCIE Option in FFE/DFE.*
- **PCIe Gen4:** This is a special DFE option defined in the PCIe Gen4 specification. For details, see *Using the PCIE Option in FFE/DFE.*
- **USB3.1 Gen2:** There is a special DFE option defined in the USB3.1 Gen2 specification. For details, see *Using the USB3.1 Gen2 option in FFE-DFE* on page 126
- **MIPI:** This is a special DFE option defined in the MIPI specification. For details, see *Using the MIPI option in FFE-DFE* on page 127.
- **CAUI-4:** This is a special DFE option defined in the CAUI-4 specification. For details, see *Using the CAUI-4 option in FFE-DFE* on page 128).
- **TBT 10.3125 Gb/s:** This is a special DFE option defined in the TBT (Thunderbolt) 10.3125 Gb/s specification. For details, see *Using the TBT (Thunderbolt) option in FFE-DFE* on page 129.
- **TBT 20.625 Gb/s:** This is a special DFE option defined in the TBT (Thunderbolt) 20.625 Gb/s specification. For details, see *Using the TBT (Thunderbolt) option in FFE-DFE* on page 129.

Adapt Taps. The following selections are available in the drop-down menu:

- **Auto:** The adaptation routine starts by identifying initial Tap settings and then adjusts them to optimize recovery of the data and clock.
- **From Current:** The adaptation routine uses current Taps values as the initial Taps settings, then adjusts them to optimize recovery of the data and clock. The initial Taps settings might be those saved from an earlier test.
- **None:** The Rx equalizer uses the current Taps either from your inputs or from a previous adaptive session. Use the entered values without changes. This option is useful when you want to load a known Taps file in the **Taps** tab to resume a test started earlier.

Most of the following parameters are defined in a serial data standard:

FFE Taps. The Feed-Forward Equalizer tap number is normally set to a number defined by the serial data standard. A value of FFE Taps = 0 means the FFE has one Tap with Tap coefficients fixed to 1, signifying that FFE is off. The default value is 0.

Sample/bit. Sample per bit specifies the number of FFE Taps per bit. If set to >1, it implies an FFE with fractional spaces. The default value is 1.

Ref Tap. The Reference Tap for the FFE indicates the number of precursor Taps. It must be set to one (1) more than a multiple of the number of FFE Taps per bit. The default value is 1.

DFE Taps. The DFE Taps number is normally set to a number defined by the serial data standard. For example, the setting for SAS is 3, and the setting for PCIE Gen3 is 1.

Amplitude. The Amplitude is the target output amplitude for the Rx Equalizer. When you select Autoset Voltages (**Autoset V** checkbox), the adaptation routine adjusts this value automatically to optimize the recovery of the data signal. The default value is 0.15 V.

Threshold. The Threshold is the middle voltage level of the signal, which may be the transition between logic levels. For biased signals, enter the mid-level value. For differential signals, the value should be close to 0 V. The default value is 0 V. Lacking clear knowledge of the correct voltage, use the Autoset Voltages function to determine the optimal value.

Use TrainSeq. Enables the Rx Equalizer to optimize its adaptation routine over a specific pattern the length of which is defined on the TrainSeq tab.

Autoset V. When Autoset Voltages is enabled, the Rx Equalizer adaptation routine adjusts the Amplitude and Threshold values to optimize recovery of the data and clock.

SEE ALSO:

- *Using CTLE to Improve Signal Recovery*
- *Using Clock Recovery for FFE/DFE Equalization*
- *Rx Configuration Menu*
- *Rx Block Overview*

Using the PCIE option in FFE-DFE

To use the PCIE option with FFE/DFE, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User**. On the Config tab, in the **Equalizer: FFE/DFE** panel, choose **PCIe Gen3** or **PCIe Gen4** from the **FFE/DFE Type** drop-down menu.

The PCIe Gen3 specification defines a one-Tap DFE with no FFE, while PCIe Gen4 defines a two-Tap DFE with no FFE, while PCIe Gen4 defines a two-Tap DFE with no FFE. The DFE Tap value is limited to a value between -30 mV and 30 mV.

When **PCIe Gen3** or **PCIe Gen4** is selected in the drop-down menu, the following field values are grayed out and their values set by internal algorithms:

- FFE Taps = **0**
- Sample/bit = **1**
- Ref Tap = **1**
- Use trainSeq = **unchecked**
- DFE Taps = **1** (Gen3) or **2** (Gen4)
- Amplitude (V) = **1**
- Autoset Voltages = **checked**
- Clock recovery is set per PCIE specification: nominal bit rate is set to 8 (Gen3) or 16 (Gen4) Gb/s, PLL Type to 1, PLL BW MHz to 10.

These fields are enabled again when **Custom** is selected in the FFE/DFE Type drop-down menu.

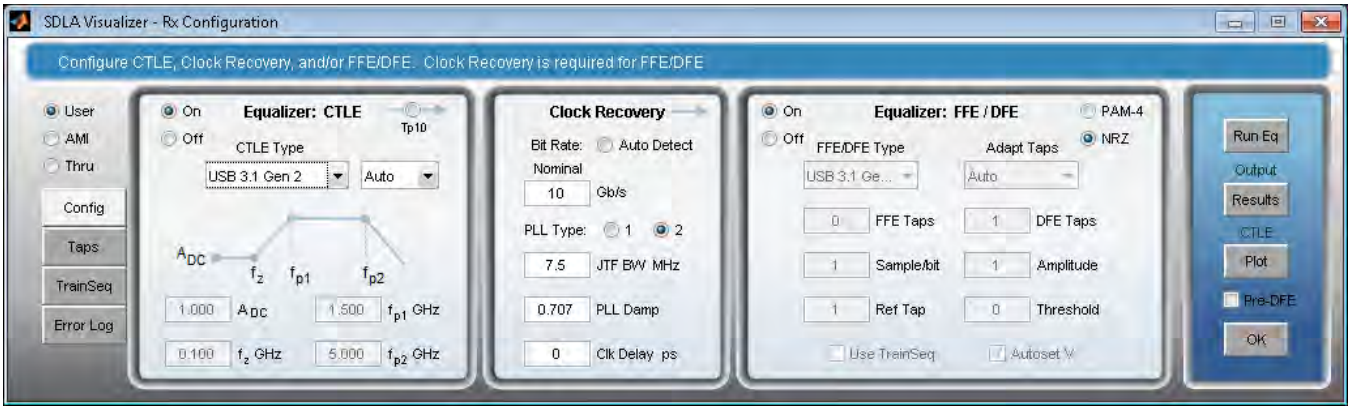
SEE ALSO:

- *Using FFE/DFE to Improve Signal Recovery*
- *Rx Configuration Menu*
- *Rx Block Overview*

Using the USB3.1 Gen2 option in FFE-DFE

To use the USB3.1 Gen2 option with FFE/DFE, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User**. On the Config tab, in the **Equalizer: FFE/ DFE** panel choose **USB3.1 Gen2** from the **FFE/DFE Type** drop-down menu.

The USB3.1 Gen2 specification defines a one-Tap DFE with no FFE. The DFE Tap value is limited to a value between -50 mV and 50 mV.



From menu, the following field values are grayed out and their values set by internal algorithms:

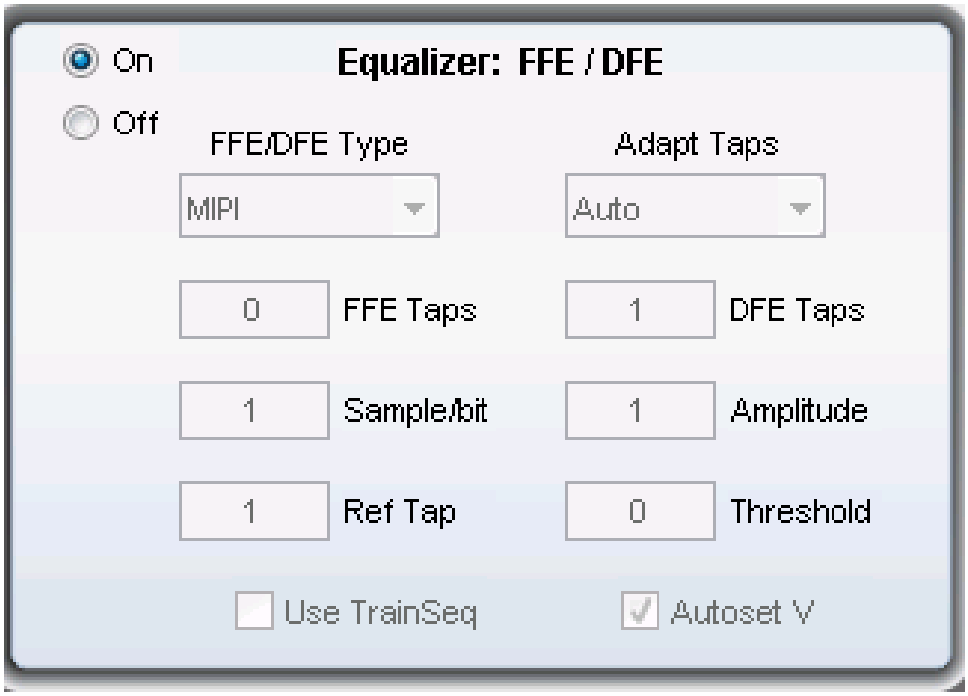
- FFE Taps = **0**
- Sample/bit = **1**
- Ref Tap = **1**
- Use trainSeq = **unchecked**
- DFE Taps = **1**
- Amplitude (V) = **1**
- Autoset Voltages = **checked**
- Clock recovery is set per USB3.1 Gen2 specification: nominal bit rate is set to 10 Gb/ s, PLL Type to 2, PLL BW MHz to 7.5MHz.

These fields are enabled again when **Custom** is selected in the FFE/DFE Type drop-down menu.

Using the MIPI option in FFE-DFE

To use the MIPI option with FFE/DFE, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User**. On the Config tab, in the **Equalizer: FFE/ DFE** panel choose **MIPI** from the **FFE/DFE Type** drop-down menu.

The MIPI specification defines a one-Tap DFE with no FFE. The DFE Tap value is limited to a value between -30 mV and 30 mV.



When MIPI is selected in the drop-down menu, the following field values are grayed out and their values set by internal algorithms:

- FFE Taps = **0**
- Sample/bit = **1**
- Ref Tap = **1**
- Use trainSeq = **unchecked**
- DFE Taps = **1**
- Amplitude (V) = **1**
- Autoset Voltages = **checked**
- Clock recovery is set per MIPI specification: nominal bit rate is set to 10 Gb/s, PLL Type to 2, PLL BW MHz to 8MHz

These fields are enabled again when **Custom** is selected in the FFE/DFE Type drop-down menu.

Using the CAUI-4 option in FFE-DFE

To use the CAUI-4 option with FFE/DFE, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User**. On the Config tab, in the **Equalizer: FFE/DFE** panel choose **CAUI-4** from the **FFE/DFE Type** drop-down menu.

The CAUI-4 specification defines a five-tap DFE with no FFE.

When **CAUI-4** is selected in the drop-down menu, the following field values are grayed out and their values set by internal algorithms:

- FFE Taps = 0
- Sample/bit = 1
- Ref Tap = 1
- Use trainSeq = unchecked

- DFE Taps = 5
- Amplitude (V) = 1
- Autoset Voltages = checked

These fields are enabled again when **Custom** is selected in the **FFE/DFE Type** drop-down menu.

Using the TBT (Thunderbolt) option in FFE-DFE

To use the TBT option with FFE/DFE, press **Rx** on the Main Menu to open the Rx Configuration Menu. Select **User** . On the Config tab, in the **Equalizer: FFE/DFE** panel, choose **TBT 10.3125 Gb/s** or **TBT 20.625 Gb/s** from the **FFE/DFE Type** drop-down menu.

The TBT specification defines a one-tap DFE with no FFE. The DFE Tap value is limited to a value between -50 mV and 50 mV.

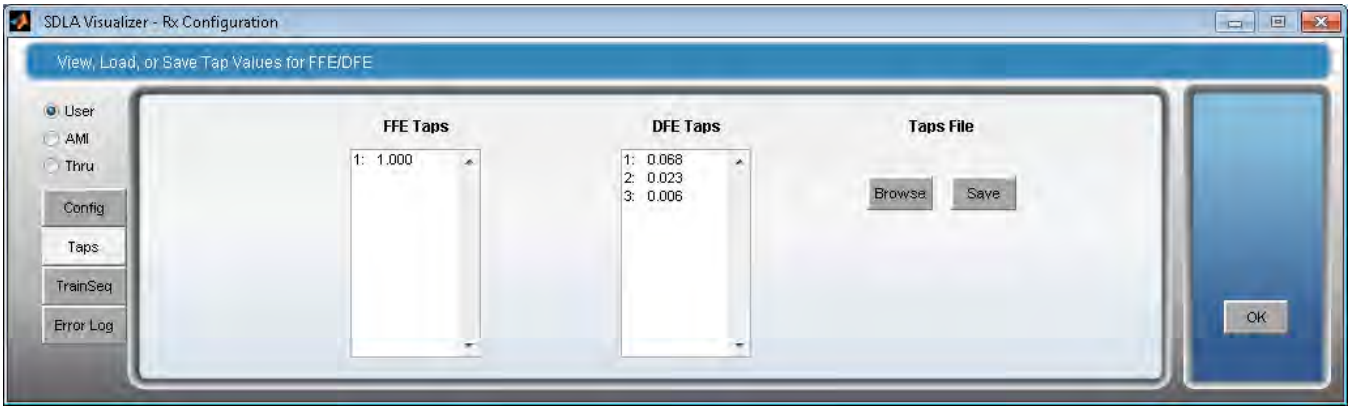
When **TBT 10.3125 Gb/s** or **TBT 20.625 Gb/s** is selected in the drop-down menu, the following field values are grayed out and their values set by internal algorithms:

- FFE Taps = **0**
- Sample/bit = **1**
- Ref Tap = **1**
- Use trainSeq = **unchecked**
- DFE Taps = **1**
- Amplitude (V) = **1**
- Autoset Voltages = **checked**

These fields are enabled again when **Custom** is selected in the **FFE/DFE Type** drop-down menu.

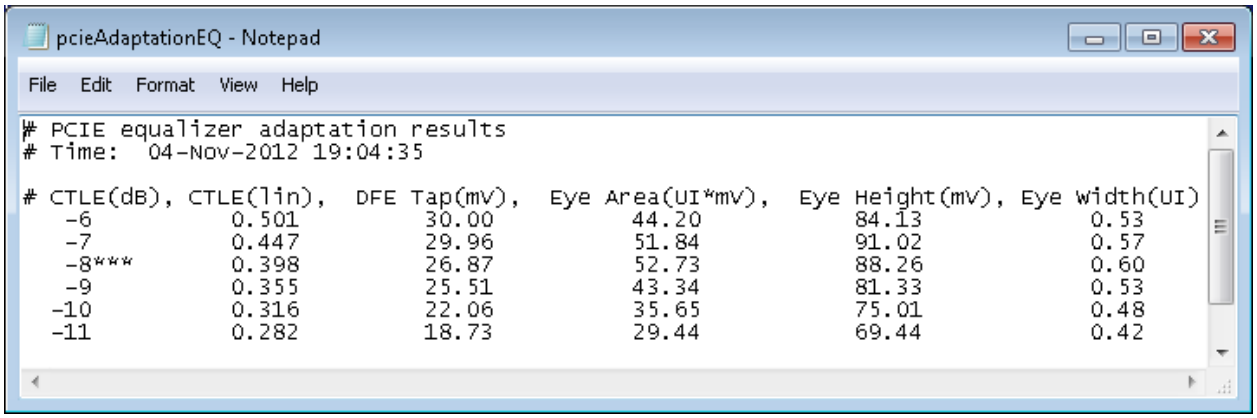
Using the taps tab

The settings on the **Taps Tab** (on the *Rx Configuration Menu* with User mode selected) reflect the settings on the **Config Tab**. For example, in the following figure, the FFE Taps have a value of 1, and the DFE field shows 3 Taps with different values. This state results from settings on the Config tab, where FFE is set to 0 and DFE set to 3. If this was the result of setting Adapt Taps to **Auto**, you could save the results in a Tap file for use in a later Rx Equalizer run.



When **PCIE3/USB3.1 Gen2/MIPI** is selected in the FFE/DFE panel (in the drop-down menu under **FFE/DFE Type**), and **Auto** or **From Current** is selected under **Adapt Taps**, the DFE adaptation algorithms attempt to maximize the eye area. The resulting DFE tap value is shown in the Taps tab.

The Config Tab **Results** button is enabled on the right panel (under **Output**) when **PCIE/USB3.1 Gen2/MIPI** is selected, and **Auto** or **From Current** is selected under **Adapt Taps**. After adaptation is finished, press **Results** to open the adaptation results file *pcieAdaptationEQ.txt*. This results file has better numerical resolution for DFE Tap(mv) than what is shown in the Taps tab. Note that the DFE tap value is between -30 mV and 30 mV per PCIE Gen3 specifications.



For a complete description of AMI files, visit the IBIS Open Forum at http://www.eda.org/ibis. See especially the I/O Buffer Information Specification for IBIS 5.1, AMI Executable Model File Programming Guide (section 10) and AMI Parameter Definition File Structure (Section 10A) at http://eda.org/pub/ibis/ver5.1/ver5_1.pdf.

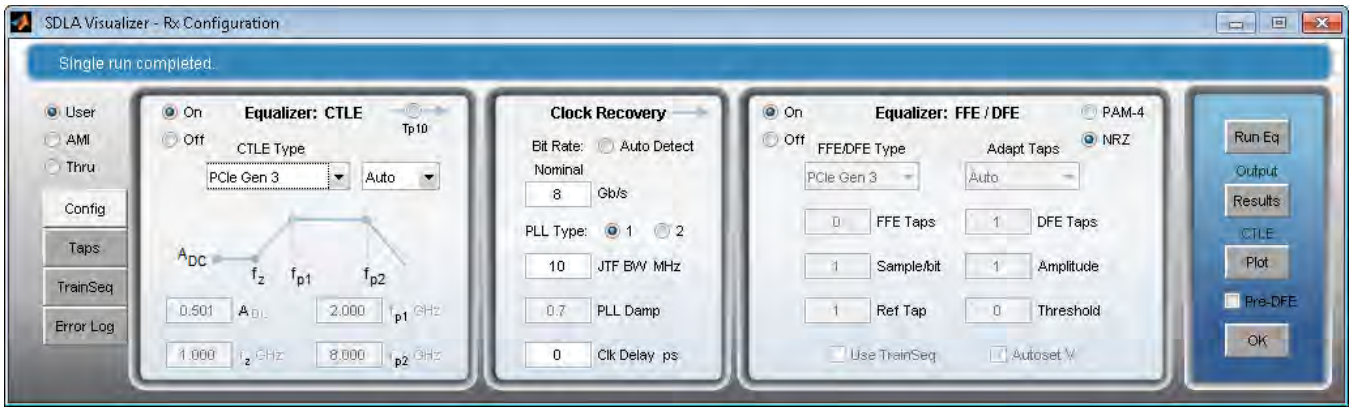
SEE ALSO:

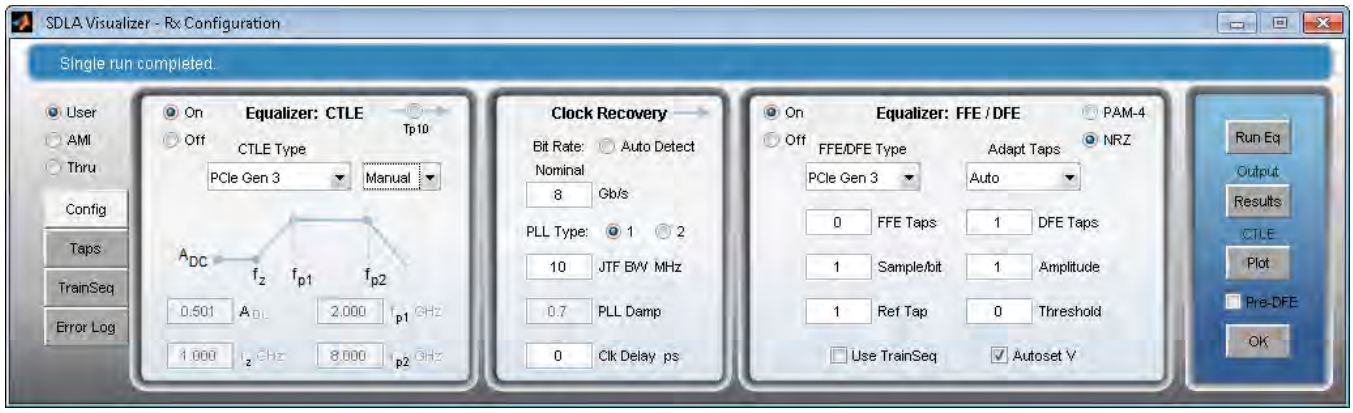
- *Using FFE/DFE to Improve Signal Recovery*
- *Rx Configuration Menu*
- *Rx Block Overview*

Manual FFE/DFE configuration for PCIE/USB/MIPI/CAUI-4/TBT options

As illustrated previously, setting **CTLE Type** to any of the PCIe/USB/MIPI/CAUI-4/TBT options grays out the Rx panel and disables changes to many of the equalization and clock recovery parameters.

SDLA now provides the option to enable editing these parameters for advanced users. Choose Manual from the drop-down box next to **CTLE Type.** This box does not appear for **Standard/IIR/FIR** and is set to **Auto** by default.

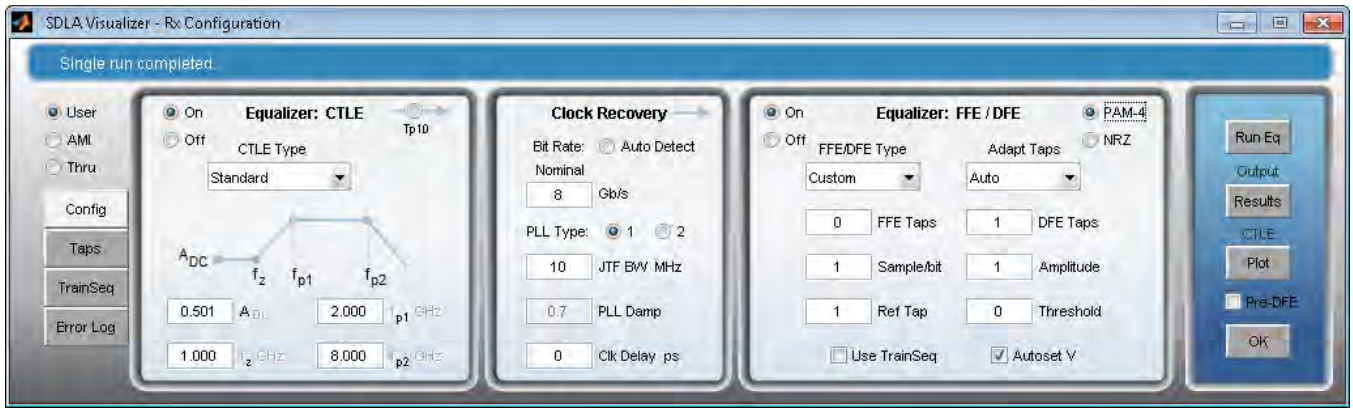




As seen in the image, **Manual** modes enables editing of the field values on the **Equalizer: FFE/DFE** panel. **Equalizer: CTLE** and **Clock Recovery** panels remain unchanged.

Equalizing PAM-4 signals

When the incoming signal is PAM-4, select **PAM-4** in the top right corner of **Equalizer: FFE/DFE** panel, as in the below image.

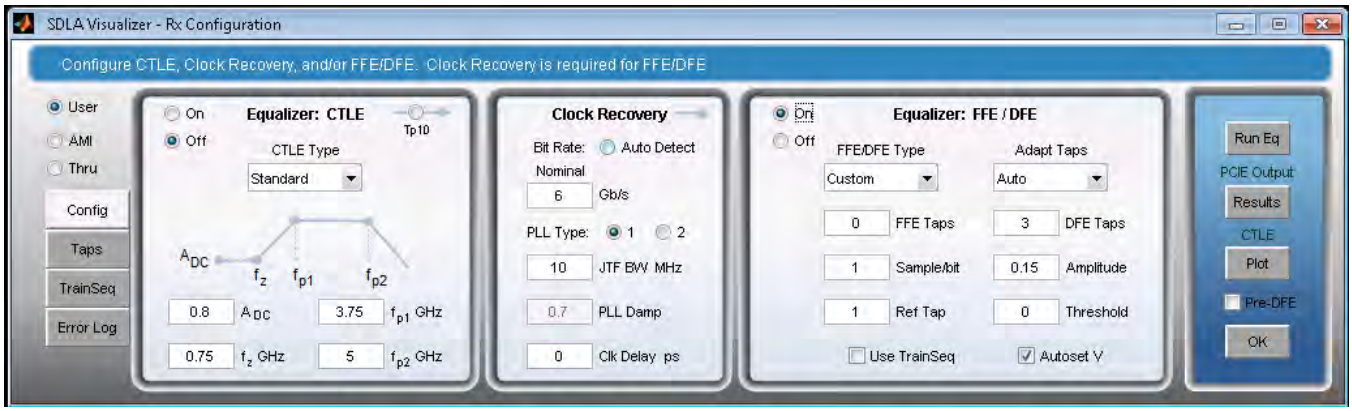


Currently PAM-4 does not apply to any of the supported standards. Therefore, once the PAM-4 option is selected, **CTLE Type** can only be set to **Standard/ IIR/FIR**, while **FFE/DFE Type** can only be set to **Custom.**

Similarly, PAM-4 DFE utilizes the LMS-based optimization criterion from SAS 6G.

Running the Rx equalizer

The following steps describe how to make a first run of the Rx Equalizer to determine whether further adjustments are necessary.



1. First, configure your input or inputs using the Main Menu.
2. Next, you need to turn on **Tp3** as it is required for the Rx Equalizer. On the Main Menu, press **Tp3** and use the *Test Point and Bandwidth Manager* to turn it on (A-B mode if it is the Dual Input case).
3. Press **Rx** on the Main Menu. On the Rx Configuration Menu, select the **User** radio button. On the **Config Tab**, enter the FFE and DFE Taps and configure the PLL fields for a Receiver as defined in the standard you are testing. (Alternatively, you can load a setup file by pressing **Recall** on the Main Menu that sets SDLA as per the standard you are testing against.)
4. Set the bit rate in the Clock Recovery panel (if it has not already been set by a standards file). Select **Auto Detect** if the nominal bit rate may not be accurate.
5. Press the **Run Eq** button.
6. To view the output waveforms, go to the oscilloscope display. The Ref4 waveform is the Data signal and is labeled **Tp4 R4**. The Ref3 waveform is the recovered Clock waveform and is labeled **Clk R3.**

SEE ALSO:

- *Rx Configuration Menu*
- *Rx Block Overview*

AMI mode

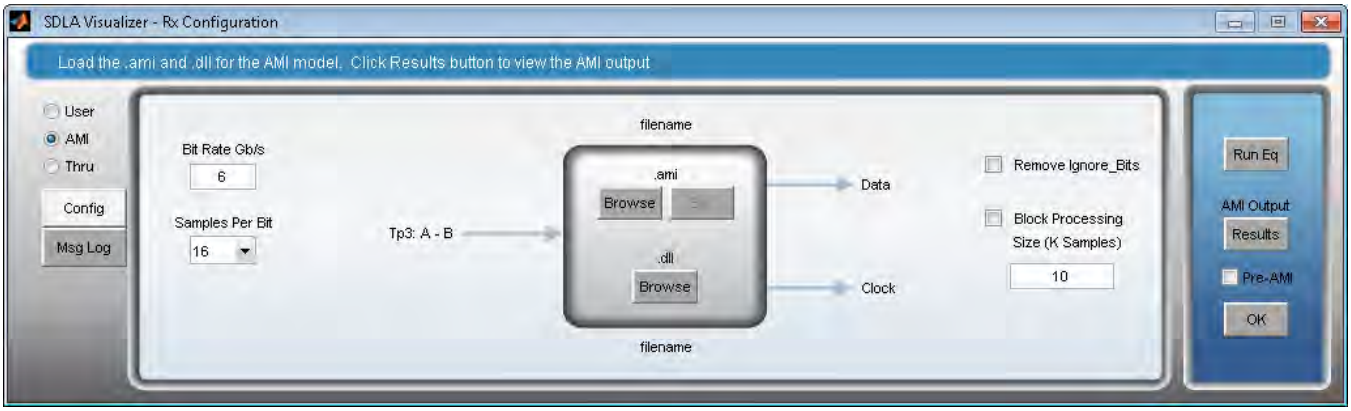
Many chip and system vendors use the IBIS Algorithmic Modeling Interface (IBIS-AMI) standard for designing and simulating multi-gigabit serial links. These models capture the behavior of transmitters and receivers as well as channels of particular design more precisely than generic implementation (for example, User Mode equalizer with CTLE and FFE/DFE). It is especially useful to apply the receiver behavioral model to the waveform captured by the scope. It allows evaluating the signal at the slicer of the receiver using various measurements and comparing it to simulation results obtained with the same model.

IBIS-AMI model is typically implemented as a combination of an .ami and a .dll file (often referenced from an .ibs file). SDLA Visualizer supports both 32 and 64 bit windows dll binaries. The .ami contains parameter definitions, their expected range and default values. SDLA Visualizer will extract the necessary information and condense the file to be used as the input string to the model. Parameters can be changed either by editing the original .ami file or the condensed file (which is easier to handle). The definition of parameters is vendor-specific and additional documentation may be needed for parameter tuning.

Version 2.1 of SLDA supports both full and condensed .ami files. If a full .ami file is specified the file is automatically condensed. The condensing operation reduces the Model_Specific section of the .ami file to essential fields, to a string that is passed to the .dll. In order to vary parameters the model uses when evaluating the Get_Wave function, edit the condensed .ami file by changing the respective parameter values, or edit the default values in full .ami.

Since the Model_Specific parameters are model-specific, consider comments or vendor documentation for additional information.

NOTE. *For specific information on how to modify an IBIS (.ami) parameter file for use by SDLA Visualizer, please refer to the readmeAmi.txt file available in C:\Users\Public\Tektronix\TekApplications\SDLA\AMI*



AMI mode is provided as an option for Rx modeling in SDLA Visualizer. It can be activated by choosing the AMI option on the Rx Configuration panel. Press **Browse** under .ami and load the ami file you want to use. Press on the lower **Browse** button to select the .dll file. For valid results the .ami and .dll files must be compatible.

NOTE. *signal labels **Tp3: A-B, Data** and **Clock** refer to I/O labels on the Main Menu Rx block.*

Samples per Bit settings control the interpolation ratio. Most AMI simulators and models expect a certain number of samples per unit interval (bit) to work properly. Please consult specific AMI model documentation to make sure whether there are specific requirements for this parameter.

Remove Ignore_Bits checkbox controls whether certain bits in the beginning of the waveform are ignored in the output waveform and measurements. The number of bits is specified as the Ignore_Bits parameter in the Reserved_Parameter section of the model (.ami file). Checking this box will eliminate the adaptation region of the waveform from the output. Sometimes, however, looking at the adaptation process may be of interest. Then the setting can be left unchecked.

Block Processing Size (K samples) specifies whether the block processing is used and the block size in K samples. Block processing is useful with long waveforms and complicated models. Block processing helps save memory. The use of block processing also may allow observing the AMI-processing in more detail. Some models implement saving of the adaptation record or log other data on each call to the Get_Wave function.

Pressing Run EQ takes the data from Tp3, processes it together with the information from the .ami and .dll files, and then loads the new waveform with equalized data into Tp4 (Ref4) and the recovered clock information into Tp5 (Ref3), if configured. Pressing **Run Eq** in the Rx block allows you to run this particular block over again without rerunning the preceding chain of operations.

NOTE. *For Run Eq to work properly, the Measurement and Simulation circuit modeling portion of SDLA (De-embed, Tx and Embed blocks) must run at least once after startup and each update (Press **Apply** on the main menu).*

Pressing **Results** (under **AMI Output**) opens a .txt file (AMI_out.txt), which is written to the folder where the .dll file is located. This file may contain output parameters from the AMI model such as the adaptation results on Taps (model-specific). Press the **Msg Log** tab to check the output message output by the AMI model.

Note that ami files may produce additional results like an adaptation record or debug information in other files. These are either stored in the location of the ami files or a specific location in the file system determined by the respective ami parameter.

Pre-AMI checkbox allows you to enable export of interpolated waveforms before AMI processing. The interpolation ratio is determined by the **Samples per Bit** and **Bit Rate** parameters (source waveform). The file can be found in *C:\Users\Public\Tektronix\TekApplications\SDLA\output filters* folder and it contains time voltage pairs. The ASCII format is the most universal but also has an effect on performance, so use it only when needed. This data can be used for comparison in EDA tools, MATLAB or other purposes.

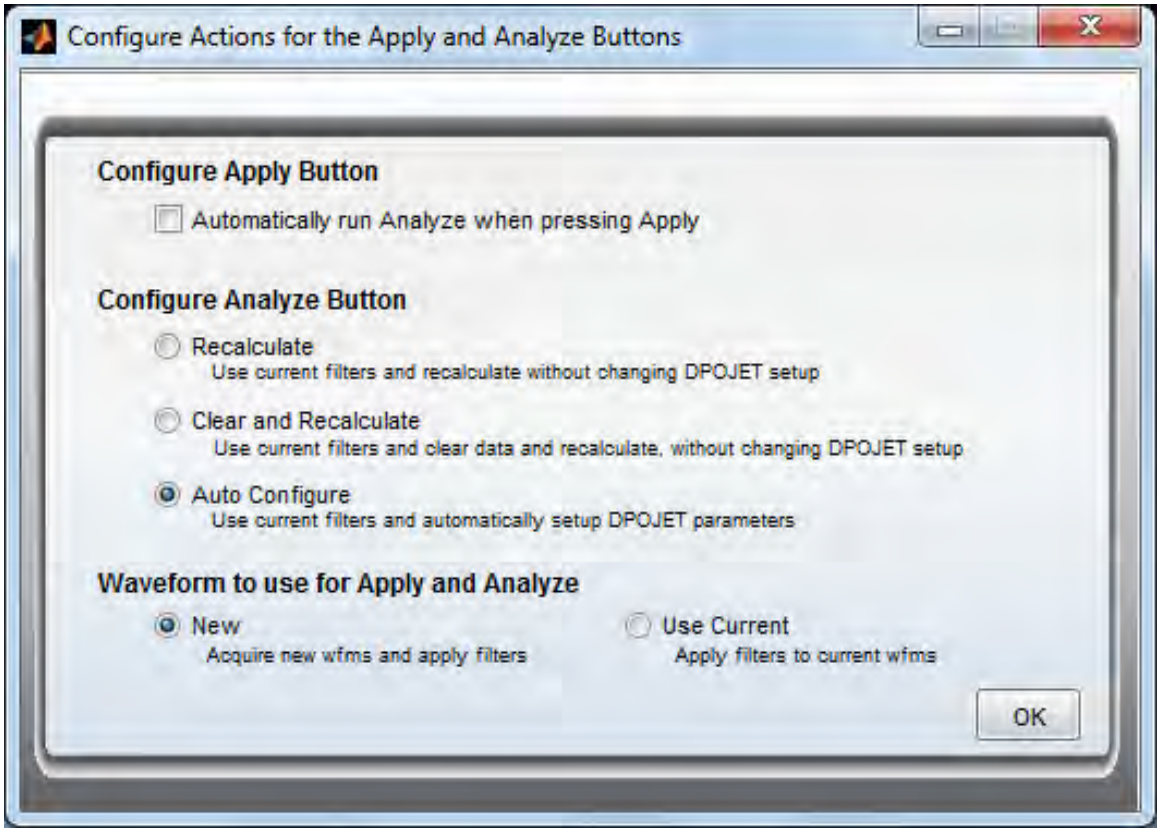
For a complete description of .ami files, visit the IBIS Open Forum at http://www.eda.org/ibis. See especially the I/O Buffer Information Specification for IBIS 5.1, AMI Executable Model File Programming Guide (section 10) and AMI Parameter Definition File Structure (Section 10A) at http://eda.org/pub/ibis/ver5.1/ver5_1.pdf.

SEE ALSO:

- *Rx Configuration Menu*
- *Rx Block Overview*

Configure actions for the apply and analyze buttons

You have some flexibility for determining what happens when you actually run the models using the **Apply** and **Analyze** buttons on the Main Menu, including how SDLA will work with DPOJET, and whether a new waveform is to be acquired or a previous one is to be used. When you press the **Config** button on the Main Menu, this menu comes up:



Configuring the Apply button

Check **Automatically run Analyze when pressing Apply** to combine the actions of the Apply and Analyze buttons. This will use the current configuration settings of the Analyze button as described below.

Configuring the Analyze button

There are three different options for configuring the Analyze button:

Recalculate: This recalculates the results in DPOJET without changing the DPOJET setup or clearing previous results. This can be used to process the measurements on multiple acquisitions. This option should not be used when new models are being applied, as it could lead to inconsistent results.

Clear and Recalculate: This clears the previous data results and automatically runs DPOJET without changing the DPOJET setup.

Auto Configure: This auto-configures DPOJET for all test points that are turned on, does TIE measurements and plots eye diagrams.

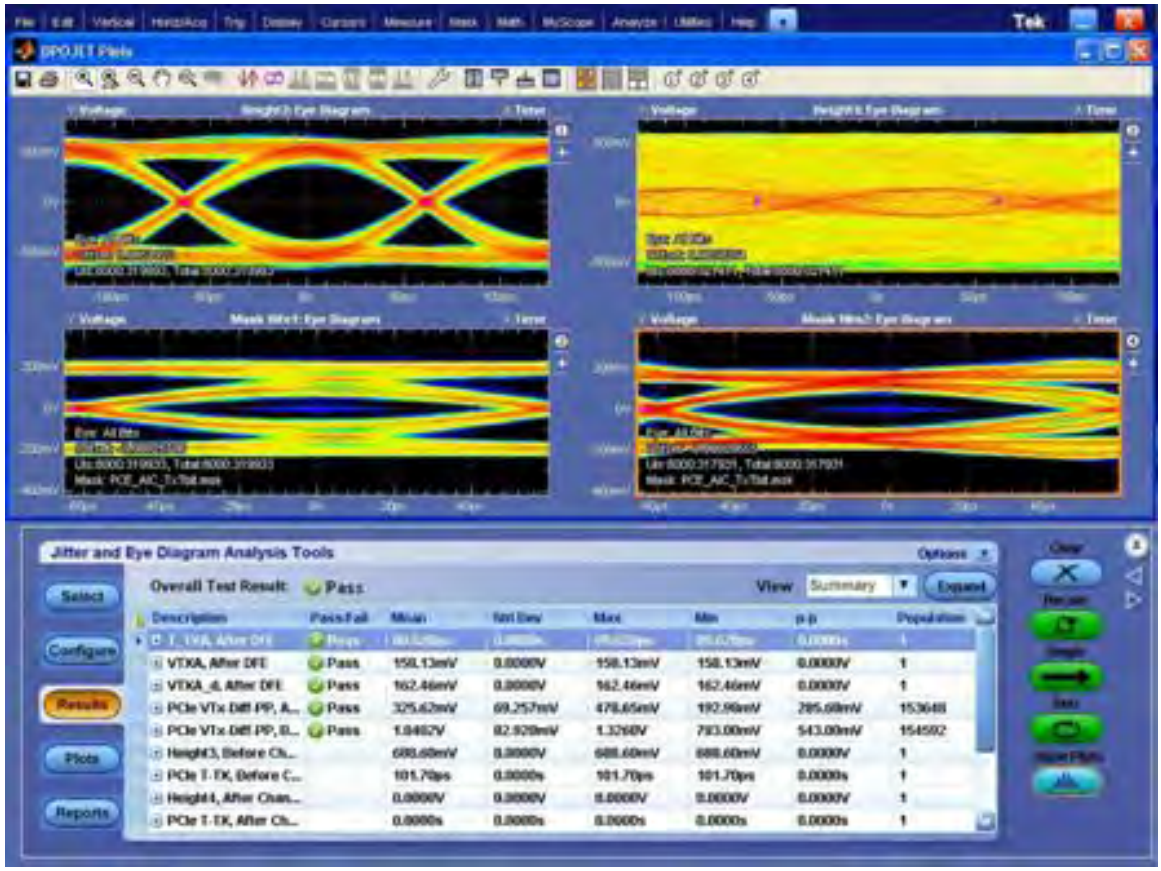
NOTE. *If custom settings have been defined in DPOJET,* ***Auto Configure*** *should not be used, as it will re-configure DPOJET.*

Waveform to use for Apply and Analyze

This option allows you to select whether a new waveform should be acquired each time the Apply or Analyze button is pressed. By default, a new waveform will always be acquired. If you desire to use the already acquired waveform, select **Use Current**.

NOTE. *It is important to properly configure the data rate when using the DPOJET Analyze function, as the clock recovery configuration in DPOJET is based on the data rate.*

The figure below shows the Analyze button configured to **Clear and Recalculate**.

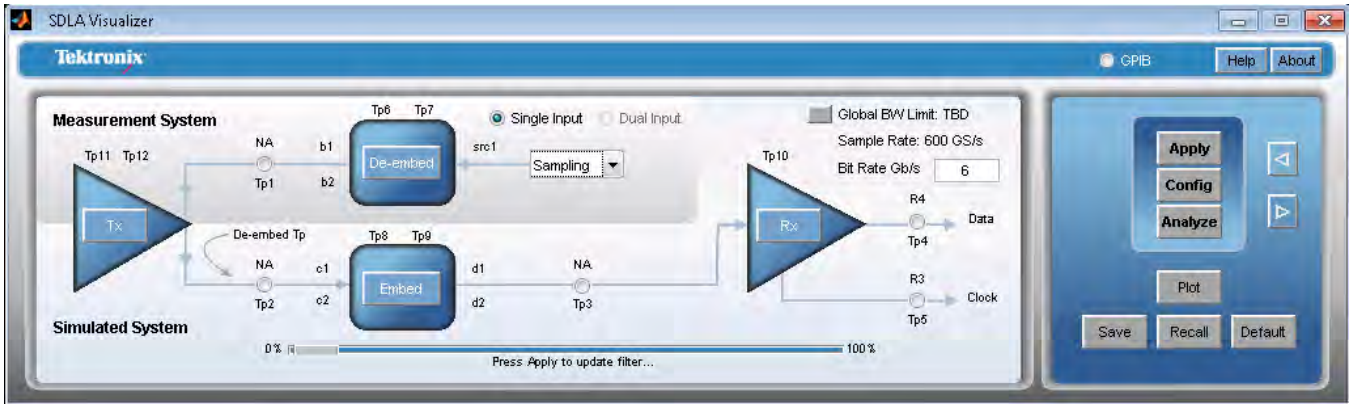


SEE ALSO:

- *Understanding the System*
- *Using DPOJET and SDLA Visualizer Together*

Creating filters for a sampling oscilloscope

The menu below shows the configuration for creating filters on a real-time oscilloscope for use on a sampling oscilloscope.

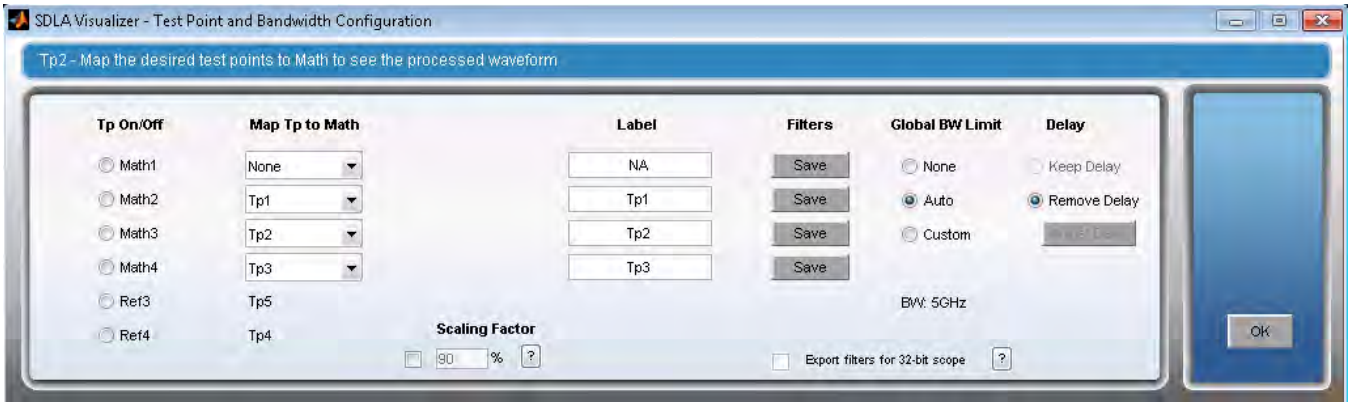


In the input source pull down box of the main menu, select Sampling as the source waveform.

When Sampling is selected as the source, Extend to 32 bits is disabled. Deselecting Sampling enables Extend to 32 bits. This applies to all of the following cases.

Single input case

Select Sampling as the source in default mode, single input and Remove Delay remain the same. The test point configuration menu should have Remove Delay on and the Adjust Delay disabled. The Export filters for 32 bit scope is also disabled as shown below:



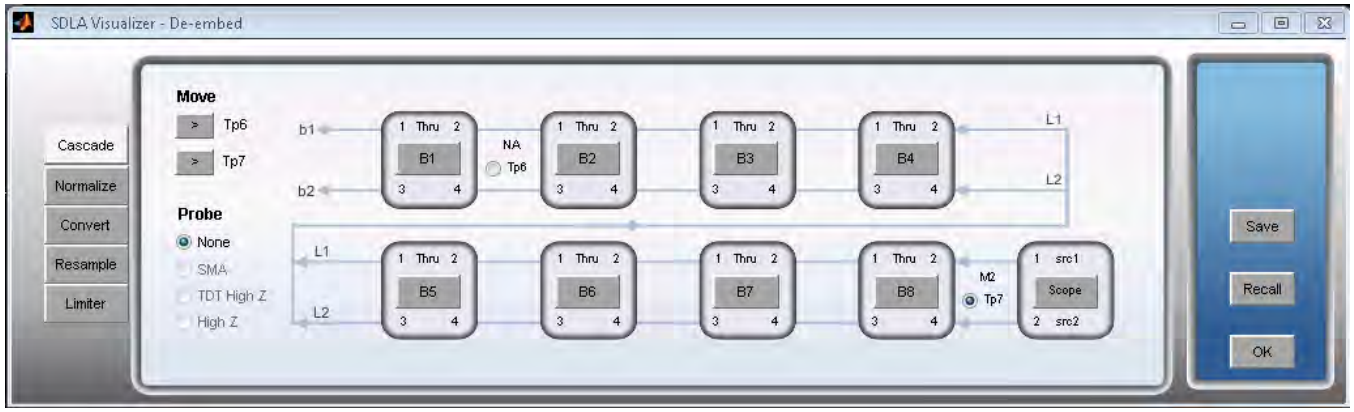
Dual input case

In Dual Input mode, Sampling is not displayed as the input source since it does not apply for Dual Input case.

When Sampling is selected as the source, Dual Input mode is disabled as shown in the main menu above.

The sample rate is always automatically updated with the bit rate in this case. When the user inputs a new bit rate anywhere in the SDLA, the sampling rate is changed to be 100 ×bit rate.

All probe options are disabled when Sampling is the source. Probes are not applicable to a sampling scope.



Running a test

Running a test: recommended order

Welcome to SDLA Visualizer, which offers a powerful, flexible set of modeling tools for de-embedding, embedding and equalizing high speed serial signals. This section describes the recommended order for running a test. The general steps and primary menus are listed below, and include links to usage details within each step. For conceptual explanations, see *SDLA Visualizer Product Overview*. For component details, see *Main Menu in Detail*.

NOTE. *If you would like to download a .PDF file of the Online Help that has been translated into Japanese, simplified Chinese, or Korean, visit www.tektronix.com and press on "Change Country" at the top. Then enter the search term "SDLA Visualizer".*

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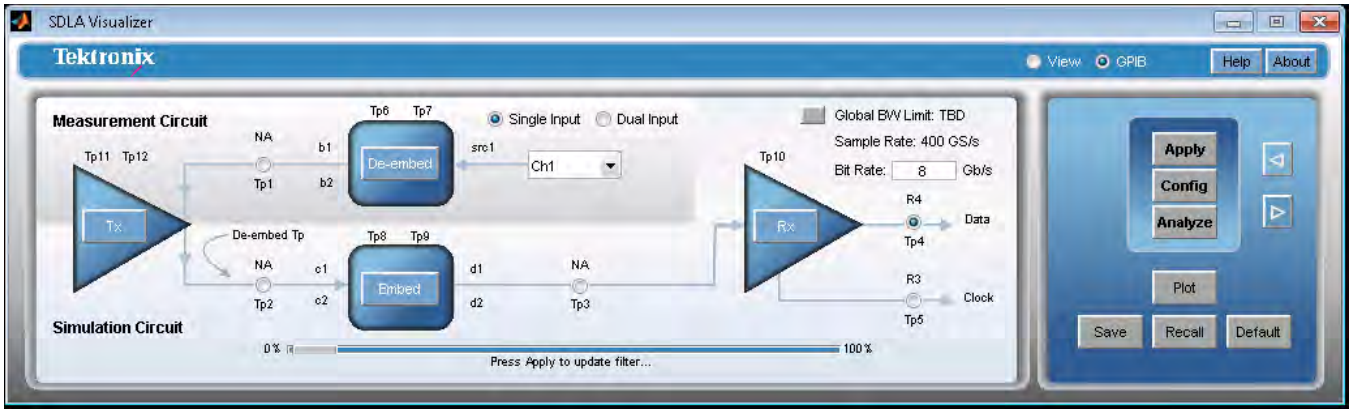
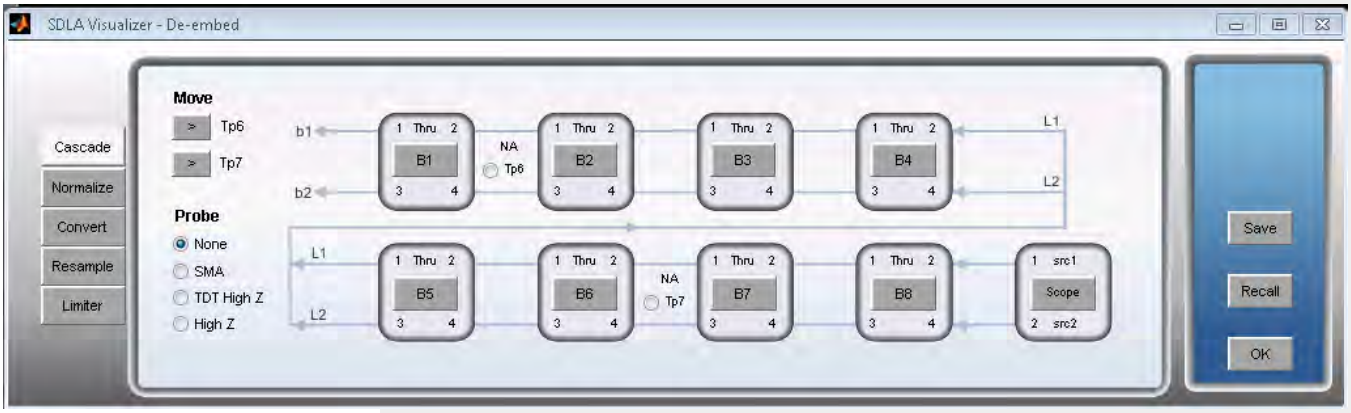
1. First, **connect the fixture and oscilloscope to the DUT**, using a probe or direct connection. Connect the source signal to an oscilloscope input channel. Adjust the oscilloscope trigger, vertical, and horizontal settings to capture signals with good fidelity. Using the oscilloscope Autoset function can simplify this adjustment. Ensure that the sample rate is set to a value for which its DSP calibration filters are on. (See the scope vertical menu.)
2. **Verify that DPOJET/JNB is installed** and that it runs correctly. You can leave DPOJET/JNB running.
3. **Bring up SDLA Visualizer** by pressing **Analyze** on the TekScope menu and selecting the program. (Use the Alt Tab keys to switch between programs.)



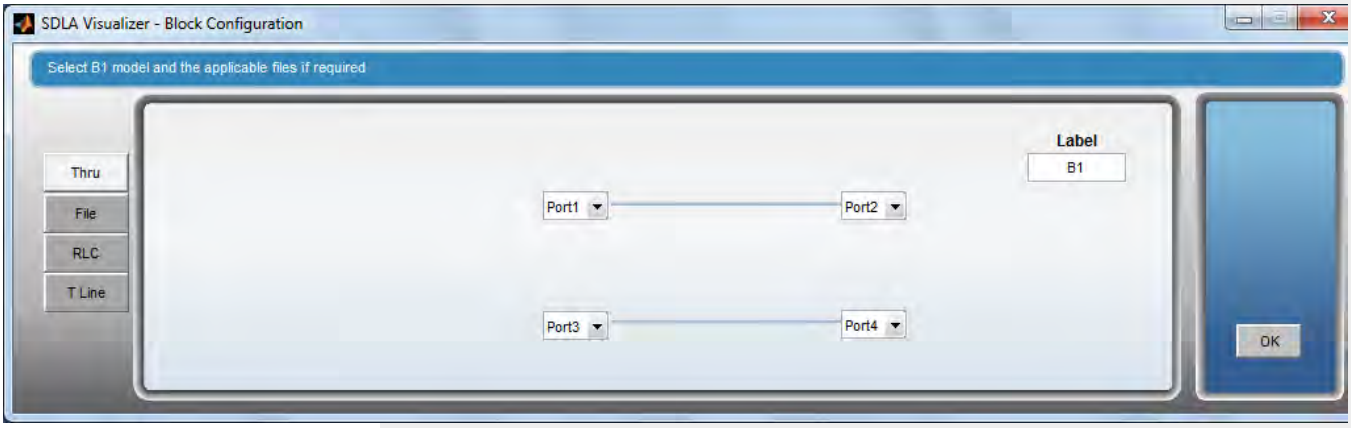
4. Now, **configure the elements of the Measurement Circuit** (the upper portion of the diagram), which represents the equipment that needs to be de-embedded or removed from the acquired signal, such as fixtures, cables, and probes. Start by defining the first element, the **De-embed Block**, where you can use a cascade of S-parameter blocks, an RLC Circuit, or a lossless transmission line to represent the model. Each element can be validated with a plotting function. The load of the circuit, in many cases the oscilloscope, is also defined here. Steps

   a. Press **De-embed** on the Main Menu. The De-embed/Embed Menu comes up.



   b. On the **Cascade** tab, select a probe option if applicable (SMA or High Z).

   c. Press on the first block **B1**. The **Block Configuration Menu** will come up.



   d. Select either the **Thru, File, RLC,** or **T Line** tab to choose how you'd like to model the element.

   If you are selecting the **File** tab, choose a model type from the **Model** drop down list. For example, select "4-Port Single-ended" when using a 4-port single-ended S-parameter model. Press on the **Browse** button to load the S-parameter model and re-assign the port assignments if necessary.

Optionally, press **Plot** to view the S-parameter plot of the selected model.

e. Press **OK** to return to the **Block Configuration Menu**.

f. Repeat this procedure for as many of blocks **B2 - B8** as your Measurement Circuit model needs. It is important to load each element in the correct order as SDLA Visualizer takes reflections and cross coupling terms into account. Unused blocks are simply treated as “thru”.

g. Press on the final block of the **Block Configuration Menu**, which will either be labeled **Scope**, **SMAProbe**, or **Load**. This will allow you to determine what will load the output ports of the measurement circuit. In many cases, this is the oscilloscope or an SMA probe connected to a scope, or an Rx input (or something else) when a High Z probe has been selected.

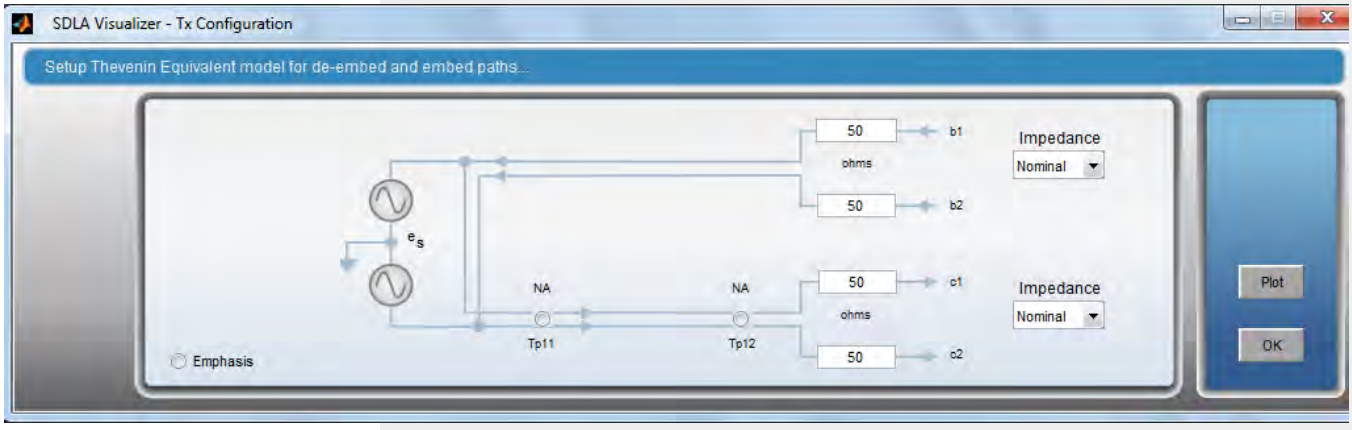
The impedance can be modeled as a nominal value, one 2-port S-parameter block, or two 1-port S-parameter blocks by choosing one of the options in the Impedance drop-down list. By default, SDLA assumes 50 Ohm impedance.

h. Optionally, you may plot the S-parameters that represent the model if the **Plot** option is available on the right.

For additional details, see *De-embed/Embed Menu*.

5. Next, define the second element of the Measurement Circuit, the **Tx Block.** Use this to set up the Thevenin Equivalent model for the de-embed path and to model the transmitter output impedance. This should be modeled either nominally to represent the actual transmitter, with two 1-port S-parameter models, or with one 2-port S-parameter model. Steps

a. First, configure the transmitter impedance by pressing on **Tx** on the Main Menu. (By default, SDLA assumes 50 Ohm impedance.) The **Tx Configuration Menu** will come up. The controls on the top are for the Measurement Circuit.



b. Next, choose one of the options in the upper **Impedance** drop-down list. Press **OK**.

c. Optionally, you may plot the S-parameters representing the model at this point by pressing **Plot** on the right.

d. The Thevenin equivalent voltage will be computed by SDLA.

For additional details, see *Tx Configuration Menu*.

6. Now, if applicable, **define the elements of the Simulation Circuit Model**, which simulates elements that are not physically present. Start by using the **Tx Block once again.** Steps

a. First, configure the transmitter impedance by pressing on **Tx** on the Main Menu. (By default, SDLA assumes 50 Ohm impedance.) The **Tx Configuration Menu** will come up (shown above). The controls on the bottom are for the Simulation Circuit.

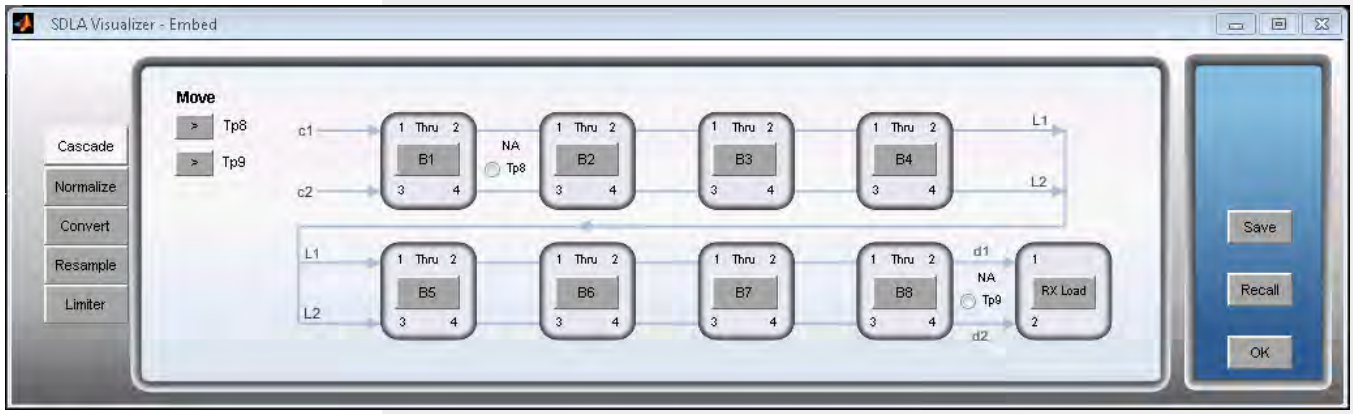
b. Next, choose one of the options in the lower **Impedance** drop-down list. The impedance can be modeled either as a nominal value, or as one 2-port S-parameter model, or two 1-port S-parameter models. Press **OK**.

c. Optionally, you may add or remove Emphasis by pressing on the **Emphasis** radio button in the Tx Configuration Menu. An **Emphasis button** will appear in the circuit diagram. Press on it to bring up the **Emphasis Menu**. Press **OK**.

For additional details, see *Tx Configuration Menu*.

7. Next, define the second element of the Simulation Circuit Model, the **Embed Block.** Use this to define the elements that make up the simulation path. The Embed Block has similar functionality to the De-embed Block described above. Steps

a. Press on **Embed** on the Main Menu. The De-embed/Embed Menu comes up. Select the **Cascade** tab.



b. Press on the first block **B1**. The **Block Configuration Menu** will come up.

c. Select either the **Thru, File, RLC,** or **T Line** tab to choose how you'd like to model the element.

If you are selecting the **File** tab, choose a model type from the **Model** drop down list. For example, select “4-Port Single-ended” when using a 4-port Single-ended S-Parameter model. Press on the **Browse** button to load the S-parameter model and re-assign the port assignments if necessary.

Optionally, press **Plot** to view the S-parameter plot of the selected model.

d. Press **OK** to return to the **Block Configuration Menu**.

e. Repeat this procedure for as many of blocks **B2 - B8** as your Simulation Circuit model needs. It is important to load each element in the correct order as SDLA Visualizer takes reflections and cross coupling terms into account. Unused blocks are simply treated as “thru”.

f. Press on the final block of the **Block Configuration Menu**, which will be labeled **Rx Load**. This will allow you to determine what will load the output ports of the Simulation Circuit. In many cases, this would model a physical receiver.

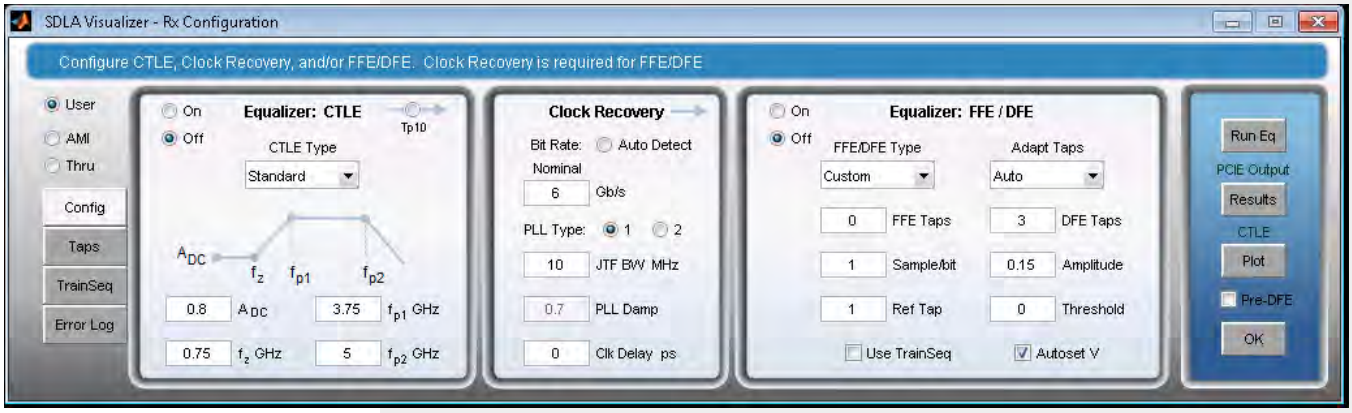
The impedance can be modeled as a nominal value, one 2-port S-parameter block, or two 1-port S-parameter blocks by choosing one of the options in the Impedance drop-down list. By default, SDLA assumes 50 Ohm impedance.

g. Optionally, you may plot the S-parameters representing the model at this point, if the **Plot** option is available on the right.

For additional details, see *De-embed/Embed Menu*.

8. Define the third element of the Simulation Circuit Model, the **Rx Block.** Use this to simulate the equalization inside the Rx block, allowing you to virtually observe the waveform at the receiver pins. CTLE, FFE/DFE and IBIS AMI models are available. Steps

a. Press on **Rx** on the Main Menu. The Rx Configuration Menu comes up.



b. Choose the type of equalizer to model: **User**, IBIS **AMI**, or **Thru** (no EQ).

c. If you select **User**, CTLE/FFE and DFE equalizers can be used. For CTLE, under **CTLE Type**, choose the method to define the CTLE (Standard, IIR, FIR, PCIe 3.0, USB3.1 Short, USB3.1 Long, USB3.1 Gen2 and MIPI). To view the output of the CTLE, select the **Tp10** radio button and assign Tp10 to an available math channel.

d. To use DFE and FFE, Clock Recovery must be configured. After configuring the Clock Recovery, select the **On** radio button to turn on the FFE/DFE block. Under **FFE/DFE Type,** choose either Custom, PCIE3, USB3.1 Gen2, or MIPI, and configure the FFE/DFE settings.

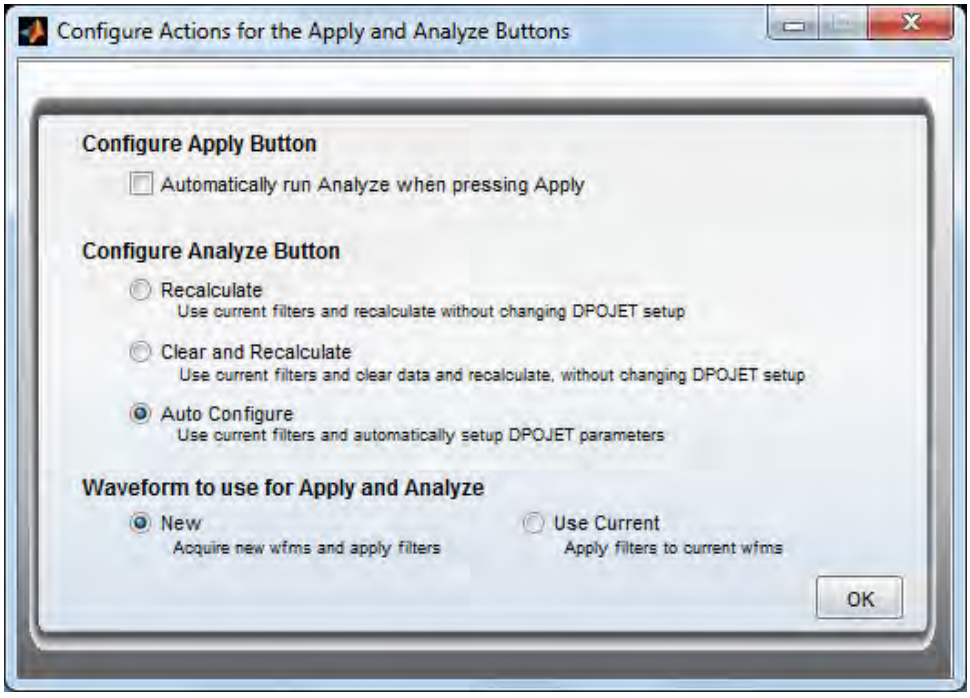
e. If you have previously pressed **Apply** on the Main Menu, and the only changes to the model are in the Rx Block, you only need to press on the **Run Eq** button to apply the Equalizer. If other changes have been made, press **OK** in the Rx Block and then press **Apply** in the Main Menu.

For additional details, see *Rx Configuration Menu*.

9. Now that the model has been defined, **configure the Test Points**. Simply press on any of the test points on the Main Menu to bring up the Test Point and Bandwidth Manager, where you can assign it to a Math channel and other options. SDLA has 12 test points, with up to four math and two reference waveforms visible on the scope graticule at one time. For details, see *Test Point and Bandwidth Manager*.

10. (RT only) After the model has been configured,

a. Press the **Config** button on the Main Menu. On the resulting menu, configure the actions you'd like to happen when the **Apply** and **Analyze** buttons are pushed. For details, see *Configure Actions for Apply and Analyze Buttons.*



b. Press the **Apply** button on the Main Menu. Wait for the status bar at the bottom to show that processing is complete. Pressing Apply creates a transfer function for each enabled test point based on the measurement and simulation circuit models defined above. The math and reference waveforms associated for each enabled test point will be automatically updated on the oscilloscope. If the Rx Block was enabled above, the clock and data output of the block will be stored in **Ref3** and **Ref4**. **DPOJET** will be run automatically if you configured it to do so in the prior step.

11. (Sampling only) After the model has been configured, press the **Apply** button on the Main Menu. Wait for the status bar at the bottom to show that processing is complete. Pressing Apply creates a transfer function for each enabled test point based on the measurement and simulation circuit models defined above. It then tells JNB to load the transfer function that corresponds to the enabled test point that is closest to the receiver.
12. Once the model has been applied, you may **plot the test points** by pressing **Plot** on the Main Menu. You may view the Magnitude, Impulse Response, Step Response, and Phase Plots to ensure that they have the response you expect. For details, see *Plots.*

13. If the plots did not show you the response you expected, you may **fine-tune the bandwidth,** by pressing the **Global BW limit** button on the Main Menu. For details, see *Test Point and Bandwidth Manager.*
14. Optionally, you may **save the test points** filters that represent the transfer function of each of the enabled test points. After applying the model, press on any test point to bring up the Test Point and Bandwidth Manager. Any enabled test point can be saved by pressing the **Save** button (not the Save button on the Main Menu, which saves the setup.) For additional details, see *Saving Test Points.*

This completes the general procedure for running the SDLA Visualizer Software. Each block has many configuration parameters not covered in this procedure. Explore the details of each processing block to get the most out of the SDLA Visualizer Software.

SEE ALSO:

- *Examples of Tasks and Troubleshooting*
- *Main Menu in Detail*
- *SDLA Visualizer Product Overview*

Examples and troubleshooting (RT only)

Examples of tasks and troubleshooting

Tasks

Here are some examples of the many tasks that SDLA Visualizer can perform:

De-embedding Cables

Embedding a Serial Data Link Channel

De-embedding a High Impedance Probe

De-embedding Significant Reflections with Dual Input Waveforms

Removing a DDR Reflection with a Single Input Waveform

Troubleshooting using S-parameter plots

SDLA's S-parameter plots can be helpful in many scenarios, including:

– Viewing a DUT with mismatched differential pairs

– Troubleshooting bad VNA measurements using overlay plots

– Troubleshooting bad phase response

– Verifying mixed mode vs. single-ended mode

– Troubleshooting bad step response

For details, see *Using Plots for Troubleshooting S-parameters*.

SEE ALSO:

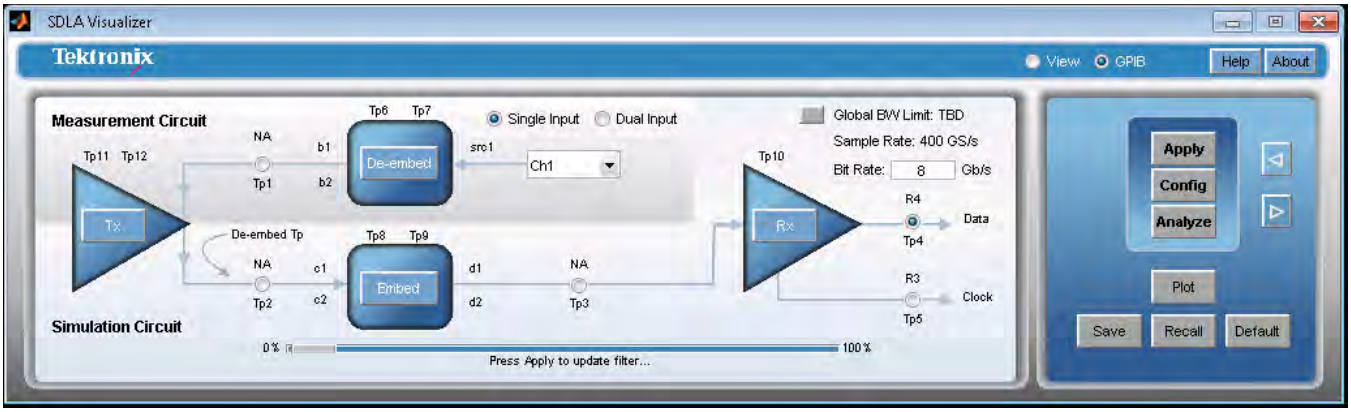
- *Running a Test: Recommended Order*

Example of de-embedding cables

This example provides step-by-step instructions on how to de-embed a pair of cables. In this example, the transmitter impedance is assumed to be 50 Ohms. The scope Rx load is also assumed to be 50 Ohms. Each cable is represented by 2-port S-parameter models (one for each leg). The goal is to view the signal from the transmitter with the cable de-embedded, and the transmitter driving a 50 Ohm load.

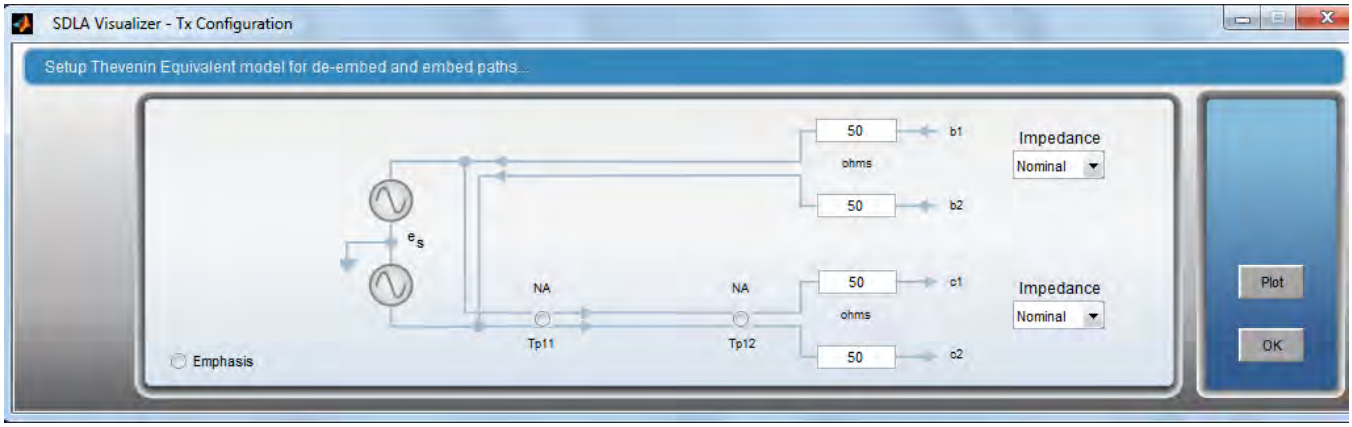
This example uses Single Input mode.

1. First, select the Single Input radio button on the Main Menu.



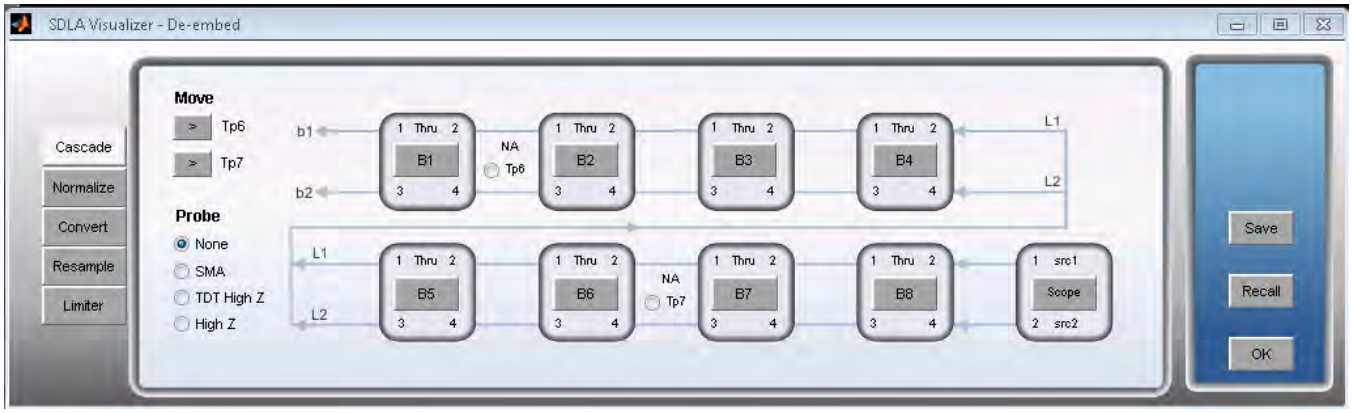
2. The next step is to define the Measurement Circuit model. This is made up of the transmitter source impedance, cable, and scope.

a. Press on **Tx** on the Main Menu to bring up the *Tx Configuration Menu*. On the top row, select **Nominal** in the Impedance drop-down list, and enter **50** Ohms in the **b1** and **b2** text boxes. Press **OK.**

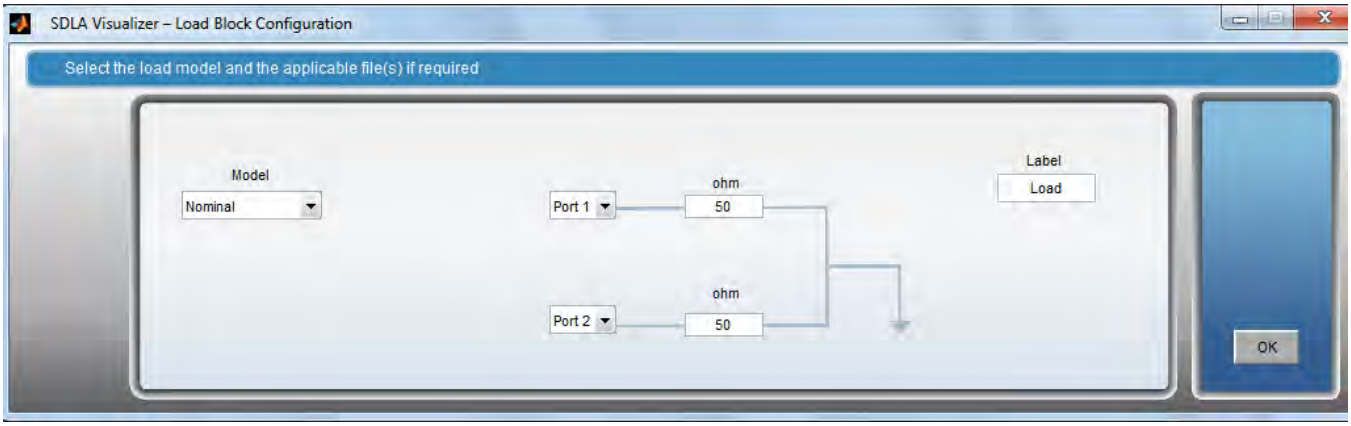


NOTE. *The impedance value should model the actual impedance of the transmitter. This can be done using either actual S-parameters or nominal values. It is important that this value match the transmitter impedance for the most accurate de-embedding.*

b. Press **De-embed** on the Main Menu to bring up the *De-embed Menu*. Select the **Cascade** Tab.

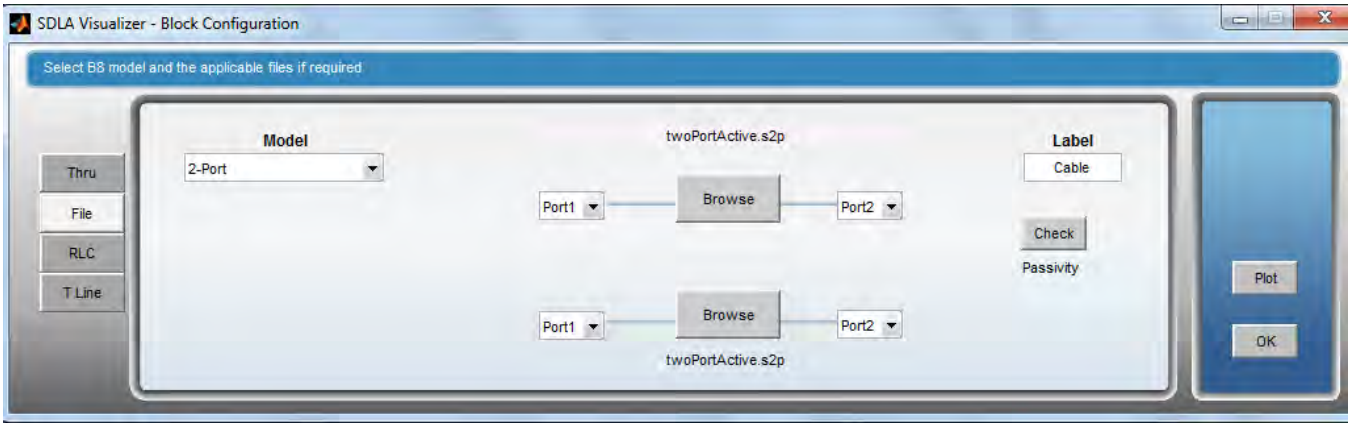


c. To model the input impedance of the scope, press on the last block of the cascade, which will be labeled **Scope**. This brings up the *Load Configuration menu*, shown below. Under “Model”, select **Nominal**. Enter **50** Ohm for the impedance on both ports. Press **OK**.



d. Press on block **B8**. This brings up the *Block Configuration Menu*, shown below. On the **File** tab, under “Model”, select **2-Port**. Press the upper **Browse** button and select “twoPortActive.s2p” from the drop-down menu. Do the same with the lower **Browse** button. Under **Label**, change “B8” to “Cable”. Press **Plot** to see the S-parameter plot of both the cables. To check the port assignments and passivity of the S-parameter files, press **Check.** Press **OK**.

NOTE. *If your cable model is represented as a 4-port S-parameter block, you may select 4-Port as the model type and load an .s4p file.*

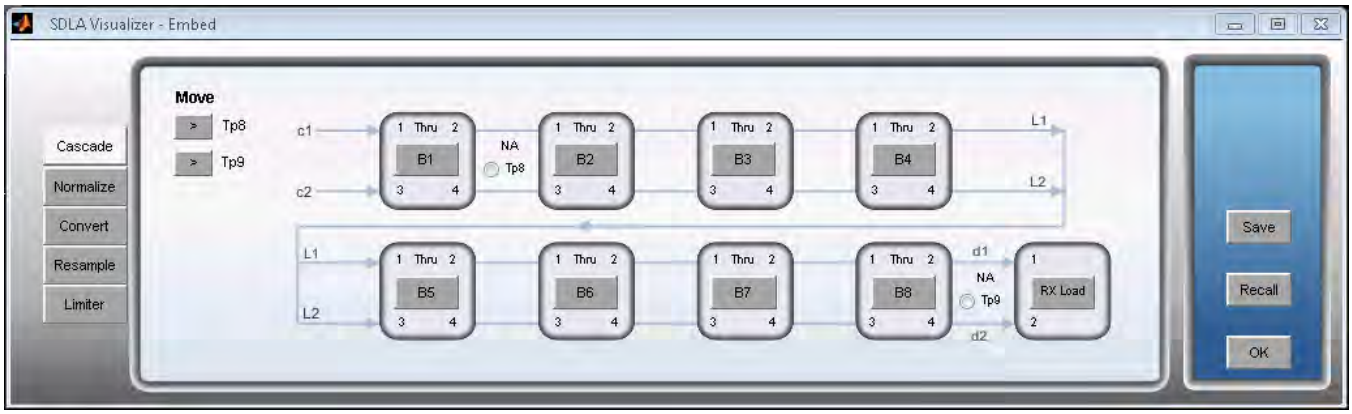


3. The next step is to define the Simulation Circuit model. In this example, we will drive the transmitted signal into an ideal 50 Ohm load.

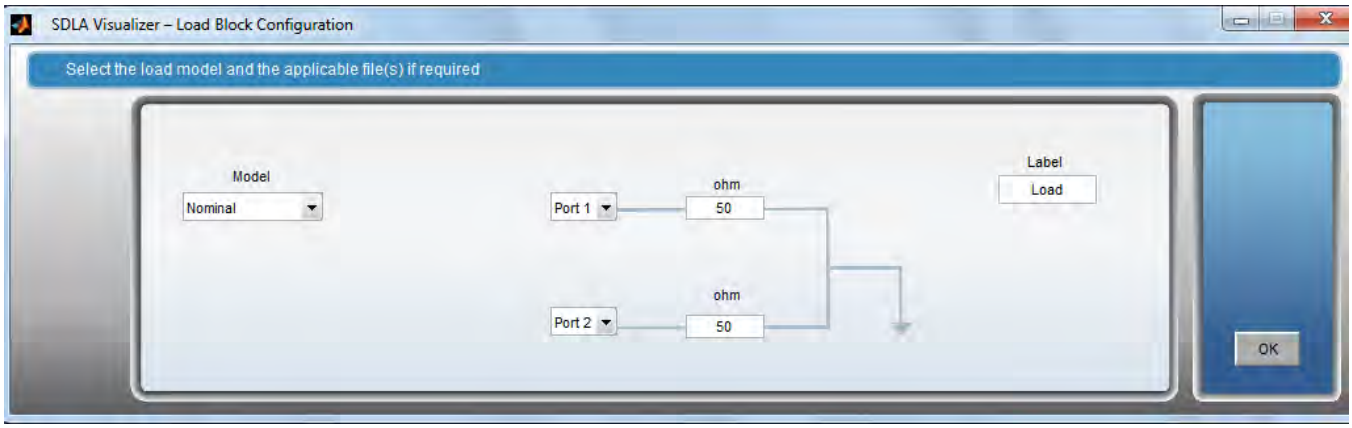
a. Press **Tx** on the Main Menu once again, which brings up the Tx Configuration Menu (shown in step 1a above). On the bottom row, select **Nominal** in the Impedance drop-down list, and enter **50** Ohms in the **c1** and **c2** text boxes. Press **OK.**

NOTE. *The impedance value should match the value in the de-embed path.*

b. Press **Embed** on the Main Menu, which brings up the Embed Menu, with the **Cascade** Tab displayed. Press on the last block of the cascade, which will be labeled **RX Load**.



c. This brings up the *Load Configuration menu*, shown below. Under "Model", select **Nominal**. Enter **50** Ohms for the impedance on both ports. Press **OK**.



d. Leave all the other blocks in the Embed cascade diagram set to Thru, since only the ideal load block will be used for this example. Press **OK.**

4. Once the Measurement Circuit and Simulation Circuit models have been defined, the desired test points can be enabled. (For more information on test points, see *Understanding Test Points*.) Since the goal is to observe the signal at the output of the transmitter driving an ideal 50 Ohm load, we want to enable **Tp2**.

NOTE. *It may seem that Tp1 will provide the de-embedded signal, but Tp1 will show the signal at the output of the Tx with the loading of the Measurement Circuit. Since we want to completely remove the effects of the Measurement Circuit, Tp2 is the correct test point.*

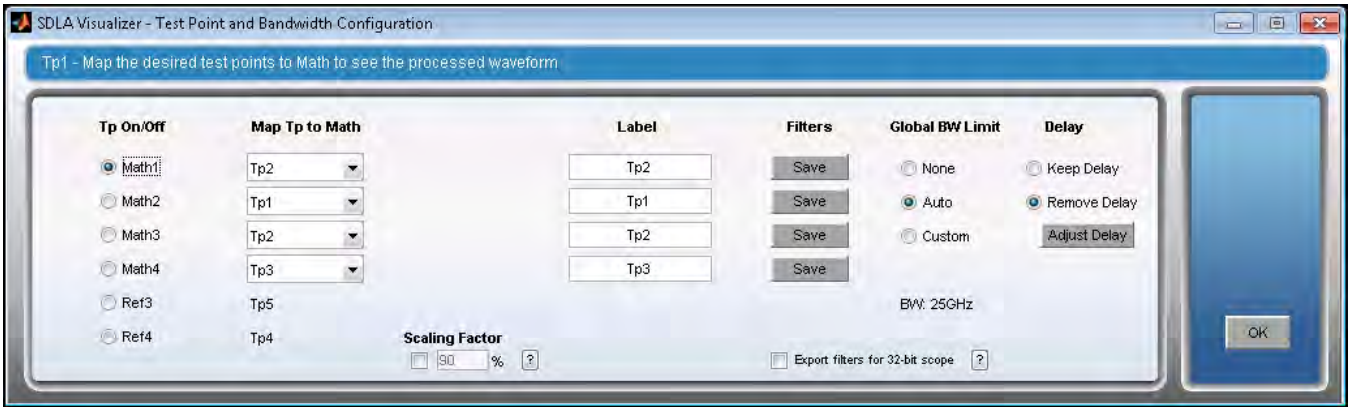
---

   a. Press on **Tp2** on the Main Menu, which brings up the Test Point and Bandwidth Menu.

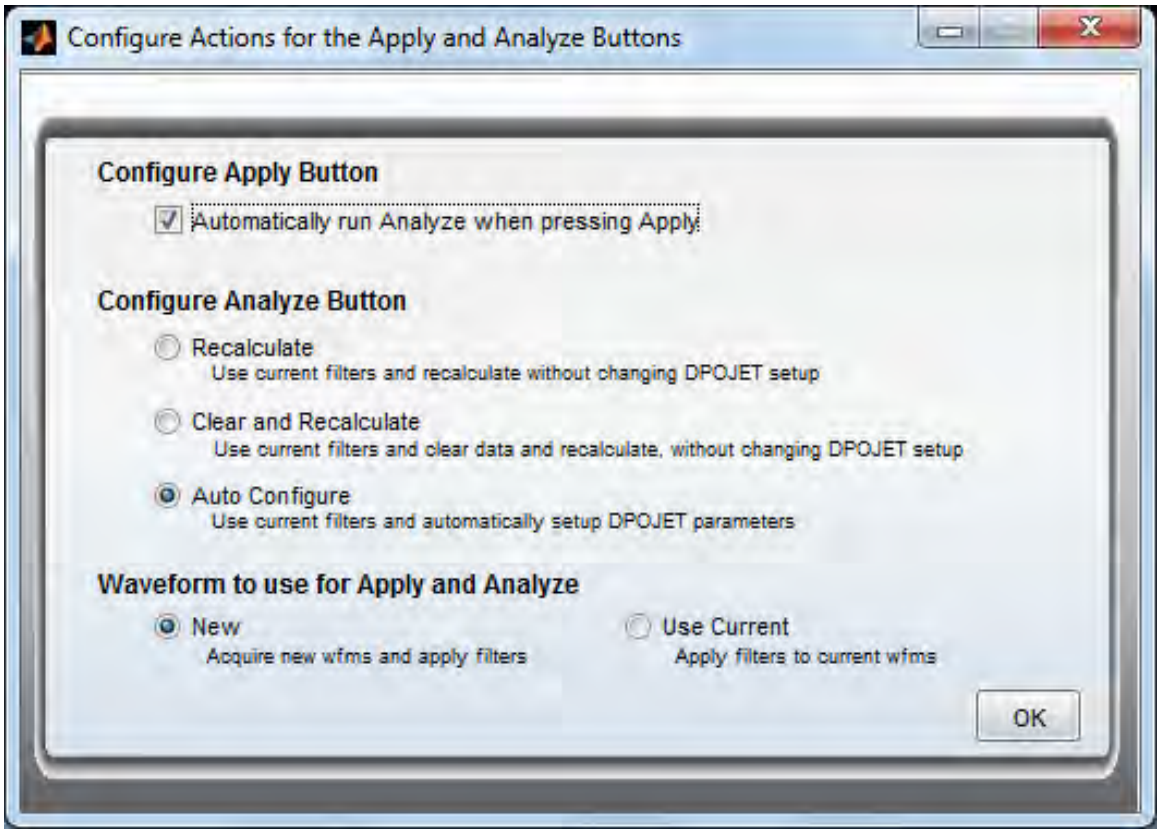
   b. Under **Map Tp to Math**, select **Tp2: Main** in the first drop-down list.

   c. Under **Tp On/Off**, select the radio button next to **Math1** Math1 will be mapped to Tp2, so that when the model is finally applied, the filter will be configured automatically in Math1.

   d. Press **OK**.



5. (RT only) Now, configure the system so that when you press **Apply** on the Main Menu, you will also automatically run DPOJET. On the Main Menu, press **Config**. On the menu that comes up, shown below, check the box that says **Automatically run Analyze when pressing Apply**. Under Configure Analyze Button, select **Auto Configure**. Press **OK**.



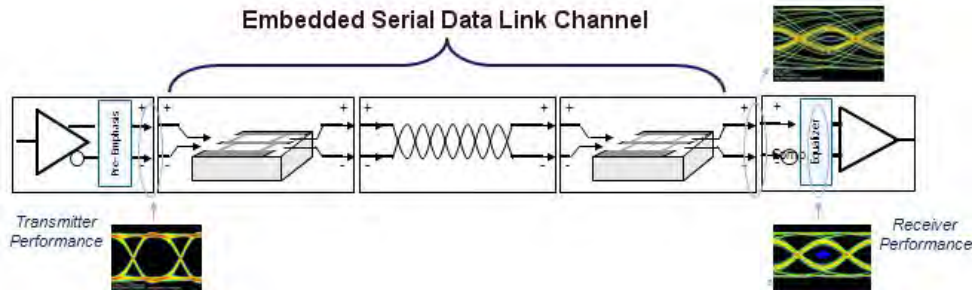
6. Now, process the models by pressing **Apply** on the Main Menu. This will compute the transfer function at **Tp2**. (RT only) The resulting waveform will be visible on the oscilloscope in Math 1. Since DPOJET was configured to run automatically, DPOJET will setup to measure TIE and plot the Eye Diagram at Tp2.
7. After SDLA Visualizer has finished processing, select **Plot** on the Main Menu to view the Phase, Magnitude, Impulse and Step response at Tp2.
8. In the upper right area of the Main Menu, observe the bandwidth setting. It may be necessary to fine-tune this based on the results, as de-embedding can amplify noise. For details on fine-tuning the bandwidth, see *Test Point and Bandwidth Manager*.

   Since cables typically have low attenuation, the auto-bandwidth may result in too wide of a bandwidth. If so, go to the Test Point and Bandwidth Manager by pressing on a test point button on the Main Menu. Under **Global Bandwidth Limit** select **Custom**, and set up the desired response.

Example of embedding a serial data link channel

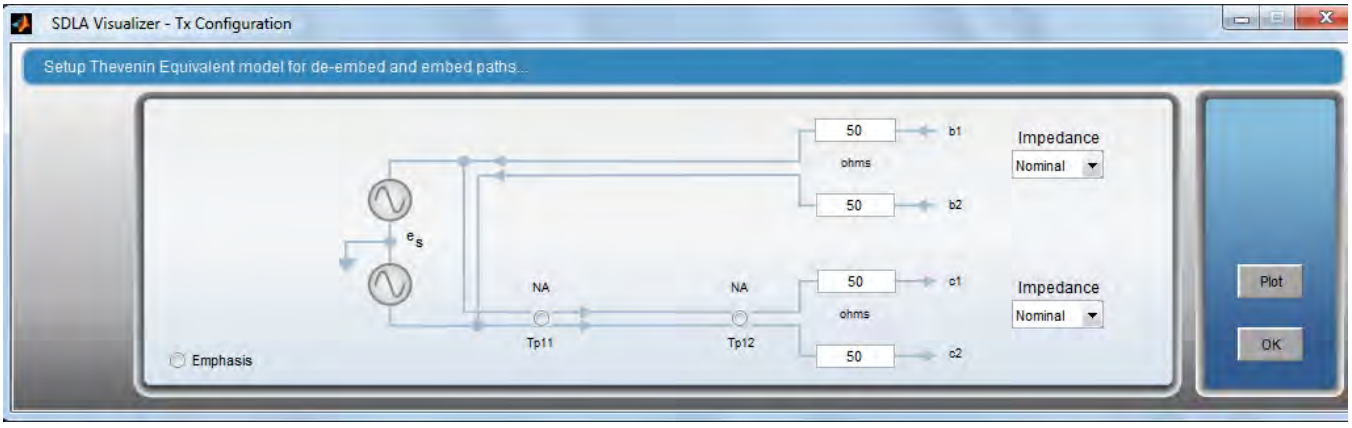
This example shows how to create and embed a model of a serial data link channel in order to simulate its effects upon the acquired signal from the DUT. In this case, the channel to be modeled consists of a twisted pair of cables, connectors and a printed circuit board.

This example uses Single Input mode.

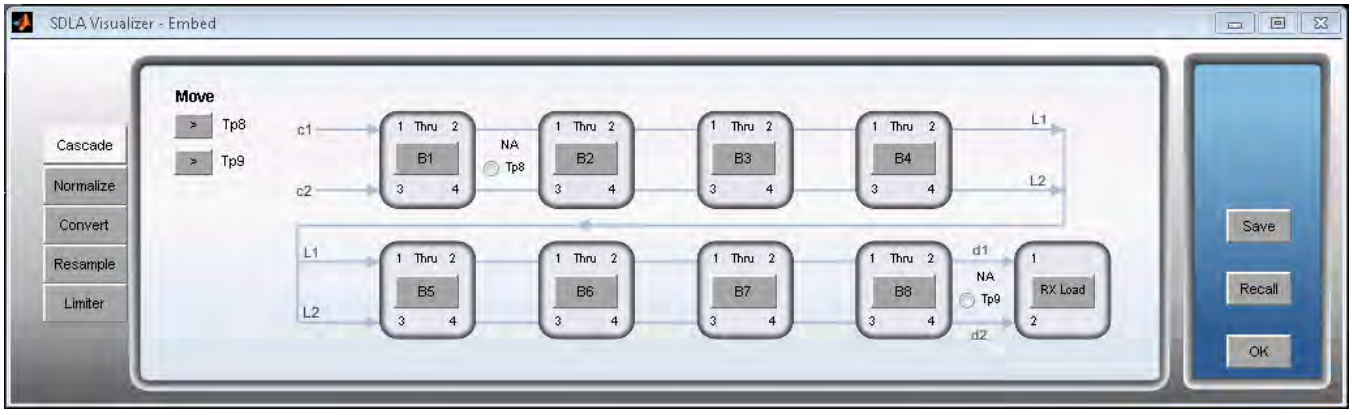


1. The first step is to define the Measurement Circuit model. Use Step 1 and 2 in the above *Example of De-embedding a Cable* as a guide for representing how the waveform was acquired.
2. Next, define the Simulation Circuit model.
   a. Press **Tx** on the Main Menu once again, which brings up the Tx Configuration Menu, shown below. On the bottom row, select **Nominal** in the Impedance drop-down list, and enter **50** Ohms in the **c1** and **c2** text boxes. The Tx source impedance for the embed path should be set the same as for the de-embed path. Press **OK.**

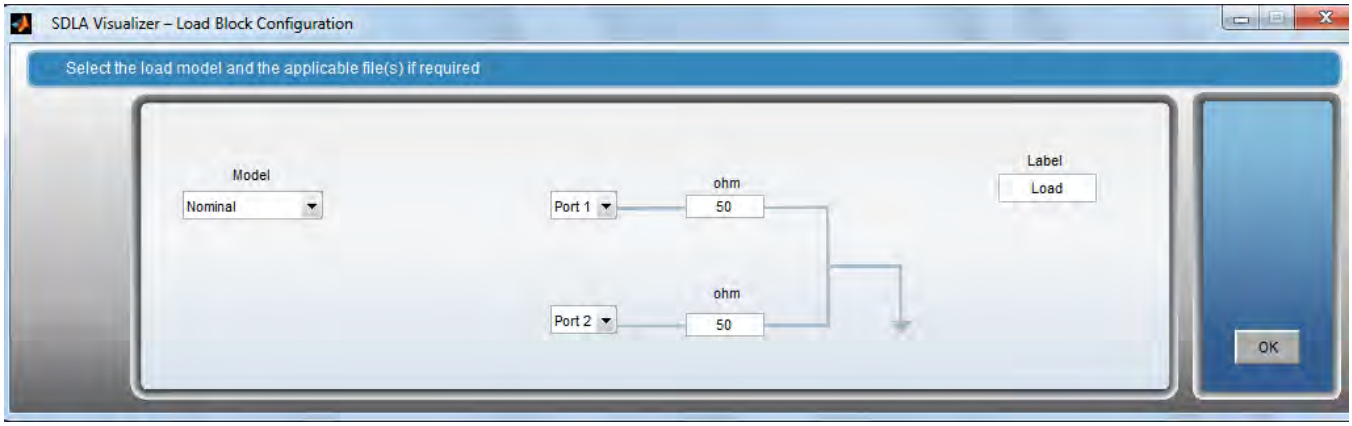
NOTE. *The impedance value should match the value that you would like to simulate. This could be the actual impedance of the transmitter, or another impedance value.*



b. Press **Embed** on the Main Menu, which brings up the Embed Menu. Select the **Cascade** Tab. Configure blocks to represent the PCB traces, connectors and twisted pair of cables using **B1**– **B8**.



c. Press on the last block of the cascade, which will be labeled **RX Load**. This brings up the *Load Configuration menu*, shown below. Under "Model", select **Nominal**. Enter **50** Ohms for the impedance on both ports. Press **OK**.



d. Optionally, configure the Rx Block by pressing **Rx** on the Main Menu.

3. Once the Measurement Circuit and Simulation Circuit models have been defined, the desired test points can be enabled. (For more information on test points, see *Understanding Test Points*.)

   a. Press on any test point on the Main Menu, which brings up the Test Point and Bandwidth Menu.

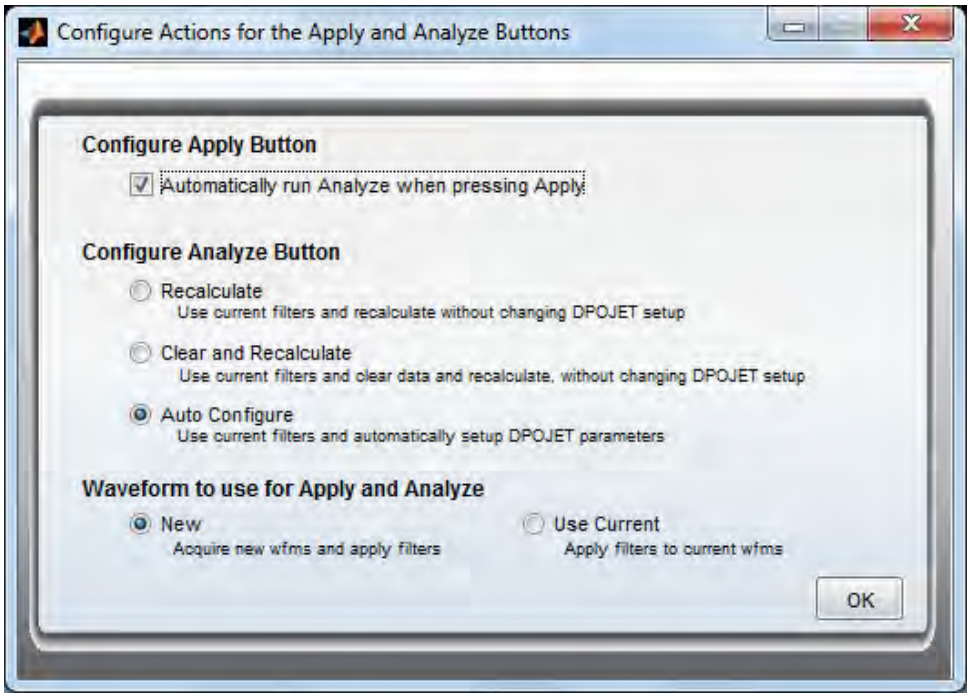
   b. Turn on, map and label the test points as appropriate. The test points in the Simulation path are: **Tp2, Tp3, Tp8, Tp9, Tp11** and **Tp12**. (If you have configured the Rx Block, those test points are **Tp4, Tp5** and **Tp10**.)

   c. Press **OK**.

4. (RT only) Now, configure the system so that when you press **Apply** on the Main Menu, you will also automatically run DPOJET.

   a. On the Main Menu, press **Config**.

   b. On the menu that comes up, shown below, check the box that says **Automatically run Analyze when pressing Apply**. Under Configure Analyze Button, select **Auto Configure**.



   c. Press **OK**.

5. (RT only) Now, process the models by pressing **Apply** on the Main Menu. This will compute the transfer functions at the configured test points. The resulting waveforms will be visible on the oscilloscope. Since DPOJET was configured to run automatically, DPOJET will setup and open. Observe the eye diagrams of the test points in the DPOJET plot window.

6. After SDLA Visualizer has finished processing, select **Plot** on the Main Menu to view the Phase, Magnitude, Impulse and Step response graphs.

Example of de-embedding a high impedance probe

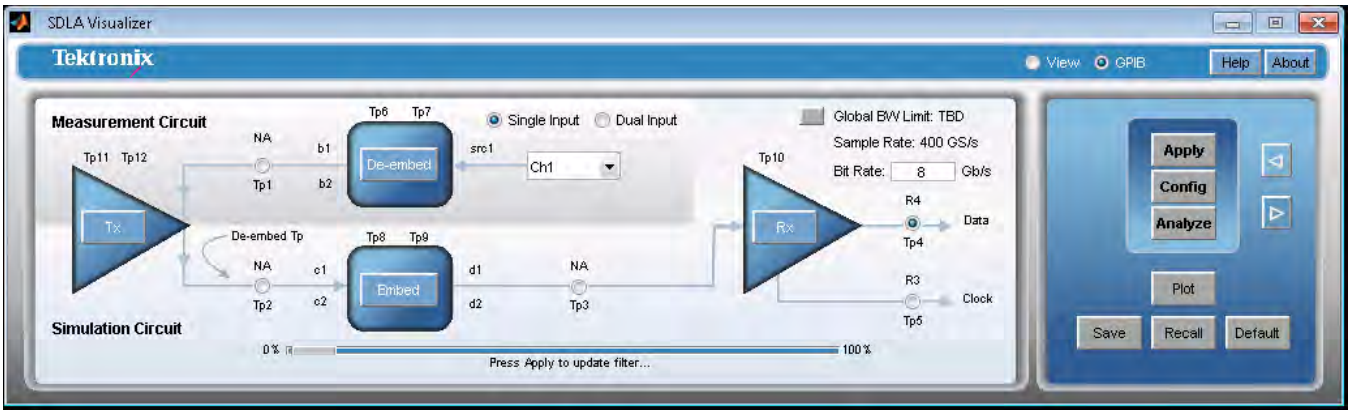
In this example,

- The user wants to use a high impedance probe to view a test point in an active system with a transmitter channel and receiver, while the probe is loading the system.
- The user also wants to view the same point in the system with the probe de-embedded and not loading the system.

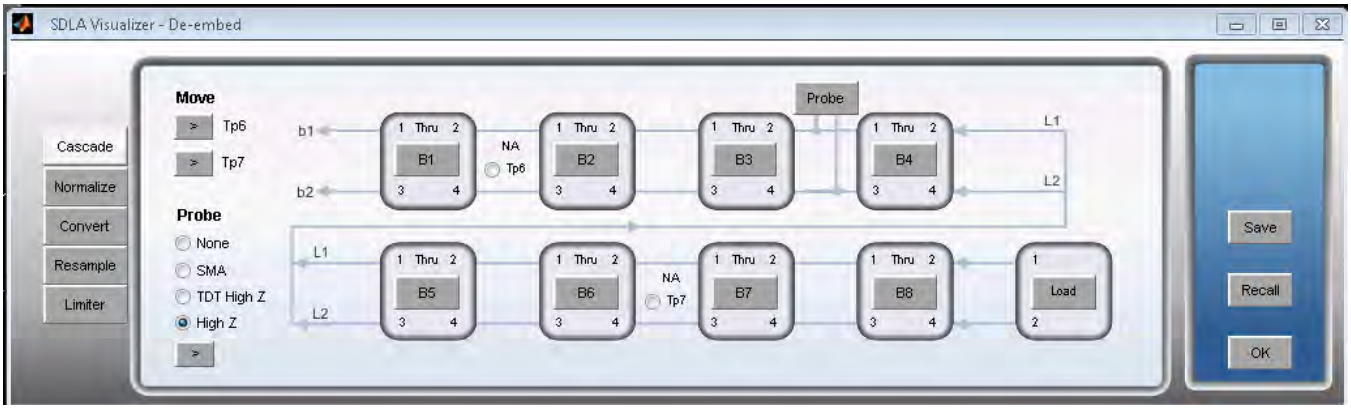
This example uses Single Input mode.

First, set up the Measurement Circuit (de-embed) path to include the high impedance probe in the circuit diagram:

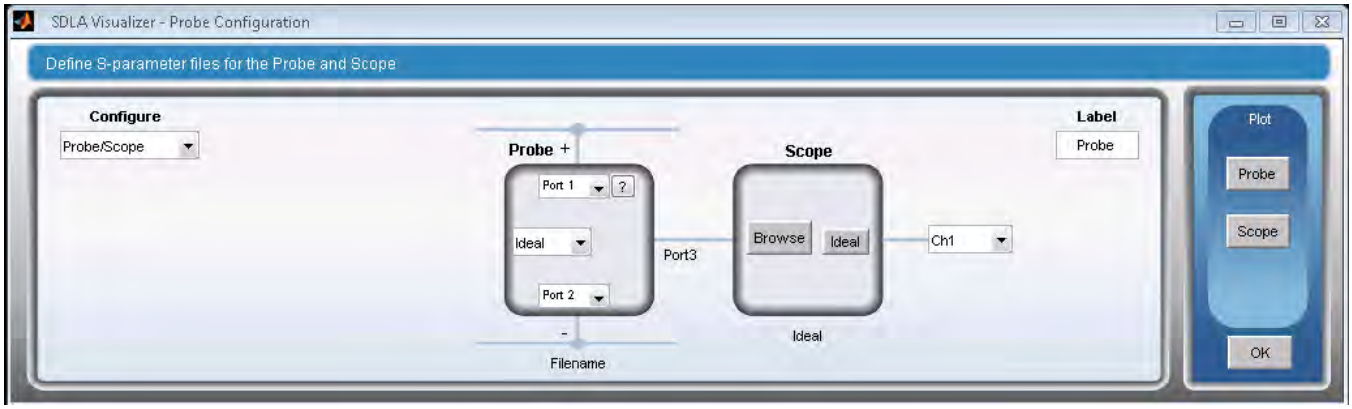
1. On the Main Menu, select the **Single Input** radio button. Then, press **De-embed.**



2. This brings up the De-embed Menu. Select the **High Z** radio button. This causes a **Probe** button to appear on the circuit diagram, as well as an arrow that lets you move the location of the probe on the diagram.

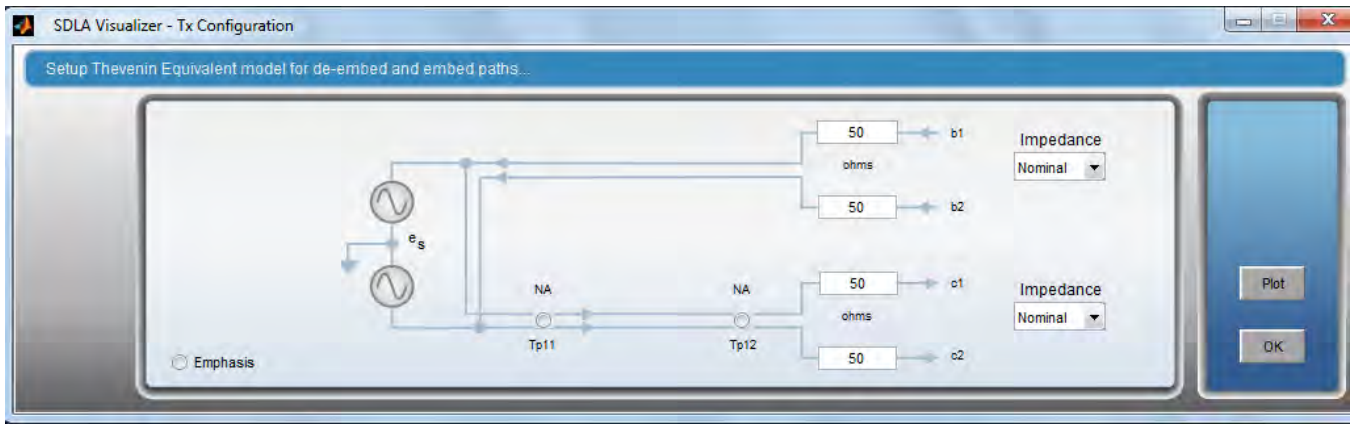


3. Press the **Probe** button. This brings up the Probe Configuration Menu:



4. In the **Probe** panel, select the correct probe model. Press **Load** to bring up the probe browse menu, and load the 3-port S-parameter file.
5. If you'd like to plot the probe S-parameters, under **Plot** on the right side, press **Probe**. Press **OK**.
6. On the De-embed Menu, the circuit diagram shows the probe in the circuit, and the test points in that circuit are with the probe loading the circuit. This includes **Tp1, Tp6**, and **Tp7**. In other words, all test points in SDLA produce waveforms according to what the circuit diagram shows. If the probe is shown in the circuit, then it is loading the circuit. (To see the circuit and test points *without* the probe loading it, press **Embed Block** on the Main Menu and recreate the same circuit, where there is no probe.)
7. For the blocks on each side of the probe connection point, load S-parameter files or create models of RLC and/or transmission line to represent the system that the probe is connected to.

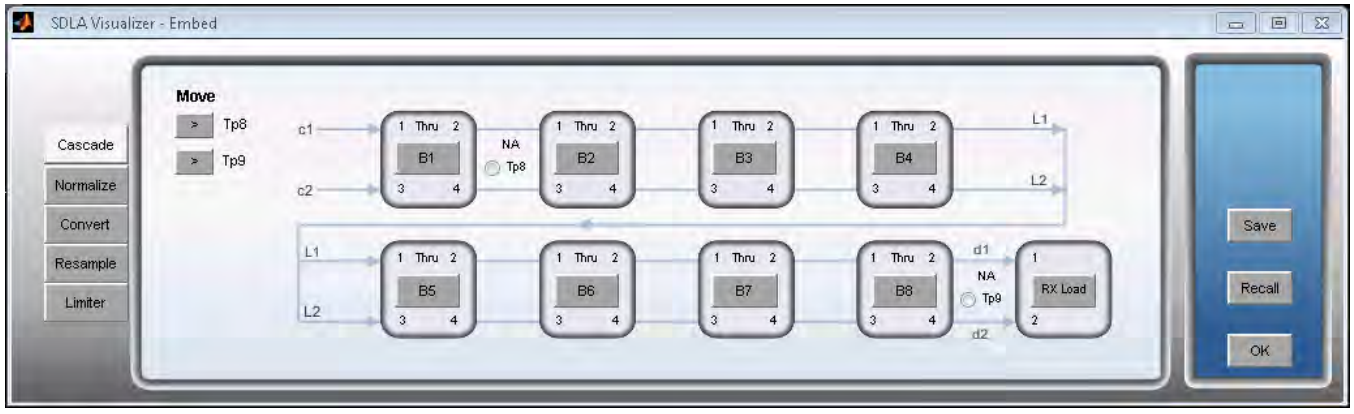
8. From the Main Menu, press **Tx**. The Tx Configuration Menu comes up:



9. Set up the Tx Block to best represent the DUT transmitter source impedance that the system is connected to. Press **OK.**

Next, set up the Simulation Circuit with the same circuit blocks and parameters that were used to set up the Measurement Circuit, but without the probe, following the steps in the diagram below.

1. From the Main Menu, press **Tx**. The Tx Configuration Menu comes up once again (see above).
2. Set up the Tx Block as above. Press **OK.**
3. Press **Embed** in the Main Menu. This brings up the Embed Menu.



4. Configure the cascade the same way as the Measurement Circuit side, but without the probe (note that no probe options are available on the Embed menu). Press **OK.**

The test points in the Simulation Circuit side now represent the system *with no probe loading*. These include **Tp2, Tp3, Tp8, Tp9, Tp11,** and **Tp12.** The test points in the measurement circuit remain with the probe loading the circuit.

Now, return to the Main Menu. Open up the Test Point and Bandwidth Manager by pressing on any test point. Turn on and map the desired test points to math waveforms.

Return to the Main Menu. Press **Apply**. This will compute the transfer functions for the enabled test points. The resulting waveforms will be visible on the oscilloscope graticule as math waveforms according to how you mapped them.

Example of de-embedding significant reflections with dual input waveforms

By using SDLA Visualizer, an accurate de-embedding result may be obtained on a real-time oscilloscope, even when the components have severe gain variations.

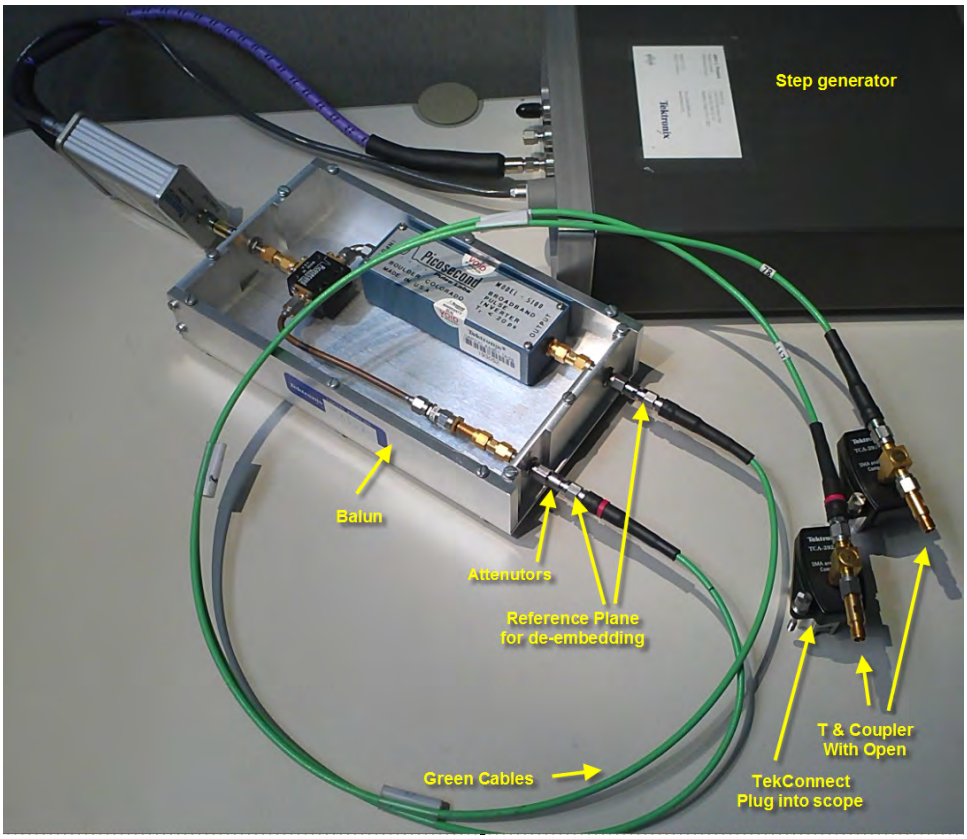
The purpose of this example is to show:

- How to set up SDLA Visualizer to de-embed significant reflections coming from an unmatched termination at the end of a pair of 38 inch cables.
- How SDLA test points can be used to represent the generator reference plane with the measurement circuit load. In this case, **Tp1** shows the output of the generator with the measurement system loading it.
- How test points can represent the generator reference plane with the ideal load, thus producing a much cleaner waveform with no observable reflections. In this case, **Tp2** shows the output of the generator terminated by an ideal 50 Ohms.

The acquisitions are averaged in order to reduce the noise from the boost, and a repetitive step function signal is used.

Equipment Setup

In the image below, a step generator is driving a balun to provide a differential step signal. Two 5X attenuators are connected to the two outputs of the balun where the green cables are connected. These ensure minimum reflections from the generator at the reference plane for de-embedding. In order to provide a large reflection for the purpose of this example, the opposite ends of the green cables are each connected to a T and coupler combination.



Below, the outputs of the T couplers are connected to the CH1 and CH2 inputs of the oscilloscope:

In order to provide a set of S-parameters that SDLA Visualizer modeling blocks can use to create real-time waveforms, the 2-port S-parameters for each cable and for each T coupler combination were measured on a VNA.

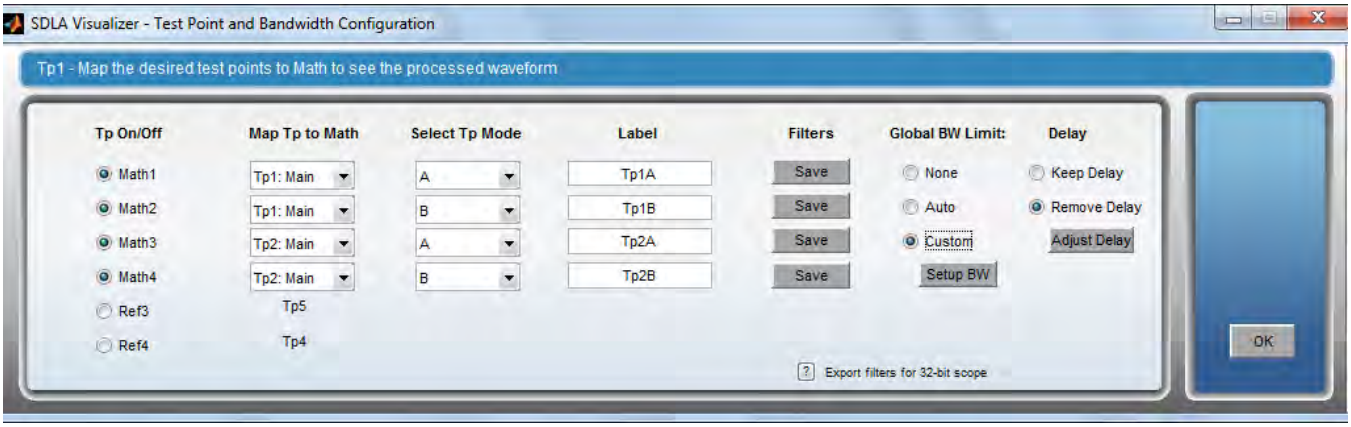
The T coupler with an open circuit is treated as a single 2-port element, with port 1 where the green cable is connected, and port 2 where the oscilloscope is connected. The open circuit port is simply part of the device characteristic. In this example, the oscilloscope and the generator reference plane impedance are assumed to be ideal 50 Ohms.

Setting Up SDLA Visualizer

First, configure the test points:

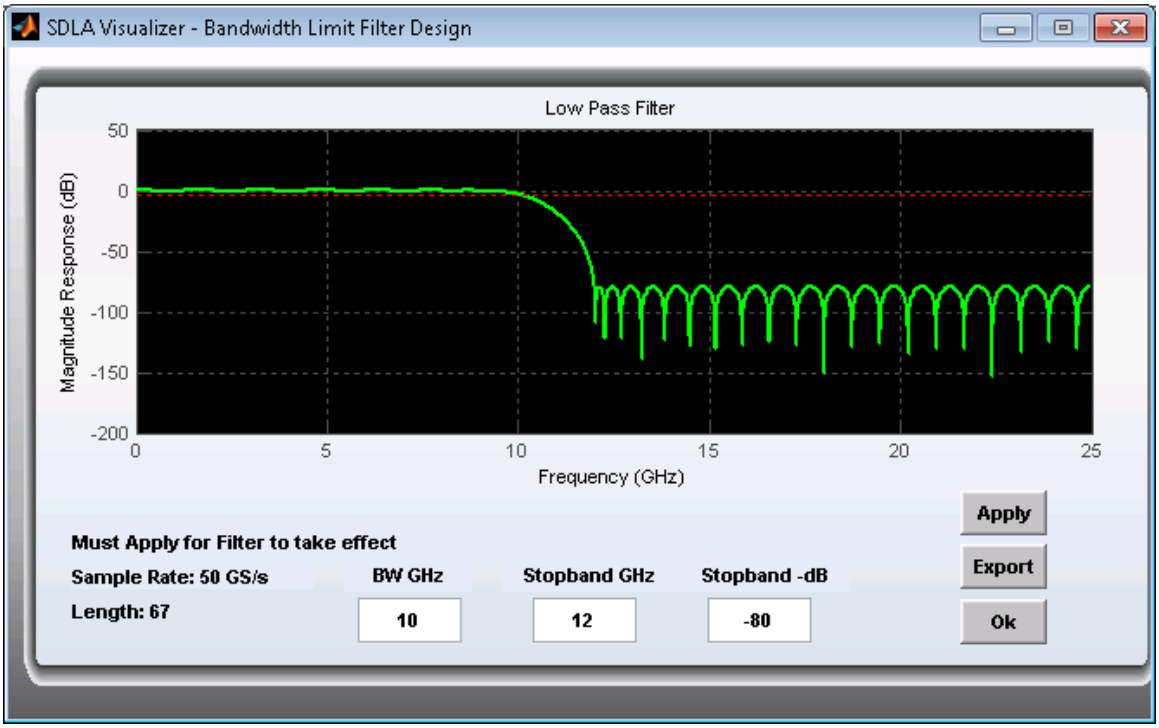
1. On the SDLA Main Menu, select **Dual Input** mode. Press a Tp button to bring up the **Test Point and Bandwidth Manager.**
2. Select all four test points to be on (Math1, Math2, Math3, and Math4).
3. Map **Tp1** to Math1 and to Math2. Tp1 is the output of the generator with cables and T and scope loading it. Select **Math1** to be the A line of the differential test point. Select **Math2** to be the B line of the differential test point.

4. Map **Tp2** to Math3 and Math4. Tp2 is the output of the generator with ideal 50 ohms loading it. Select **Math3** to be the A line of the differential test point. Select **Math4** to be the B line of the differential test point.



Next, configure the bandwidth limit:

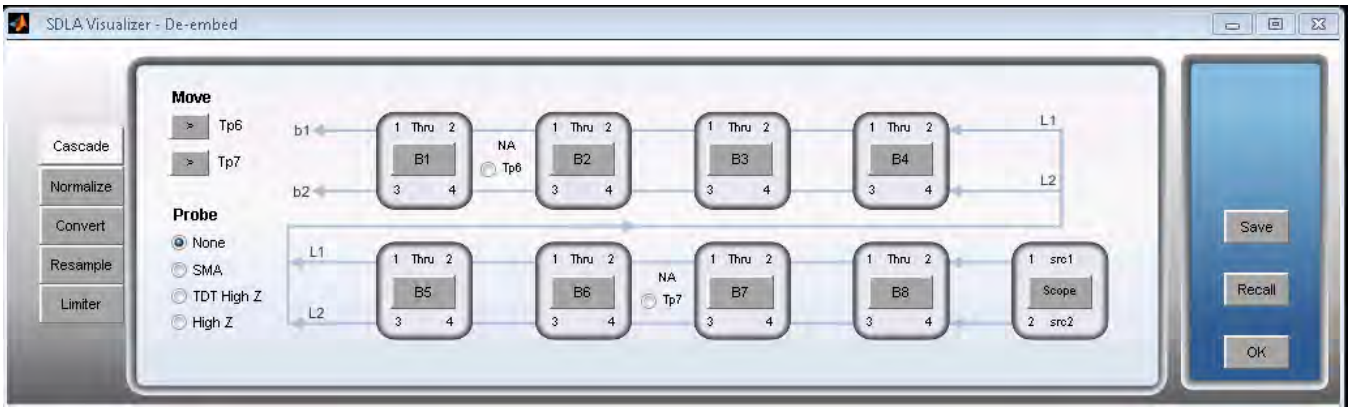
1. On the Test Point and Bandwidth Manager, under **Global Bandwidth Limit**, select **Custom** (shown above).
2. On the resulting **Bandwidth Limit Filter Design** menu (shown below), set **BW GHz** to 10.



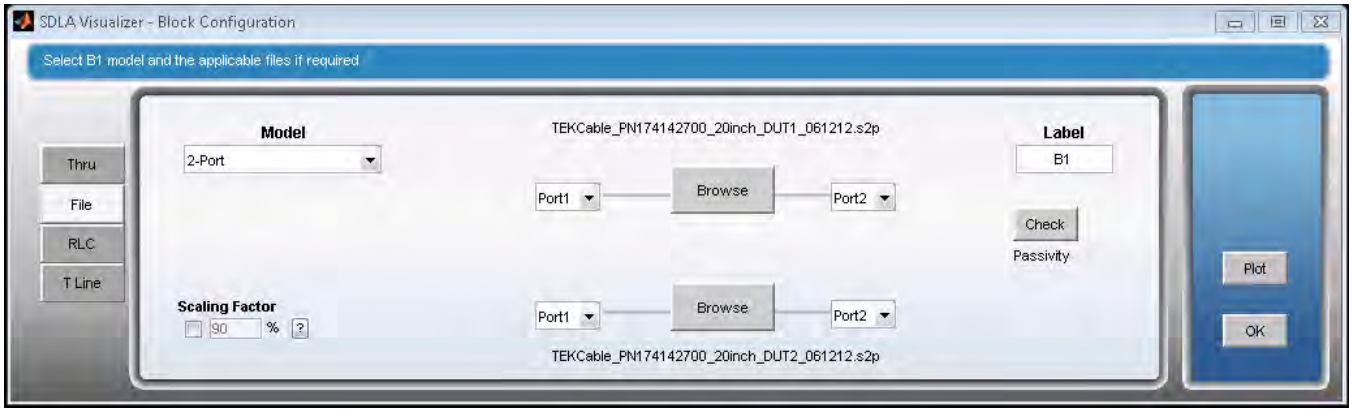
3. Set **Stopband GHz** attenuation to 12.
4. Set **Stopband -dB** to -80.
5. Press **Apply**. This saves the BW limit filter for the simulation.
6. Press **Close** to return to the Test Point and Bandwidth Manager. Under **Delay**, select **Keep Delay**.

Now, configure the De-embed Block:

1. In the SDLA Main Menu, press **De-embed**. This opens the De-embed Menu shown below.



2. Under **Probe**, select **None**.
3. In the cascade diagram, press the first cascade block (**B1)** to open up the **Block Configuration Menu** for B1, shown below. Select the **File** tab at the left.

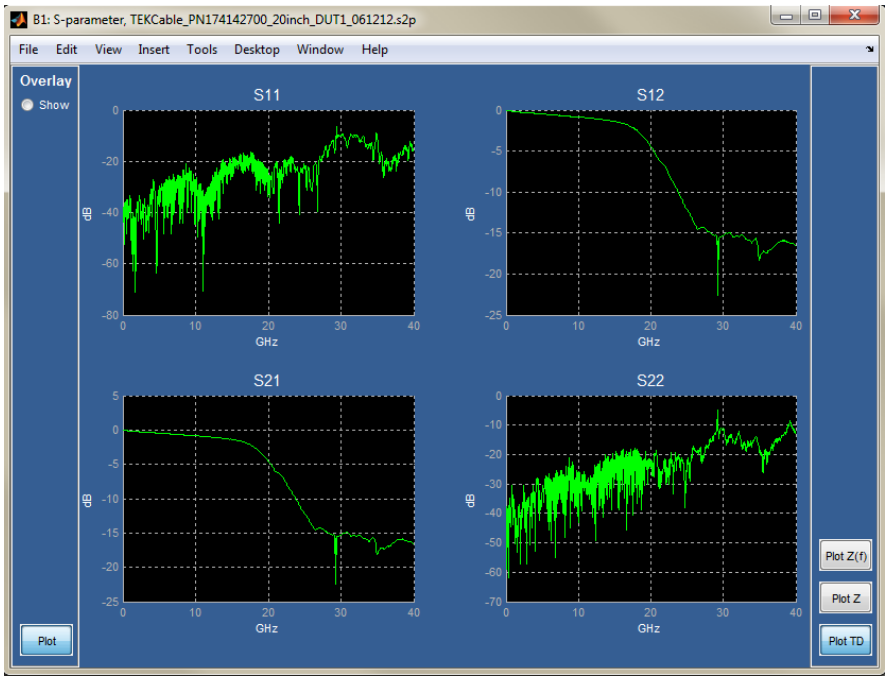


4. Under **Model**, select **2-port.**
5. Press the upper **Browse** button to load a 2-port S-parameter file for one of the cables.

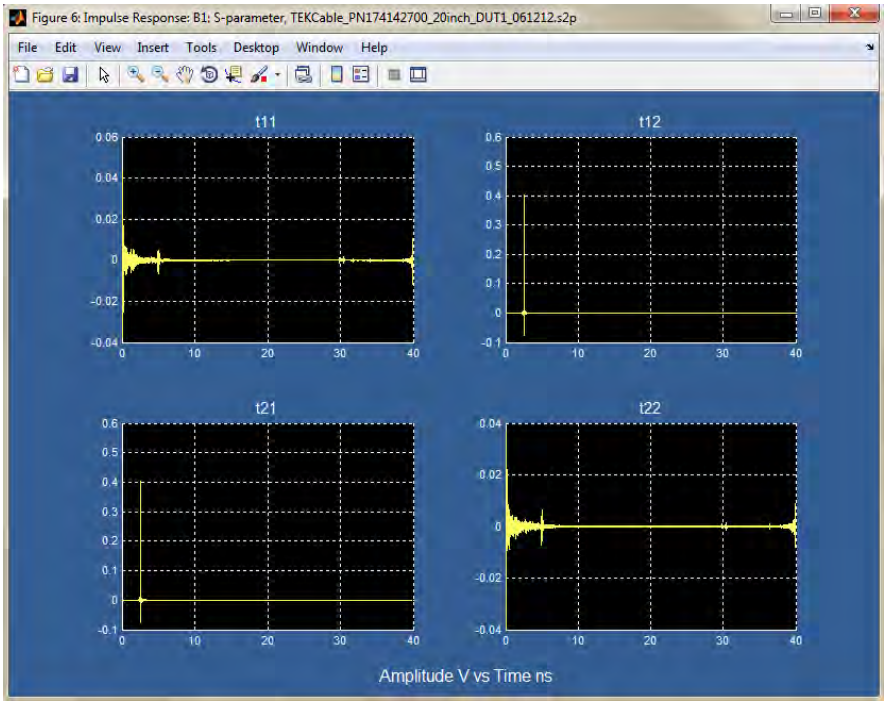
6. Press the lower **Browse** button to load a 2-port S-parameter file for the other cable.
7. Edit the block label to say “cables”.

Next, view the S-parameter plots for the cables:

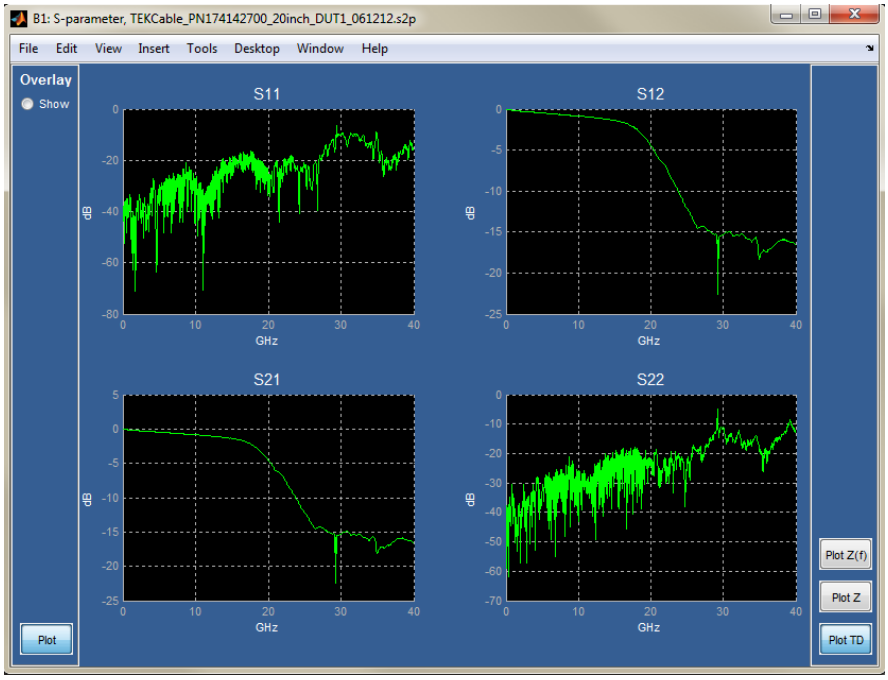
1. Press the **Plot** button to bring up the cable S-parameter plots that will appear in two windows. One cable is shown below:



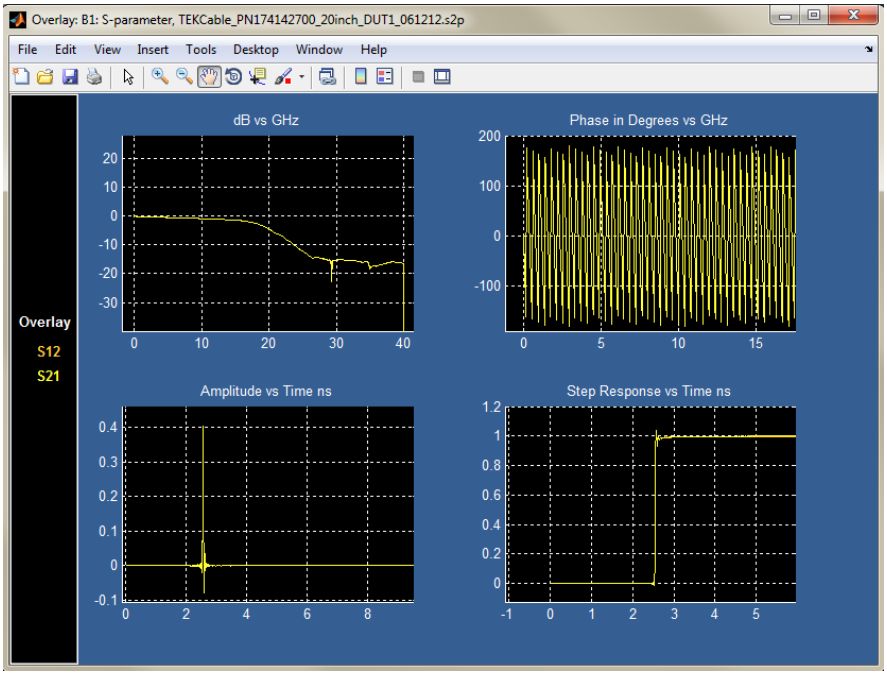
2. Press the **Plot TD** button in the S-parameter plot menu to open another window, shown below, containing the time domain plots for each S-parameter:



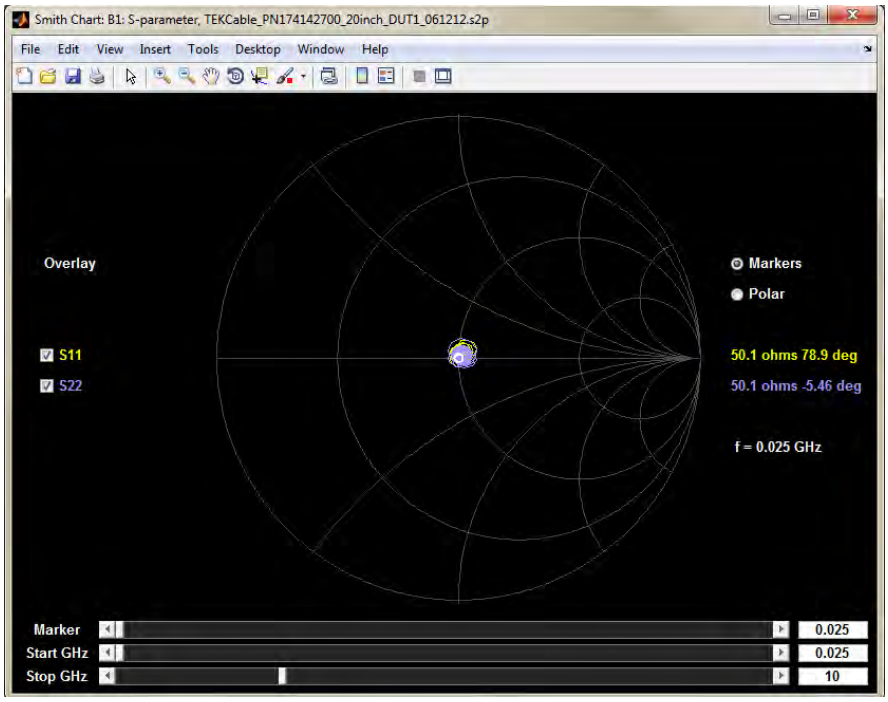
3. Return to the main S-parameter Plot window, shown below. Select the Overlay **Show** radio button. A set of check boxes appears that allow any of the S-parameters to be selected for the overlay plot.



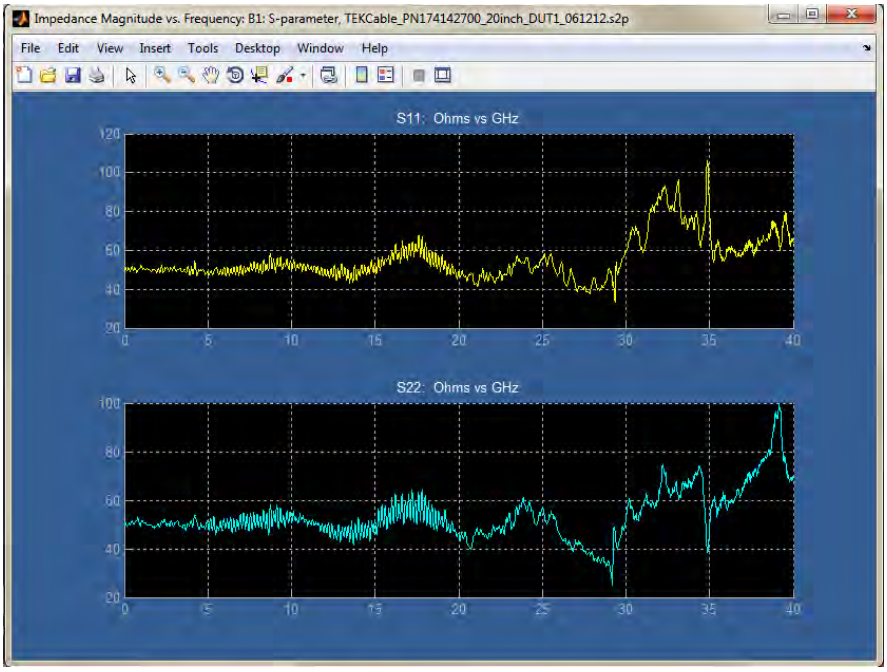
4. At the bottom of the Overlay panel, select **Plot**. This brings up another window, shown below, that contains the overlaid plots. These show magnitude, phase, impulse and step response for the various S-parameters:



5. To view a Smith Chart, return again to the main S-parameter Plot window, and press **Plot Z** on the right. Another window will open, shown below, that contains a Smith chart showing each reflection coefficient to view the impedance for one of the green cables:

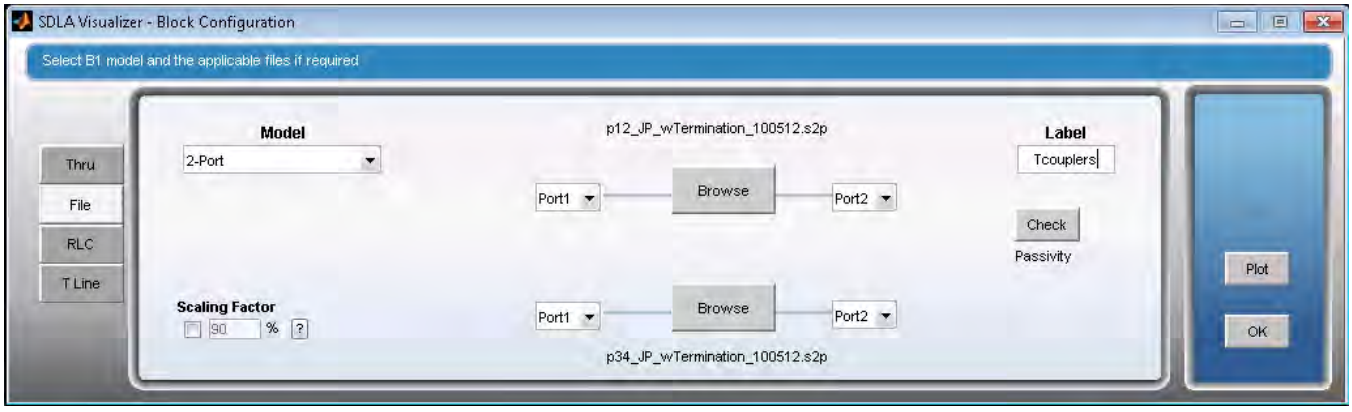


6. To view a chart of the magnitude of the impedance into each port, return to the main S-parameter Plot window, and press the **Plot Z(f)** button on the right. This opens another window, shown below.



Now, set up the block model for the T and coupler circuits:

1. Now, return to the De-embed Menu and set up the second block in the cascade diagram, **B2**, to represent the T and coupler circuits, as shown below:

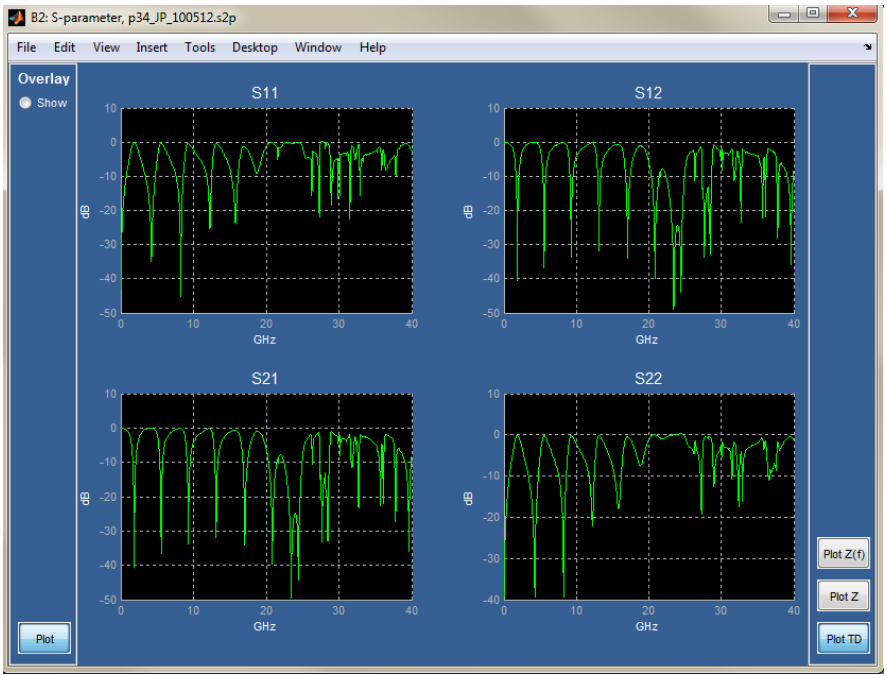


2. Select the **File** tab at the left.
3. Under **Model**, select **2-port.**
4. Press the upper **Browse** button to load a 2-port S-parameter file for one of the combined T and coupler components.

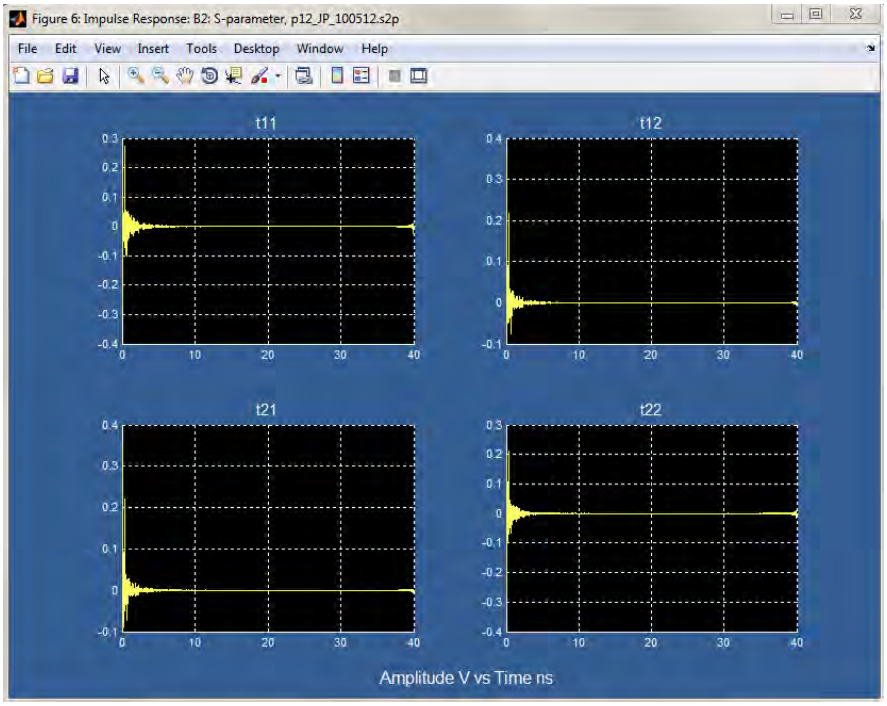
5. Press the lower **Browse** button to load a 2-port S-parameter file for the other combination of T and coupler.
6. Edit the block label to say “T coupler.”

Next, view the plots for the T and coupler combination:

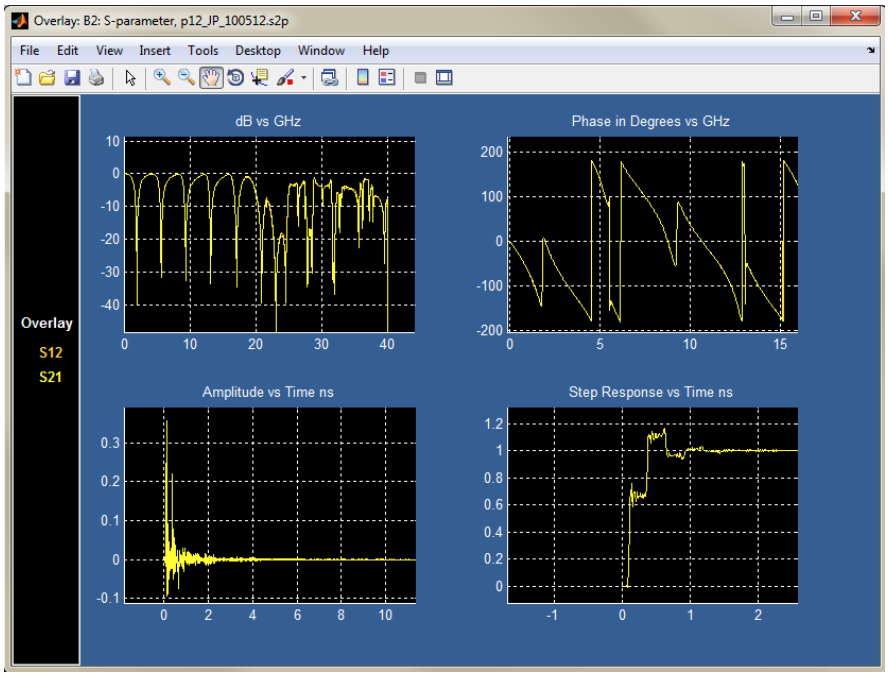
1. Press the **Plot** button. This brings up the main S-parameter Plot window, shown below. Observe that the S21 of the T coupler has some deep nulls of -30 to -40 dB. De-embedding these will require significant gain in the transfer function. Gain will cause a boost in noise at those frequencies. In this example, the oscilloscope should be put into average mode in order remove the excessive noise.



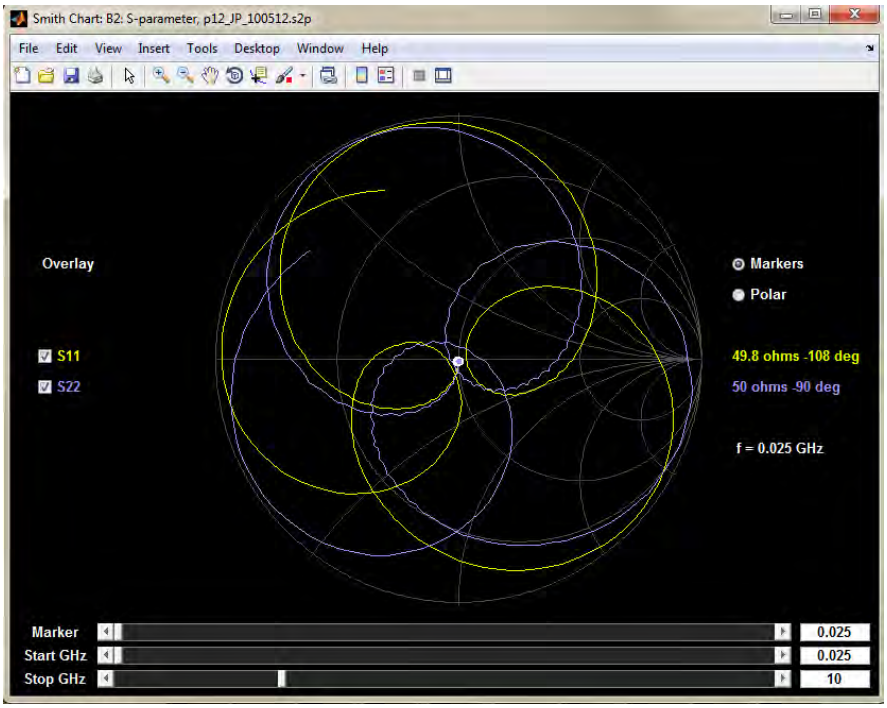
2. The time domain step response for the T and coupler combination, shown below, shows the reflection characteristic response that will be observed on the waveforms acquired on the oscilloscope:



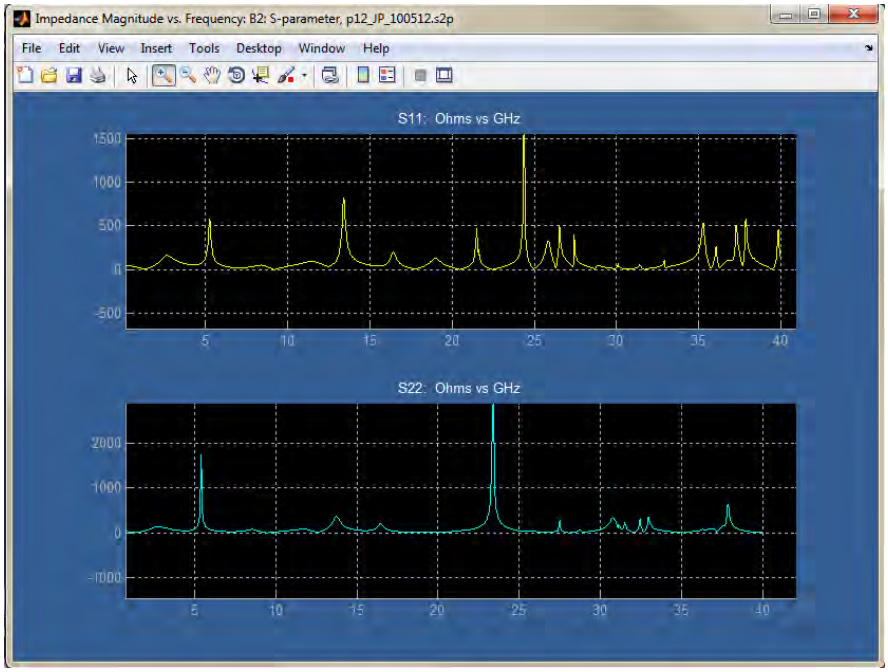
3. The **Overlay** plots for the T and coupler combination are shown below. The step response for S21 is shown in the lower right corner. This general response shape can be seen on the step response edges of the acquired waveform, because this discontinuity in impedance is very close to the input port of the oscilloscope.



1. The reflection coefficients, **s11** and **s22,** and the resulting impedance for the T coupler are shown on the Smith Chart below. Note that the range is over a large percentage of the chart. This makes for a challenging de-embed operation, given the 8-bit resolution of the scope and the noise within the scope. Averaging will help with these issues.



2. The image below shows the Impedance magnitude vs. frequency plot for the T and coupler combination:



Now, apply the models: Go to the SDLA Main Menu and press **Apply**. This will cause SDLA to generate transfer functions based on the S-parameter models of the system. SDLA does this by taking into account all of the S-parameters throughout the system. In other words, cross-coupling, reflections, and transmission terms are all part of the transfer function. These transfer functions represent the filters applied to the acquired waveforms from the oscilloscope to obtain the test point waveforms defined in SDLA.

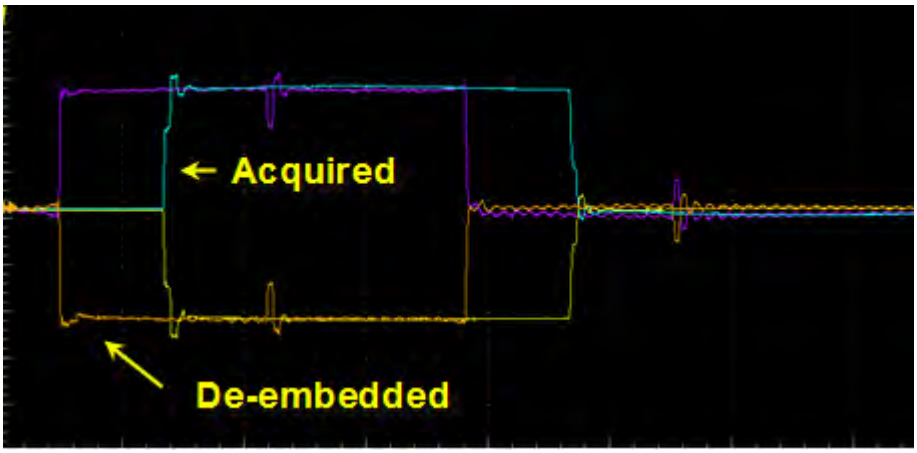
Next, view the live waveforms on the oscilloscope display:

Once the filters for each test point transfer function are computed, they are automatically loaded into the oscilloscope math menu, and live waveforms appear on the scope display.

1. The image below shows the **Tp1** waveforms, which are the outputs of the Tx model with the cables and T coupler combination still loading the step generator. The waveforms acquired on the scope are in yellow and Cyan. The waveforms de-embedded to reference plane with cables still loading that point are shown in purple and orange.

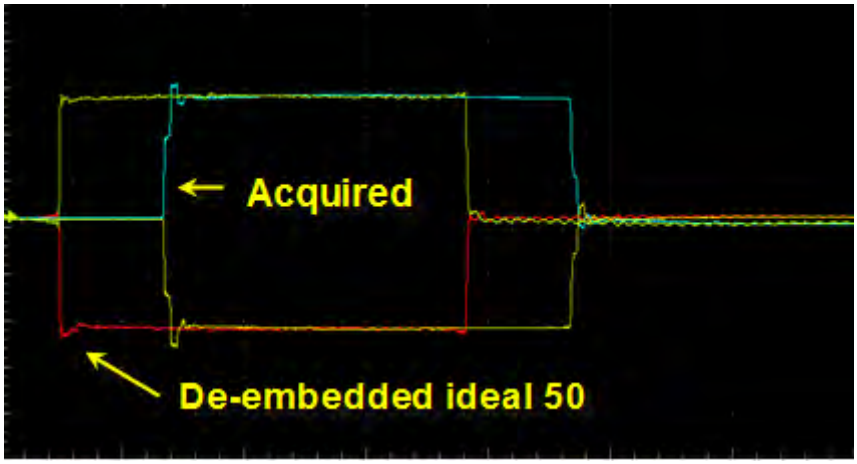
   The resulting reflections and time delays are correctly represented in the de-embedded waveforms. These are the A and B signals that were acquired directly on the oscilloscope at the output from the T couplers.

   The reflections due to the open circuit of the coupler can be seen on the acquired waveform at the rising and falling edges where the steps entered the oscilloscope (yellow and cyan). On the de-embedded waveforms (purple and orange), the rising and falling edges have the reflections removed, and the shape of the pulse is as expected at the reference plane into the cables. There is a delay of approximately 4.1 ns through the cable. At 8.2 ns, the round trip time of 8.2 ns, the reflection arrives back at the reference plane input to the green cables. Also, when the pulses (purple and orange) go back to zero, another round trip reflection off the input side to the scope arrives back to the reference plane 8.2 ns later.



2. The image below shows **Tp2**, which in SDLA is at the output of the Tx model with the embed side of the system loading the Tx model. In this example, Tp2 provides the waveforms with the measured cables and components removed, and the step generator reference plane terminated in an ideal 50 ohms. All blocks were left set to default Thru models, and the load was default 50 ohms.

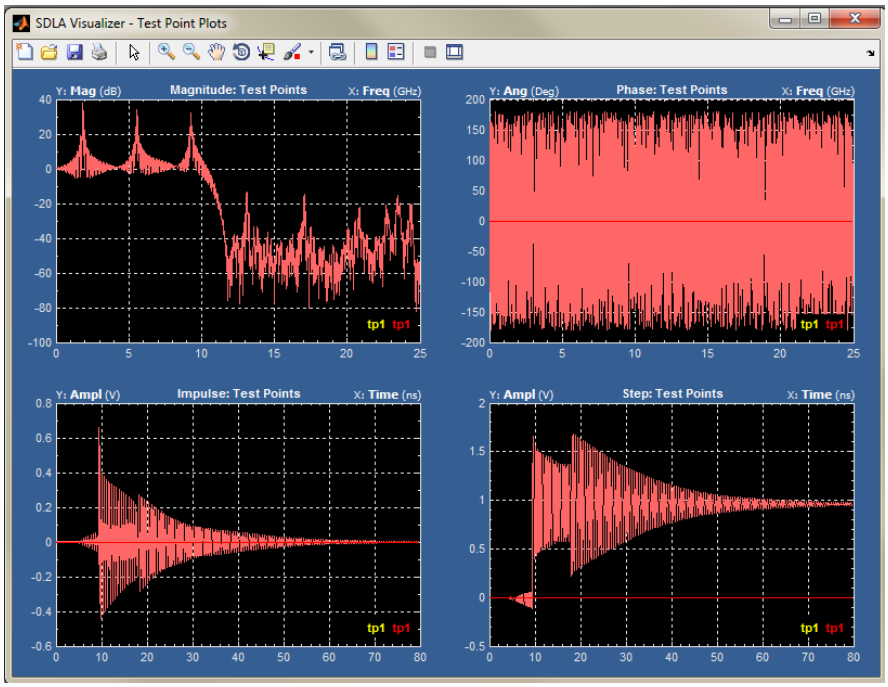
   Note that the de-embedded waveforms shown at the Tx reference plane below do not have major reflections; the wave-shape is the expected shape of the step generator. The major reflections on the acquired waveforms were removed when transforming it to the waveform in the simulated circuit at Tp2. The acquired waveforms from Ch1 and Ch2 of the scope are shown in yellow and cyan. These are the waveforms acquired through the cable and T/coupler combination. The de-embedded waveforms with measurement circuit replaced by ideal 50 ohms are shown as green and red. SDLA Visualizer is capable of showing up to four test point waveforms simultaneously while up to 48 are available to view.



Finally, view the plots of the test point filters:

Once the **Apply** button is pressed in the SDLA Main Menu and the transfer function filters have been computed, you may view the plots of the test point filters that result. Press the **Plot** button in the Main Menu, as shown below.

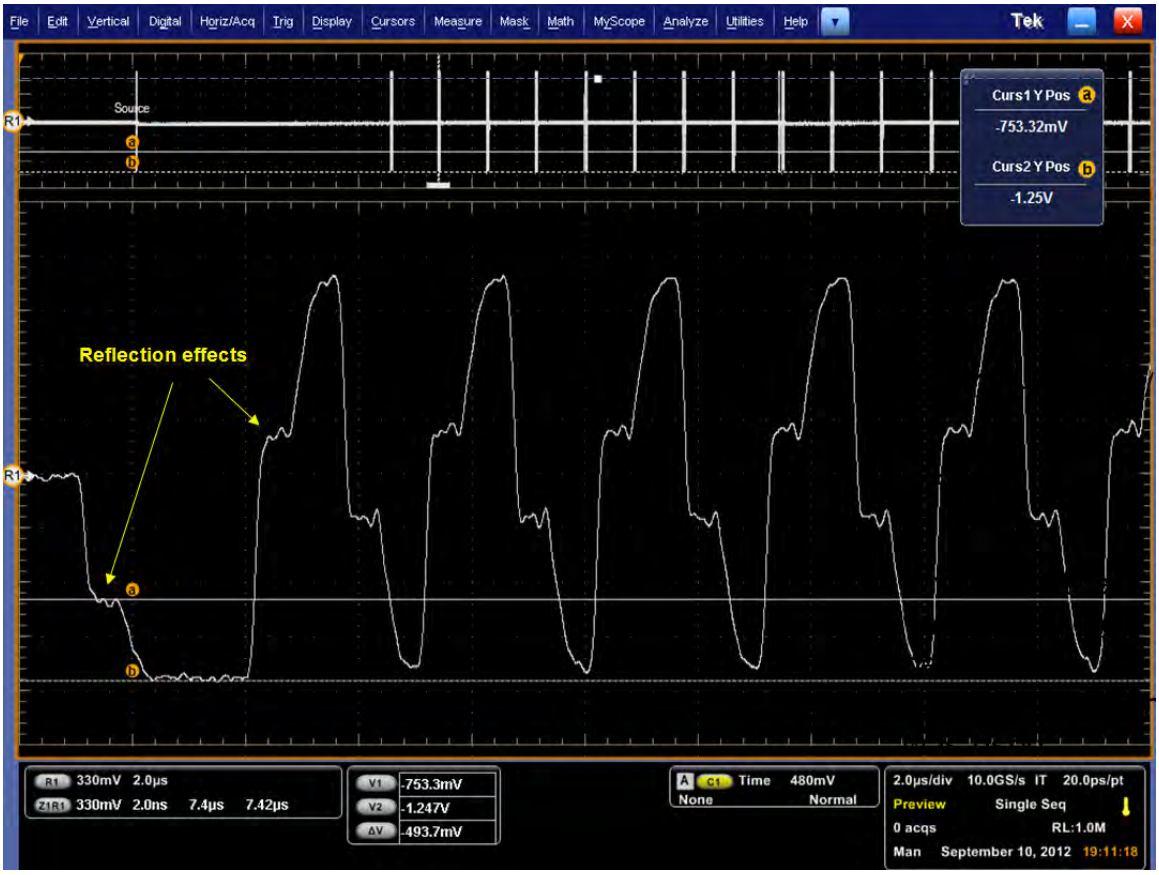
Notice that the magnitude vs. frequency plot shows high gain at the frequencies where the T coupler **S21** shown large dips. This is necessary in order to de-embed out the effects of the T-coupler, which causes major reflections. This results in the impulse response at the lower left to ring for a long period of time. In addition, the step response at the lower right also shows the ringing over a long period of time. This results in long lengths in numbers of filter coefficients when the sample rate is high.



Example of removing a DDR reflection with a single input waveform

This example demonstrates how SDLA Visualizer can be used to remove reflections for a low-speed DDR case, using a simplified set of block models.

In this situation, several elements are in place between the probe point and the Rx load resistor: a delay line that can be modeled using a T-line model, a package that is modeled using an S-parameter block, and a non-ideal load resistor. Because the probe point is not near the load resistor, and the load resistor is non-ideal, a large reflection can be observed in the waveform acquired at the probe point:



Even though the waveform at the actual probe point is not suitable for any jitter measurements due to the large reflection, the waveform at the load resistor has a regular pulse shape. This example shows how SDLA can be set up to de-embed the reflection from the waveform at the load resistor.

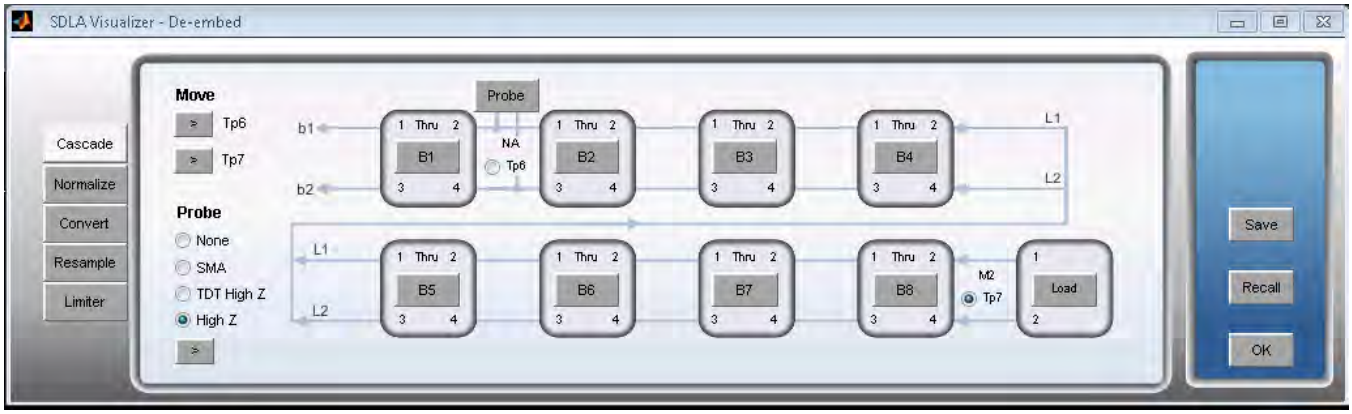
In this example, three blocks in the De-embed cascade diagram will be used to model the delay line, package and load resistor:

- the delay line will be modeled using a T-line model in Block **B2**,
- the package will be modeled using a 4–port S-parameter file in Block **B3**,
- and the non-ideal load resistor will be modeled as nominal impedance in the **Load Block** (final block in the cascade).

First, set up.

1. On the Main Menu, select the **Single Input** radio button.

   In the **De-embed block**, select the **Hi Z** probe option. Ideal Hi Z probe is assumed.

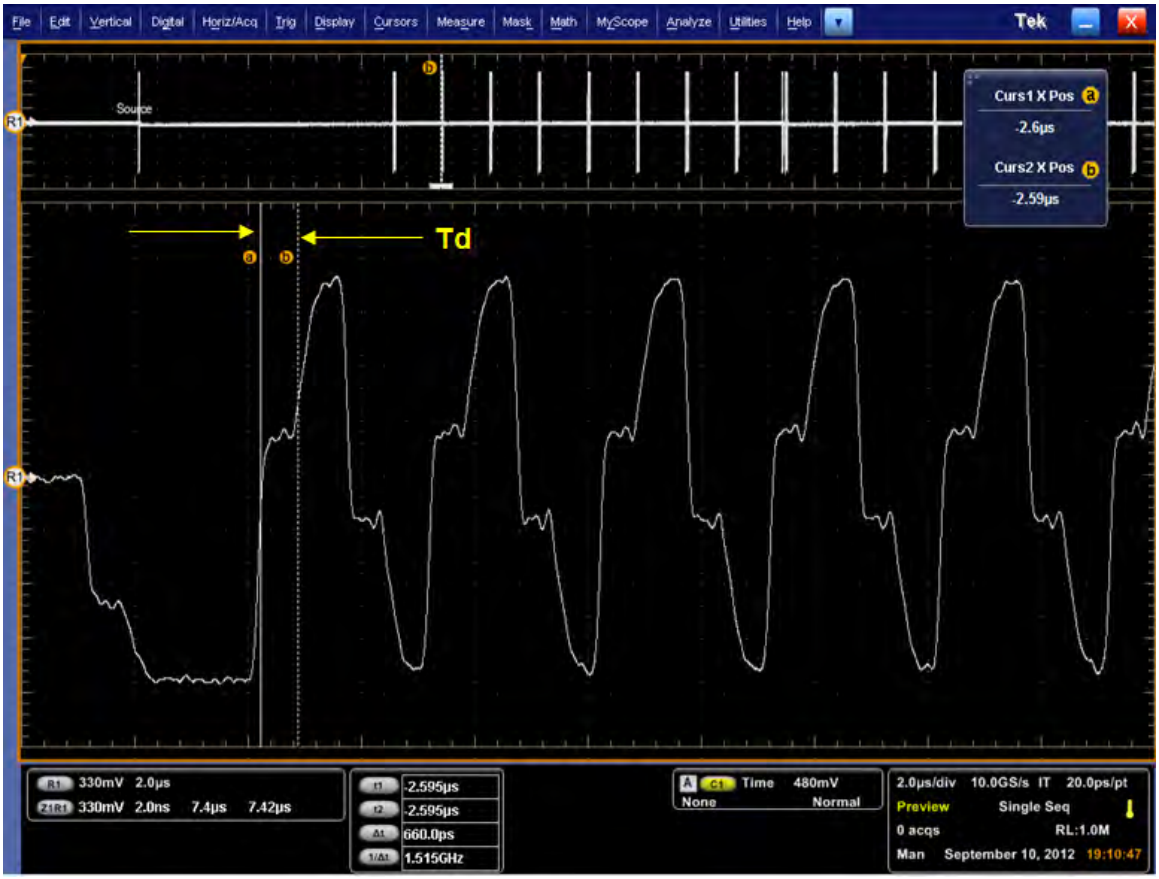


Next, model the T-line:

1. Estimate the transmission line delay using the horizontal cursor measurement tools to get the delay for round trip reflection. Then, divide by 2:

   Td = 660ps/2

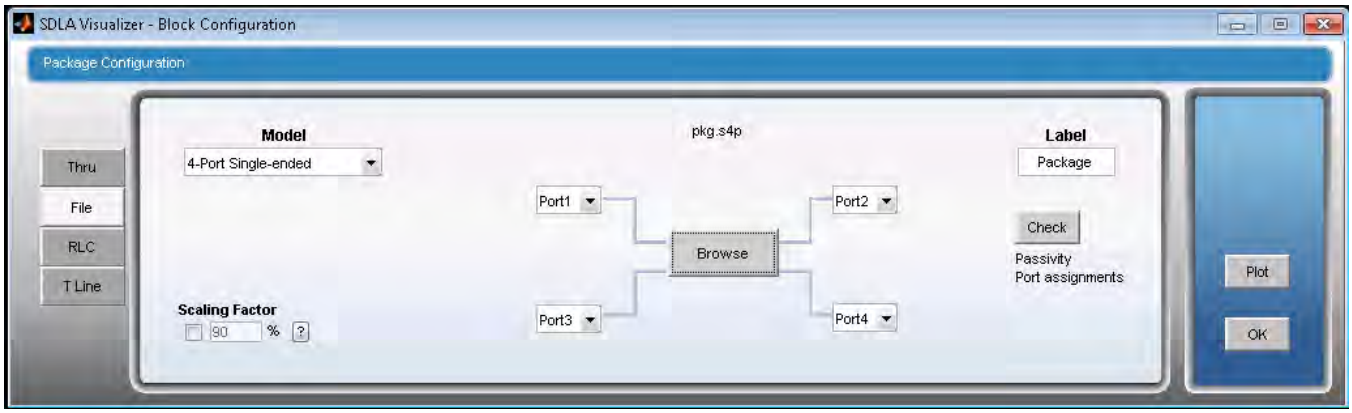
   = 330ps



2. Set up a block using a lossless transmission line model with 330ps delay. Select block **B2** in the **De-embed** menu and select the **T-line** tab. Enter 0.33 in the **Delay ns** field. Press **OK**.

Next, model the package:

1. The package is modeled using a 4-port single-ended S-parameter file. Press **B3** on the De-embed cascade diagram and press **Browse** to select an appropriate file. Note that the port assignments are different from the default port assignments: [1 3 2 4] instead of [1 2 3 4].



2. To see if the port assignments are correct, you can press the **Check** button located on the **File** tab. You can also check the S-parameter plot to identify insertion loss terms to assign ports properly. Press **OK.**

Now, configure the Load Block.

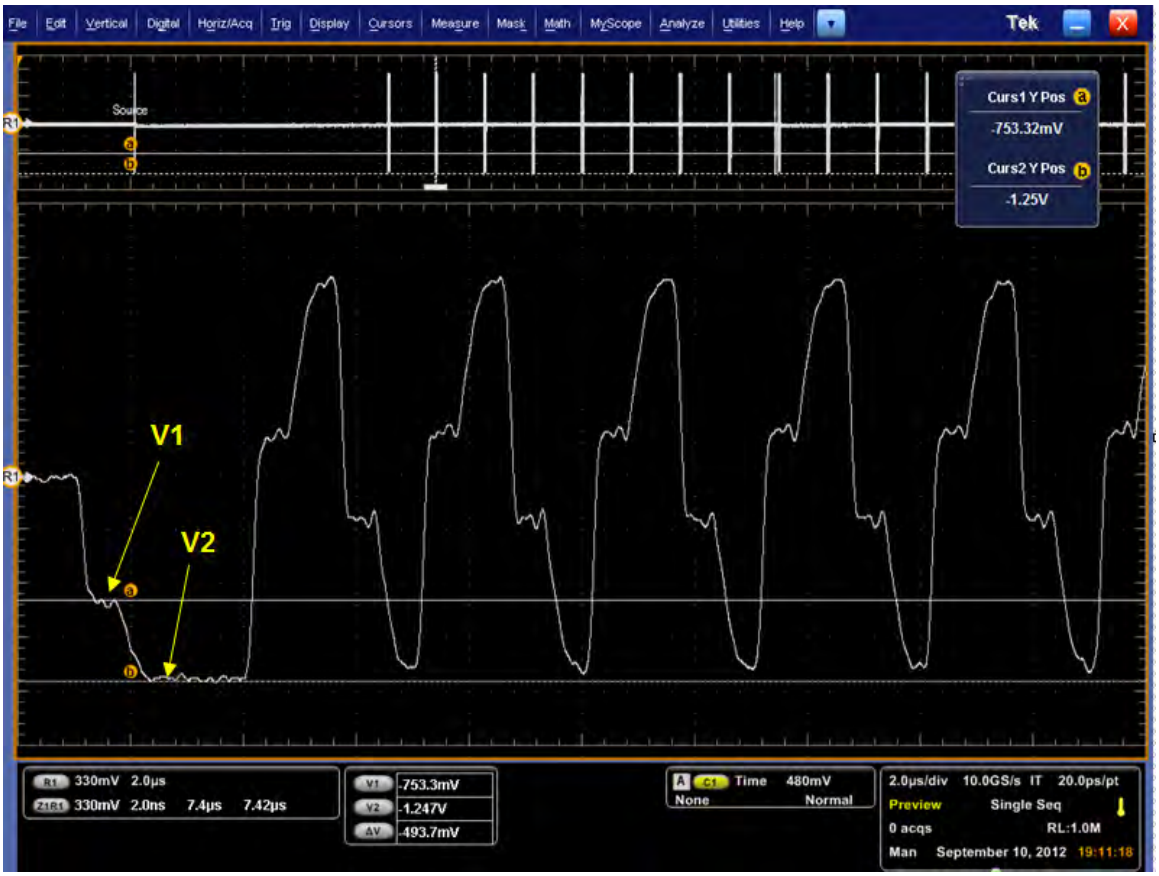
1. First, estimate the value of the load resistance in order to enter it into the Load Block. Use the vertical cursor measurements to get a ratio of reflected to incident voltage.
2. Next, compute the resistance:

   T(Γ) = (V2-V1)/V1

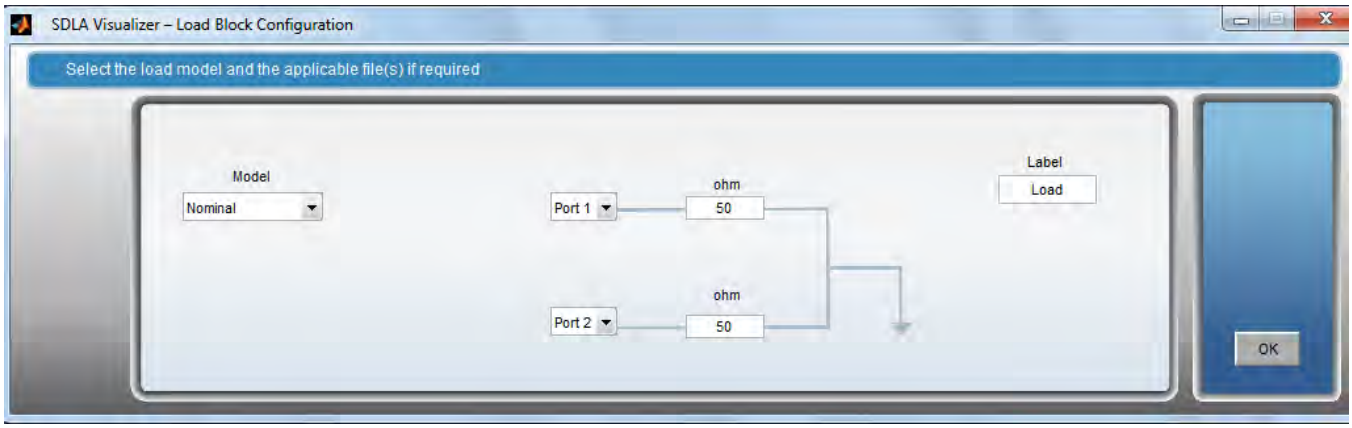
   = (1.25-0.75)/0.75

   R = Zo(1+T)/(1-T)

   = 200 Ohms



3. Set up the Load Block using 200 Ohms resistance. On the De-embed Block, pressing on the Load Block (the final block). This brings up the Load Configuration Menu, below. Enter this value into Port 1 of the Load Configuration Menu. Press **OK.**



After all the blocks have been set up in the De-embed menu, return to the Main Menu and press **Apply**. SDLA creates the filter for **Tp7** and turns on the de-embedded waveform on the scope, as shown below.

- White represents the original acquired signal WITH the reflection.
- Purple represents the de-embedded result showing the reflection removed. This is the waveform that the Rx block “sees” at the Rx load resistor. Note that the de-embedded waveform has regular pulse shapes; measurements such as jitter can be performed upon it.


File Edit Vertical Digital Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
Source
Reflection removed
Reflection
330mV 2.0µs
1.0V 2.0µs
330mV 2.0µs
330mV 2.0ns 7.4µs 7.42µs
1.0V 2.0ns 7.4µs 7.42µs
330mV 2.0ns 7.4µs 7.42µs
Time 480mV
None Normal
2.0µs/div 10.0GS/s IT 20.0ps/pt
Preview Single Seq
0 acqs RL:1.0M
Man September 10, 2012 17:28:25

GPIB remote control

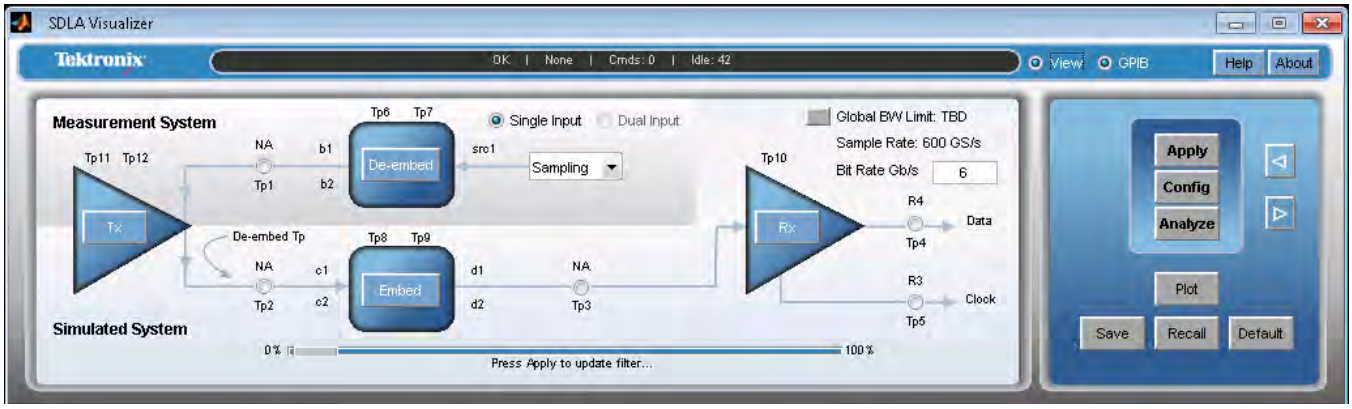
Using GPIB remote control

You can use GPIB commands to control SDLA Visualizer remotely, and to monitor the SDLA GPIB activity using the application Main Menu. The GPIB commands listed are separate from, and handled differently than, the DPO70000 Series Oscilloscope GPIB commands. (Note that a TekScope command, *APPLICATION:ACTIVATE SDLA*, is used to start the SDLA Visualizer application.) Press here to see the *set of SDLA Visualizer commands available*.

Analysis results are available by querying the DPOJET/JNB application either by using its GPIB command set, or (RT only) from the oscilloscope front panel. Use the GPIB command interface for the DPOJET/JNB application to retrieve measurement results. (Refer to the DPOJET/JNB online Help or the PDF document derived from it for DPOJET/JNB GPIB control information.)

GPIB Control Menu

Select **GPIB** on the upper right corner of the SDLA Visualizer Main Menu to enable the GPIB function. Press **View** to monitor command traffic to and from SDLA Visualizer. In the following illustration, GPIB is enabled, and View is selected to show SDLA Visualizer command traffic (GPIB On and View Off are the defaults). Other GPIB command traffic is not shown. Use an application such as the TekVisa OpenChoice Call Monitor to see all GPIB traffic.



The GPIB status includes the following values:

- Sent – shows the status sent after executing the last command. May be OK or ERROR.
- Received – shows the last value read from the SDLA Visualizer handshaking variable. It is either OK, meaning no command is available, or it shows the received command now being processed.

- Last – shows the last instruction executed.
- Cmds – contains the count of the commands received since you enabled the GPIB function.
- Idle – contains the count of the number of polls of the handshaking variable by the SDLA Visualizer application since completing the last command. GPIB communications is enabled by default.

Using the SDLA Visualizer application's GPIB interface consumes additional compute resources.

Handshaking Protocol

The SDLA Visualizer application handles GPIB communications through its own protocol handshaking.

The requirements for SDLA Visualizer GPIB communications with a controller are as follows:

1. Once the SDLA Visualizer application has started, it writes an "OK" status to the SDLA Visualizer handshake variable. This tells the controller application that it may now write a valid SDLA Visualizer command into the "sdla' variable.
2. The GPIB controller polls the handshake variable (variable:value? "sdla") until it detects the OK status.
3. The GPIB controller writes a command string into the SDLA Visualizer handshake variable. For example, sending the command 'variable:value "sdla", "p:apply"' writes the string "p:apply" into the variable "sdla".
4. The SDLA Visualizer GPIB function polls the handshake variable, reads the command string and interprets it as a command. If the command is bad, it writes an ERROR handshake value to the variable.
5. A good command is parsed and executed. On successful execution, it writes an OK to the handshake variable. When the GPIB controller reads the OK status, it may send a new command string.

GPIB commands

This section lists the commands available for remote control of the SDLA Visualizer application.

NOTE. *"sdla" must be in lower-case characters.*

APPLICATION:ACTIVATE "Serial Data Link Analysis"

This command instructs the oscilloscope to start the SDLA Visualizer application. It is a set-only parameter. (Note: this is a TekScope command, not an SDLA Visualizer command).

NOTE. *This command must use the exact syntax below.*

Syntax APPLICATION:ACTIVATE "Serial Data Link Analysis"

Arguments "Serial Data Link Analysis" which must be just as defined in the syntax and enclosed in double quotes (" ").

Returns NONE

VARIABLE:VALUE "sdla", "p:exit"

Closes the SDLA Visualizer application. The current state of the application is not saved.

Syntax VARIABLE:VALUE "sdla", "p:exit"

Arguments "p:exit" forces the application to close.

VARIABLE:VALUE? "sdla"

Reads the value of the SDLA Visualizer handshake variable. The returned status must be “OK” before you can send any other commands.

Syntax VARIABLE:VALUE? "sdla"

Arguments None

Returns OK: The SDLA Visualizer application is running and ready for a command.

ERROR: The SDLA Visualizer application was not able to parse or run the previous command.

VARIABLE:VALUE "sdla", "p:adapttaps:<value>"

Configure the equalizer adapt taps setting (RT only).

Syntax VARIABLE: VALUE "sdla", "p:adapttaps:<value>"

Arguments "p:adapttaps:<value>" specifies the adapt taps could be any one of [auto | from_current | none].

Example variable:value "sdla", "p:adapttaps:auto" sets the adapt tap to be auto.

VARIABLE:VALUE "sdla", "p:bitrate:<value>"

Sets the bit rate for the source waveform. Determine the native bit rate of the source waveform and use that value.

Syntax VARIABLE:VALUE "sdla", "p:bitrate:<value>"

Arguments "p:bitrate:<value>" specifies the bit rate of input source waveform. The <value> must be an integer in either engineering notation (6.25e6) or as a regular number (6250000).

Example variable:value "sdla", "p:bitrate:6e9" sets the source bit rate to 6 Gb/s.

VARIABLE:VALUE "sdla", "p:ctletype:<type>"

Configure the equalizer CTLE type.

Syntax VARIABLE: VALUE "sdla", "p:ctletype: <type>"

Arguments "p:ctletype <type>" specifies the CTLE type to be any one of **[Standard | IIR | FIR | PCIE3 |PCIE4 | USBGEN1S | USBGEN1L | USBGEN2 | MIPI | CAUI4 | TBT1 | TBT2]**. Valid types for sampling scopes are [Standard | IIR | FIR]

Example variable:value "sdla", "p:ctletype:PCIE3" sets the CTLE type to PCIE3 on real-time oscilloscopes.

VARIABLE:VALUE "sdla", "p:dfestate:<state>"

Configures the equalizer DFE state (RT only).

Syntax VARIABLE: VALUE "sdla", "p:dfestate:<state>"

Arguments "p:dfestate:<state>" sets the DFE to be one of state: on | off

Example variable:value "sdla", "p:dfestate:on" sets the DFE on.

VARIABLE:VALUE "sdla", "p:ffedfetype:<type>"

Configure the equalizer FFE/DFE type.

Syntax VARIABLE:VALUE "sdla", "p:ffedfetype:<type>"

Arguments "p: ffedfetype:<type>" specifies the adapt taps could be any one of [Auto | PCIE3 | PCIE4 | USBGEN2 | MIPI | CAUI4 | TBT1 | TBT2].

Example variable:value "sdla", "p:ffedfetype:auto" sets the FFE/DFE type to auto.

VARIABLE:VALUE "sdla", "p:RunEQ"

Runs the Equalizer.

Syntax VARIABLE: VALUE "sdla", "p:RunEQ"

Arguments "p:RunEQ" forces the equalizer to run.

Example variable:value "sdla","p:RunEQ"

VARIABLE:VALUE "sdla", "p:source:<source>"

Sets the input source waveform for the SDLA Visualizer application to operate on (RT only).

Syntax VARIABLE:VALUE "sdla", "p:source:<source>"

Arguments "p:source<source>" specifies the first input source waveform as any one of ch1 | ch2 | ch3 |ch4 | math1 |math2| ref1 | ref2.

Example variable:value "sdla", "p:source:ch1" sets the source waveform to be the oscilloscope CH1 input.

VARIABLE:VALUE "sdla", "p:sourcetype"

Specifies whether to use Single Input mode (one differential signal source) or Dual Input mode (two sources used; usually each input is a leg of a differential signal) (RT only).

Syntax VARIABLE:VALUE "sdla" "p:sourcetype" <1|2>

Arguments 1 sets the source type to Single Input mode.

2 sets the source type to Dual Input mode.

VARIABLE:VALUE "sdla", "p:recall:<path and file name >"

Loads a setup file from “path and file name ”. The setup file may be one of the included Standards setup files or a setup file you created with the SDLA Visualizer application interface. The setup file includes configuration of Rx/Tx, the enabled filter blocks and test points, and any custom FIR filters you specified in your custom setup.

Syntax VARIABLE:VALUE "sdla", "p:recall:<path and file name >"

Arguments "p:recall:<path and file name >" where <path and file name > specify the path on a mapped drive and a setup file with the .sdl suffix. The path and file name must not contain space characters, but they may contain upper and lower case characters.

Example variable:value "sdla", "p:recall:C:\TekApplications\MyDirectory\mysetup.sdl" recalls the SDLA Visualizer application setup file named mysetup.sdl.

VARIABLE:VALUE "sdla", "p:source2:<source2>"

Specifies the second source waveform to be processed by the SDLA Visualizer application when using Dual Input mode (RT only).

Syntax VARIABLE:VALUE "sdla", "p:source2:<source2>"

Arguments "p:source2<source2>" specifies the second input source waveform as any one of ch1 | ch2 | ch3 |ch4 | math1|math2 | ref1 | ref2.

VARIABLE:VALUE "sdla", "p:analyze"

Starts the DPOJET/JNB application and configures it to display the eye diagrams for the SDLA Visualizer application waveform(s) resulting from the Apply operation.

Syntax VARIABLE:VALUE "sdla", "p:analyze"

Arguments "p:analyze" starts the DPOJET/JNB application to display the SDLA Visualizer application waveforms. For JNB the Run button must also be pressed on the JNB display.

VARIABLE:VALUE "sdla", "p:apply"

Computes the enabled filter blocks and test points and performs equalization if enabled. The result is the same as selecting the front panel Apply button. The Apply computation may take over 60 seconds, depending on input data and sample rate. Make sure that your polling time-out is sufficiently long.

Syntax VARIABLE:VALUE "sdla", "p:apply"

Arguments "p:apply" starts computation of the enabled filters and equalization.

Index

F

G

H

I

L

M

N

O

P

R

S

T

U

V

W